Developments for Improved-Performance Vertical-Cavity Surface-Emitting Lasers

Licentiate Thesis by

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Abstract

The vertical-cavity surface-emitting laser (VCSEL) is a type of laser diode that emits light from the surface of the chip from which it is manufactured rather than from a cleaved edge as so far has been common for most telecommunication lasers. VCSEL’s low cost, high power efficiency and low power consumption properties make it a very attractive signal source for many applications such as fiber optical communication, optical interconnects, 3D sensing, absorption spectroscopy, laser printing, etc.

In this work, we have developed and evaluated new designs and technologies for extending the performance of VCSELs based on the GaAs material system. A novel scheme for single-mode emission from large size VCSELs, with active region size up to 10 µm, is proposed and discussed. Oxide-free designs of the VCSEL structure either based on an epitaxially regrown p-n-p layer or a buried tunnel junction (BTJ) for lateral current confinement are fabricated and characterized; the latter scheme yielding significant dynamic and static performance improvement as compared to epitaxially regrown design. In addition, the first room-temperature operation of a heterojunction bipolar transistor (HBT) 980nm VCSEL, a so-called transistor-VCSEL, is demonstrated. This novel three-terminal operational VCSEL is believed to have the potential for a ultrahigh modulation bandwidth due to altered carrier dynamics in the cavity region.
List of Papers


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Chapter 1

Introduction

1.1 Introduction to VCSELs

Vertical-cavity surface-emitting lasers (VCSELs) represent a new breed of compact, low-cost and power-efficient semiconductor lasers that have become instrumental for a range of applications (1). In particular, they are widely used for gigabit per second speed optical links based on multimode optical fiber (2). These VCSELs operate multimode at a wavelength of 850 nm for typical short-distance data communication applications but during the recent decade there has also been extensive efforts to develop long-wavelength (1.3-1.55 µm) singlemode VCSELs for medium range data communication such as access or metropolitan networks (3).

As schematically illustrated in Fig. 1, a typical electrically pumped VCSEL consists of several elements: active layer (usually quantum wells, shown as the red region in the figure), laser cavity (red, blue and khaki region), top and bottom distributed Bragg reflectors (DBRs, yellow and green alternate region), optical and electrical confinement layers (brown layer), and electrodes (black layer) as shown in Fig. 1. The VCSEL has an ultra short cavity (on the order of the emitting wavelength – a one- or a few-lambda cavity) and a corresponding very short gain region, which puts requirements on very high reflectance top and bottom DBRs (4).

The surface emitting properties of VCSELs together with their short cavity and high reflectivity DBR enable several advantages compared to traditional edge emitting lasers (EELs), e.g. low cost wafer-scale manufacturing and testing before packaging, easy formation of one and two dimension laser arrays, a circular beam profile that is good for high efficiency fiber coupling, inherent single longitude mode emission, low threshold current and low power consumption.
1.2 Long wavelength VCSELS

On today’s commercial market, short wavelength (mainly 850 nm) VCSELS are already available for short-distance data communication over multimode fiber (5). However, the development of VCSELS working at longer wavelengths (1.3-1.55 µm) have been much slower due to inherent material problem. This includes the lack of a lattice-matched materials system that can provide both sufficiently high-refractive index contrast DBRs as well as a high-gain active material. Significant research efforts have been devoted to this problem. Nowadays, several companies are marketing long-wavelength VCSEL products, including Beam-Express SA (Switzerland), Alight Technologies (Denmark), Vertilas GmbH (Germany), and RayCan (Korea) (6-9).

Beam-Express fabricates long-wavelength VCSEL which combines InAlGaAs/InP quantum wells (QWs) with AlGaAs/GaAs DBRs using wafer fusion technology (10). This approach removes the limitations imposed by lattice-matched epitaxy, and can thereby benefit from the combination of different material systems regardless of lattice constant or crystallographic orientation. In this case, high index contrast and excellent thermal conductivity GaAs-based DBRs are thereby combined with high-gain InP-based active layer for long wavelength. Using this technology, singlemode 1300-nm VCSELS with emission power up to 5.4 mW at 25°C (3.1 mW at 75°C) with 10 Gb/s data transmission (11) as well as 1550-nm singlemode VCSELS with output power of 8 mW at 0°C (1.5 mW at 100°C) (12) have been demonstrated.
Alight are marketing InGaNAs-QW 1300-nm photonic-crystal enabled singlemode VCSELs. Their 9-µm oxidation confinement VCSELs can maintain single-mode emission up to 12 mA over a temperature interval of 10-90°C. The emission power is 2.8 mW (1.4 mW) at 10°C (90°C) with a modulation speed up to 10 Gbps (13).

Vertilas GmbH fabricates various wavelength VCSELs (from 1310 nm to 2014 nm) intended for near-IR gas analysis and optical data communication. These VCSELs are based on the InP material system and use a buried tunnel-junction (BTJ) technology for electrical and optical confinement and hybrid metallic/dielectric DBRs for efficient heat dissipation. Published results have included 8.2 mW singlemode output power for 7-µm 1550-nm BTJ VCSELs (14) and 1.3-µm short-cavity VCSELs with 25 Gbit/s error-free transmission (15).

Raycan also markets long-wavelength VCSELs with modulation speed up to 10 Gb/s for both 1310 and 1550 nm (9). These VCSELs are fully monolithic InP-based structures, including MOVPE-grown InAlGaAs/InAsAs top and bottom DBRs and InGaAs QWs. The current confinement scheme is based on a tunnel junction in combination with an air gap structure (16).

The 1300-nm VCSEL technology developed at KTH has relied on a different approach based on standard materials and methods for short-wavelength VCSELs, i.e., AlGaAs/GaAs DBRs and InGaAs/GaAs QW active layer (17-21). This is made possible from the application of highly strained InGaAs quantum wells to push the peak of the gain curve up to 1220 nm and a negative gain-cavity detuning to set the emission wavelength in the 1.3-µm band. This approach provides the basis for the present study of which the most recent results will be summarized in chapter 4.

1.3 Single-mode VCSELs

VCSELs are inherently longitudinal singlemode emitters due to their short optical cavity and limited spectral extension of the gain but due to the extended lateral dimension of the device it usually supports multiple transversal modes. However, many applications require transversal singlemode emission. This is particularly important for longer-distance optical communication in the 1.3- or 1.55- µm bands where modal dispersion becomes an issue.

There are mainly two main approaches for forcing the VCSEL into singlemode operation, of which some of the common schemes are illustrated in Fig. 2. Either the modal gain of the fundamental mode is increased or the modal losses of the higher order transverse mode are increased. Sometimes both approaches are applied simultaneously. The first approach can be implemented by shrinking the lateral current injection area as shown in Figs. 2 a) and b). A uniform current injection will here result in an even better overlap of the carrier concentration profile (and hence the gain) and the fundamental mode intensity profile in the active region, which leads to considerably lower lasing threshold current for the fundamental mode. Therefore the
device will maintain singlemode emission within a certain range of drive currents (22, 23). However, the small active region exhibits both higher thermal and electrical resistance which limits the device lifetime and high-speed performance (24). From a more practical perspective, a precise control of the small diameter active region is difficult for the commonly used oxidation method (25). A tunnel-junction confinement can improve the current injection uniformity for larger active region (26, 27). Furthermore, tunnel junction-based carrier injection enables the replacement of p-doped layers with n-doped layer, which reduces the electrical resistance and the optical loss, thereby improving the VCSEL’s performance (28, 29).
The second approach can be implemented by introducing selective losses for the high-order modes, e.g., by using a surface relief (Fig. 2 c and d) to increase the mirror losses of the higher order modes. As the intensity distribution of different modes have different overlap with the surface structuring of the top mirror, a selective loss between different modes is introduced. In this way, the high-order modes can be suppressed (30, 31). An extended cavity (Fig. 2 e) increases the diffraction losses of the higher-order modes since these have larger propagation angles (32). The anti-guiding structure (Fig. 2 f) also increases the diffraction losses of high order modes by enabling easier penetration of high order mode into passive region (33, 34). The concept of introducing absorption losses (Fig. 2 g) is simply accomplished by making the output metal window such small size that is comparable to the active region (35-37). Thus, the strongly absorptive metal will cut the high order mode from emitting out of the top DBR. Photonic crystal filter VCSELs (Fig. 2 h), are based on the etching of a pattern of holes in the top mirror (13). The modal distribution of the emission can thereby be tailored by changing the size, shape, depth and pitch of holes. In the present work, we
apply the surface relief-technique as well as novel intra-cavity patterning approach [Paper B] of which the details will be instructed in section 2.3.

1.4 High-speed VCSELs

The increasing demand for optical communication, e.g. for internet and other networking services, puts requirements on power-efficient emitters with increasingly higher modulation capabilities (2). VCSELs here benefit from their small modal volume which enables high speed modulation at very low current levels. Substantial effort has been devoted into developing high-modulation speed VCSEL to meet future bandwidth requirements. Directly modulated 850 nm VCSELs have reached a record value of 28 GHz (38), which have been used to demonstrate error-free data transmission with bit rate up to 47 Gbit/s. Higher data rate up to 64 Gbit/s have recently also been demonstrated using the same VCSELs and electronic bandwidth equalization (39). To meet the requirements of the next generation optical networks, single-channel transmission rates up to 25 Gbit/s is needed and several vendors such as IBM/Finisar, VI system (40), TE Connectivity (41), Philips (42), Avago (43), Subnitomo (44), Furukawa (45), and Vertilas (15) have been developing corresponding VCSEL product. Even higher single-channel data rates up to and beyond 40 Gbit/s will be required in near future (46), and a systematic optimization of current VCSELs as well as the development of new design concepts will be an active and challenging research task.

The optimization of high-speed VCSELs includes several measures:

1. Reduction of electrical parasitic by minimizing the device resistance and capacitance
2. Optimization of the active layer to provide high differential gain
3. Improvement of thermal conductivity and reduce heat generation
4. Improvement of the optical confinement
5. Optimization of the photon life time (trade-off between resonance frequency and damping)(47)

In the present study we also investigate an alternative concept of a three-terminal “transistor VCSEL”. This is based on the recent development of transistor lasers (48) where a heterojunction based transistor (HBT) is homogeneously integrated with a semiconductor laser, thereby providing additional means of controlling the carrier dynamics in the cavity region. Such devices have been proposed to have a number of advantages, including a greatly increased modulation bandwidth (49).
1.5 This work

The work in this thesis regards the development of large-area 1300-nm singlemode VCSELs (papers A,B), 1300-nm buried tunnel-junction (BTJ) VCSELs (paper E) and 980-nm transistor VCSELs (papers C, D). Singlemode VCSELs were realized using a surface relief technique (paper A) as well as a novel approach where the fundamental mode profile is engineered to match the gain profile as deduced from an uneven carrier injection (paper B). The latter approach was examined both theoretically and experimentally and it was shown that despite the doughnut-shaped near-field pattern the far-field shape is close to Gaussian. Large-area (10 µm) singlemode VCSELs were demonstrated using this approach but only at modest output power (~1 mW at room temperature) and it remains to be proven that it can work as intended also for higher output powers.

To improve the current injection profile and to reduce the electrical parasitics optical loss as well as to simplify the fabrication process, a buried tunnel-junction (BTJ) current confinement scheme was implemented in 1300-nm InGaAs/GaAs VCSELs. As compared to our previous designs based on peripheral npn-blocking regions and a two-step epitaxial regrowth process, these single-regrowth devices showed significantly improved dynamic performance.

Finally, a three-terminal Pnp 980-nm transistor-VCSEL (T-VCSEL) was designed and fabricated (papers C,D). This design was directly inherited from our epitaxially regrown 1300-nm VCSELs with npn blocking layers. These devices constituted the first demonstration of room-temperature operation of such lasers and similar static characteristics compared to conventional diode-type VCSELs were obtained (paper C). In addition, voltage-controlled operation could be demonstrated and a numerical model was implemented that could describe the static performance with high accuracy (paper D).
Chapter 2

Basic concepts

2.1 Application-driven performance requirements

High-performance emitters are required at all levels of the optical communication network. The performance requirements these emitters have to face regards diversified aspects such as modulation bandwidth, noise properties, output power, operating voltage, operating current, power efficiency, temperature stability, etc., but a low-cost technology is also of outmost importance for high-density installations. This makes VCSELs very attractive for a bulk of these applications. In the present work we have specifically studied 1300-nm VCSELs for medium-reach applications such as metro and access networks. The corresponding performance requirements are thereby dictated by different applications and associated industrial standard bodies. Within the project LASTECH (Laser and system technologies for access and datacom) financed by the Swedish Foundation for Strategic Research (SSF) we formulated target performances for a generic 1300-nm VCSEL technology as: Emission wavelength > 1260 nm; singelmode chip-level output power >2 mW; bandwidth > 20 GHz (suitable for 25 Gb/s data transmission); and high-temperature operation up to 85°C. It should be mentioned that these are very ambitious target specifications that still are beyond state-of-the-art for any 1300-nm VCSEL technology.

Beyond the 1300-nm VCSELs the work was also directed towards T-VCSELs. While the fabricated devices operated at 980 nm, the concept is generic and can in principle be implemented for any wavelength permitted by the GaAs materials system. The target result here is to demonstrate a performance that goes significantly beyond what can be achieved with a conventional VCSEL technology, meaning a modulation bandwidth greater than 30 GHz.

2.2 Extended-wavelength InGaAs/GaAs VCSELs

As stated earlier, the 1300-nm VCSELs developed at KTH relies on highly strained InGaAs/GaAs QWs in combination with a negative gain-cavity detuning to reach the 1.3-μm window. By a careful adjustment of the MOVPE growth parameters it was
demonstrated that MQW InGaAs/GaAs edge-emitting lasers with up to five QWs can reach a wavelength as long as 1240 nm without any penalty in threshold current or output power \((50)\) and this concept has been used to demonstrate 10 Gbit/s oxidation-confined VCSELs at room temperature and 85°C\((51)\) as well as regrown VCSELs with optical output power as high as 8 mW \((21)\). The relation between the cavity resonance and gain curve is schematically illustrated in Fig. 3 \((52)\). Of importance for the high-temperature operation is that the gain curve moves faster with temperature towards longer wavelength (~0.4 nm/K) than the cavity resonance (~0.1 nm/K) making the match between the two improve with temperature. This leads to a temperature-tolerant operation as required for these (un-cooled) applications.

![Fig.3: Illustration of the room-temperature misalignment between the cavity resonance (= lasing wavelength) \(\lambda_{FP}\) and material gain\((52)\).](image)

2.3 Designs for single-mode emission

Some common methods for achieving single-mode VCSEL emission have been reviewed in section 1.3. In the present work we have investigated two different approaches for realizing singlemode VCSELs as either based on a surface relief [paper A] or a shallow etch in the cavity region before depositing the out-coupling dielectric DBR [paper B]. In the following, these two approaches will be described in some more detail.

The surface relief technique is schematically illustrated in Fig. 4. The topmost quarter-lambda thick amorphous-silicon layer in the dielectric DBR stack is patterned and etched through in the peripheral region, thus leaving a small square. In this way, a low-loss central region is created that will support the fundamental mode while the higher-order modes which have different spatial distributions will experience higher loss due to the reduced reflectance in the peripheral region.
The method involving a shallow intra-cavity patterning is illustrated in Fig. 4. A very thin layer of GaAs, typically 10 nm, is etched away in the center of topmost cavity layer before deposition of the top DBR. In this way, the fundamental mode shape is changed for a better fit with the gain profile in the active region; see Fig.6 (paper B). As a consequence, the fundamental mode will experience a higher gain as compared to the higher-order modes and will therefore reach lasing threshold first with increasing drive current.

Fig.4: Schematic illustration of the surface relief technique for forcing the device to singlemode operation. The diagram shows the relationship between the mirror reflectivity (as seen from the cavity) and the etch depth.

Fig.5: Three-dimensional illustration of a VCSEL with shallow intra-cavity patterning for singlemode emission (paper B)
2.4 Designs for efficient lateral carrier confinement

The traditional carrier confinement of GaAs based VCSEL is based on a lateral oxidation of a high-aluminum content layer in the epitaxial material stack above the active region. Since this layer is only partially oxidized, a conductive aperture is formed that effectively can funnel the current into the region of interest (53). This method is easy and efficient and widely used in the fabrication of short-wavelength VCSELS. However, it has some drawbacks. For example, strain and possibly defects are introduced during the oxidation process (54) that may affect the reliability, especially in case of small device (24). It is also difficult to control the oxide aperture diameter with high accuracy since the oxidation process depends critically and non-linearly on several parameter such as oxidation time, oxidation temperature and aluminum content of the layer (25).

Fig. 6(a): (top) Calculated two dimensional carrier profile, (middle) Cross-section of carrier profile, and (bottom) Cross-section of the calculated gain profile. Scale of x axis is µm. (paper B)  
Fig. 6(b): (top) Calculated HE11 mode (blue) and gain profile (red) without shallow etch. (bottom) HE11 mode (blue) and gain profile (red) with a 10 nm shallow etch in the cavity region. Scale of x axis is µm. (paper B)

Fig. 7: Cross-sectional schematics of a VCSEL with epitaxially regrown P-N-P blocking layer for current confinement.
In this work, two different current confinement schemes were applied. The first scheme is based on epitaxial regrowth of P-N-P current blocking layer around a central conductive mesa. As shown in Fig. 7, an n-doped layer is regrown in the otherwise p-type cavity region. Therefore, a N-P junction is formed in the vertical direction. When current is injected from the P contact, the N-P junction is reverse biased and the current is blocked and thereby forced to go laterally and pass through the central active region. The advantages of this approach are that it eliminates the strain and defects that oxidation confinement may introduce and the size of aperture can be well defined by standard optical lithography. Furthermore, this approach can be used for any material system while oxidation confinement only has been successfully implemented in the GaAs material system.

![Fig. 7: Sketch of a VCSEL with BTJ.](image)

The second current confinement scheme is based on the regrowth around a buried tunnel-junction situated in the cavity region as shown in Fig. 8. The tunnel junction consists of 2 degenerately doped n and p layer. The band diagram of a unbiased TJ can be seen in Fig. 9(a). When the VCSEL is forward biased, the TJ is thereby reverse biased. The band diagram of a reverse biased TJ is shown in Fig. 9 (b). Electrons in the valence band on the p-side can directly tunnel to the empty states in the conduction band on the n-side. In this way, the current is confined to only go through the TJ since the surrounding area consists of a reverse biased p-n junction.
The Pnp-type transistor-VCSEL fabricated in the present work is schematically illustrated in Fig. 10. Similar to the 1300-nm VCSELs discussed above it is based on an epitaxial regrowth confinement where a pnp-type blocking layer forces the injected emitter current to the central region of the device. By virtue of the dielectric top mirror and the epitaxial regrowth confinement the device structure is rather shallow and thereby provides a comparably easy access to the electrical contacts. Especially the base contact may otherwise be tricky to realize since it corresponds to a rather thin layer in the epitaxial structure which may be difficult to hit with any accuracy if it is needed to etch all the way through a (several micrometer thick) semiconductor top-DBR. The double intra-cavity contacting scheme also allows for undoped DBRs and thereby lower optical loss as compared to a more conventional VCSEL structure (55). Still, the functionality of the device depends critically on the detailed design as discussed in paper D. In particular it is of critical importance to get a correct biasing of the different layers to extend the transistor active range of operation well beyond the lasing threshold.

2.5 Heterojunction bipolar transistor VCSELs

Fig. 9 (a): Band diagram of a TJ.  
Fig. 9 (b): Band diagram of a reverse biased TJ.

Fig. 10: Three-dimensional representation of the fabricated T-VCSEL. (Paper D)
Chapter 3

Results and discussion

3.1 Epitaxially regrown VCSELs

The purpose of developing an epitaxially regrown VCSEL design as opposed to previous designs based on selective oxidation confinement (18) was threefold:

1. A better controlled manufacturing process
   These devices can make use of standard photolithography with good control of lateral dimensions and shapes rather than the oxidation process that relies on precise calibration of the oxidation rate. Thereby they also fit better to standard semiconductor monolithic manufacturing processes.

2. Option for higher efficiency devices
   By virtue of the intracavity contacting scheme it is possible to use an undoped semiconductor bottom DBR which provides significantly lower optical loss and higher output power than n-doped ones (55). The methodology also provides an additional degree of freedom in the positioning of the current aperture as compared to oxidation confinement that requires a high-aluminum content layer positioned some distance apart from the active region due to the significant strain imposed by the expanding layer during oxidation.

3. Potentially improved reliability
   There has been considerable concerns regarding the reliability of oxidation confined VCSELs due to the mechanical strain induced by the process. To date, though, reliable 850-nm high speed and highly efficient VCSELs are availed from multiple vendors. However, this concern may become of importance again for later device generations with even higher requirements on efficiency, current density and modulation bandwidth.

As far as the manufacturing process is concerned we have indeed fabricated thousands of VCSELs with very even size distributions and corresponding uniform output characteristics. However, we also note that regrowth process itself influences what exact device shapes are possible to fabricate. In the present work we have used square-shaped mesas oriented along the [011] crystallographic axes. Small deviations
from this exact geometry are possible, e.g. slightly rhombic devices that might be necessary to control the polarization mode, but other geometries such as circular mesas may not be possible due to the evolution of the regrowth front. Details of the design and fabrication process of these devices are given in Appendix 1.

Figure 11, taken from paper A, shows LIV characteristics from multimode VCSELs fabricated according to this design. Notably, an output power as high as 8 mW is obtained from a 10x10-μm² sized mesa and there is still a significant output power even at a high temperature of 85°C.

![Graph showing LIV characteristics](image)

Fig.11: Output power and voltage drop of a 10 μm expitaxially regrown VCSEL. (Paper A)

The results from pulsed measurements on these devices (Fig.12) shows that the rollover as the drive current is increased is due to Joule heating and not to a breakdown of the pnp-structure current blocking capabilities.
In the first generation of devices, singlemode emission was only obtained for small active areas (4 µm or less) with superimposed mode filter (2 µm). The corresponding LIV characteristics and emission spectra are shown in Fig. 13. The obtained singlemode power for this device drops from 1.5 to 0.8 mW as the temperature is increased from 5 to 85°C. Although a somewhat good result it does not match the performance requirements stated in Sec. 2.1. The reason for lack of singlemode performance in case of larger–area devices is believed to be due to the regrowth process that produces are convex like shape of the cavity surface(56). This collects all the modes to a small volume in the center of the device and the spatial mode filter from a surface structuring is not efficient. A possible solution to this problem was found to be a reduced growth temperature of the second regrowth step which was

Fig.12: Light-current characteristics in pulsed operation (50 ns pulses, 0.1% duty cycle, dotted line) and continuous current drive (solid line) of three different VCSELs (a) 4 µm, (b) 6 µm and (c) 8 µm. (Paper A)
shown to result in a much planar mesa geometry (56). However, this approach has the drawback in a potential loss of crystalline quality from the low-temperature growth (and thereby increased losses) and a limitation in achievable n-type doping concentration in that later. Although, the latter constrain not is of importance for standard p-i-n-type VCSEL structures it will be serious in case of the BTJ-type VCSELs discussed below where the current-injection top layer is supposed to be n-doped.

As an alternative option we examined the design based on an intracavity shallow etch (Sec. 2.3 and paper B); see Appendix 2 for details regarding the design and fabrication process. As shown in Fig. 14 this resulted in singlemode emission also for large area devices up to 10x10-μm², however at reduced output power of ~1 mW. The reason for the reduced power was believed to be due to a poor alignment between modulation doped layers and the standing wave optical field in these devices; we also noted a similar drop in multimode power. However, an attempt to study the near-field of these devices failed to show a doughnut-shaped pattern and it remains unclear what effect actually governed the singlemode emission in these devices.

Fig.13: Output power and voltage drop of a single-mode VCSEL from structure 24768B. (Paper A)
As discussed in Sec. 2.4, BTJ-VCSELs have potential advantages in both processing simplicity and performance. Instead of the two-step regrowth in the pnp-blocking layer devices discussed above it is sufficient with a single step which also makes a more shallow structure feasible. In addition, the carrier injection profile is flattened and the n-doped current injection region allows for reduced series resistance and reduced optical loss. However, the growth of an optimized abrupt and heavily doped n⁺p⁺-junction is somewhat challenging. In the present work, the tunnel junction consists of a 20-nm In₀.₁₀As:Si (1x10¹⁹ cm⁻³)/10-nm GaAs:C (5x10¹⁹ cm⁻³) stack. A reduced series resistance may be obtained from an increased In concentration and/or increased doping levels. Still better performance would be expected for heterojunctions with altered band alignments that either pushes down the conduction band on the n-side (e.g. by alloying with N) (57) or pushes up the valance band on the p-side (e.g. by alloying with Sb) (58). Further details of the design and processing sequence of these devices are provided in Appendix 3.

Figure 18 a) compares the size-dependent series resistance between BTJ-VCSELs and epitaxially regrown VCSELs according to the previous section. Notably, the series resistance of the BTJ-VCSELs is significantly lower for typical drive currents (5-10 mA), although it increases with decreasing current. The latter is a consequence of the reduced density of states close to the band edges and may be improved from an optimized tunnel junction as discussed above. Figure 18 b) and c) show LIV characteristics and small-signal modulation response for BTJ VCSELs of various sizes as indicated.
Fig. 15 (a): Comparison of the differential resistance between BTJ VCSELs and epitaxially regrown VCSELs with pnp blocking layers for various device sizes as indicated. (Paper E)

Fig. 15 (b): L-I-V characteristics for BTJ singlemode VCSELs measured at 20°C. (Paper E)
3.3 Transistor VCSELs

As already discussed in Secs. 1.4 and 2.5, T-VCSELs were primarily introduced as a possible means to significantly increase the modulation bandwidth beyond what is possible to achieve with a conventional type VCSEL. However, these devices are slightly more complicated in design and fabrication due to their three-terminal configuration. The layer configuration and overall design must be carefully adjusted to get a proper biasing of the emitter, base and collector regions. We have here fabricated T-VCSELs very much according to our experience with standard type diode VCSELs, i.e., we use an epitaxial regrowth process with pnp-type blocking layers to funnel the current to the central region of the device. From a T-VCSEL perspective this design has the important advantage that it is a rather shallow structure and that it thereby is rather easy to contact the buried base region. Details of the device design and associated processing is found in Appendix 4.

Figure 16 shows light-versus-base current and light-versus collector-emitter voltage characteristics of this first generation of T-VCSELs. The obtained temperature-dependent performance in terms of threshold current and output power are comparable to those usually obtained in a standard-type diode VCSEL. The option for voltage-controlled operation is unique to transistor lasers and may find important application, e.g., in terms of simplified driver circuitry (59).
One problem with these T-VCSELs is that the saturation current for the transistor is lower than the threshold current for the laser. This means that when stimulated emission is reached the transistor no longer provides any current gain and it is not possible to observe typical transistor-laser signatures such as gain compression at lasing threshold (49). However, it should be noted that this only is true inasmuch as the global IV-characteristics of the device is considered, that is, the IV-characteristics being measured directly on the emitter, base and collector contacts. Looking in more detail on the potential distribution within the device it is clear that the transistor gradually goes into saturation due to a lateral voltage drop along the base-collector junction. When it becomes forward-biased (and thereby in saturation) in the center of the device, it is still reverse-biased (and thereby in the active mode of operation) in the peripheral region. This is discussed in detail in paper D where we also present results from a numerical modeling of the device performance based on a commercial simulation package(60).
Chapter 4

Summary and outlook

The purpose of this work has been to examine new concepts for extended performance VCSELs. In particular, we have examined different designs for efficient current injection, different schemes for singlemode stabilization and a new three-terminal transistor-VCSEL approach that may break the present bandwidth limitation of VCSELs.

Both the pnp-blocking layer and BTJ current injection structures were shown to have some clear advantages with respect to the standard oxidation-confinement design. These advantages regard the manufacturing process (e.g. standard lithography), potential reliability issues, and freedom in design (placement of current aperture and accessibility of the interior cavity region for mode shaping) but also some performance advantages were noted, primarily related to the low-loss structure with undoped mirrors. It was furthermore shown that singlemode emission can be obtained for large-area VCSELs using two different schemes (surface relief and shallow intracavity etching). Finally it was demonstrated that T-VCSELs can reach similar static performance figures as standard type VCSELs, which is an important prerequisite for the high-speed optimization of such devices.

There are many outstanding elements of device optimization to do regarding all devices considered in this thesis. Then it comes to singlemode 1300-nm VCSELs, the most promising approach seems to be the BTJ-VCSELs. An optimized tunnel junction design will reduce the series resistance as well as the forward voltage, both of which will be vital for an improved high-frequency performance. Beyond this, a reduced device area as well as better optimized doping profiles throughout the device will further reduce the parasitics and the intrinsic bandwidth may be enhanced from an optimized photon life time and reduced cavity length. Increased singlemode performance may be gained from a lower-temperature regrowth and thereby a less convex cavity shape. This, in turn, may call for alternative n-type doping species such as sulphur or tellurium to allow a sufficiently high doping concentration in this region.

The transistor VCSELs will need a careful design optimization with respect to layer thicknesses and doping as well as the overall device layout. It is here of critical importance to extend the active mode of transistor operation well beyond the lasing threshold. This optimization is neither straightforward nor fully intuitive but needs to
be based on extensive simulations. However, it is clear that a npn rather than a pnp device configuration might be helpful in this respect because the higher electron mobility as compared to the hole mobility, and tunnel junction carrier injection may be beneficial also in this case. Very recent results from our group shows that the situation for Pnp-T-VCSELs can be significantly improved just from a small alternation of the base thickness (61).
Guide to the papers

**Paper A: Performance optimization of epitaxially regrown 1.3-μm vertical-cavity surface-emitting lasers**
1.3 μm GaAs VCSELs based on an epitaxial regrowth confinement with pnp-type current blocking layers were fabricated and evaluated. A multi-mode power as high as 7 mW for a 10-μm device was demonstrated whereas the single-mode power was restricted to 1.5 mW for a 4-μm device due to a non-optimal cavity shape.

Author contribution: Taking part in characterization of the device and discussion of the results.

**Paper B: Single-mode InGaAs/GaAs 1.3-μm VCSELs based on a shallow intra-cavity patterning**
A novel intra-cavity patterning method for single-mode emission by engineering of the cavity mode profile to match the gain profile is proposed. Devices based on this concept were fabricated and characterized and singlemode emission from large-area VCSELs (active region size up to 10 μm) was demonstrated.

Author contribution: Device design, fabrication and characterization as well as writing the paper.

**Paper C: Room-temperature operation of transistor vertical-cavity surface-emitting laser**
The very first room-temperature operation of a transistor VCSEL is demonstrated. This device is based on epitaxially regrown current confinement scheme and shows comparable static performance figures as compared to conventional VCSELs.

Author contribution: Device design, fabrication and characterization as well as writing the paper.

**Paper D: Minority current distribution in InGaAs/GaAs transistor-vertical-cavity surface-emitting laser**
By comparing the experimental data and simulation, it is found that there is an inhomogeneous potential distribution along the base-collector interface. As a result, the device is operating at active mode in an interior part of the device while operating in the saturation mode globally. Future design optimizations regarding the base width and doping are proposed.

Author contribution: Device design, fabrication, and part of the characterizing as well as discussion of the results.
Paper E: 1.3 μm buried tunnel junction InGaAs/GaAs VCSELs
1.3-μm GaAs-based VCSEL using buried-tunnel junction current confinement was fabricated and characterized. Significantly reduced differential resistance at high drive current and better dynamic performance compared to epitaxial regrown pnp confined VCSEL was observed. A maximum single-mode power about 1.85 mW and 3db modulation bandwidth of 9 Ghz was achieved.

Author contribution: Device design and fabrication, and part of the characterization as well as writing the paper.
Reference

54. Lei C, Deng H, Dudley JJ, Lim SF, Liang B, Tashima M, et al., editors. Manufacturing of


56. Würtemberg RMv. Design and fabrication of long wavelength vertical cavity lasers on GaAs substrates. Stockholm: Royal Institute of Technology (KTH); 2008.


61. Xiang Y. To be published.
Appendixes

List of tools used in process

**Asterix**

**Full equipment name:** Aixtron 200/4 MOVPE  
**General purpose:** Horizontal reactor with gasfoil rotation. Growth of III/V epitaxial semiconductors. InP, GaAs, GaSb, InAs

**Pekka**

**Full equipment name:** Plasmalab 80Plus (Oxford PECVD System) Chamber A  
**General purpose:** Deposition of dielectric thin films

**APL-HMDS**

**Full equipment name:** YES-5E Vacuum Bake / Vapour Prime Processing System (Serial # 88487)  
**General purpose:** The YES HMDS system combines vapor priming and vacuum dehydration baking. Hexamethyldisilazane (HMDS) is used to improve photoresist adhesion to oxides. The HMDS reacts with the oxide surface in a process known as silylation, forming a strong bond to the surface. The methyls, meanwhile, will bond with the photoresist, enhancing the photoresist adhesion.

**DSW-Stepper**

**Full equipment name:** DSW 8500/2035 g-line stepper  
**General purpose:** Exposure of photoresist-coated wafers

**Esa**

**Full equipment name:** Plasmalab80Plus (Oxford RIE System) Chamber B  
**General purpose:** Reactive Ion Etching

**Tegal**

**Full equipment name:** Plasmaline 515  
**General purpose:** etching of photoresist film in oxygen plasma

**Gallus**

**Full equipment name:** Oxford Instrument ICP380 Etch System  
**General purpose:** Dry etching of GaAs and InP

**Barbara**

**Full equipment name:** Provac PAK 600 Coating System  
**General purpose:** Metal evaporation
Zita

**Full equipment name:** Balzers BAE 250 Coating System
**General purpose:** Metalization by thermal evaporation

STS

**Full equipment name:** Plasma Enhanced Chemical Vapor Deposition (PECVD)
**General purpose:** Deposition of silicon oxide, silicon nitride and amorphous silicon

Peo

**Full equipment name:** Programmable Process Furnace PEO-603
**General purpose:** Heat treatment of III-V material

KDF

**Full equipment name:** KDF 844NT
**General purpose:** Deposition of metals, metal alloys

The process of VCSEL is optimized based on tools in KTH electrum lab.

For more detail of these tools, please check lims.electrumlab.se.
Appendix 1: Epitaxially regrown VCSEL

A

Layer configuration of epitaxially regrown VCSEL
PL: 1220nm; Cavity: 1265nm

<table>
<thead>
<tr>
<th>Layer</th>
<th>Material</th>
<th>Mole fraction (x)</th>
<th>Thickness (nm)</th>
<th>[Na – Nd] (cm^-3)</th>
<th>Type</th>
<th>Dopant</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>GaAs</td>
<td>25</td>
<td>1.2x10^18</td>
<td>p</td>
<td></td>
<td>Zn</td>
</tr>
<tr>
<td>19</td>
<td>GaAs</td>
<td>134</td>
<td>1.2 x10^19</td>
<td>p</td>
<td></td>
<td>Zn</td>
</tr>
<tr>
<td>18</td>
<td>GaAs</td>
<td>50</td>
<td>1.2x10^18</td>
<td>p</td>
<td></td>
<td>Zn</td>
</tr>
<tr>
<td>17</td>
<td>GaAs</td>
<td>135</td>
<td>1.2 x10^17</td>
<td>p</td>
<td></td>
<td>Zn</td>
</tr>
<tr>
<td>16</td>
<td>Al(x)Ga(1-x)As</td>
<td>0.22 - 0</td>
<td>10</td>
<td>1x10^18</td>
<td>p</td>
<td>Zn</td>
</tr>
<tr>
<td>15</td>
<td>Al(x)Ga(1-x)As</td>
<td>0.22</td>
<td>30</td>
<td>1 x10^-8</td>
<td>p</td>
<td>Zn</td>
</tr>
<tr>
<td>14</td>
<td>Al(x)Ga(1-x)As</td>
<td>0 – 0.22</td>
<td>10</td>
<td>1 x10^-8</td>
<td>p</td>
<td>Zn</td>
</tr>
<tr>
<td>13</td>
<td>GaAs</td>
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<td></td>
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<tr>
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<td>In(x)Ga(1-x)As</td>
<td>0.42</td>
<td>7*</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>GaAs</td>
<td>41</td>
<td>U/D</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>Al(x)Ga(1-x)As</td>
<td>0.22 - 0</td>
<td>10</td>
<td>1 x10^18</td>
<td>n</td>
<td>Si</td>
</tr>
<tr>
<td>8</td>
<td>Al(x)Ga(1-x)As</td>
<td>0.22</td>
<td>30</td>
<td>1 x10^-8</td>
<td>n</td>
<td>Si</td>
</tr>
<tr>
<td>7</td>
<td>Al(x)Ga(1-x)As</td>
<td>0 – 0.22</td>
<td>10</td>
<td>1 x10^-8</td>
<td>n</td>
<td>Si</td>
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<tr>
<td>6</td>
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<td>608.7</td>
<td>1-2 x10^18</td>
<td>n</td>
<td>Si</td>
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<tr>
<td>5</td>
<td>GaAs</td>
<td>5</td>
<td>U/D</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Grading</td>
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<td>20</td>
<td>U/D</td>
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<tr>
<td>4</td>
<td>Al(x)Ga(1-x)As**</td>
<td>0.875</td>
<td>85.7</td>
<td>U/D</td>
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<tr>
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<td>U/D</td>
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<tr>
<td>3x35</td>
<td>GaAs**</td>
<td>73.1</td>
<td>U/D</td>
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<tr>
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<td>20</td>
<td>U/D</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2x35</td>
<td>Al(x)Ga(1-x)As**</td>
<td>0.875</td>
<td>85.7</td>
<td>U/D</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Grading</td>
<td></td>
<td>20</td>
<td>U/D</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>GaAs</td>
<td>500</td>
<td>U/D</td>
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</table>

*Calibrated for PL at as long wavelength as possible

**Graded interfaces

Regrowth structure 1

<table>
<thead>
<tr>
<th>Layer</th>
<th>Material</th>
<th>Mole fraction (x)</th>
<th>Thickness (nm)</th>
<th>[Na – Nd] (cm^-3)</th>
<th>Type</th>
<th>Dopant</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>GaAs</td>
<td>120</td>
<td>1-2 x10^18</td>
<td>n</td>
<td>Si</td>
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</tr>
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</table>
Regrowth structure 2 Low temperature 570C

<table>
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<th>Layer</th>
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<th>Mole fraction (x)</th>
<th>Thickness (nm)</th>
<th>[Na – Nd] (cm^-3)</th>
<th>Type</th>
<th>Dopant</th>
</tr>
</thead>
<tbody>
<tr>
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<td>70(69)</td>
<td>1.5 x10^17</td>
<td>p</td>
<td>Zn</td>
<td></td>
</tr>
<tr>
<td>3x3</td>
<td>GaAs</td>
<td>50</td>
<td>5 x10^19</td>
<td>p</td>
<td>Zn</td>
<td></td>
</tr>
<tr>
<td>2x3</td>
<td>GaAs</td>
<td>135</td>
<td>1.5 x10^17</td>
<td>p</td>
<td>Zn</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>GaAs</td>
<td>25</td>
<td>5 x10^19</td>
<td>p</td>
<td>Zn</td>
<td></td>
</tr>
</tbody>
</table>

B

Process list of epitaxially regrown VCSEL

1. Epitaxy

Growth according to specification by Asterix

2. Regrowth

Deposition of silicon oxide and nitride

Oxide etch

HCl:H2O, 1:2, 30 s.

Rinse in di-H2O.

Remove water droplets with N2 gun.

Deposit oxide in Pekka, 100 nm.

Deposition Nitride in Pekka, 60 nm

Lithography – Act1

HMDS, APL

Spinning, 4000 rpm, 30 s (712)

Hotplate, 95ºC, 60 s, contact hotplate

Exposure 0.31 s, DSW, Mar3Act1, Edge exposure

Hot-plate, 115ºC, 60 s, contact hotplate

Developing, 30 s, CD-26

Rinse in water, 1 min

Visual inspection

Nitride etch – Act1

Ash 30”, 15 mTorr, 45W, 25 sccm O2 (Esa)

Etch 7”, 15 mTorr, 45W, 25 sccm CF4 (Esa)

Ash 2”, 15 mTorr, 45W, 25 sccm O2 (Esa)

Removal of resist

Acetone + propanol + H2O, 5’ + 5’ + 5’

Ash 30”, 15 mTorr, 45W, 25 sccm O2 (Esa)

Lithography – Act2
HMDS, APL
Spinning, 4000 rpm, 30 s (712)
Hotplate, 95°C, 60 s, contact hotplate
Exposure 0.31 s, DSW, Mar3Act2, Edge exposure
Hot-plate, 115°C, 60 s, contact hotplate
Developing, 30 s, CD-26
Rinse in water, 1 min
Visual inspection

**Nitride etch – Act2**
Ash 30'', 15 mTorr, 45 W, 25 sccm O2 (Esa)
Etch 7'', 15 mTorr, 45 W, 25 sccm CF4 (Esa)
Ash 2', 15 mTorr, 45 W, 25 sccm O2 (Esa)

**Removal of resist**
Acetone + propanol + H2O, 5' + 5' + 5'
Ash 30'', 15 mTorr, 45 W, 25 sccm O2 (Esa)

**Oxide etch**
BHF:H2O, 1:25, 2'30''

**Nitride etch**
Etch 3’, 150 mTorr, 30 W, 45 sccm CF4, 5 sccm O2 (Esa)

**Oxide etch**
BHF:H2O, 1:25, 30''

**GaAs wet etch**
Etch,H2O:NH4OH:H2O2 (1000:20:7), 90'', no stirring, (Target 200 nm)

**Regrowth – blocking layer**
Regrowth according to specification
HCl:H2O, 1:2, 30 s.
Rinse in di-H2O.
Remove water droplets with N2 gun.
BHF etch to remove oxide mask, 30''

**Regrowth – conduction layer**
Regrowth according to specification

**Oxide deposition**
Deposit 200 nm Oxide (Pekka)

### 3. N-pit

**Lithography – N-pit**
HMDS, APL
Spinning, 4000 rpm, 30 s (712)
Hot-plate, 95°C, 60 s
Pattern exposure 0.31 s, DSW, Mar3npit, edge exposure
Hot-plate, 115°C, 60 s
Developing, 30 s, CD-26
Rinse H2O 1’
Visual inspection

Etching – N-pit oxide mask
Ash, 5’, (Tegal)/ 30”, 15 mTorr, 45W, 25 sccm O2 (Esa)
Etch, BHF:H2O 1:25, Rate approx 40 nm/min. (Target 250 nm).

GaAs etch – N-pit
RIE in Gallus – SiCl4 = 3 sccm, Ar = 2 sccm, P = 2 mTorr, RIE Power = 40 W, t = 8’ + 8’. Target 1200 nm
(Etch rate of photoresist is 1/3 of GaAs)
2’, 15 mTorr, 45W, 25 sccm O2 (Esa)
Acetone + propanol + H2O, 5’ + 5’ + 5’
2’, 15 mTorr, 45W, 25 sccm O2 (Esa)

Oxide etch
BHF 30”.

Nitride deposition
Deposit Si3N4 in Pekka, 135 nm, CiP21, 25’.

4. N-metal

Lithography – N-metal
HMDS,APL
Spinning, 4000 rpm, 30 s (S1818)
Hot-plate, 115ºC, 60 s
Pattern exposure 0.40s, DSW, Mar3nmp
Developing, 40 s, 351:H2O, 1:5, No agitation
Rinse H2O 1’
Visual inspection

Evaporation – N-metal
Ash, 15 mTorr, 45W, 25 sccm O2, 30s (Esa)
Etch, 15 mTorr, 45W, 25 sccm CF4, 5 sccm O2, 200 s (Esa)
Etch, 150 mTorr, 25W, 50 sccm CF4, 5 sccm O2, 100 s (Esa)
Ash, 150 mTorr, 25W, 50 sccm O2, 100s (Esa)
HCl:H2O, 1:2, 30 s.
Rinse in di-H2O.
Remove water droplets with N2 gun.
### Evaporation in Barbara

<table>
<thead>
<tr>
<th>Metal</th>
<th>Thickness [Å]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ti</td>
<td>100</td>
</tr>
<tr>
<td>Pd</td>
<td>400</td>
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<td>Ti</td>
<td>400</td>
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<tr>
<td>Ge</td>
<td>800</td>
</tr>
<tr>
<td>Pd</td>
<td>400</td>
</tr>
<tr>
<td>GaAs</td>
<td></td>
</tr>
</tbody>
</table>

**Lift-off N-metal**

Acetone beaker + blow
Propanol and di-H2O. Blow dry with N2 gun.
Visual inspection.
Ash in Tegal for 5 min, 200 W

### 5. P-metal

**Lithography – P-metal**

HMDS,APL
Spinning, 4000 rpm, 30 s (S1818)
Hot-plate, 115°C, 60 s
Pattern exposure 0.40s, DSW, Mar3pmp
Developing, 40 s, 351:H2O, 1:5, No agitation
Rinse H2O 1’
Visual inspection

**Evaporation –P-metal**

Ash, 15 mTorr, 45W, 25 sccm O2, 30s (Esa)
Etch, 15 mTorr, 45W, 25 sccm CF4, 5 sccm O2, 200 s (Esa)
Etch, 150 mTorr, 25W, 50 sccm CF4, 5 sccm O2,100 s (Esa)
Ash, 150 mTorr, 25W, 50sccm O2, 100s (Esa)
HCl:H2O, 1:2, 30 s.
Rinse in di-H2O.
Remove water droplets with N2 gun.

**Evaporation in Zita and Barbara**

<table>
<thead>
<tr>
<th>Metal</th>
<th>Thickness [Å]</th>
</tr>
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<td>Au</td>
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<td>270 (Z)</td>
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<tr>
<td>Au</td>
<td>50 (Z)</td>
</tr>
<tr>
<td>Wafer</td>
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</tbody>
</table>

**Lift-off P-metal**

Acetone beaker + blow
Propanol and di-H2O. Blow dry with N2 gun.
Visual inspection.
Ash in Tegal for 5 min, 200 W
6. Mirror hole

Lithography – Mirror hole
HMDS, APL
Spinning, 4000 rpm, 30 s (S1818)
Hot-plate, 115°C, 60 s
Pattern exposure 0.40s, DSW, Mar3mirr, 6, 7, 8, 9
Developing, 40 s, 351:H2O, 1:5, No agitation
Rinse H2O 1’
Visual inspection

Etch – Mirror hole
Ash, 15 mTorr, 45W, 25 sccm O2, 30s (Esa)
Etch, 15 mTorr, 45W, 25 sccm CF4, 5 sccm O2, 200 s (Esa)
Etch, 150 mTorr, 25W, 50 sccm CF4, 5 sccm O2, 100 s (Esa)
Ash, 150 mTorr, 25W, 50 sccm O2, 100s (Esa)
Resist removal (Acetone + 2-prop. + H2O + Tegal)

7. Mirror deposition

Deposit first top mirror layer, SiO2, 216 nm, STS
Anneal in Ulrika, 325C, 30 min
Deposit remainder of top mirror, and sio2 mask for surface relief
1x a-Si, 88 nm, STS
2x SiO2, 216 nm, STS
2x a-Si, 88 nm, STS
1x SiN, 158nm, STS
1x a-Si, 88 nm, STS

8. Surface relief

Lithography – surface relief
HMDS, APL
Spinning, 4000 rpm, 30 s (S1818)
Hot-plate, 115°C, 60 s
Pattern exposure 0.40s, DSW, Mar3rel
Developing, 40 s, 351:H2O, 1:5, No agitation
Rinse H2O 1’
Visual inspection

Mirror etch
Ash, 15 mTorr, 45W, 25 sccm O2, 30s (Esa)
Bake 120°C hotplate 1’ or convection oven 30’
BHF:H2O 1:25 2’30’’ etch oxide mask
Resist removal
Acetone + propanol + H2O + Tegal,
5’ + 5’ + 5’ + 5’
50% KOH 3’30” etch a-si
BHF 1:25 3’ etch oxide mask

**Lithography- Relief protection**
HMDS, APL
Spinning, 4000 rpm, 30 s (S1818)
Hot-plate, 115°C, 60 s
Pattern exposure 0.40s, DSW, Mar3relp
Developing, 40 s, 351:H2O, 1:5, No agitation
Rinse H2O 1’
Visual inspection

**SiN layer etch**
Ash, 15 mTorr, 45W, 25 sccm O2, 30s (Esa)
Convection oven 30’ 110 ºC
BHF etch SiN 158nm
Resist removal
Acetone + propanol + H20 + Tegal,
5’ + 5’ + 5’ + 5’

9. **Via holes**

**Lithography – Via holes**
HMDS, APL
Spinning, 4000 rpm, 30 s (S1818)
Hot-plate, 115°C, 60 s
Pattern exposure 0.50s, DSW, Mar3via
Developing, 40 s, 351:H2O, 1:5, No agitation
Rinse H2O 1’
Visual inspection

**Etch – Via holes**
4xAsh, 15 mTorr, 45W, 25sccm O2, 30” (Esa)
4xEtch, 15 mTorr, 45W, 25sccm CF4, 8’ (Esa).
4xEtch, 150 mTorr, 45W, 50sccm CF4, 5 sccm O2, 3’ (Esa).
4xEtch, 15 mTorr, 45W, 25sccm CHF3, 25’ (Esa).

**Removal of resist**
Ash, 15 mTorr, 45W, 25sccm O2, 2’ (Esa)
Acetone + propanol + H20 + Tegal,
5’ + 5’ + 5’ + 5’

10. **Surface metal**

**Sputtering**
Sputter in KDF:
TiW, 1.5kw, speed 75, pass 8
Au, 1.5kw, speed 200, pass 8

**Lithography – Surface metal**

HMDS, APL
Spinning, 4000 rpm, 30 s (Si818)
Hot-plate, 115°C, 60 s
Pattern exposure 0.40s, DSW, Mar3sup
Developing, 60 s, 351:H2O, 1:5, Agitation
Rinse H2O 1’
Visual inspection

**Plating – Surface metal**

Ash, 15 mTorr, 45W, 25 sccm O2, 30s (Esa)
Plate 4.5 mA, 35’
(Choose current according to the open area on the wafer. (1cm^2 = 1mA))
Ash, 15 mTorr, 45W, 25 sccm O2, 2’ (Esa)
Acetone + propanol + H2O + Tegal, 5’ + 5’ + 5’ + 5’

**Etch - Surface metal**

Au KI-etch, 3’30” (Check every minute)
TiW H2O2-etch, 15’
Sketch of process flow of epitaxially regrown VCSEL

Fig17(a). VCSEL base structure

Fig17(b). Mesa definition and etching

Fig17(c). First regrowth step (n-type, red region)

Fig17(d). Second regrowth step (p-type) and removal of oxide mask

Fig17(e). Dielectric DBR, contacts (n, p)
Appendix 2: Epitaxially regrown VCSEL with intra-cavity patterning

A
Layer configuration of epitaxially regrown VCSEL with intra-cavity patterning.
See Appendix 1 A

B
Process list of epitaxially regrown VCSEL with intra-cavity patterning
See Appendix 1 B, most process procedure is same. Except some minor change as following:

1. Add inter-cavity pattern between Step 2 (Regrowth) and Step 3 (N-pit)

Intra-cavity patterning
Lithography – Intra-cavity patterning
HMDS, APL
Spinning, 4000 rpm, 30 s (712)
Hot-plate, 95°C, 60 s
Pattern exposure 0.31 s, DSW, xinse
Hot-plate, 115°C, 60 s
Developing, 30 s, CD-26
Rinse H2O 1’
Visual inspection
Etching – etch oxide mask
Ash, 5’, (Tegal)/ 30”, 15 mTorr, 45W, 25 sccm O2 (Esa)
Etch, BHF:H2O 1:25, Rate approx 40 nm/min. (Target 250 nm).
Acetone + propanol + H2O, 5’ + 5’ + 5’
Ash, 5’, (Tegal)/ 30”, 15 mTorr, 45W, 25 sccm O2 (Esa)
GaAs etch – Intracavity patterning
RIE in Gallus – SiCl4 = 3 sccm, Ar = 2 sccm, P = 2 mTorr, RIE Power = 40 W. 10’’ Target 10 nm
Oxide etch
BHF remove the mask
Oxide deposition
Deposit 200 nm Oxide (Pekka)

2. Remove step 8 (Surface relief)
Sketch of process flow of regrown VCSEL with intra-cavity patterning

Please see figure 17, put figure 18 between figure 17 (d) and (e).

Fig18. Intra-cavity patterning
Appendix 3: BTJ VCSEL

A
Layer configuration of BTJ VCSEL

PL: 1220nm; Cavity: 1265nm

<table>
<thead>
<tr>
<th>Layer</th>
<th>Material</th>
<th>Mole fraction (x)</th>
<th>Thickness (nm)</th>
<th>[Na – Nd] (cm^3)</th>
<th>Type</th>
<th>Dopant</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>GaAs</td>
<td>20</td>
<td>2 x10^{18}</td>
<td>n</td>
<td>Si</td>
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<tr>
<td>19</td>
<td>In(x)Ga(1-x)As</td>
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<td>20</td>
<td>1 x10^{19}</td>
<td>n</td>
<td>Si/Te</td>
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<tr>
<td>18</td>
<td>GaAs</td>
<td>10</td>
<td>1 x10^{17}</td>
<td>p</td>
<td>C/Zn</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>GaAs</td>
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<td>1-2 x10^{17}</td>
<td>p</td>
<td>Zn</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>Al(x)Ga(1-x)As</td>
<td>0.22 - 0</td>
<td>10</td>
<td>1 x10^{18}</td>
<td>p</td>
<td>Zn</td>
</tr>
<tr>
<td>15</td>
<td>Al(x)Ga(1-x)As</td>
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<td>30</td>
<td>1 x10^{18}</td>
<td>p</td>
<td>Zn</td>
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<tr>
<td>14</td>
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<tr>
<td>13</td>
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<td>11x3</td>
<td>In(x)Ga(1-x)As</td>
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</tr>
<tr>
<td>10</td>
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<td>U/D</td>
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</tr>
<tr>
<td>9</td>
<td>Al(x)Ga(1-x)As</td>
<td>0.22 - 0</td>
<td>10</td>
<td>1 x10^{18}</td>
<td>n</td>
<td>Si</td>
</tr>
<tr>
<td>8</td>
<td>Al(x)Ga(1-x)As</td>
<td>0.22</td>
<td>30</td>
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<td>n</td>
<td>Si</td>
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<tr>
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<td>Al(x)Ga(1-x)As</td>
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<tr>
<td>6</td>
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<td>GaAs</td>
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<td>U/D</td>
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<td></td>
</tr>
<tr>
<td></td>
<td>Grading</td>
<td>20</td>
<td>U/D</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Al(x)Ga(1-x)As**</td>
<td>0.875</td>
<td>85.7</td>
<td>U/D</td>
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<td></td>
</tr>
<tr>
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<td>Grading</td>
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<td>U/D</td>
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<td></td>
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</tr>
<tr>
<td>3x35</td>
<td>GaAs**</td>
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<td>U/D</td>
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<td></td>
</tr>
<tr>
<td></td>
<td>Grading</td>
<td>20</td>
<td>U/D</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2x35</td>
<td>Al(x)Ga(1-x)As**</td>
<td>0.875</td>
<td>85.7</td>
<td>U/D</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Grading</td>
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<td>U/D</td>
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<tr>
<td>1</td>
<td>GaAs</td>
<td>500</td>
<td>U/D</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Calibrated for PL at as long wavelength as possible
**Graded interfaces

Regrowth structure

<table>
<thead>
<tr>
<th>Layer</th>
<th>Material</th>
<th>Mole fraction (x)</th>
<th>Thickness (nm)</th>
<th>[Na – Nd] (cm^3)</th>
<th>Type</th>
<th>Dopant</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GaAs</td>
<td>810</td>
<td>1-2 x10^{18}</td>
<td>n</td>
<td>Si</td>
<td></td>
</tr>
</tbody>
</table>
B

Process list of BTJ VCSEL

See Appendix 1 B, most process procedure is same. Except some minor change as following:

1. Change step 2 (Regrowth) to list below.

Regrowth

Deposition of silicon oxide and nitride
Oxide etch
HCl:H2O, 1:2, 30 s.
Rinse in di-H2O.
Remove water droplets with N2 gun.
Deposit oxide in Pekka, 100 nm.
Deposition Nitride in Pekka, 60 nm
Lithography – Act1
HMDS, APL
Spinning, 4000 rpm, 30 s (712)
Hotplate, 95°C, 60 s, contact hotplate
Exposure 0.31 s, DSW, Mar3Act1, Edge exposure
Hot-plate, 115°C, 60 s, contact hotplate
Developing, 30 s, CD-26
Rinse in water, 1 min
Visual inspection
Nitride etch – Act1
Ash 30”, 15 mTorr, 45W, 25 sccm O2 (Esa)
Etch 7”, 15 mTorr, 45W, 25 sccm CF4 (Esa)
Ash 2”, 15 mTorr, 45W, 25 sccm O2 (Esa)
Removal of resist
Acetone + propanol + H2O, 5’ + 5’ + 5’
Ash 30”, 15 mTorr, 45W, 25 sccm O2 (Esa)

Lithography – Act2
HMDS, APL
Spinning, 4000 rpm, 30 s (712)
Hotplate, 95°C, 60 s, contact hotplate
Exposure 0.31 s, DSW, Mar3Act2, Edge exposure
Hot-plate, 115°C, 60 s, contact hotplate
Developing, 30 s, CD-26
Rinse in water, 1 min
Visual inspection
Nitride etch – Act2
Ash 30”, 15 mTorr, 45W, 25 sccm O2 (Esa)
Etch 7”, 15 mTorr, 45W, 25 sccm CF4 (Esa)
Ash 2”, 15 mTorr, 45W, 25 sccm O2 (Esa)

**Removal of resist**
Acetone + propanol + H2O, 5’ + 5’ + 5’
Ash 30”, 15 mTorr, 45W, 25 sccm O2 (Esa)

**Oxide etch**
BHF:H2O, 1:25, 2’30”

**Nitride etch**
Etch 3’, 150 mTorr, 30W, 45 sccm CF4, 5 sccm O2 (Esa)

**Oxide etch**
BHF:H2O, 1:25, 30’

**GaAs wet etch**
Etch,H2O:NH4OH:H2O2 (1000:20:7), 20”, no stirring, (Target 55 nm)

**Oxide Mask remove**
BHF etch to remove oxide mask, 30”

**Regrowth – conduction layer**
Regrowth according to specification

**Oxide deposition**
Deposit 200 nm Oxide (Pekka)

2. Remove step 4 (N-metal) and 5 (P-metal) and use the following list instead.

**N-P metal contact**

**Lithography – N-P metal**
HMDS, APL
Spinning, 4000 rpm, 30 s (S1818)
Hot-plate, 115ºC, 60 s
Pattern exposure 0.40s, DSW, Mar3nmp, Mar3pnmm
Developing, 40 s, 351:H2O, 1:5, No agitation
Rinse H2O 1’
Visual inspection

**Evaporation – N-P metal**
Ash, 15 mTorr, 45W, 25 sccm O2, 30s (Esa)
Etch, 15 mTorr, 45W, 25 sccm CF4, 5 sccm O2, 200 s (Esa)
Etch, 150 mTorr, 25W, 50 sccm CF4, 5 sccm O2, 100 s (Esa)
Ash, 150 mTorr, 25W, 50 sccm O2, 100s (Esa)
HCl:H2O, 1:2, 30 s.
Rinse in di-H2O.
Remove water droplets with N2 gun.
Evaporation in Barbara

<table>
<thead>
<tr>
<th>Metal</th>
<th>Thickness [Å]</th>
</tr>
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<tr>
<td>Ti</td>
<td>100</td>
</tr>
<tr>
<td>Pd</td>
<td>400</td>
</tr>
<tr>
<td>Ti</td>
<td>400</td>
</tr>
<tr>
<td>Ge</td>
<td>800</td>
</tr>
<tr>
<td>Pd</td>
<td>400</td>
</tr>
<tr>
<td>GaAs</td>
<td></td>
</tr>
</tbody>
</table>

**Lift-off N-P metal**

Acetone beaker + blow

Propanol and di-H2O. Blow dry with N2 gun.

Visual inspection.

Ash in Tegal for 5 min, 200 W

---

**C**

**Sketch of process flow of BTJ VCSELs.**

Please see figure 17, remove the figure 17(c).
### Appendix 4: Transistor VCSEL

#### A

Layer configuration of buried transistor VCSEL

**PL: 965nm; Cavity: 980nm**

<table>
<thead>
<tr>
<th>No.</th>
<th>Material</th>
<th>Mole fraction, x</th>
<th>Thickness (nm)</th>
<th>Doping (cm⁻³)</th>
<th>Periods</th>
</tr>
</thead>
<tbody>
<tr>
<td>26</td>
<td>GaAs</td>
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<td>100</td>
<td>Zn: 2×10¹⁷</td>
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<tr>
<td>25</td>
<td>GaAs</td>
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<td>40</td>
<td>Zn: 2×10¹⁸</td>
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<tr>
<td>24</td>
<td>GaAs</td>
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<td>74.4</td>
<td>Zn: 2×10¹⁷</td>
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<tr>
<td>23</td>
<td>GaAs</td>
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<td>36.2</td>
<td>Zn: 2×10¹⁸</td>
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<tr>
<td>22</td>
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<td>Zn: 2×10¹⁸</td>
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<tr>
<td>21</td>
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<td>0.875</td>
<td>40</td>
<td>Zn: 2×10¹⁸</td>
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</tr>
<tr>
<td>20</td>
<td>AlₙGa₁₋ₙAs₀-₀.₈₇₅</td>
<td>0-0.875</td>
<td>10</td>
<td>Zn: 2×10¹⁷</td>
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</tr>
<tr>
<td>19</td>
<td>GaAs</td>
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<td>237</td>
<td>Si: 6×10¹⁸</td>
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<tr>
<td>18</td>
<td>GaAs</td>
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<td>15</td>
<td>U/D</td>
<td>1</td>
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<tr>
<td>17</td>
<td>GaAs</td>
<td>-</td>
<td>16</td>
<td>U/D</td>
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<td>16</td>
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<td>U/D</td>
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<td>15</td>
<td>GaAs</td>
<td>-</td>
<td>15</td>
<td>U/D</td>
<td>1</td>
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<tr>
<td>14</td>
<td>GaAs</td>
<td>-</td>
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<td>Si: 6×10¹⁸</td>
<td>1</td>
</tr>
<tr>
<td>13</td>
<td>GaAs</td>
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<td>40</td>
<td>U/D</td>
<td>1</td>
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<tr>
<td>10</td>
<td>GaAs</td>
<td>-</td>
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<td>9</td>
<td>GaAs</td>
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<td>48</td>
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<td>8</td>
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<td>20</td>
<td>U/D</td>
<td>36</td>
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<tr>
<td>3</td>
<td>AlₙGa₁₋ₙAs₀.₈₇₅</td>
<td>0.875</td>
<td>60.4</td>
<td>U/D</td>
<td>36</td>
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<tr>
<td>2</td>
<td>AlₙGa₁₋ₙAs₀-₀.₈₇₅</td>
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<td>20</td>
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<td>36</td>
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<td>GaAs</td>
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Regrowth structure 1

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<th>No.</th>
<th>Material</th>
<th>Mole fraction, x</th>
<th>Thickness (nm)</th>
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<th>Periods</th>
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<tr>
<td>1</td>
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Regrowth structure 2

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<th>Thickness (nm)</th>
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<tr>
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<tr>
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<td>GaAs</td>
<td>-</td>
<td>40</td>
<td>(\text{Zn: }2\times10^{18})</td>
<td>4</td>
</tr>
</tbody>
</table>

**B**

**Process list of Transistor VCSEL**

1. **Epitaxy**

   **Growth according to specification**

2. **Regrowth**

   **Deposition of silicon oxide and nitride**

   Oxide etch  
   HCl:H\(_2\)O, 1:2, 30 s.  
   Rinse in di-H\(_2\)O.  
   Remove water droplets with N2 gun.  
   Deposition  
   Deposit oxide in Pekka, 100 nm.  
   Co-run a piece of silicon for ellipsometry in Rudolph.  
   Deposition Nitride in Pekka, 60 nm  

   **Lithography – Act1**

   HMDS, APL  
   Spinning, 4000 rpm, 30 s (712)  
   Hotplate, 95°C, 60 s, contact hotplate  
   Exposure 0.31 s, DSW, \(\text{xin2Act1}\), Edge exposure  
   Hot-plate, 115°C, 60 s, contact hotplate  
   Developing, 30 s, CD-26  
   Rinse in water, 1 min
Visual inspection

**Nitride etch – Act1**
- Ash 30”, 15 mTorr, 45W, 25 sccm O2 (Esa)
- Etch 7’, 15 mTorr, 45W, 25 sccm CF4 (Esa)
- Ash 2’, 15 mTorr, 45W, 25 sccm O2 (Esa)

**Removal of resist**
- Acetone + propanol + H2O, 5’ + 5’ + 5’
- Ash 30”, 15 mTorr, 45W, 25 sccm O2 (Esa)

**Lithography – Act2**

**HMDS,APL**
- Spinning, 4000 rpm, 30 s (712)
- Hotplate, 95ºC, 60 s, contact hotplate
- Exposure 0.31 s, DSW, xin2Act2, Edge exposure
- Hot-plate, 115ºC, 60 s, contact hotplate
- Developing, 30 s, CD-26
- Rinse in water, 1 min

**Visual inspection**

**Nitride etch – Act2**
- Ash 30”, 15 mTorr, 45W, 25 sccm O2 (Esa)
- Etch 7’, 15 mTorr, 45W, 25 sccm CF4 (Esa)
- Ash 2’, 15 mTorr, 45W, 25 sccm O2 (Esa)

**Removal of resist**
- Acetone + propanol + H2O, 5’ + 5’ + 5’
- Ash 30”, 15 mTorr, 45W, 25 sccm O2 (Esa)

**Oxide Mask etch**
- BHF:H2O, 1:25, 2’30”

**Nitride mask etch**
- Etch 3’, 150 mTorr, 30W, 45 sccm CF4, 5 sccm O2 (Esa)

**Remove oxidation**
- HCL:H2O, 1:2, 2’30”

**GaAs wet etch**
- Etch,H2O:NH4OH:H2O2 (1000:20:7), 90”, no stirring, (Target 200 nm)

**Regrowth – blocking layer**
- Regrowth according to specification
- BHF etch to remove oxide mask, 30”

**Alignment mark protection**
- Deposit 100 nm Oxide (Pekka)

**Lithography – Xinalp\mapreg,2,3,4,5,7,8,9,10**
- Ash 5’, 100 mTorr, 45W, 30 sccm O2 (ARIEL)
- BHF 2’ remove oxide mask
- Acetone + propanol + H2O, 5’ + 5’ + 5’
- Ash 5’, 100 mTorr, 45W, 30 sccm O2 (ARIEL)
- HCL:H2O, 1:2, 30”
- Bubble 5’
Regrowth – conduction layer
Regrowth according to specification………
BHF 2’ remove oxide mask

*Shallow etch patterning
(Can be skipped if no shallow etch structure needed)
Deposit 100 nm Oxide (Pekka)
Lithography map xinsetch\mapreg,1
Ash 5’, 100 mTorr, 45W, 30 sccm O2 (ARIEL)
BHF 1:25 2’30” oxide etch
Acetone + propanol + H2O, 5’ + 5’ + 5’
Ash 5’, 100 mTorr, 45W, 30 sccm O2 (ARIEL)
HCL 1:2 30” oxide remove
H2O:NH4OH:H2O2 2000:10:3.5 5” Target 5nm
BHF 30” oxide etch
Oxide deposition
Deposit 200 nm Oxide (Pekka)

3. Base-pit

Lithography – B-pit
HMDS, APL
Spinning, 4000 rpm, 30 s (712)
Hot-plate, 95°C, 60 s
Pattern exposure 0.31s, DSW, xin2bpit, edge exposure
Hot-plate, 115°C, 60 s
Developing, 30 s, CD-26
Rinse H2O 1’
Visual inspection

Etching – B-pit oxide mask
Ash, 5’, (Tegal)/ 30”, 15 mTorr, 45W, 25 sccm O2 (Esa)
Etch, BHF:H2O 1:25, Rate approx 40 nm/min. Check on test sample. (Target 250 nm).

GaAs etch – B-pit
RIE in Gallus – SiCl4 = 3 sccm, Ar = 2 sccm, P = 2 mTorr, RIE Power = 40 W, t = 6’20” + 6’20”.
2’, 15 mTorr, 45W, 25 sccm O2 (Esa)
Acetone + propanol + H2O, 5’ + 5’ + 5’
2’, 15 mTorr, 45W, 25 sccm O2 (Esa)

Oxide etch
BHF 30”.
Oxide deposition
Deposit 200 nm Oxide (Pekka)
4. Collector-pit

Lithography – C-pit
HMDS, APL
Spinning, 4000 rpm, 30 s (712)
Hot-plate, 95°C, 60 s
Pattern exposure 0.31s, DSW, xin2cpit, edge exposure
Hot-plate, 115°C, 60 s
Developing, 30 s, CD-26
Rinse H2O 1’
Visual inspection

Etching – C-pit oxide mask
Ash, 5’, (Tegal)/ 30”, 15 mTorr, 45W, 25 sccm O2 (Esa)
Etch, BHF:H2O 1:25, Rate approx 40 nm/min. Check on test sample. (Target 250 nm).

GaAs etch – C-pit
RIE in Gallus – SiCl4 = 3 sccm, Ar = 2 sccm, P = 2 mTorr, RIE Power = 40 W, t = 6’20” + 6’20”.
2’, 15 mTorr, 45W, 25 sccm O2 (Esa)
Acetone + propanol + H2O, 5’ + 5’ + 5’
2’, 15 mTorr, 45W, 25 sccm O2 (Esa)

Oxide etch
BHF 30”.

Nitride deposition
Deposit Si3N4 in Pekka, 135 nm, CiP21, 25’.

5. N-metal

Lithography – N-metal
HMDS, APL
Spinning, 4000 rpm, 30 s (S1818)
Hot-plate, 115°C, 60 s
Pattern exposure 0.40s, DSW, xin2nmp
Developing, 40 s, 351:H2O, 1:5, No agitation
Rinse H2O 1’
Visual inspection
Evaporation – N-metal
Ash, 15 mTorr, 45W, 25 sccm O2, 30s (Esa)
Etch, 15 mTorr, 45W, 25 sccm CF4, 5 sccm O2, 200 s (Esa)
Etch, 150 mTorr, 25W, 50 sccm CF4, 5 sccm O2, 100 s (Esa)
Ash, 150 mTorr, 25W, 50sccm O2, 100s (Esa)
HCl:H2O, 1:2, 2’30”
Evaporation in Barbara

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<th>Thickness [Å]</th>
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<td>GaAs</td>
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**Lift-off N-metal**

Acetone beaker + blow
Propanol and di-H2O. Blow dry with N2 gun.
Visual inspection.
Ash in Tegal for 5 min, 200 W

**6. P-metal**

**Lithography – P-metal**

HMDS, APL
Spinning, 4000 rpm, 30 s (S1818)
Hot-plate, 115ºC, 60 s
Pattern exposure 0.40s, DSW, Xin2mp
Developing, 40 s, 351:H2O, 1:5, No agitation
Rinse H2O 1’
Visual inspection

**Evaporation – P-metal**

Ash, 15 mTorr, 45W, 25 sccm O2, 30s (Esa)
Etch, 15 mTorr, 45W, 25 sccm CF4, 5 sccm O2, 200 s (Esa)
Etch, 150 mTorr, 25W, 50 sccm CF4, 5 sccm O2, 100 s (Esa)
Ash, 150 mTorr, 25W, 50sccm O2, 100s (Esa)
HCL:H2O, 1:2, 2’30”

Evaporation in Zita and Barbara

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<th>Metal</th>
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**Lift-off P-metal**

Acetone beaker + blow
Propanol and di-H2O. Blow dry with N2 gun.
Visual inspection.
Ash in Tegal for 5 min, 200 W
7. Mirror hole

Lithography – Mirror hole
HMDS, APL
Spinning, 4000 rpm, 30 s (S1818)
Hot-plate, 115ºC, 60 s
Pattern exposure 0.40s, DSW, Xin2mirr, 6, 7, 8, 9
Developing, 40 s, 351:H2O, 1:5, No agitation
Rinse H2O 1’
Visual inspection

Etch – Mirror hole
Ash, 15 mTorr, 45W, 25 sccm O2, 30s (Esa)
Etch, 15 mTorr, 45W, 25 sccm CF4, 5 sccm O2, 200 s (Esa)
Etch, 150 mTorr, 25W, 50 sccm CF4, 5 sccm O2, 100 s (Esa)
Ash, 150 mTorr, 25W, 50sccm O2, 100s (Esa)
Resist removal (Acetone + 2-prop. + H2O + Tegal)

8. Mirror deposition

Deposit first top mirror layer, SiO2, 168 nm, STS
Anneal in PEO, 325C, 30 min
Deposit remainder of top mirror, and sio2 mask for surface relief
1x a-Si, 68 nm, STS
2x SiO2, 168 nm, STS
2x a-Si, 68 nm, STS

9. Via holes

Lithography – Via holes
HMDS, APL
Spinning, 4000 rpm, 30 s (S1818)
Hot-plate, 115ºC, 60 s
Pattern exposure 0.50s, DSW, Xin2via
Developing, 40 s, 351:H2O, 1:5, No agitation
Rinse H2O 1’
Visual inspection

Etch – Via holes
4xAsh, 15 mTorr, 45W, 25sccm O2, 30’ (Esa)
4xEtch, 15 mTorr, 45W, 25sccm CF4, 6’ (Esa).
4xEtch, 150 mTorr, 45W, 50sccm CF4, 5 sccm O2, 3’ (Esa).
4xEtch, 15 mTorr, 45W, 25sccm CHF3, 20’ (Esa).

Removal of resist
Ash, 15 mTorr, 45W, 25sccm O2, 2’ (Esa)
Acetone + propanol + H2O + Tegal,
10. Surface metal

Sputtering
Sputter in KDF:
TiW, 1.5kw, speed 75, pass 8
Au, 1.5kw, speed 200, pass 8

Lithography – Surface metal
HMDS, APL
HMDS, 10 min
Spinning, 4000 rpm, 30 s (S1818)
Hot-plate, 115°C, 60 s
Pattern exposure 0.40 s, DSW, Xin2 sup
Developing, 60 s, 351:H2O, 1:5, Agitation
Rinse H2O 1'
Visual inspection

Plating – Surface metal
Ash, 15 mTorr, 45W, 25 sccm O2, 30 s (Esa)
Plate 4.5 mA, 35’
Ash, 15 mTorr, 45W, 25 sccm O2, 2’ (Esa)
Acetone + propanol + H2O + Tegal,
5’ + 5’ + 5’ + 5’

Etch - Surface metal
Au KI-etch, 3’30” (Check every minute)
TiW H2O2-etch, 15’
Sketch of process flow of Transistor VCSELs.

Fig 19(a). Transistor VCSEL base structure

Fig 19(b). Emitter mesa definition and etching

Fig 19(c). Regrowth of current confinement layer (yellow region)

Fig 19(d). Removal of oxide mask and second regrowth

Fig 19(e). Base and collector meds define.

Fig 19(f). Contact evaporation and mirror deposition