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Examensarbete

## **A Study and Design of High Performance Voltage-Controlled Oscillators in 65nm CMOS Technology**

Master thesis performed in **Electronic Devices**

by

**Kamran Afghari**

LiTH-ISY-EX--12/4646--SE

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<b>Abstract</b>  In recent years, oscillators are considered as inevitable blocks in many electronic systems. They are commonly used in digital circuits to provide clocking and in analog/RF circuits of communication transceivers to support frequency conversion. Nowadays, CMOS technology is the most applicable solution for VLSI and especially for modern integrated circuits used in wireless communications. The main purpose of this project is to design a high performance voltage-controlled oscillator (LC VCO) using 65nm CMOS technology. To meet the state-of-the-art requirements, several circuit solutions have been explored and the design work ended-up with a Quadrature VCO. The circuit operates at center frequency of 2.4 GHz. The phase noise of QVCO obtained by simulation is -140 dBc/Hz at 1MHz offset frequency which is 6 dB less compared to conventional LC VCOs. The power consumption is 3.6mW and the tuning voltage can be swept from 0.2 V to 1.2 V resulting in 2.25 GHz - 2.55 GHz frequency range.
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<b>Keywords</b> QVCO, Power Consumption, Phase Noise, Tuning Voltage, Communication Transceivers
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## Abstract

In recent years, oscillators are considered as inevitable blocks in many electronic systems. They are commonly used in digital circuits to provide clocking and in analog/RF circuits of communication transceivers to support frequency conversion. Nowadays, CMOS technology is the most applicable solution for VLSI and especially for modern integrated circuits used in wireless communications. Additionally, the trend towards single chip implementation makes the circuit design increasingly challenging.

The main purpose of this project is to design a high performance voltage-controlled oscillator (LC VCO) using 65nm CMOS technology. In the beginning, a brief study of different VCO architectures is carried out. Next, a wide comparison between different VCO topologies is performed in terms of phase noise and power consumption. The effect of VCO phase noise on RF transceivers is also analyzed. In the following, all the phase noise contributors in a typical LC VCO are identified to enable design optimization.

To meet the state-of-the-art requirements, several circuit solutions have been explored and the design work ended-up with a Quadrature VCO. The design is verified for the intended tuning range and process, temperature, and supply voltage (PTV) variations.

The circuit operates at center frequency of 2.4 GHz. The phase noise of QVCO obtained by simulation is -140 dBc/Hz at 1MHz offset frequency which is 6 dB less compared to conventional LC VCOs. The power consumption is 3.6mW and the tuning voltage can be swept from 0.2 V to 1.2 V resulting in 2.25 GHz - 2.55 GHz frequency range.



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## Abbreviations

VCO	Voltage-Controlled Oscillator
QVCO	Quadrature Voltage-Controlled Oscillator
Q	Quality factor
FOM	Figure of Merit
PLL	Phase-Locked Loop
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
IF	Intermediate Frequency
RF	Radio Frequency
OFDM	Orthogonal Frequency-Division Multiplexing
QAM	Quadrature Amplitude Modulation
DC	Direct Current
ISF	Impulse Sensitivity Function
AM	Amplitude Modulation



# 1. INTRODUCTION

Nowadays, oscillators are considered as inevitable blocks in many electronic devices. They are mainly applicable in communication systems such as radio transceivers. Also, other applications take advantage of high performance oscillators. For instance, clock generation in microprocessors can be achieved by some types of VCOs. Today, CMOS technology is the most popular solution for designing a high performance voltage-controlled oscillator. It should be pointed out that in most cases a VCO is not a standalone block but rather a part of a larger system like PLL-based frequency synthesizer.

## 1.1 Objective and Scope

The first objective of this project was a broad analysis of different VCO topologies used in the contemporary applications. A specific objective was to design a high performance VCO based on a design study of different LC VCO circuits. By practical comparison of critical specifications like phase noise and power consumption the choice of the right circuit could be done. To meet the state-of-the-art specifications, a quadrature VCO (QVCO) was chosen as the ultimate design goal.

The QVCO was assumed to drive a balanced mixer for frequency conversion in a data OFDM transceiver. Since the OFDM-QAM signal is extremely sensitive to the local oscillator phase noise, the phase noise was the primary specification that the QVCO was optimized for. Additionally, to check for the application in a PLL, the process, temperature, and supply voltage (PTV) variations and tuning range were taken carefully into account.

## 1.2 VCO Design Specifications

To design a VCO, different requirements should be fulfilled. In this section, we define the VCO metrics individually. In particular, we should meet the oscillation frequency, power consumption, tuning range and phase noise requirements which are the most important in a VCO design. The oscillation frequency may vary from one design to another due to different applications and architectures. The tuning voltage range is determined by required frequency variations in different applications. The other major issues that should be considered especially in a high performance VCO design are phase noise and power consumption. Generally, it is difficult to fulfill all of the requirements at the same time. For instance, there is usually a tradeoff between power consumption and phase noise. On the other hand, some VCO topologies can improve the phase noise performance while other architectures can dissipate less power. Consequently, regarding the design specifications and their priorities, the designers have to choose the appropriate VCO topology but still are exposed to design tradeoffs.

The specifications for our ultimate VCO design aimed at 65-nm CMOS technology are as shown in Table 1.1.

QVCO specifications	Value
Center frequency	2.4 GHz
Supply voltage	1.2 V
Phase noise at 1MHz offset frequency	< -130 dBc/Hz
Power consumption	< 5 mW
Tuning voltage	0.2 - 1.2 V
Frequency range	2.25 - 2.55 GHz

Table 1.1: Ultimate VCO design specifications

### **1.3 VCOs in Phase-Locked Loops**

Voltage-controlled oscillators are mostly implemented as a component of phase-locked loops (PLLs). PLLs can be used in different areas such as clocking of microprocessors, providing carriers for wireless transceivers or other transmission systems. Usually, in communication applications PLLs require VCOs with a wide tuning range to serve up- or down-conversion over the system bandwidth. Interestingly, in PLLs the VCO phase noise requirements can be relaxed. In other words, the noise produced by a voltage-controlled oscillator at the oscillation frequency will be to some extent filtered out by the system. Therefore, VCO topologies with wide tuning range are usually preferred.

In high performance applications where a low phase noise or jitter is required, VCOs using LC tanks are preferred for their high Q-factor. Therefore, LC-based VCOs will be in focus of the presented designs.

### **1.4 Thesis Organization**

In this project, firstly, various VCO architectures are analyzed in detail. In particular, regarding phase noise and power consumption, a wide comparison is carried out. As a result, we have come up to the state-of-the-art design in which the VCO specifications can be fulfilled.

In the following chapter, the foundations of the oscillator theory are discussed. Moreover, different VCO architectures such as the ring oscillator, negative  $g_m$  oscillator, and CMOS LC VCOs are analyzed. At the end of this chapter the advantages and drawbacks regarding different topologies are compared.

In Chapter 3, we study the oscillator noise using different models acknowledged in literature. Afterwards, the phase noise is defined and its effect on an RF transceiver is analyzed. Finally, the phase noise contributors in a VCO are discussed.

In chapter 4, some state of the art topologies are presented and their specification requirements are defined.

In Chapter 5, seven variants of low-noise low-power LC VCO are designed for the same power consumption and then they are compared in terms of phase noise.

In Chapter 6, complementary simulations of the QVCO regarding PTV variations are presented showing it is in line with the state-of-the-art designs.

In Chapter 7, conclusions from the presented design are provided. At the end of this chapter, the performance of the designed LC QVCO circuit is compared with other reported LC VCOs.

## 2. OSCILLATOR BASICS

### 2.1 Introduction

In the second chapter, we describe the basic oscillation theory. This theory refers to the feedback system model or the negative resistance one-port model. Different types of oscillators including the ring, negative  $g_m$  oscillators, CMOS LC VCOs and some other topologies are discussed. Nowadays, among different types of oscillators, mostly the LC cross-coupled VCOs are preferred. Hence, their advantages and drawbacks are mainly emphasized in this project.

### 2.2 Oscillator Transfer Function

A VCO can be modeled as a feedback system as shown in Fig. 2.1. The equivalent transfer function of this system can be formulated as:

$$G(j\omega) = \frac{Y(j\omega)}{H(j\omega)} = \frac{H(j\omega)}{1-H(j\omega)} \quad (2.1)$$

According to the above equation, at the desired frequency of  $\omega_0$ , if  $H(j\omega_0)=1$ , the closed loop gain will be driven to infinity. It causes the system noise to increase and produces a periodic signal. From another point of view, the oscillation will be stable if  $H(j\omega_0)$  is precisely on the imaginary axis [11]. Practically, the small signal loop gain should be at least two to fulfill the initial oscillation conditions. As we know, this value decreases gradually and goes to unity as the amplitude improves due to the nonlinearities.

The following equations are two conditions that should be satisfied for the oscillation startup at  $\omega_0$ :

$$|H(j\omega_0)| = 1 \quad , \quad \arg(H(j\omega_0)) = 0^\circ \quad (2.2)$$

The phase in (2.2) should be changed to a value of  $180^\circ$  when the loopback gain is negative. These equations are known as Barkhausen's criteria. However, in special situations, the two above conditions can not satisfy the oscillation startup completely. In other words, the Barkhausen's criteria are necessary but not sufficient. For example, in some practical cases, the output remains saturated or grounded, even though the startup conditions are satisfied.

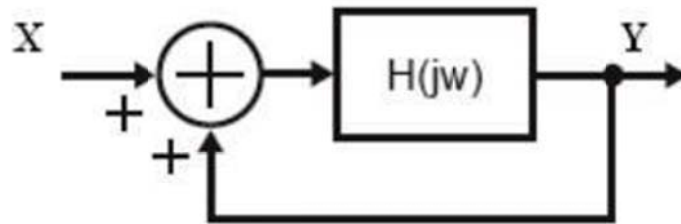


Figure 2.1: Oscillator's feedback system

Nowadays, designers use various topologies to satisfy the Barkhausen's criteria mentioned in the above section. Moreover, LC and ring oscillators are mainly preferred in high frequency oscillator design.

## 2.3 Ring Oscillators

A ring oscillator is a device composed of an odd number of inverters connected in a feedback loop. In other words, the NOT gates are placed in a chain in which the output of last inverter is fed back into the first one. The total delay of each inverter cell determines the oscillation frequency which is formulated as following:

$$f_0 = \frac{1}{2Nt_d} \quad (2.3)$$

Considering the power consumption and phase noise performance, the number of stages is chosen. There are different topologies regarding the ring oscillators but the differential and the single-ended models are mainly discussed in this project.

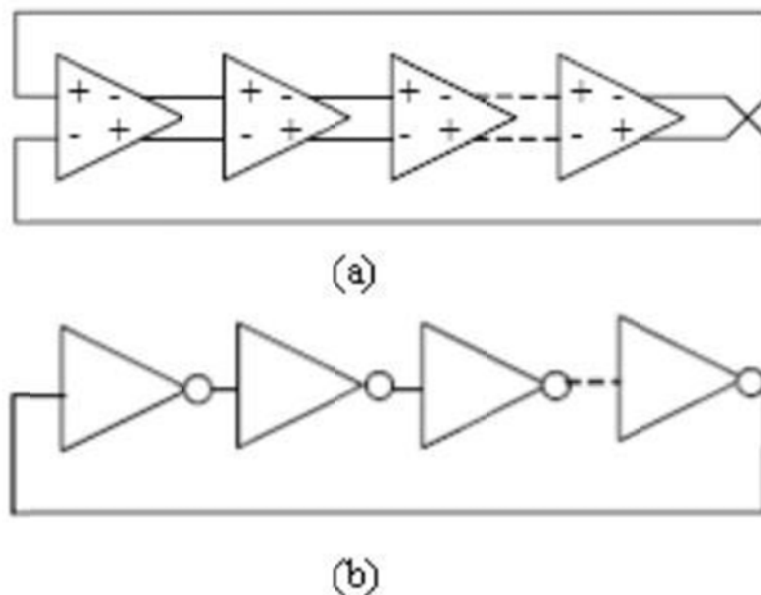


Figure 1.2: Ring oscillator architecture

a) Differential model

b) Single-ended model

In single-ended model, as far as the inverters have high output gain, the Barkhausen's criteria is always satisfied. Since each delay cell has a large signal phase shift of  $180^\circ$ , the single-ended model is designed with an odd number of cells. The current is only used during transitions of the NOT gates.

The intrinsic capacitors are charged and discharged by this constant current generated by the transistors. Therefore, the delay time of each cell is defined.

In order to have a quicker transitions and higher oscillation frequency, we should apply a higher current.

Another improved type of delay cell is current-starved inverter. As shown in the Fig. 2.3, the frequency can be controlled when two extra transistors are added to the cell.

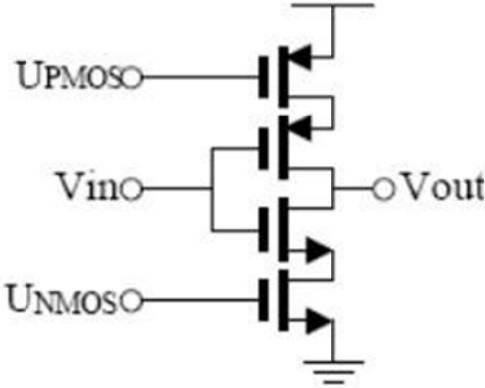


Figure 2.2: Current starved inverter

As shown in the Fig. 2.4, the differential structure consists of an NMOS or PMOS differential transistors and an output load. The cell delay is determined by the charge stored in the circuit and the current driving the load. Resistors can be used for a fixed frequency. If PMOS transistors are applied as our loads, we can improve the oscillator to be tunable with different range of voltages. PMOS or NMOS transistors can be applied as cross-coupled or symmetric models.

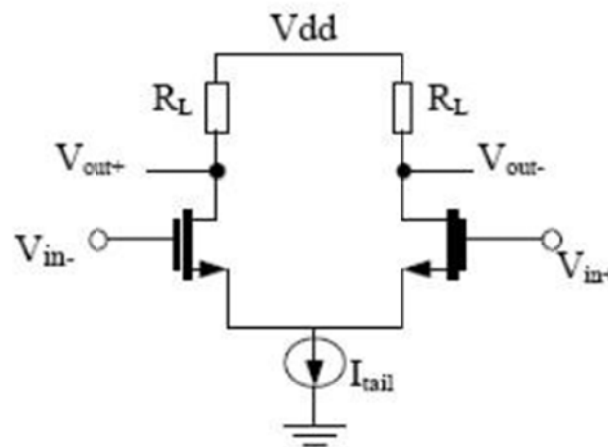


Figure 2.3: Differential symmetric pair

For a given power consumption, frequency and number of stages, the differential ring oscillator has a worse performance than its single-ended counterpart. In other words, the differential ring oscillator's phase noise is  $N(1+V_{char}/(R_L \cdot I_{tail}))$  times higher than the single-ended structure [20]. On the other hand, the single-ended architecture consumes less power than the differential model. Additionally, it has a better phase noise for specific power consumption due to the inverse proportionality of the phase noise to power dissipation. However, differential ring oscillators are often preferred in digital circuits due to their better common noise rejection [20]. Moreover, less noise is injected to the other components on the chip. Nowadays, this architecture is widely used for state of

the art designs. For instance, a quadratic signal is generated by differential architecture since even number of inverters should be maintained.

Passive devices are not used in ring oscillators. Regarding this issue, there are benefits and drawbacks which can be discussed. The main advantage of using active elements is easy integration on chip. Additionally, inductors occupy a considerable amount of area on chip. However, using an inductor with a capacitor on the chip makes a band pass filter that leads to better phase noise performance. Overall, ring oscillators show worse phase noise performance than the LC VCOs. The main usage of ring oscillators is for data transmission as clock recovery or clock propagation on the chip.

## **2.4 LC Oscillators**

An LC oscillator consists of a resonator tank in which the inductor and the capacitor are connected in parallel. There are various LC VCO architectures but Colpitts and Negative  $g_m$  oscillators are the most popular structures. In the following sections, these two models are widely compared regarding their benefits and drawbacks.

### **2.4.1 LC Tank**

In VCO implementation, LC network is mainly in focus due to its filtering benefits. Since the LC tank consists of an inductor and a capacitor connected in parallel, it is also called a parallel resonator circuit. In an ideal condition, if a current impulse is applied to the LC tank, the energy transfers back and forth between the inductance and the capacitance. This leads the circuit to oscillate for an infinite period time. However, this occurs in an ideal case where both of the elements are lossless. In other words, some dissipation is inevitable for the inductor and the capacitor. Otherwise, they should have an infinite quality factor that is not possible in practice. Actually, the resonator's loss is due to the series resistances of the inductor and the capacitor. As far as RF VCOs oscillate over a small range of

frequencies, the parasitic resistances can be remodeled to their parallel structure. The overall resistance is shown by  $R_p$  in the following figures.

It dissipates the energy and thus leads the oscillation to fade away. In order to compensate this lossy circuit, an active circuit should be added in parallel to the tank. This active circuit produces a negative resistance to cancel the  $R_p$ . Therefore, it helps the oscillation to survive.

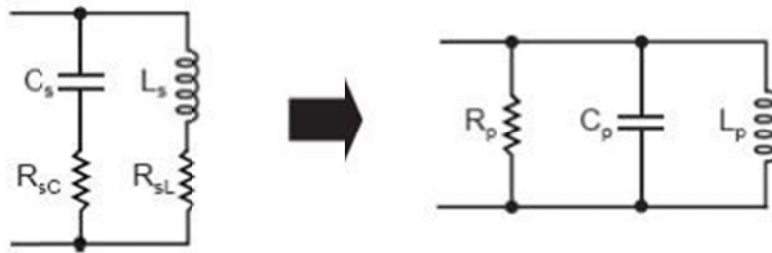


Figure 2.4: Series resistance conversion into equivalent parallel resistance

The main drawback is that integrated inductors have very low quality factors and occupy a larger area on the chip than the ring oscillators. Nevertheless, LC oscillators have a better phase noise performance compared to ring oscillators.

The magnitude and phase behavior of an LC tank is shown in the Fig. 2.6. At the resonance frequency, the network behaves like a resistance. In other words, it is purely real. The resonance frequency is formulated as following:

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \quad (2.4)$$

Where, L and C are inductance and capacitance respectively.

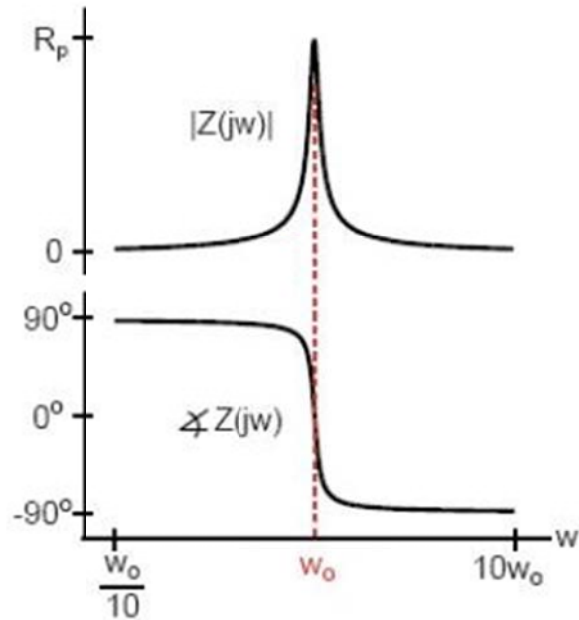


Figure 2.5: Phase behavior and magnitude of a resonator

### 2.4.2 One-port Model of LC VCO

Negative  $g_m$  or one-port model represents the oscillator as the combination of two individual one-port models. This approach makes the analysis of LC oscillators much easier. The procedure is depicted in the Fig. 2.7.

As mentioned before, the resonance circuit with the series loss of the inductor and the capacitor can be modeled as its parallel equivalent. At each period,  $R_p$  prevents oscillation to be stable by consuming some amount of stored LC tank energy. Therefore, an active negative resistance which is equal to  $-R_p$  should compensate the loss of the tank. In other words, we should create a lossless tank with the infinite parallel resistance at the resonance frequency. This condition is satisfied by the following equation:

$$\frac{1}{G_m} = R_p \quad (2.5)$$

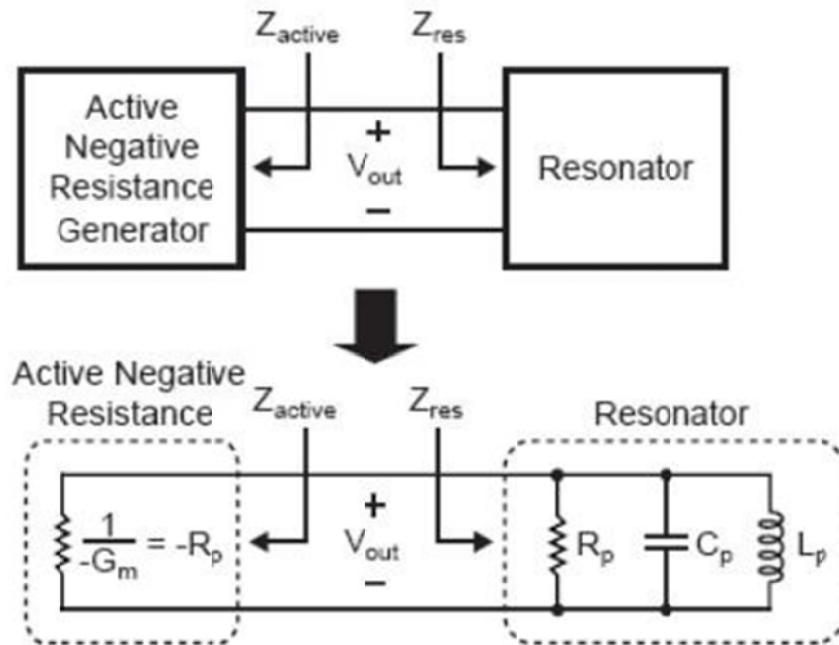


Figure 2.7: One-port model of an LC VCO

As mentioned earlier,  $G_m$  is called as the large signal transconductance when the VCO is in stable condition.

### 2.4.3 Cross-Coupled LC Oscillator

As mentioned in above sections, in negative  $G_m$  procedure, the loss of the tank is neutralized by active devices for a stable oscillation. In CMOS cross-coupled LC VCO, the transistors act similar to an active negative resistance. To satisfy oscillation startup condition, negative resistance usually is defined at least two times larger than the parallel loss of the tank. The main advantage of this topology is the simple design and implementation on the chip. The cross-coupled LC oscillator is categorized into three types: PMOS, NMOS and CMOS cross-coupled. Each of them can be implemented using top-biased, bottom-biased or self-biasing current source.

### 2.4.3.1 NMOS Cross-Coupled LC Oscillator

As shown in the Fig. 2.8, a bottom-biased NMOS cross-coupled LC oscillator is presented. The losses of the tanks are depicted as well. It consists of an NMOS differential pair and two resonators in which their series and parallel resistive losses are analyzed in detail.

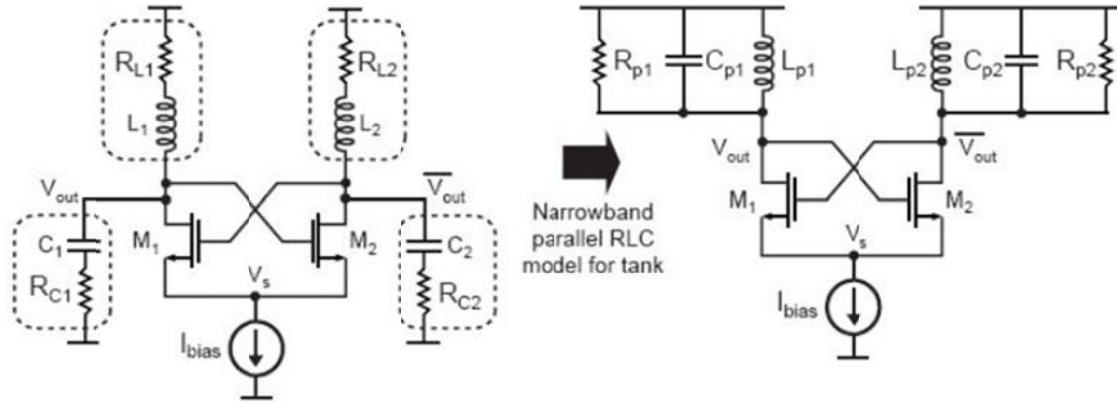


Figure 2.6: Bottom biased LC oscillator with equivalent losses

In this section, the NMOS cross-coupled LC oscillator is analyzed. For the simplicity, the circuit is divided into two parts. It is assumed that the common-mode noise is grounded so that the  $V_{source}$  is biased to ground. However, this assumption is not completely true because the current source has a finite output resistance. As we know, the output nodes have differential swing with a phase difference of  $180^\circ$ . Therefore, the gates of the transistors are expressed as  $V_{out}$  and  $-V_{out}$ . The resistance seen from output node to ground is formulated as:

$$\frac{V_{out}}{I_{d1}} = \frac{V_{out}}{-G_m V_{out}} = -\frac{1}{G_m} \quad (2.6)$$

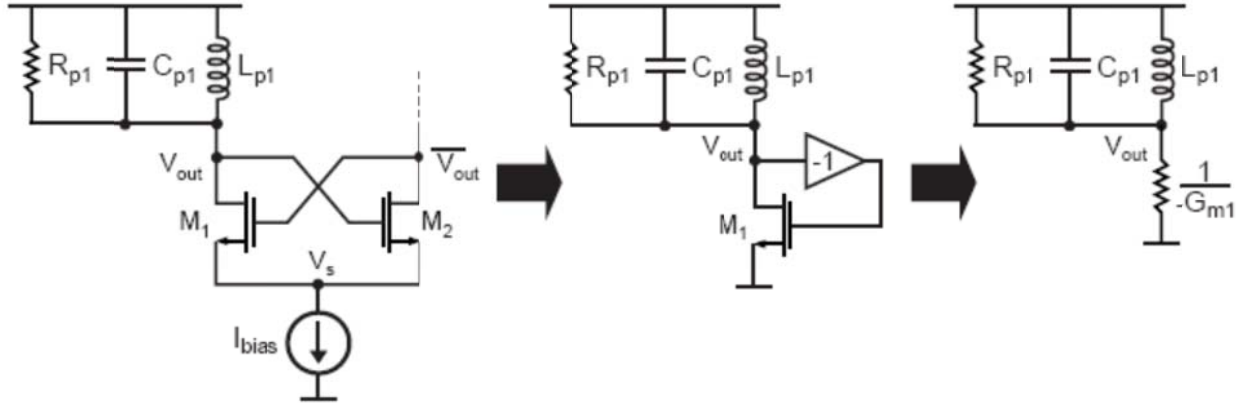


Figure 2.7: NMOS LC oscillator analysis

Therefore, if the two tanks are same, we can convert them to an equivalent circuit in which:  $L_p=2L_{p1}$ ,  $C_p=C_{p1}/2$ ,  $R_p=2R_{p1}$  and the negative resistance would be  $-2/G_{m1}$ .

For a cross-coupled VCO to be in stable condition, the small signal loop gain should be greater than unity. Therefore, the gain value should be chosen as two in the minimum case. Therefore, the startup condition is as following:

$$\frac{1}{g_{m1}} \geq \alpha_{\min} R_{p1} \quad (2.7)$$

In the above equation,  $\alpha_{\min}$  satisfies the startup condition which should be at least two.

Next, we should find out the relationship between the small signal gain and the large signal gain. The small signal gain is  $\alpha_{\min}$  times larger than the large signal gain. As the oscillation enters the steady state, the small signal gain of the circuit will decrease. Finally, it will be equal to the large signal gain because of the nonlinearities. The nonlinear characteristic is figured out by analyzing the transistors function in triode and cut-off region. In cut-off region, the positive output swing is clipped under the bias voltage. Additionally, the large signal transconductance of an NMOS transistor is equal to  $\mu_n C_{ox} (W/L) V_{ds}$  in linear region. Actually, in linear region, we have the direct proportionality of the transconductance to drain voltage. On the other hand, by applying a small voltage

of  $\Delta V$  at  $V_{g1}$ , the  $V_{g2}$  or  $V_{d1}$  will decrease correspondingly. If  $\Delta V$  is considered large enough, the transistor will enter the linear region. Here, the  $g_{m1}$  starts to decrease and the loop gain will be stable at one.

As observed in the results, symmetrical waveforms are obtained at the output. Therefore, each transistor is on in half of the period so the current behavior is depicted as a square waveform for each transistor [21]. The mean value of the output would be the same as for the circuit operating in DC mode. The current obtained at the center frequency is equal to  $(1/\pi)I_{bias}$ . The LC tank filters out the current harmonics so the output amplitude is formulated as:

$$V_o = \frac{2}{\pi} I_{bias} R_p \quad (2.8)$$

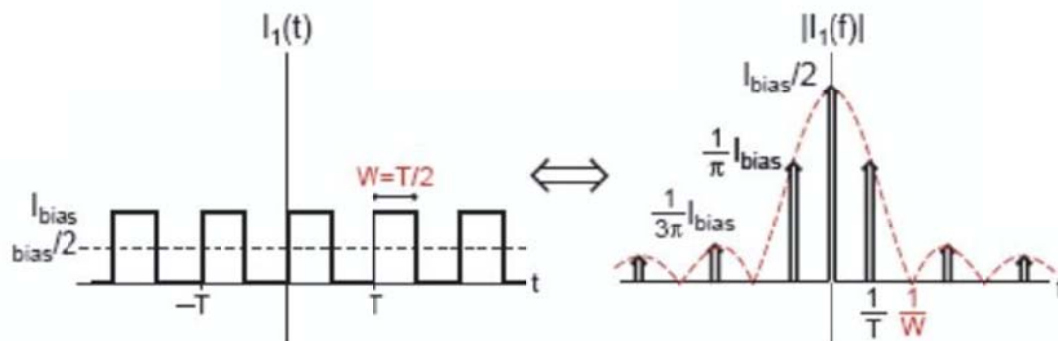


Figure 2.8: Waveforms of a cross-coupled LC oscillator

### 2.4.3.2 CMOS Cross-Coupled LC Oscillator

A CMOS cross-coupled LC oscillator consists of two NMOS and PMOS transistor pairs. In this topology, usually one inductor is used. A differential voltage is applied on the inductor which leads to better output waveforms than the previous topology. To obtain symmetrical waveforms, we should generate equal parallel resistance on the both sides of the resonator. If not, the phase noise would increase. Therefore, if the inductance is not designed symmetrical, two inductors in series should be implemented alternatively.

In this structure, as shown in Fig. 2.11, the PMOS transistors reuse the bias current. Therefore, a larger output voltage is generated. As the output voltage increases, one of the NMOS transistors is switched on while the other one goes off. This is the same case for the PMOS pair but in the other way. For instance, in the half period, the current is driven into the  $M_4$  and then the resonator and finally it is conducted by the  $M_1$ . One of the advantages of this structure over other topologies is that the current goes through the resonator's resistance in each half period. Consequently, the output would be twice larger than the PMOS or NMOS cross-coupled architecture. Regarding the Leeson's equation, the output voltage improvement leads to better phase noise performance.

Additionally, the PMOS transistors produce an extra negative resistance which can increase the overall negative resistance when added to NMOS pair. Consequently, the complementary architecture obtains an overall negative resistance of  $-2/G_{m,NMOS}-2/G_{m,PMOS}$ . To produce symmetrical waveforms, the NMOS and PMOS transconductance should be the same. So, the overall negative resistance would be  $-4/G_m$ . Additionally, when using the complementary architecture, the startup condition would be satisfied easily for a specific bias current.

Moreover, when equal transconductance is considered for the NMOS and PMOS pair, the most symmetric output can be obtained comparing to the NMOS or PMOS cross-coupled counterparts. Therefore, the rise and fall times will boost and hence the flicker noise upconversion will improve [20]. In our design, we

obtain a more reasonable phase noise in  $1/f^3$  region compared to NMOS cross-coupled architecture. The  $1/f^2$  phase noise is improved as well. However, the PMOS transistors are the main contributors of thermal noise in this region.

There are also some drawbacks when using CMOS cross-coupled LC VCOs. We encounter some output swing constraints in this architecture. In an NMOS cross-coupled architecture, considering the voltage headroom, the output voltage swing is set at  $V_{dd}-V_{diff}$  while in a complementary architecture the output voltage degrades to  $(V_{dd}-V_{diff})/2$ . However, when the output is biased at  $V_{dd}$ , the VCO will be more influenced by the supply voltage distortions.

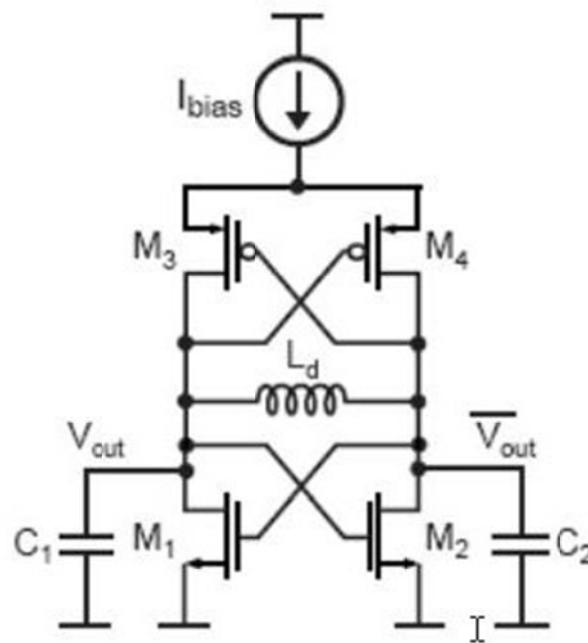


Figure 2.9: Top-biased complementary LC oscillator

In a complementary LC architecture, adding PMOS pair to the circuit leads to extra parasitic capacitances seen in the resonator. Regarding the bias current, the PMOS and NMOS sizing may vary correspondingly. In other words, the sizing of PMOS transistors should be chosen quite larger than NMOS pair. This will balance the overall transconductance of the design. Therefore, the required

transconductance is met in the complementary LC architecture. Since the overall intrinsic parasitic capacitance enhances in this topology, the resonator value should be calculated carefully to meet the desired oscillation frequency. Consequently, decreasing the value of the capacitor leads to tuning range limitations.

### **3. OSCILLATOR NOISE**

In this chapter, we mainly describe the oscillator phase noise. In the beginning, a brief definition of the phase noise is given. Afterwards, its effect on RF transceivers is analyzed. In the following sections, the Leeson's phase noise model is discussed and followed by two other models using the impulse sensitivity function. Finally, a detailed analysis of the phase noise sources in a complementary LC oscillator is carried out.

#### **3.1 General Idea**

There are some types of noise sources which influence the functionality of an LC VCO. The external noise is produced by the other components that are interacting with the oscillator. The filter generating the tuning voltage of the oscillator and the frequency divider in a Phase-Locked Loop are the blocks which can produce extrinsic noise in our circuit. The internal noise is generated by the circuit layout of the components designed in the VCO. As a matter of fact, both noise sources can inject some disturbances into our design. Therefore, the output amplitude and frequency are influenced by this issue. Since the transistors nonlinearities compensate the amplitude noise, its effect is commonly neglected during the VCO design. Actually, a small deviation of frequency is regarded as phase noise in analog circuits. Nevertheless, if we consider the output in a time-dependent scale, it is considered as a deviation in zero crossing points. The phase noise plays an important role in VCO functionality. In the digital circuits, phase noise can be defined as jitter. In the Fig. 3.1, the difference can be identified clearly.

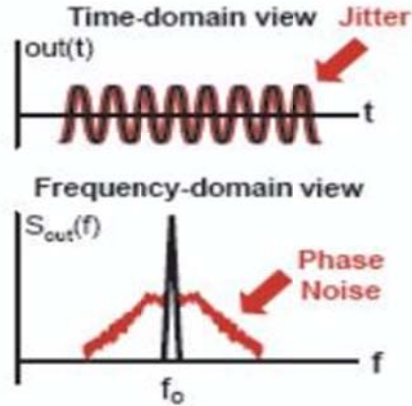


Figure 3.1: Comparison of phase and jitter noise

We can formulate the circuit output as  $x(t) = A \cos[\omega_0 t + \varphi_n(t)]$ . The output waveform is sinusoidal where  $A$  is the amplitude of VCO,  $\omega_0$  is the desired center frequency and  $\varphi_n(t)$  is the corresponding phase noise. For a detailed analysis, the output signal can be rewritten as following:

$$x(t) = A[\cos(\omega_0 t)\cos(\varphi_n(t)) - \sin(\omega_0 t)\sin(\varphi_n(t))] \quad (3.1)$$

For small values of phase noise, we get:

$$\sin(\varphi_n(t)) \approx \varphi_n(t) \quad (3.2)$$

$$\cos(\varphi_n(t)) \approx \cos(0) = 1 \quad (3.3)$$

Therefore, the output is approximated as following:

$$x(t) \approx A \cos(\omega_0 t) - A \varphi_n(t) \sin(\omega_0 t) \quad (3.4)$$

As shown in the Fig. 3.2, the output waveform of an ideal and a real oscillator is compared. Moreover, the resonator is responsible for wiping out the unwanted signals to some extent. As we move away from the center frequency, less undesired signals are observed due to the filtering technique. Therefore, the real oscillator spectrum differs from what is expected in theory. In practice, the phase noise is similar to a skirt in frequency domain.

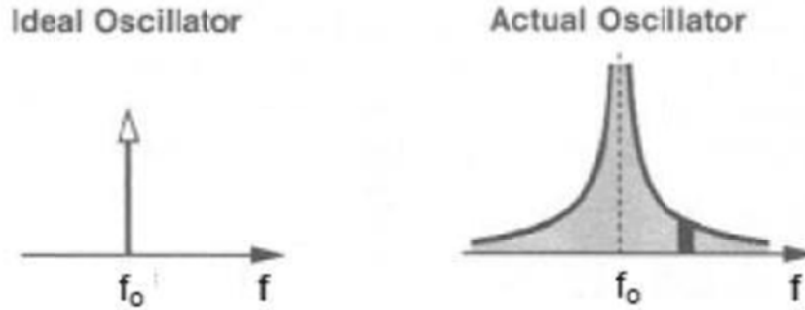


Figure 3.2: Output waveform comparison of an ideal and a real oscillator

Here, we propose a formula for calculating the phase noise over a 1Hz bandwidth. Therefore, we should consider a specific distance from our carrier frequency. This distance is called an offset frequency which is depicted by  $\Delta\omega$  in the equation (3.5). To obtain the phase noise at this offset frequency, we take advantage of logarithmic scale in which the noise power is divided by the carrier power. The corresponding formula is as following:

$$L(\Delta\omega) = 10 \log\left(\frac{P_{\text{tone}}(\Delta\omega, 1\text{Hz})}{P_{\text{carrier}}}\right) \quad (3.5)$$

$P_{\text{tone}}$  shows the noise power at the desired offset frequency from the carrier over a 1Hz bandwidth and  $P_{\text{carrier}}$  represents for the carrier power.  $L(\Delta\omega)$  is defined by dBc/Hz which represents the phase noise value. In other words, it illustrates how much the  $P_{\text{tone}}$  is below the  $P_{\text{carrier}}$  in dB scale.

### 3.2 Phase Noise Effect on RF Transceiver Topologies

As we know, the signal reaching to an antenna should be set at a lower frequency. This frequency is called IF or intermediate frequency. However, the signal shape should not change. On the other hand, we encounter some disturbances staying near our signal. Therefore, after downconversion, we get both desired signal and unwanted interferer. The phase noise of the local oscillator covers the main signal and the interferer and hence the signals overlap each other at the intermediate

frequency. Overall, the signal to noise ratio will decrease at the intermediate frequency. This phenomenon is called reciprocal mixing.

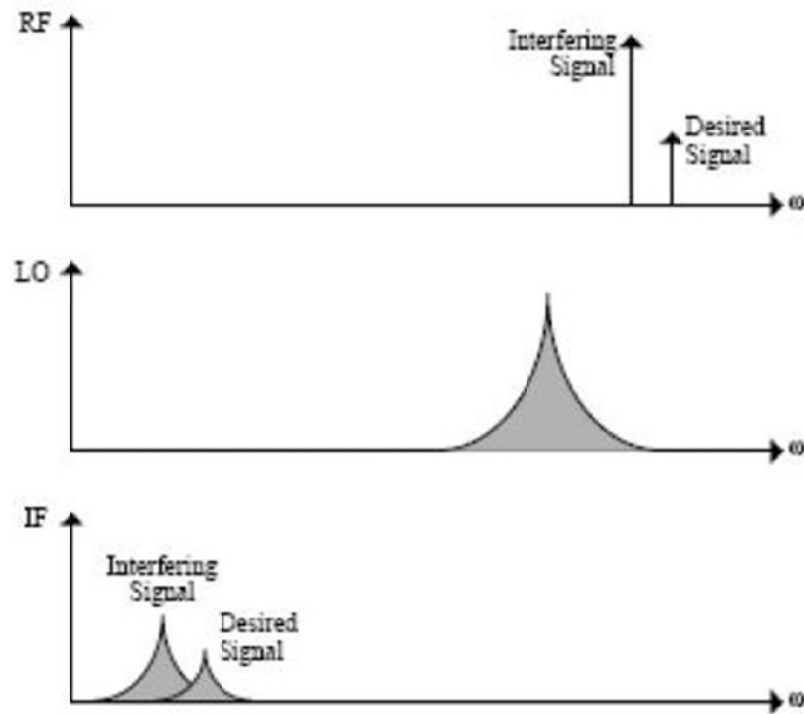


Figure 3.3: Phase noise impact on receivers

The Fig. 3.3 corresponds to the receivers. However, it is the same for transmitting the signals. In a transceiver, the power amplifier strengthens the unwanted signal which is modulated by the oscillator. On the other hand, the interferer spectrum gets larger as the offset frequency moves farther. This issue corrupts the desired signal to some extent.

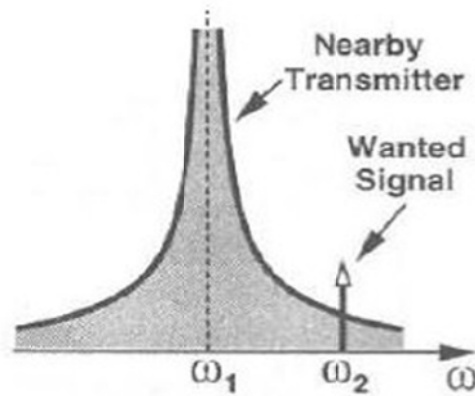


Figure 3.4: Phase noise impact on transmitters

### 3.3 Analysis of Oscillator Phase Noise

In this section, several theories are analyzed in detail regarding the oscillator phase noise and its impact on the circuit performance. Additionally, two famous models are presented in the following sections. At the end of this chapter, the phase noise contributors are identified one by one.

#### 3.3.1 Leeson's Equation of Phase Noise

In this part, the VCO is assumed as a one-port model. We divide the internal noises of an oscillator into two groups. The first noise contributor is the tank circuit while the second one is because of the active devices. In other words, the lossy resonator and the transistor pairs are the main noise contributors that should be taken into account. The active components mainly produce flicker and thermal noise in the circuit. The corresponding model is given in the Fig. 3.5.

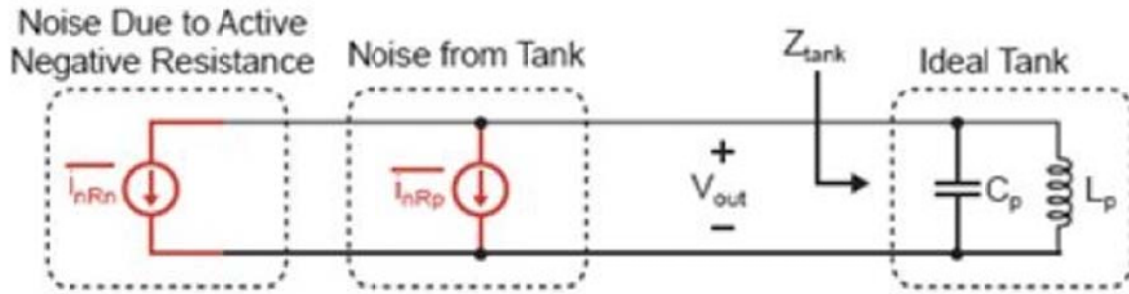


Figure 3.5: LC oscillator model with noise generators

As depicted in the model, the noise sources of an LC oscillator are identified clearly and this would help us to specify how these elements influence on the phase noise. To simplify the calculations, we define an ideal resonator. However, if a non-ideal tank is assumed, its loss will be covered by the active devices.

At our desired frequency of  $\omega$ , the impedance seen at the resonator input is as following:

$$Z(\omega) = \frac{j\omega L_p}{1 - \omega^2 L_p C_p} \quad (3.6)$$

If we consider an offset frequency of  $\Delta\omega$  from the oscillation frequency, we get:

$$\omega = \omega_0 + \Delta\omega \quad (3.7)$$

On the other hand, the oscillation frequency is:

$$\omega_0 = \frac{1}{\sqrt{L_p C_p}} \quad (3.8)$$

By replacing (3.7) in (3.6), we get:

$$Z(\omega_0 + \Delta\omega) = \frac{j(\omega_0 + \Delta\omega)L_p}{1 - (\omega_0 + \Delta\omega)^2 L_p C_p} \quad (3.9)$$

Now, we expand the frequency terms in the denominator. So, we get:

$$Z(\omega_0 + \Delta\omega) = \frac{j(\omega_0 + \Delta\omega)L_p}{1 - \omega_0^2 L_p C_p - 2\Delta\omega(\omega_0 L_p C_p) - \Delta\omega^2 L_p C_p} \quad (3.10)$$

As it is clear from (3.8),  $1 - \omega_0^2 L_p C_p$  is equal to zero. On the other hand, the  $\Delta\omega^2 L_p C_p$  term is so small that can be ignored. So, we get:

$$Z(\omega) \approx \frac{j(\omega_0 + \Delta\omega)L_p}{-2\Delta\omega(\omega_0 L_p C_p)} \quad (3.11)$$

Since  $\omega_0$  is quite larger than  $\Delta\omega$ , we can ignore  $\Delta\omega$  in the numerator. So the equation (3.11) will be refined as following:

$$Z(\omega) = -\frac{j}{2} \frac{1}{C_p} \left( \frac{\omega_0}{\Delta\omega} \right) \quad (3.12)$$

As explained in the previous chapter, the tank generates a parallel resistance which is illustrated by  $R_p$ . By obtaining the value of equivalent parallel resistance, we can easily calculate the quality factor of the tank. The equation is as following:

$$Q = \omega_0 R_p C_p \quad (3.13)$$

By replacing (3.13) in (3.12), we obtain the following formula which can show the tank impedance as a function of the quality factor and the equivalent parallel resistance.

$$Z(\omega) = -\frac{j}{2} \frac{R_p}{Q} \left( \frac{\omega_0}{\Delta\omega} \right) \quad (3.14)$$

Here, we square both sides of the equation and hence we obtain the absolute value of the tank impedance as a function of the offset frequency.

$$|Z_{tank}(\omega)|^2 \approx \left( \frac{R_p \omega_0}{2Q\Delta\omega} \right)^2 \quad (3.15)$$

Next, a new equation for calculating the overall output noise is presented. By using (3.15), we obtain:

$$\frac{\overline{v_{out}^2}}{\Delta\omega} = \left( \frac{\overline{i_{nRp}^2}}{\Delta\omega} + \frac{\overline{i_{nRn}^2}}{\Delta\omega} \right) |Z_{tank}(\omega)|^2 \quad (3.16)$$

As observed in (3.16), the overall noise of the oscillator is determined. The equation is rewritten as following:

$$\frac{\overline{v_{out}^2}}{\Delta\omega} = \frac{\overline{i_{nRp}^2}}{\Delta\omega} \left( 1 + \frac{\overline{i_{nRn}^2}}{\Delta\omega} / \frac{\overline{i_{nRp}^2}}{\Delta\omega} \right) |Z_{tank}(\omega)|^2 \quad (3.17)$$

The term in the parenthesis can be defined as following:

$$F(\Delta\omega) = 1 + \frac{\overline{i_{nRn}^2}}{\Delta\omega} / \frac{\overline{i_{nRp}^2}}{\Delta\omega} \quad (3.18)$$

On the other hand, for the parallel resistance noise generated by the tank, we get:

$$\frac{\overline{i_{nRp}^2}}{\Delta\omega} = \frac{4kT}{R_p} \quad (3.19)$$

The output noise spectral density is formulated as below:

$$\frac{\overline{v_{out}^2}}{\Delta\omega} = \frac{\overline{i_{nRp}^2}}{\Delta\omega} F(\Delta\omega) |Z_{tank}(\omega)|^2 = 4KTF(\Delta\omega)R_p \left( \frac{1}{2Q} \frac{\omega_0}{\Delta\omega} \right)^2 \quad (3.20)$$

To obtain the phase noise formula, we apply the equipartition theory to the (3.20). It proves that if a sinusoidal wave is obtained at the output, the noise is equally divided into two parts. One equation is dedicated to the phase noise while the other one points to the amplitude noise [22].

$$\left. \frac{\overline{v_{out}^2}}{\Delta\omega} \right|_{Phase} = 2KTF(\Delta\omega)R_p \left( \frac{1}{2Q} \frac{\omega_0}{\Delta\omega} \right)^2 \quad (3.21)$$

The following formula is presented for calculating the phase noise at  $\Delta\omega$  offset frequency.

$$L(\omega) = 10 \log \frac{S_{noise}(\Delta\omega)}{P_{signal}} \quad (3.22)$$

The final formula can be rewritten as:

$$L(\omega) = 10 \log \left( \frac{2KTF(\Delta\omega)}{P_{signal}} \left( \frac{1}{2Q} \frac{\omega_0}{\Delta\omega} \right)^2 \right) \quad (3.23)$$

The value of  $F(\Delta\omega)$  is considered as two and hence the overall phase noise is formulated as:

$$L(\omega) = 10 \log \left( \frac{4KT}{P_{\text{signal}}} \left( \frac{1}{2Q} \frac{\omega_0}{\Delta\omega} \right) \right)^2 \quad (3.24)$$

As it is understood from the phase noise formula, we get -20dBc/Hz transition per decade. However, in practice, the phase noise does not follow this concept completely. In other words, the noise of active devices needs a more complicated analysis. In this model, since the transistors are the main contributors of the thermal noise, they are considered as resistors. Nevertheless, the flicker noise produced by the transistor pairs should be taken into account. On the other hand, the bias circuitry generates some noise which influences the output waveform. Moreover, the active devices show low impedance when functioning in the triode region and hence this causes the resonator's quality factor to degrade.

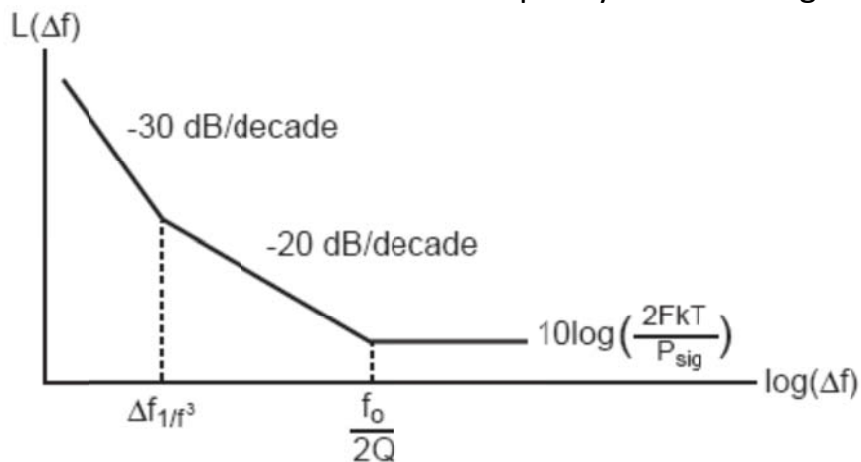


Figure 3.6: Phase noise spectrum of a real oscillator

As observed in Fig. 3.6, the phase noise spectrum differs from what is expected for an ideal oscillator. For a non-ideal oscillator, the phase noise changes -30dB per decade for low offset frequencies. However, for some offset frequencies as shown in Fig. 3.6, the ramp is set at -20dB/decade. Moreover, at high offset frequencies, the noise floor causes the ramp to go to zero.

Leeson has presented an experimental model which fulfills the equation (3.24) and the phase noise behavior of a real oscillator simultaneously [12]. The Leeson's experimental formula is as following:

$$L(\omega) = 10 \log \left( \frac{2KTF}{P_{signal}} \left( 1 + \left( \frac{1}{2Q} \frac{\omega_0}{\Delta\omega} \right)^2 \right) \left( 1 + \frac{\Delta\omega_{1/f^3}}{|\Delta\omega|} \right) \right) \quad (3.25)$$

In equation (3.25),  $\Delta\omega_{1/f^3}$  is the point where  $1/f^2$  and  $1/f^3$  regions meet. Leeson's formula depicts the inverse proportionality of the phase noise to the resonator's power dissipation. Based on this issue, we optimize the phase noise value by improving the oscillation amplitude. Additionally, for our design, we have chosen efficient inductors with high quality factor.

### 3.3.2 Hajimiri and Lee's Phase Noise Equation

Since Leeson's model is empirical, it cannot identify the effect of all noise generators on the phase noise. On the other hand,  $\Delta\omega_{1/f^3}$  and F terms are experimental in (3.25). For instance, if there are several active components producing flicker noise in the circuit, Leeson's formula does not rule any more. In other words, there is no data to identify whose flicker noise should be chosen for calculating the  $\Delta\omega_{1/f^3}$ . As understood from (3.25), increasing the quality factor improves the overall phase noise performance. However, the F parameter rises as well which degrades the phase noise performance [14]. Therefore, the Leeson's model cannot completely interpret the phase noise behavior of an oscillator. Subsequently, Lee and Hajimiri presented another model to study the impulse response of an ideal oscillator [13].

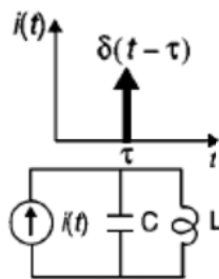


Figure 3.7: Impulse response of an ideal oscillator

In this part, the impact of current impulse on the tank is investigated as shown in the Fig. 3.8. For instance, if we apply an impulse at the output peak, the amplitude changes while the phase remains the same. The amplitude variation is estimated as  $\Delta v = \Delta q / c$ . In this formula,  $\Delta q$  shows the charge across the tank. In other case, if we apply a pulse at the time axis where the signal is crossing the

zero point, the output phase will be affected. However, during any other time of oscillation, the impulse leads to phase and amplitude variation simultaneously. The phase variation of the system is identified by the time of impulse occurrence. Consequently, an oscillator is considered as a time-varying system. Moreover, the value of amplitude variation is directly proportional to the pulse amplitude.

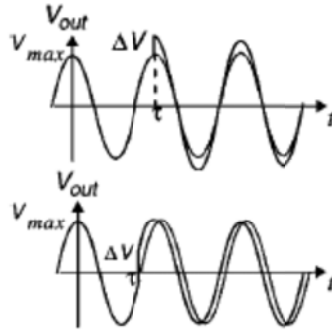


Figure 3.8: Impulse impact on a time-varying system

As explained in previous sections, the designers usually do not care about the amplitude noise due to the nonlinearities of active devices in the oscillator. Figure 3.9 briefly describe this phenomenon.

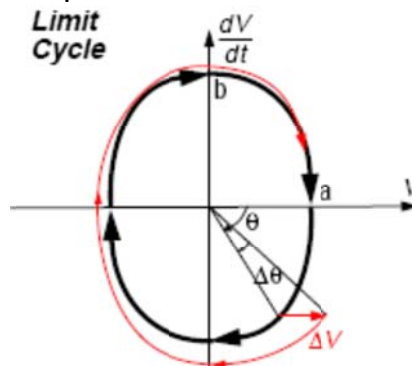


Figure 3.9: Amplitude noise of an oscillator in one period

Therefore, to optimize the phase noise performance, the noise disturbances should occur at the peak of output signal.

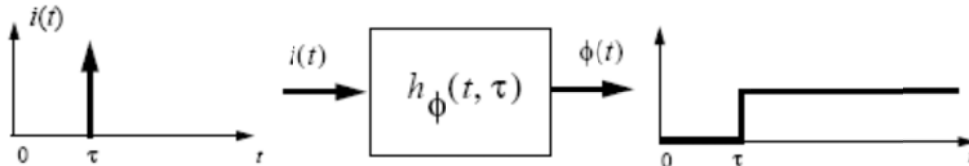


Figure 3.10: Current impulse behavior on a time-varying system

The impulse response of a time-varying system is depicted in Fig. 3.10. As shown in the figure, a phase variation is introduced in the system. Overall, the oscillator's phase variation due to the current impulse is formulated as following:

$$h_{\varphi}(t, \tau) = \frac{\Gamma(\omega_0 \tau)}{q_{max}} u(t - \tau) \quad (3.26)$$

$\Gamma(x)$  represents for impulse sensitivity function (ISF). It illustrates the phase variation when a current impulse is applied at a specific time.

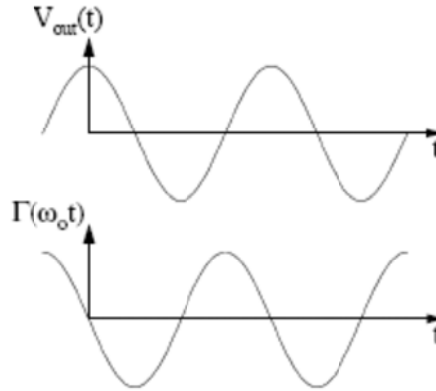


Figure 3.11: Impulse sensitivity function of a real oscillator

Obviously, when the oscillator is more susceptible to current impulse driven into the resonator, the amplitude of ISF function rises. This leads to phase variation of the output signal.

Here, we take advantage of the superposition principle to calculate the phase noise generated by the current impulse.

$$\varphi(t) = \int_{-\infty}^{\infty} h_{\varphi}(t, \tau) i(\tau) d(\tau) = \frac{1}{q_{max}} \int_{-\infty}^t \Gamma(\omega_0 \tau) i(\tau) d(\tau) \quad (3.27)$$

To obtain a clear understanding of equation (3.27), we present the following block diagram. It shows how a current impulse influences the output signal.

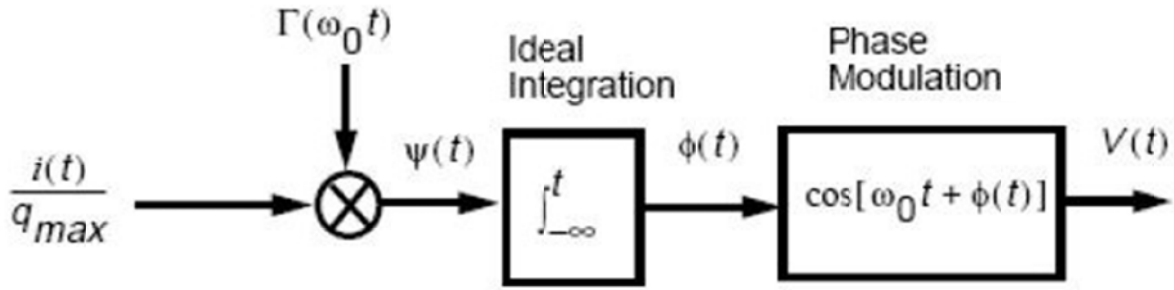


Figure 3.12: Current impulse effect on the output signal

Since ISF function is periodic, we take advantage of Fourier series to remodel it as the following equation:

$$\Gamma(\omega_0 \tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_0 \tau + \theta_n) \quad (3.28)$$

All of the parameters are real in equation (3.28). The harmonics phase is depicted by  $\theta_n$  in the ISF function equation. Therefore, the overall phase of the ISF function is as following:

$$\varphi(t) = \frac{1}{q_{max}} \left[ \frac{c_0}{2} \int_{-\infty}^t i(\tau) d(\tau) + \sum_{n=1}^{\infty} c_n \int_{-\infty}^t i(\tau) \cos(n\omega_0 \tau + \theta_n) d(\tau) \right] \quad (3.29)$$

To get a clear idea of the equation (3.29), the equivalent block diagram is presented as shown in Fig. 3.13. In this model, the coefficients of impulse sensitivity function should be calculated to estimate the overall phase noise. In other words, several noise components are generated due to current impulse injection to the tank. They are located at different frequencies regarding to the Fourier coefficients of impulse sensitivity function. This behavior is illustrated in Fig. 3.13. The ISF block diagram and the procedure of converting the current noise to phase noise are illustrated in Fig. 3.13 and 3.14 respectively.

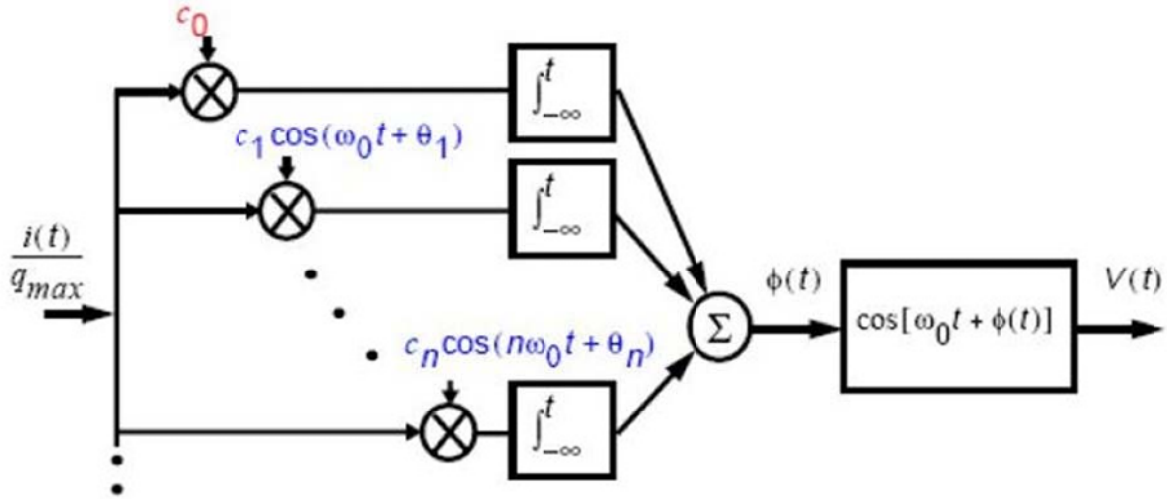


Figure 3.13: ISF block diagram

The  $1/f$  noise of the transistor pairs at the center frequency of  $\omega_0$  is upconverted to  $1/f^3$  region. Actually, the flicker noise stays close to the carrier. Additionally, the  $c_1$  coefficient in Fourier series represents for the noise near to oscillation frequency. On the other hand, the thermal noise of the components is the main contributor of phase noise in  $1/f^2$  region. The  $c_2$  coefficient determines the noise of  $2\omega_0$  while  $c_3$  represents the noise corresponding to  $3\omega_0$  and so forth.

The equivalent phase noise of ISF block diagram is calculated as equation (3.30). The relative phase noise is considered in  $1/f^2$  region.

$$L(\Delta\omega) = 10 \log \frac{\Gamma_{rms}^2 \frac{i_n^2}{\Delta f}}{q_{max}^2 \cdot 4\Delta\omega^2} \quad (3.30)$$

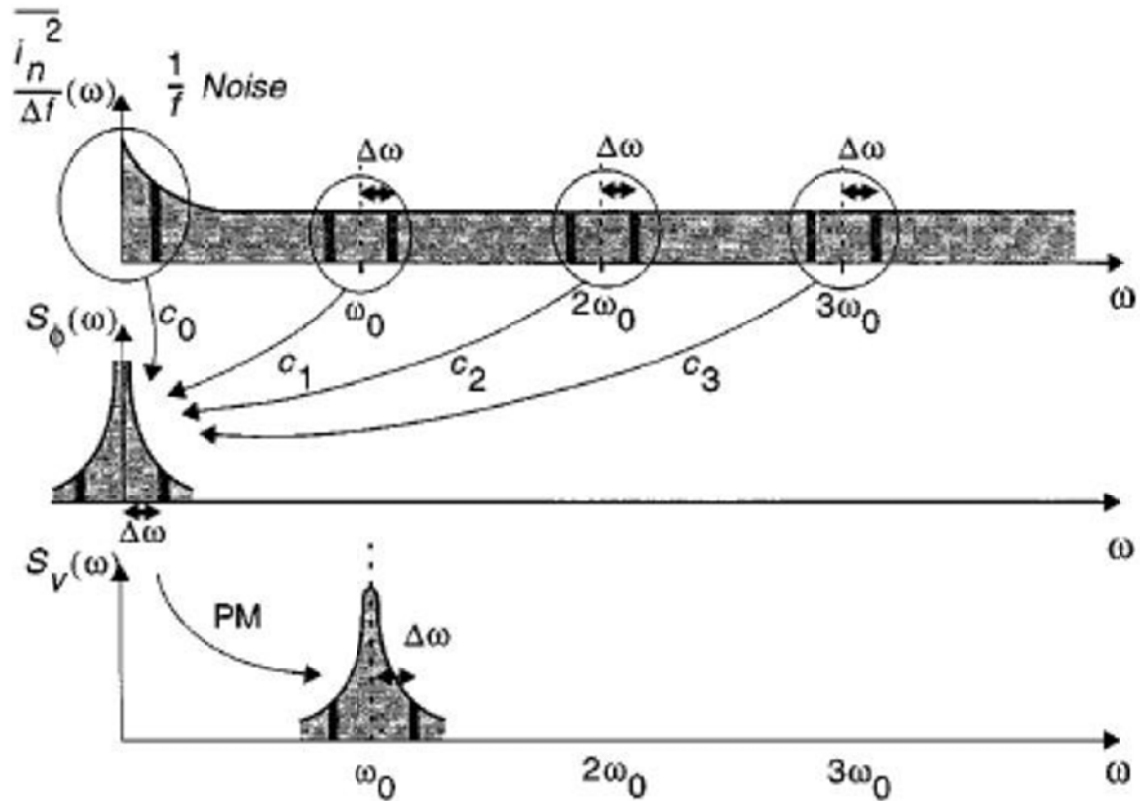


Figure 3.14: Procedure of current noise conversion into phase noise [14]

In equation (3.30),  $i_n$  represents for the magnitude of current noise,  $\Delta f$  is regarded as the bandwidth of noise impulse, flicker noise frequency of the components is illustrated by  $\omega_{1/f}$ , the desired offset frequency for calculating the phase noise is shown by  $\Delta\omega$ , the maximum charge tolerated by capacitors in the tank is given by  $q_{\max}$  and finally the  $\Gamma_{\text{rms}}$  shows the root mean square of the impulse sensitivity function.

Here, we have presented a formula to determine the phase noise of the  $1/f^3$  region. To obtain a precise value of phase noise in  $1/f^3$  region, we should define the current noise generated by the relative flicker noise. The expression is as following:

$$\overline{i_{n,1/f}^2} = \overline{i_n^2} \frac{\omega_{1/f}}{\Delta\omega} \quad (3.31)$$

The  $c_0$  coefficient in Fourier series indicates the DC value of the impulse sensitivity function. Therefore, we combine the equations (3.30) and (3.31) to determine the phase noise produced in  $1/f^3$  region.

$$L(\Delta\omega) = 10 \log \left( \frac{c_0^2}{q_{max}^2} \frac{\frac{i_n^2}{\Delta f}}{8\Delta\omega^2} \frac{\omega_{1/f}}{\Delta\omega} \right) \quad (3.32)$$

To calculate the relative corner frequency of  $1/f^3$ , we set the equations (3.30) and (3.32) equal to each other. Therefore, we get:

$$\Delta\omega_{1/f^3} = \omega_{1/f} \frac{c_0^2}{4\Gamma_{rms}^2} = \omega_{1/f} \left( \frac{\Gamma_{dc}}{\Gamma_{rms}} \right)^2 \quad (3.33)$$

As we know,  $\sum_{n=0}^{\infty} c_n^2$  is equal to  $2\Gamma_{rms}^2$  so we can improve the phase noise performance at all offset frequencies by reducing the coefficients of impulse sensitivity function. It is understood from equation (3.33) that we can reduce the noise spectrum of  $1/f^3$  region by reducing the constant value of impulse sensitivity function. In practice, this idea is achieved by reducing the rise and fall times of the oscillator to generate more symmetrical outputs. Additionally, this formula reveals the interaction between the phase noise and the resonator dissipation. In other words, if the resonator dissipation is compensated by transistor pairs; the overall phase noise will be improved. This idea is verified when the output is at its peak value.

### 3.3.3 F-Parameter

Rael and Abidi dedicated their research to identify the effect of noise generators on overall phase noise performance of a VCO [15]. They presented a formula in which all noise sources and their effects are taken into account. Their experimental equation is as following:

$$F = 1 + \frac{2\gamma R_p I_{bias}}{\pi V_0} + \gamma \frac{4}{9} g_{d0,bias} R_p \quad (3.34)$$

Now, we consider that the oscillator is in current-limited region. Therefore, the second term in equation (3.34) will be equal to  $2\gamma$ . On the other hand, by

increasing the bias current, the phase noise performance will improve. Nevertheless, the output amplitude is restricted by the  $V_{dd}$  in voltage-limited region. Therefore,  $V_0$  does not change while the bias current increases. This causes the F-parameter to increase and consequently the phase noise performance will be corrupted. Overall, the best phase noise is achieved when the transistors are biased between the current-limited and voltage-limited regions.

### 3.4 Analysis of Phase Noise Sources in CMOS LC VCOs

In this section, the phase noise contributors are identified in our design. Therefore, it is better to analyze each of the phase noise contributors individually. However, unlike previous chapter, the resonator noise is explained briefly. Moreover, a complementary mechanism for achieving a better noise performance is introduced. A simple schematic of LC VCO is shown in Fig. 3.15. As we see, the phase noise contributors are illustrated individually.

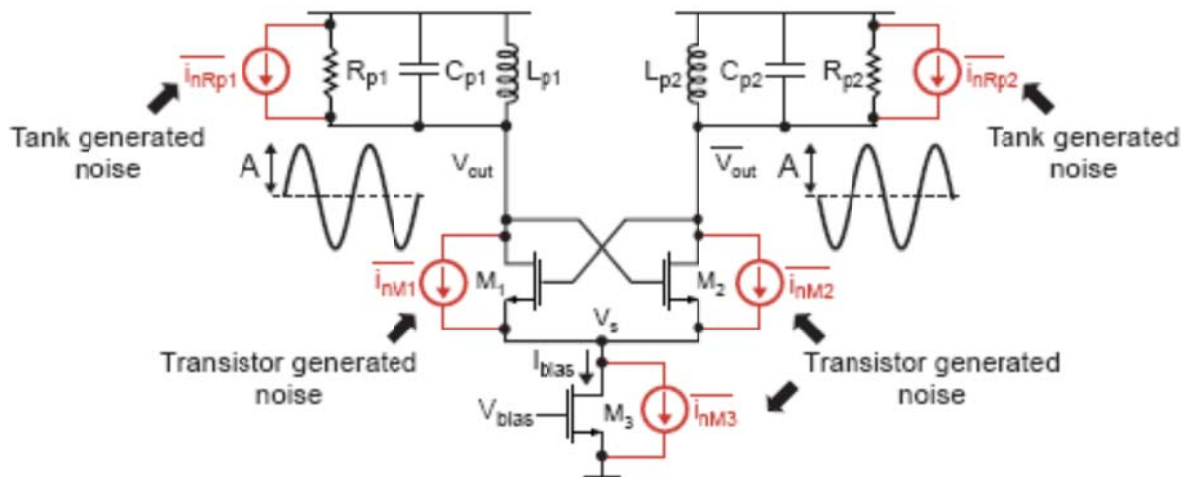


Figure 3.15: Noise sources in LC cross-coupled VCO

#### 3.4.1 Transistor Noise Contribution

As we described briefly in Section 3.3, when the circuit is oscillating in very low or high frequencies, it suffers from the phase noise corresponding to the active devices. Therefore, it is more logical to investigate all of the noise contributors in an oscillator regardless of the operation frequency.

### 3.4.2 Noise Contributors in MOSFET

The noise contributors in a MOSFET device are divided into two groups of internal and external noises. As shown in Fig. 3.16, a lumped model is presented in which all of the noise generators are illustrated. The external noises shown in the figure are produced by terminal parasitic capacitors. Additionally, the resistances of the metal to semiconductor connection can add some extrinsic noise to our design. On the other hand, the internal noise is also divided into two groups of thermal and flicker noise.

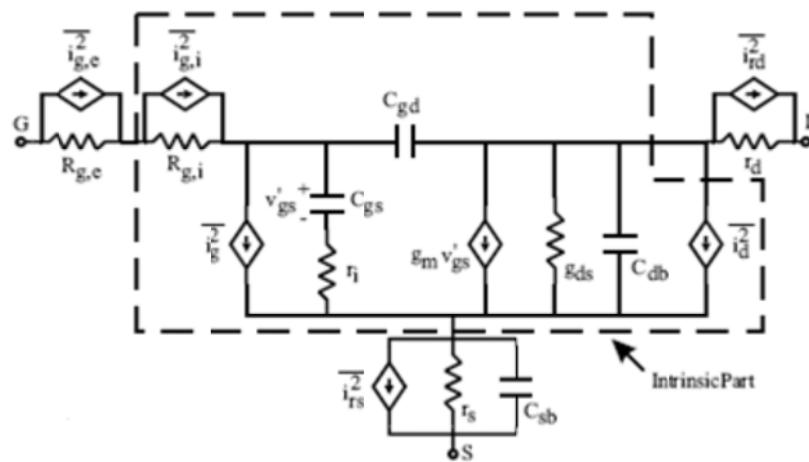


Figure 3.16: Lumped noise model

#### 3.4.2.1 Thermal Noise

There are some sources which are the main contributors of the thermal noise. The noise produced by the resistance of the gate is one of the main sources. The gate resistance is expressed as following:

$$R_g = \frac{W \times R}{N \times L} \quad (3.35)$$

In equation (3.35),  $R_g$  generates thermal noise in which  $R$  is defined as sheet resistance and  $N$  represents for number of fingers. However, the resistance seen at the gate of the transistors can be optimized when performing the circuit layout. If we consider the gate resistance as an individual element, its value will be optimized as following:

$$R_{g,i} = \frac{R_g}{3} \quad (3.36)$$

Nevertheless, in the layout procedure, the gate resistance can be even less than above and hence this leads to better phase noise performance. As a result, the overall noise seen from the gate resistance is formulated as following:

$$\overline{v_{g,i}^2} = 4kTR_{g,i}\Delta f \quad (3.37)$$

The Boltzmann's constant is shown by  $k$  while  $T$  represents the relative temperature. As understood from equation (3.35), the gate resistance is proportional to width, length and number of fingers. Therefore, we should keep these issues in mind while performing the final layout of the circuit. The channel noise is considered as the other contributor of thermal noise in the circuit. The second source of thermal noise in a MOSFET is the thermal channel noise. The carriers in the channel produce a relatively large drain noise which is regarded as a current noise. It is the most considerable noise source in a MOSFET. If the transistor is saturated, its corresponding noise is estimated as following:

$$\overline{i_d^2} = 4kT\gamma g_{d0}\Delta f \quad (3.38)$$

In equation (3.38), the gamma changes proportionally to the bias current while  $g_{d0}$  represents the channel transconductance. However, we can replace  $g_m$  instead of  $g_{d0}$  since the oscillator is functioning in the saturation region. The gamma parameter is proportional to the drain to source voltage. In other words, increasing  $V_{ds}$  produces a larger  $\gamma$ . For simplicity, gamma is estimated as  $2/3$  in our design. However, for short channel devices, the value differs.

On the other hand, a parasitic capacitance is seen between the gate and source of the transistor which generates a negligible noise called the induced gate noise. The corresponding expression is as following:

$$\overline{i_d^2} = 4kT\beta \frac{(\omega C_{gs})^2}{k_{gs}} \Delta f \quad (3.39)$$

In equation (3.39),  $\beta$  is a parameter depending on the bias current while  $k_{gs}$  is a coefficient for long channel devices. It is usually set to 4 in our design. Moreover, the induced gate noise will change due to the frequency variations. Obviously, we cannot use the above equation when the circuit is oscillating at very high frequencies.

### 3.4.2.2 Flicker Noise

As a matter of fact, for the lower oscillation frequencies, the noise spectral density improves. The flicker noise behaves differently from what we discussed about thermal noise. Actually, the flicker noise range is estimated between 100 kHz to some MHz. Since it is inversely proportional to frequency, we call it 1/f noise. Here, we discuss about a theory to clarify the flicker noise behavior. It shows that the charges stored near the silicon interface under the transistor's gate contribute to flicker noise. This theory is called the carrier density fluctuation. On the other hand, it illustrates that the gate bias voltage cannot affect the flicker noise while the noise power interacts closely with the charges stored beneath the gate of MOSFET.

The flicker noise is formulated as following for the saturation region.

$$\overline{i_f^2} = K_f \frac{g_m^2 \Delta f}{C_{ox}^2 W L f^\alpha} \quad (3.40)$$

### 3.4.2.3 Bias Noise

In the related bias circuit, there are also several noise contributors that should be taken into account. As mentioned before, if the circuit is oscillating at low frequencies, the flicker noise is mostly in focus while at high frequencies the circuit suffers from the thermal noise. In the design, the transistor pairs behave like mixers due to their switching capability. Therefore, the fundamental harmonic at  $\omega_n$  is upconverted to  $\omega_0 - \omega_n$  and  $\omega_0 + \omega_n$ . The frequencies are located symmetrically from the center frequency. Since the phase variations compensate each other, the overall noise is generated as AM.

### 3.4.2.4 Switching Pair Noise

In this section, we discuss the switching pair noise. It can be analyzed easily compared to previous models. As mentioned earlier, we focus on flicker noise at low frequencies due to its dominant effect on the circuit performance. In this region, a small impedance is measured from the transistor drain. However, we neglect it and hence it will be considered as short. Consequently, the flicker noise can be modeled as parallel with the bias noise [15]. Moreover, the flicker noise will be upconverted. On the other hand, the active devices linearity plays an important role in the overall phase noise performance. To reduce the flicker noise, we can decrease the width of transistors.

### 3.4.2.5 Resonator Noise

Finally, we should consider the noise corresponding to our tank circuit. As discussed in previous chapter, we can assume all of the noise contributors in the VCO as a negative resistance thermal noise. On the other hand, the F-parameter connects all of the noise sources to each other. For simplicity, we ignore the noise of active devices and hence the F-parameter will be equal to unity. In other words, we are analyzing the equation (3.34) that is presented by Rael and Abidi for the tank noise. The following formula expresses the noise produced by the loss of passive elements in the resonator.

$$L(\omega) = 10 \log \left( \frac{2kT}{P_{signal}} \left( \frac{1}{2Q} \frac{\omega_0}{\Delta\omega} \right) \right)^2 \quad (3.41)$$

## **4. STATE-OF-THE-ART DESIGN**

### **4.1 Introduction**

In this chapter, we present some low phase noise LC architectures. One of the most recent topologies is a quadrature VCO with integrated back gate coupling. Nowadays, quadrature VCOs are widely applicable in transceivers. One of the drawbacks of this topology is higher power consumption than the previous LC VCO architectures. To get an optimum result regarding the power and the phase noise simultaneously, a much simpler design is presented. At the end of this chapter, we compare all of the benefits and drawbacks of different VCO architectures. Finally, a low noise low power CMOS LC oscillator is designed.

### **4.2 Low Phase Noise QVCO**

Nowadays, CMOS technology is the most applicable solution for modern wireless communication devices. The challenge of being implemented on a single chip makes the design much complicated. In this topology, high efficient transmission is performed by the help of quadrature-amplitude modulation and the frequency division technique. Recently, some transceivers use quadrature oscillators to drive mixers for performing frequency conversion. However, the signal is susceptible to the phase noise disturbances. There are different methods to produce the quadrature signal. The differential voltage controlled oscillator, the quadrature coupling of two simple LC VCOs, the ring oscillators and the frequency division technique are the most common procedures for producing a low phase noise signal. The quadrature topology is popular among designers due to its high performance regarding the phase noise. The quadrature topology can be done in different ways. Back-gate coupling or adding some transistors to the VCO core are some common procedures. One of these approaches is called source resistive degeneration which has a noticeable impact on phase noise improvement in quadrature VCOs. In this state-of-the-art design, we take advantage of source resistive degeneration and back gate coupling simultaneously. In other words, we put the both procedures into one single model to achieve a significant output with low power dissipation and low phase noise at the same time.



used as coupling elements. A simple conventional quadrature VCO is depicted in Fig. 4.2.

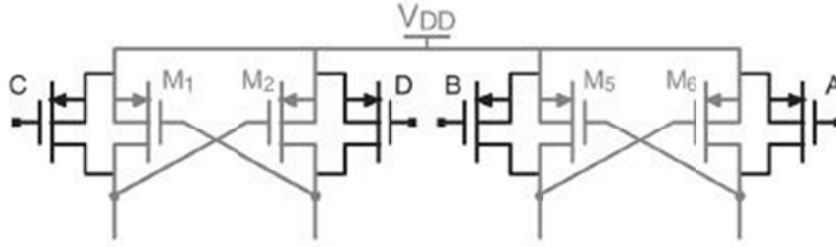


Figure 4.2: Conventional Quadrature VCO

In our proposed design, these extra transistors are omitted due to the back-gate coupling technique. Consequently, the circuit performance improves due to the reduction of noise sources. As described in previous chapters, adding more transistors leads to extra noise of the circuit. Flicker noise of NMOS and PMOS transistors are the main factors that should be considered in our design. Therefore, the corresponding phase noise can be formulated as following:

$$L(\Delta\omega) = 10 \log \left[ \frac{c_0^2}{q_{max}^2} \left( \frac{\overline{i_{n,N}^2}/\Delta f}{2\Delta\omega^2} \cdot \frac{\omega_{1/f,N}}{\Delta\omega} + \frac{\overline{i_{n,P}^2}/\Delta f}{2\Delta\omega^2} \cdot \frac{\omega_{1/f,P}}{\Delta\omega} \right) \right] \quad (4.1)$$

$C_0$  shows the symmetry of the output signal. Actually, it is the coefficient of the Fourier series for the impulse function. The  $\overline{i_{n,N}^2}/\Delta f$  represents the overall noise density produced by NMOS pairs and its corresponding frequency is shown as  $\omega_{1/f,N}$ . For the PMOS transistors, the terms  $\overline{i_{n,P}^2}/\Delta f$  and  $\omega_{1/f,P}$  represents the overall noise density and the corner frequency respectively. NMOS transistors are the main noise contributors in our design due to the flicker noise up-conversion. Therefore, it is useful to take care of this issue by applying some resistors on the source of NMOS transistors. This is called source resistive degeneration technique. Therefore, by applying a resistance at each NMOS source, the transconductance will decrease by a coefficient of  $1/(1 + g_{m,NMOS}R_{source})$ . As far as  $\omega_{1/f,N}$  is proportional to  $g_{m,NMOS}$ , the angular corner frequency decreases as well. On the other hand, the transconductance is set at a fixed point

by the help of  $R_{\text{source}}$ . This technique gives more symmetry to the drain current. In this case, more improvement in phase noise is achieved.

A designer might think that this technique can be considered for PMOS transistors as well. However, in our circuit, the PMOS transistors should have quite large  $g_m$  for phase locking. Consequently, this procedure might not be suitable for PMOS transistors. On the other hand, we encounter some limitations when designing the  $R_{\text{source}}$ . High  $R_{\text{source}}$  value can ruin the oscillation initial condition and produce some additional disturbances.

The circuit is designed in CMOS 65nm technology. There is a big challenge for selecting a proper inductance. The quality factor of the inductor should be considered as well. We use a spiral structure for designing the inductor. Its value is 2.1 nH and its corresponding quality factor is 15. As observed in the final results, the value of  $R_{\text{source}}$  is 26 ohm.

#### 4.2.2 Design Specifications

The oscillation frequency is functioning between 2.25 to 2.55 GHz when the  $V_{\text{tune}}$  is tuned from 0.2 to 1.2 V. Our designed output power varies from -0.5 to -1.6 dBm. In the frequency range of 2.25 to 2.55 GHz, the best result is achieved at 2.4 GHz. The varactor used in our design has a hyperbolic capacitance versus voltage curve. This makes the middle of tuning range a critical point. At 2.4 GHz, the phase noise is -140dBc/Hz at 1 MHz offset frequency. Our designed quadrature VCO consumes 3mA from a 1.2V supply voltage. The equation for calculating the figure of merit for VCO is as following:

$$\text{FOM} = L\{\Delta\omega\} - 20 \log\left(\frac{\omega_0}{\Delta\omega}\right) + 10 \log(P_{\text{DC}}) \quad (4.2)$$

### 4.2.3 Simulation Results

As described in the introductory part, we have designed a 2.4 GHz quadrature VCO. Its corresponding phase noise is -140 dBc/Hz at 1 MHz offset frequency. In the design procedure, two simple CMOS LC VCO are coupled together to satisfy the oscillation condition at the desired frequency. The body terminal of PMOS transistors are connected together via coupling capacitors. Additionally, four resistances are added to the source of NMOS transistors to reduce the transconductance as much as possible. Therefore, we have less  $g_m$  variation at the output. On the other hand, phase noise is decreased as well. This is called source resistive degeneration technique.

### 4.3 Low Noise Low Power CMOS LC VCO

Oscillators are inevitable blocks in designing communication systems. There are different LC VCO topologies in communication electronics. LC VCOs are mainly applicable in highly efficient transmitters and receivers. VCOs are used as inputs for the mixers to produce desired outputs. Therefore, they are quite noticeable in highly integrated transceivers. Low noise and high signal amplitude should be achieved for obtaining a reasonable performance in a VCO design. To obtain a state-of-the-art design, two specifications should be met at the same time. LC VCOs are mostly popular due to this issue. They achieve an ultra-low noise with low power dissipation simultaneously. Therefore, the designers are encouraged to design efficient LC VCO topologies. Nowadays, lots of investments have been focused on designing CMOS LC VCOs using on-chip resonators. The drawback is that fully integrated LC VCOs consume lots of power. Therefore, external LC VCO topologies are still used in recent cell phones. In this design, we aim for an optimal circuit using fully integrated VCOs. Our goal is to produce outputs with lower phase noise and power dissipation comparing with conventional off-chip LC VCO topologies. This work mainly concentrates on design of fully integrated VCOs with optimized power consumption and phase noise lower than VCOs with external resonators. For this design, we mainly discuss the complementary LC VCO structure. Then, we compare its performance, regarding phase noise and power consumption, with conventional VCOs.

### 4.3.1 CMOS LC VCO

There are some noticeable advantages that make CMOS LC VCO an identical topology. Complementary VCOs are more economical than their conventional counterparts. Old topologies use only NMOS or PMOS transistors. In our design, we use both type of transistors at the same time. By adding PMOS transistors to conventional NMOS only VCOs, much larger transconductance is achieved. As we know, the tank used in the circuit is lossy. Since we generate a noticeably large transconductance, less current is needed to compensate the resonator loss. Therefore, much power is saved in this topology. On the other hand, using the PMOS and NMOS pairs simultaneously, we produce symmetrical waveforms at the output. Consequently, the flicker noise upconversion to the  $1/f^3$  region is reduced. The CMOS LC VCO is illustrated in the Fig. 4.3. If the VCO requirements are fulfilled, the circuit oscillates properly. In the theory, the amplitude increases gradually and stops in a point. Actually, when the negative resistance cannot compensate the resonator loss any further, the output will be stable. However, it is the case when the  $V_{dd}$  is not putting constraints on the output swing at the oscillation startup point. When operating at the current limited regime, the CMOS cross-coupled VCO is the best choice for the state-of-the-art design. Applying the same voltage and bias current, it generates a better phase noise comparing with its NMOS or PMOS counterparts. The phase noise can be analyzed in different aspects. First, the CMOS cross-coupled VCO tolerates a larger charge for the output swing. This maximum swing is illustrated as  $q_{max}$  in the Hajimiri's model. As the phase noise is inversely proportional to the maximum charge, the CMOS cross-coupled VCO generates a better phase noise comparing with its conventional counterparts. On the other hand, we can improve it to the Without Tail (WT) structure. The WT structure shows even a better performance than the fixed biasing topology. In the WT topology, the number of transistors is reduced. In another words, we decrease the number of noise sources. Therefore, the flicker noise sources are just of the cross-coupled pairs. Since switched biasing is applied in the design, the cross-coupled pairs do not affect the phase noise performance that much due to their low flicker noise. Overall, in this design, we improve the phase noise performance by omitting the tail transistor. On the other hand, since

the tail transistor is neglected, we do not have voltage headroom limitation in our design. However, the tail transistor in the fixed biasing structure put some constraints on the voltage headroom which can be problematic for low voltage topologies. In fixed biasing topology, the output signal has a low power. Since phase noise is defined as signal to noise ratio, low signal power can worsen the phase noise performance. Therefore, in the fixed biasing model, an individual circuit should be designed to bias the extra transistor. Consequently, the circuit dissipates more power and on the other hand we should model more noise generators for the fixed biasing design. In the FB topology, the noise produced by the extra biasing circuit is transferred to the tail transistor. In our design, we have solved this problem as well.

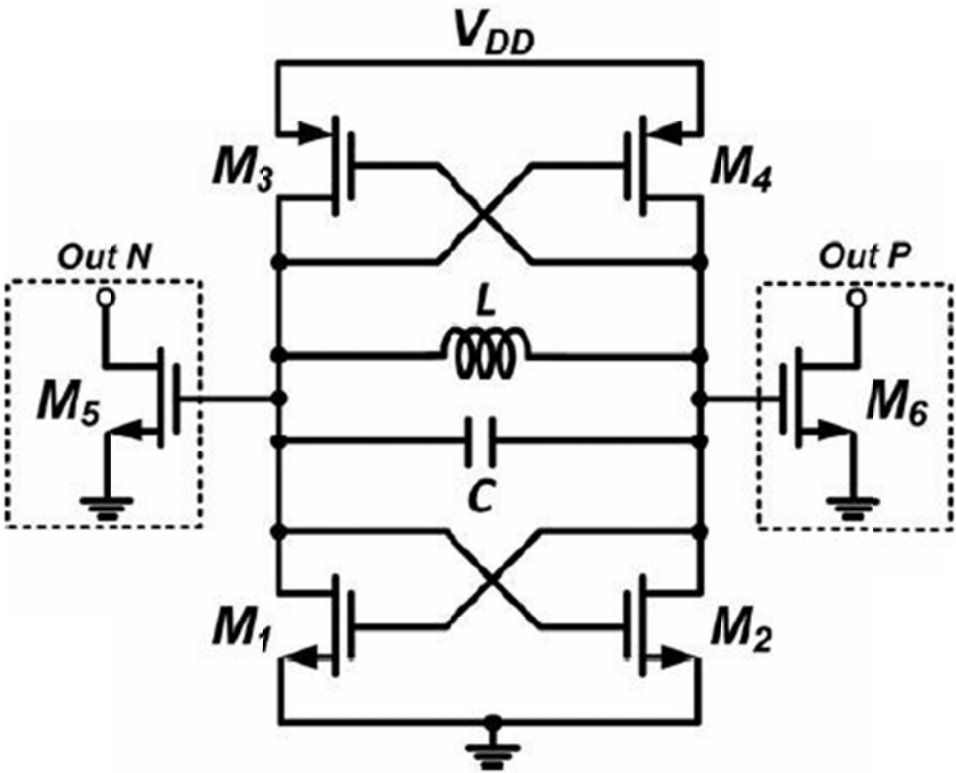


Figure 4.3: CMOS LC oscillator circuit schematic

In our presented structure, since the amplitude changes all the time, the current varies correspondingly. To maintain a proper oscillation condition, the NMOS and PMOS pairs used in our design should produce an appropriate negative

resistance. The transconductance produced by cross-coupled pairs should be inversely proportional to the overall resistance of the resonator. As obtained in our experimental simulations, we can optimize the power dissipation by improving the quality factor of our resonator. As a matter of fact, this will optimize the required transconductance as well. However, using fully integrated inductors generates some obstacles for the design. Fully integrated VCOs have low quality factors. On the other hand, there are some boundaries for increasing the quality factor of the inductors.

### 4.3.2 Power Analysis

If we apply  $V_{dd}$  as our supply voltage to the circuit, the voltage measured at the output could be estimated as  $V_{dd}/2$ .  $V_m$  represents the output amplitude by which the gate to source voltages can be formulated as following:

$$V_{gs1}=V_{dd}-V_{gs3}=V_{dd}/2+V_m\sin(\omega t) \quad (4.3)$$

$$V_{gs2}=V_{dd}-V_{gs4}=V_{dd}/2-V_m\sin(\omega t) \quad (4.4)$$

The NMOS transistors switch on when  $V_{gs} \geq V_{th,NMOS}$  and the PMOS transistors switch on when  $V_{sg} \geq |V_{th,PMOS}|$ . As observed in the theory, if we subtract the NMOS and PMOS current from each other the resonator current will be identified. Since one of the PMOS or NMOS transistors is switched on at each cycle, a larger current is conducted into the resonator. Consequently, when the current is driven by one of the  $M_1$  or  $M_3$  at each cycle, the power dissipation is reduced. On the other hand, since we reduce the number of transistors in each cycle, less noise is driven into the resonator. As observed in above equations, we should consider some limitations for choosing the right supply voltage. If we apply a supply voltage which is larger than the overall threshold voltage of the  $M_1$  and  $M_3$  transistors ( $V_{th,NMOS}+V_{th,PMOS}$ ), they will be switched on at the same time. Consequently, the circuit dissipates more power and extra noise will be conducted into the resonator. Increasing the overall noise in the circuit has an inverse impact on the phase noise performance. Overall, to dissipate less power and improve the phase noise performance, we should present a state-of-the-art structure. In this topology,  $M_1$  and  $M_3$  are not allowed to conduct at the same

time in each cycle. This is the same case for  $M_2$  and  $M_4$  transistors. Now, it is understood the reason to minimize the supply voltage to overall threshold of PMOS and NMOS transistors. Applying the  $V_{dd}$  equal to  $V_{th,NMOS}+V_{th,PMOS}$ , the output voltage will be estimated as NMOS threshold voltage ( $V_{th,NMOS}$ ). This ensures that  $M_1$  and  $M_3$  or  $M_2$  and  $M_4$  transistors would not be switched on simultaneously. Therefore, it guarantees that each of the NMOS or PMOS transistors is switched on for half of the oscillation cycle.

The other issue that should be analyzed in details is choosing a right inductor with a suitable resistance. The noise produced by the inductor has a power equal to  $v_n^2 = 4KTR$ . Optimizing the inductor's value has several impacts on the performance of the whole circuit. By reducing the inductor's value, its overall resistance will be decreased as well. Consequently, the phase noise performance will be improved because less noise is produced by the resistance. On the other hand, when the inductor generates less resistance, the corresponding transconductance for the transistors will reduce as well. This leads to less current and hence the power consumption will be optimized. Another advantage of choosing a small inductor is to decrease the reciprocal effect of inductors designed on our chip. On the other hand, when the inductor's size is minimized, a larger capacitor should be chosen to keep the oscillation frequency at the desired value. Larger capacitors will increase the maximum charge that can be tolerated. Based on Hajimiri's formula, increasing the  $q_{max}$  will improve the phase noise performance. If we consider a defined unit area on the chip, the capacitance value that can be allocated to that area is much larger than the inductance that can be specified to that space. Therefore, by reducing the inductor size and increasing the capacitor's value to fix the oscillation frequency at the desired value, the needed area on the chip will be minimized.

However, there are some constraints for decreasing the inductor's value. The tank amplitude can be modeled using a current source which turns on and off very fast from one transistor pair to the other. Since the voltage direction on the resonator changes in every moment, the current direction reverses dynamically through the resonator. Therefore, we can model the whole circuit as current source switching in two directions of  $I_{bias}$  and  $-I_{bias}$ . The current source is feeding the parallel RLC

tank all the time.  $R_{eq}$  is defined as the equivalent resistance of the resonator. At the resonance frequency, the inductor and the capacitor cancel each other due to their admittances. At the end, what remains is the equivalent resistance of the tank ( $R_{eq}$ ). Since the LC tank mainly weakens the effect of individual harmonics of the input current, the fundamental harmonic can produce a noticeable output swing. Its corresponding amplitude can be estimated as  $(4/\pi)I_{bias}R_{eq}$ . However, the output can be estimated as a sinusoidal waveform at higher frequencies. In sinusoidal waveforms, the output can be estimated as  $I_{bias}R_{eq}$ . Therefore, without considering these limitations, reducing the inductor value can be problematic. When decreasing the inductor value, the equivalent parallel resistance decreases as well. Consequently, the tank amplitude decreases noticeably. In our design, the overall resistance in parallel is estimated as  $R_p = r_s \times Q^2$  which is around  $320\Omega$ . To fulfill the startup condition, the transconductance should fit in the following formula:

$$g_{m,tank} \geq 1/R_p \quad (4.5)$$

To minimize the flicker noise upconversion effect, equal transconductance for the NMOS and PMOS transistors should be chosen. The width and length of transistors is decided by following equations:

$$\left(\frac{W}{L}\right)_{NMOS} = \frac{g_{m,NMOS}^2}{I_B \mu_n C_{ox}} \quad (4.6)$$

$$\left(\frac{W}{L}\right)_{PMOS} = \frac{g_{m,PMOS}^2}{I_B \mu_p C_{ox}} \quad (4.7)$$

To minimize the short channel noise, proper length and width should be chosen. Regarding phase noise calculation, Hajimiri presents a model as following:

$$L(\Delta\omega) = 10 \log \left[ \frac{\frac{i_n^2}{\Delta f} \sum_{n=0}^{\infty} c_n^2}{8q_{max}^2 (\Delta\omega)^2} \right] \quad (4.8)$$

$C_n$  represents the coefficients of the VCO Fourier series. As mentioned earlier,  $q_{\max}$  shows the maximum charge that can be stored in the capacitor. The noise power spectrum is shown by the term  $\frac{i_n^2}{\Delta f}$ . As discussed earlier, we can reduce the inductor noise by decreasing its value. Regarding this issue, the current needed for the compensation of lossy resonator will minimize. Consequently, the VCO suffers from less noise which is one of our goals. To meet the desired center frequency, if we reduce the inductor size the capacitor value should be increased. Applying the proper  $V_{dd}$  equal to the overall threshold voltage of an NMOS and a PMOS transistor, only two transistors will conduct in each of the half oscillation periods. This issue saves the power and decreases the overall noise. Overall, the phase noise performance will be improved.

## 5. LC VCO DESIGN

In this part, some basic cross-coupled LC oscillators are compared regarding low phase noise and power consumption. Selecting the most appropriate model, the oscillator is improved by reducing the effect of the phase noise to achieve a high FOM. Additionally, some LC voltage-controlled oscillators are implemented in order to decrease the power consumption as well as satisfying the phase noise. Usually, the bias current is maintained the same.

### 5.1 CMOS Cross-Coupled Models

The most common cross-coupled LC model is implemented. Additionally, NMOS, PMOS and CMOS cross-coupled topologies are analyzed in detail. In the following sections their benefits and drawbacks are compared as well.

#### 5.1.1 Analysis and Comparison

The aim of this chapter is to do a deep analysis between VCO models by applying equal power and using elements in 65nm library. We choose an inductor with a value of 3nH. Its quality factor is almost 10 at 2.4GHz. The supply voltage is fixed at 1.2V. The current source is set to 2.7mA. As we know, the CMOS model has larger swing output. The output of the CMOS topology is proportion to the bias current and the loss of tank.

The active devices are the standard 1.2V PMOS and NMOS transistors in the cadence tool. It indicates that  $V_{ds}$ ,  $V_{bs}$  and  $V_{gs}$  voltages should not go beyond 1.2V. An appropriate capacitor is chosen and its value is set regarding the oscillation frequency at 2.4GHz. An initial condition of  $\Delta V$  is applied to the capacitors. We keep the transconductance of NMOS and PMOS transistors the same. By selecting the same  $g_m$  for PMOS and NMOS transistors, a better phase noise is obtained since a symmetrical output is accomplished. The comparison is made by sweeping the transistor parameters in PSS analysis.

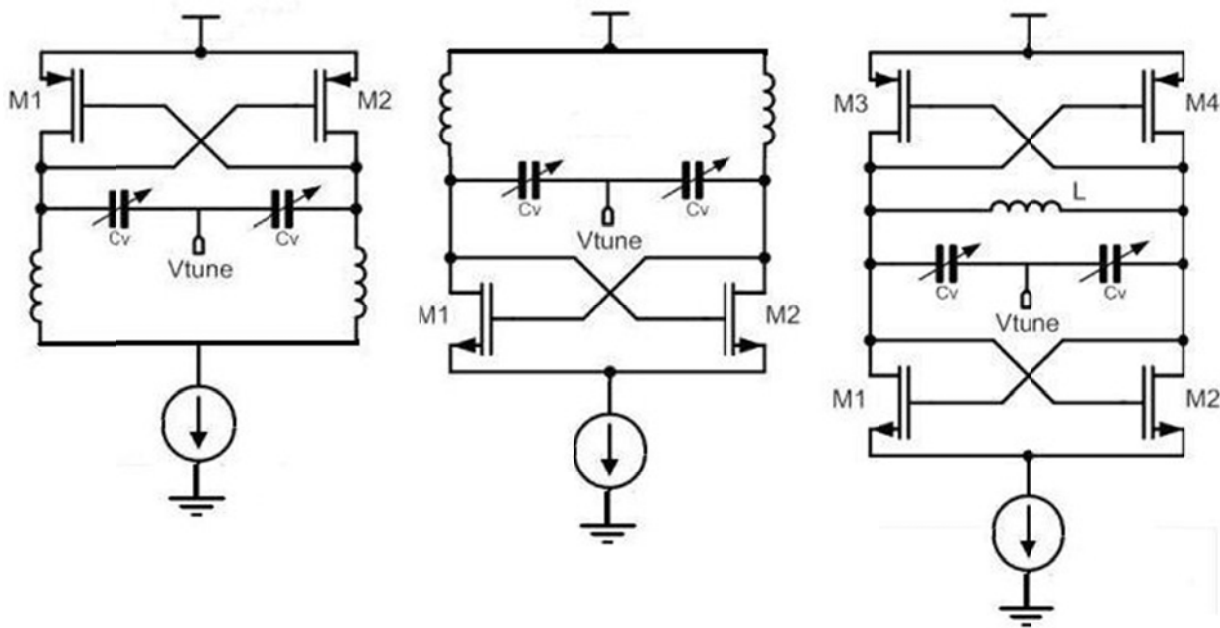


Figure 5.1: Different designs of CMOS cross-coupled VCO

However, we have not taken some issues into consideration. In our comparison, the current source is ideal. Half of the bias current is driven by the transistors on each side. It can lead to a negative voltage drop on bias current. For example, in CMOS topology if the  $W/L$  ratio is low, the  $V_{gs}$  will be able to have a larger value than  $V_{dd}/2$ . However, the designer must take the voltage headroom into account. Additionally, the noise of the bias circuit should be considered as well. On the other hand, the oscillation initial situation is not the same in theory and in practice. It starts at a lower loop gain compared to a practical circuit. The other issue is considering the ideal capacitance in our comparison. The capacitor has a very large quality factor. When using a varactor in the design, the quality factor is considerably less. In the real design the dimensions of the transistors are swept. Therefore, the total parasitic capacitance varies leading to shifts of frequency. In cross-coupled CMOS, the frequency change considerably due to low mobility of PMOS couples. Regarding the Leeson's formula, as the frequency rises, the phase noise of the circuit will increase.

However, the designer gets into an ambiguous understanding through this comparison. It is almost complicated to interpret the phase noise performance in detail. In PSS analysis, the results are shown briefly in the following figures for different offset frequencies. As mentioned before, it is considerably tough to interpret the graphs. Hence, the designer can hardly give precise comments on phase noise behavior.

In this section, we compare different topologies regarding the  $W_p/W_n$  ratio. The sizing of NMOS transistors providing an appropriate gain is 18/0.15. For PMOS design, the dimension of the transistors is 48/0.15. In theory, for low offset frequencies, PMOS satisfies the phase noise requirements but NMOS transistors may not fulfill the phase noise performance. As we know, high transistor width causes lower flicker noise. At 1MHz offset, cross-coupled structure accomplishes the most desirable phase noise performance while the phase noise of other structures is approximately 6dBc/Hz greater than the CMOS cross-coupled topology. As mentioned before, at high offset frequencies the flicker noise effect decreases and the most noticeable region is  $1/f^2$  region. Overall, the discussion shows that a sophisticated circuit should be designed for low offset frequencies.

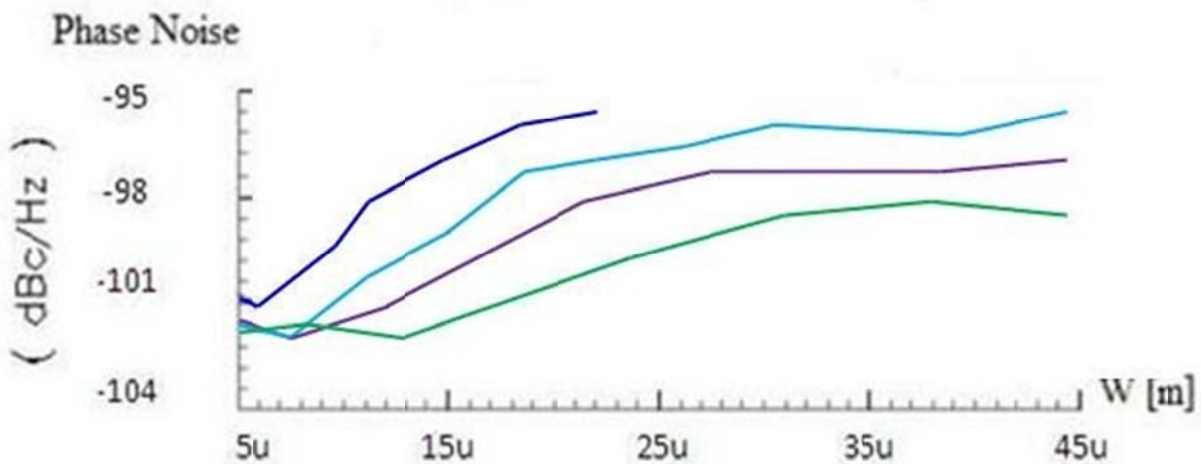


Figure 5.2: NMOS phase noise at 100 kHz offset frequency

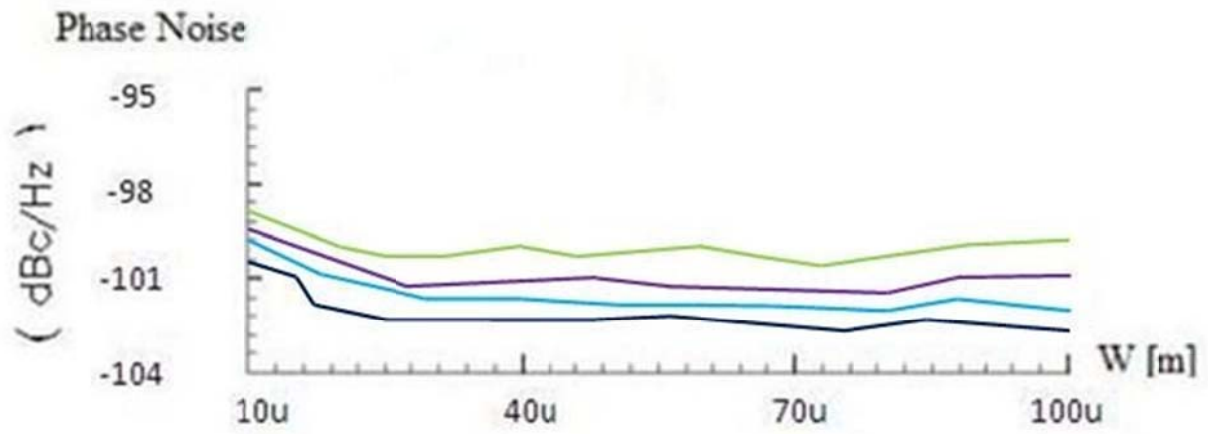


Figure 5.3: PMOS phase noise at 100 kHz offset frequency

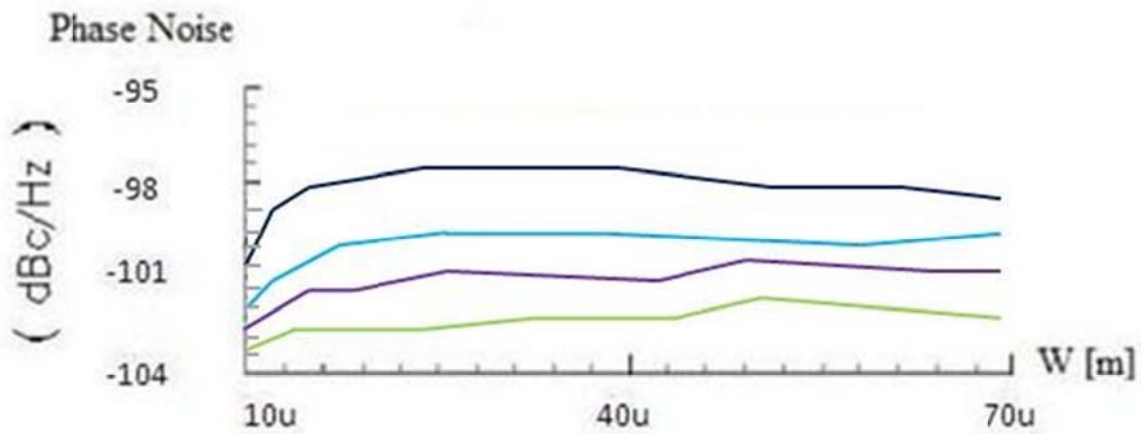


Figure 5.4: CMOS phase noise at 100 kHz offset frequency

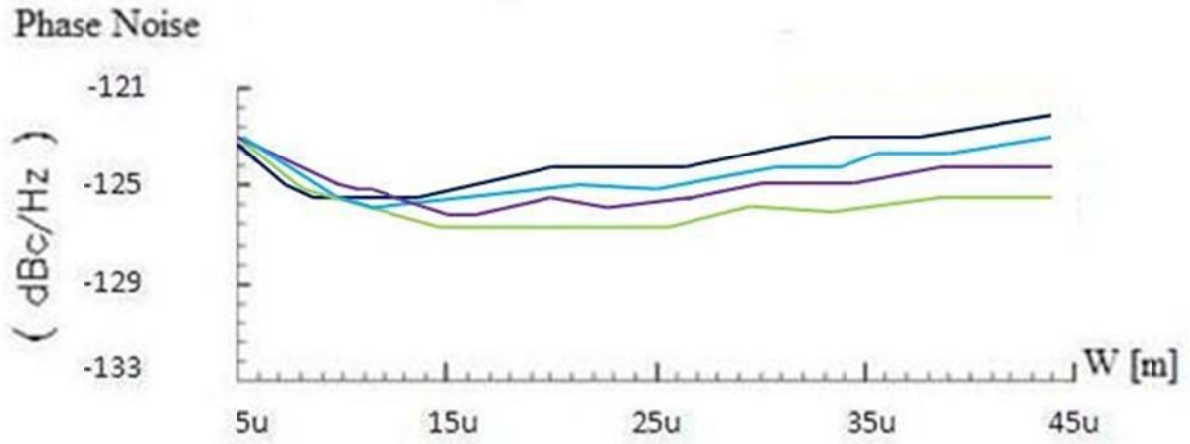


Figure 5.5: NMOS phase noise at 1MHz offset frequency

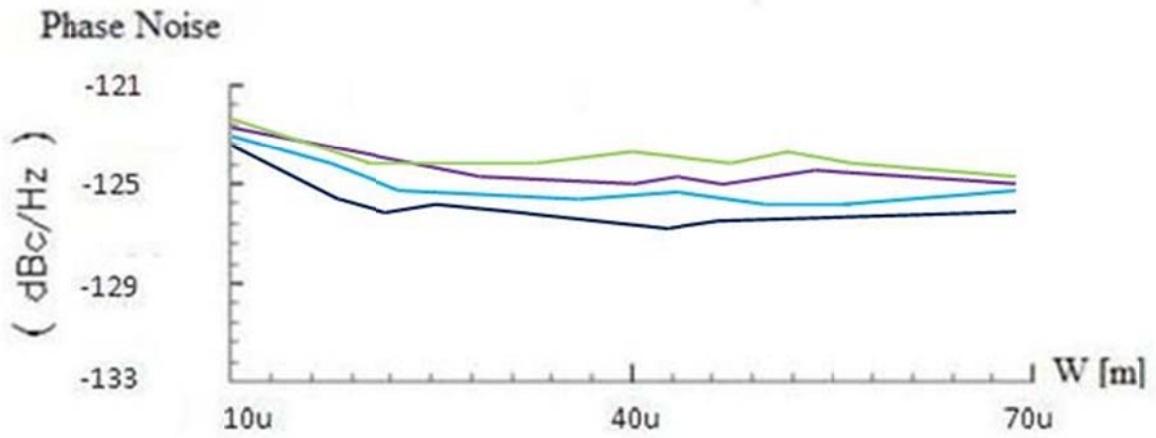


Figure 5.6: PMOS phase noise at 1MHz offset frequency

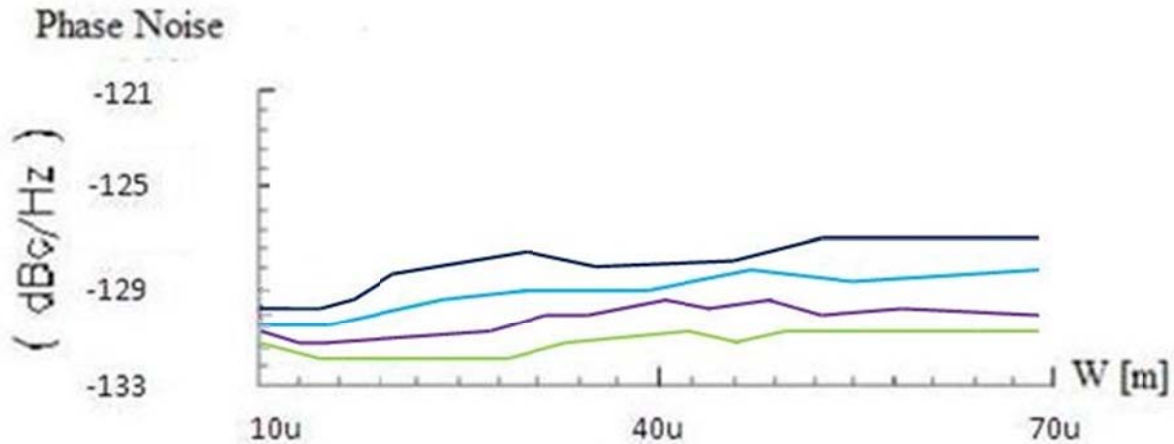


Figure 5.7: CMOS phase noise at 1MHz offset frequency

## 5.1.2 Design Procedure

Various types of cross-coupled LC VCO are analyzed in this section. In this design, a 500mV output swing is obtained with a bias current set at 2.7mA. When choosing the proper transistor dimension, the phase noise specifications are fulfilled for all designed VCO topologies. The lowest length should be used for CMOS transistors to decrease parasitic capacitors. The transistor which is used in the bias circuit should have a low overdrive voltage due to the limited supply voltage.

### 5.1.2.1 Cross-Coupled LC VCO

At this point, the cross-coupled LC oscillator with NMOS bias circuit shown in the Fig. 5.8 is implemented. Applying a supply voltage of 1.2V, with proper W/L ratios, the  $V_{gs}$  will be so high that the headroom voltage of the bias transistor decreases. Therefore, it avoids the desired current to flow in the circuit. As described in previous chapter, we can upgrade the circuit to the WT topology to solve this problem.

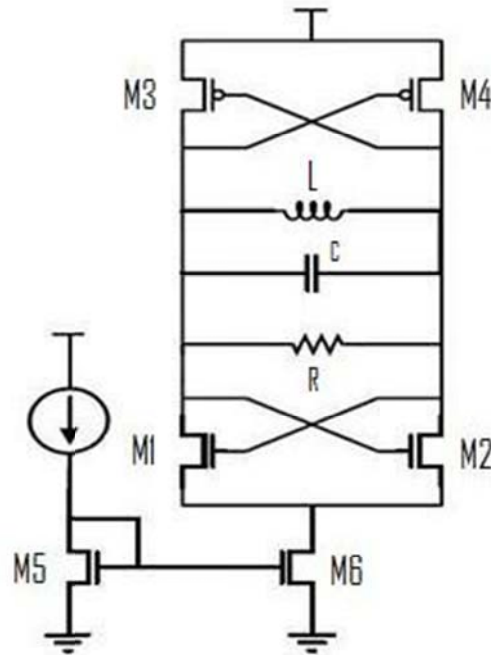


Figure 5.8: CMOS cross-coupled LC oscillator with NMOS bias circuit

When analyzing the circuit, there are some conditions that should be taken into the account during our design. When increasing the W/L ratio of the switching pair, the designer encounters some issues. By increasing the W/L ratio, the bias transistor copes with the voltage drop so the current flows easily through the circuit. However, the parasitic elements reveal more than before. Consequently, the tuning range would be limited.

CMOS LC Oscillator	PMOS		NMOS		Reference Current		Capacitance [pF]
	W[ $\mu\text{m}$ ]	L[ $\mu\text{m}$ ]	W[ $\mu\text{m}$ ]	L[ $\mu\text{m}$ ]	W[ $\mu\text{m}$ ]	L[ $\mu\text{m}$ ]	
PMOS-Bias	60	0.15	34	0.15	25	0.15	0.62
NMOS-Bias	60	0.15	34	0.15	50	0.15	1.3
Self-Bias	27	0.15	15	0.15	-	-	0.9

Table 5.1: CMOS cross-coupled LC VCO dimensions

Below, we present a simulation of the CMOS cross-coupled topology. The important challenge is the bias transistor in the design. As mentioned in previous sections, it should operate in saturation region. On the other hand, there is a low voltage drop on  $V_{ds}$ . In the simulation, the tail current is 2.4mA which is less than the theoretical assumption. The sizing of transistors is larger than other topologies. The parasitic capacitors play an important role for estimating the overall capacitance. Therefore, a 0.62pF capacitor is needed to set the oscillation at the desired frequency when using the PMOS transistor for the bias circuitry.

As we observe in the following simulation results, the self-biased architecture is more preferable. In this design, we minimize the tuning range limitations. Therefore, by choosing the suitable width and length for the transistors, we can easily meet the design specifications.

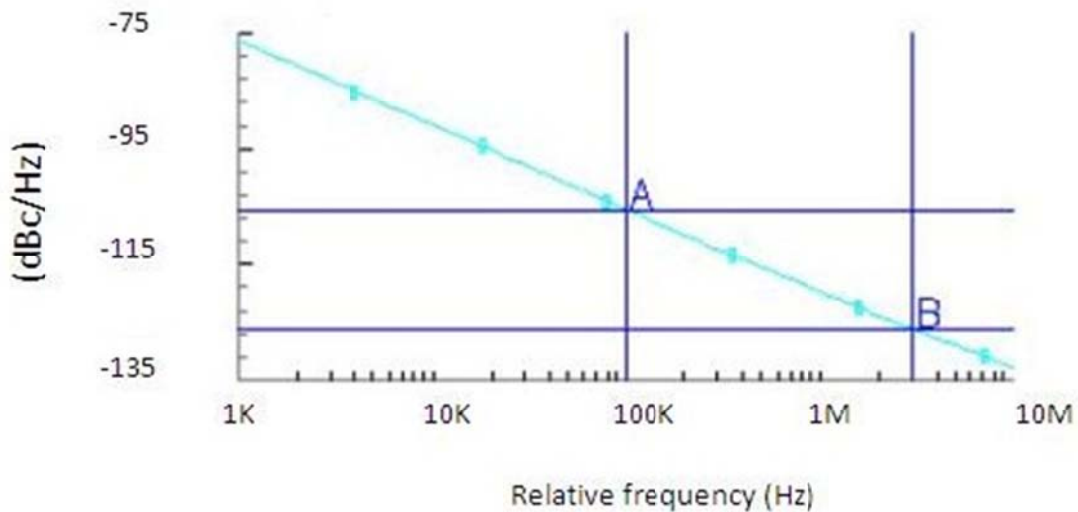


Figure 5.9: Phase noise of CMOS cross-coupled VCO with NMOS bias circuit

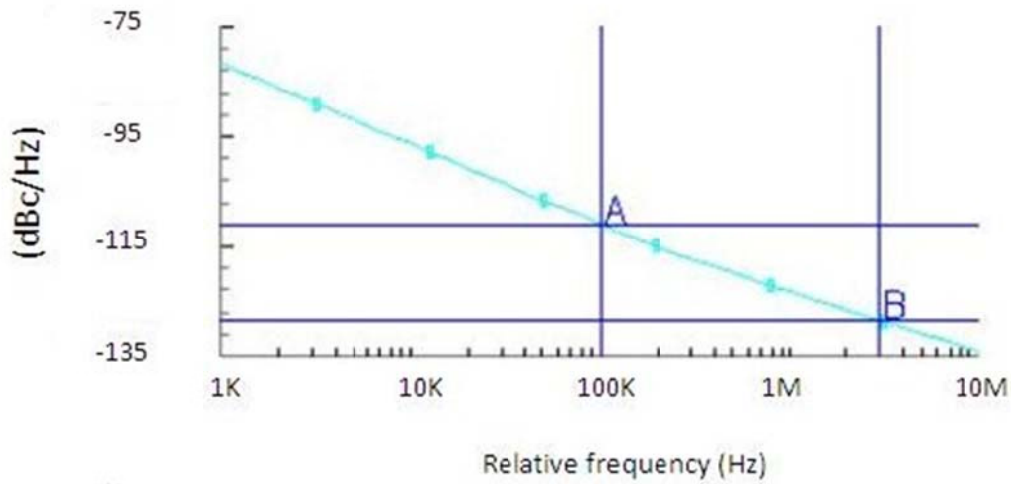


Figure 5.10: Phase noise of CMOS cross-coupled VCO with PMOS bias circuit

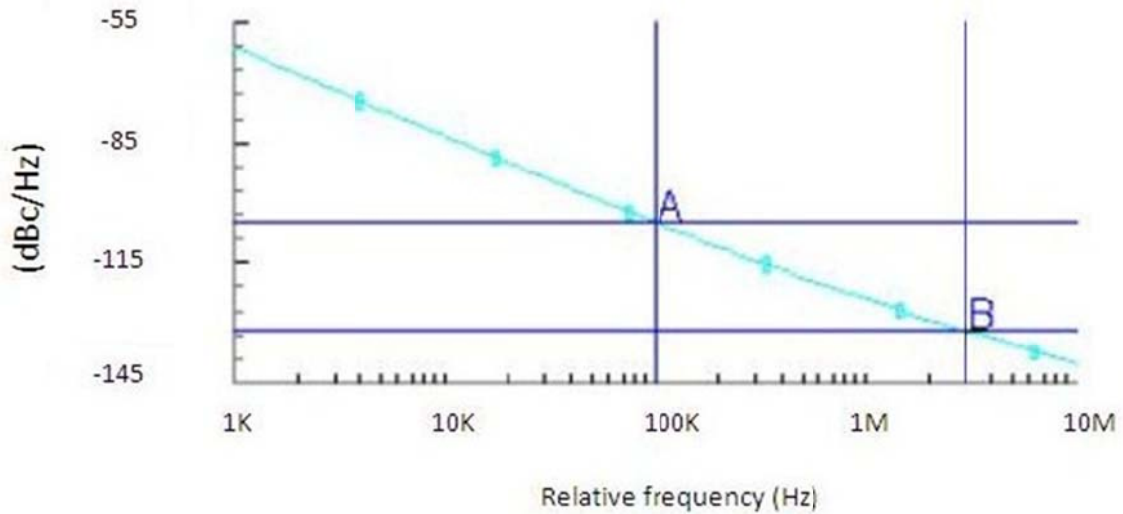


Figure 5.11: Phase noise of self-biased CMOS cross-coupled VCO

### 5.1.2.2 NMOS LC VCO

Two different designs are analyzed in this section. In this topology, we can satisfy biasing condition easily. Therefore, the sizing of the transistors is decreased by a coefficient. We increase the value of capacitance so the circuit will oscillate at the desired frequency.

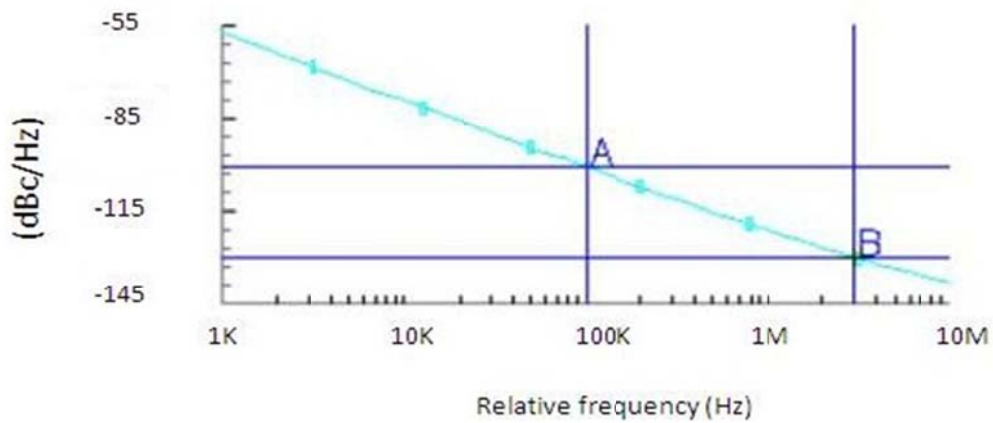


Figure 5.12: Phase noise of NMOS VCO with NMOS bias circuit

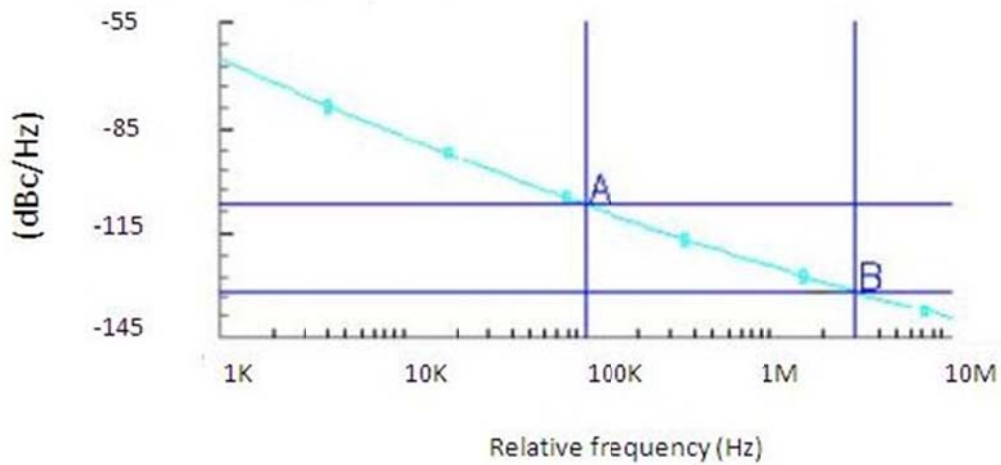


Figure 5.13: Phase noise of NMOS VCO with PMOS bias circuit

In the following table, we specify the transistor dimensions of an NMOS LC VCO.

NMOS LC Oscillator	NMOS		Reference Current		Capacitance
	W[ $\mu\text{m}$ ]	L[ $\mu\text{m}$ ]	W[ $\mu\text{m}$ ]	L[ $\mu\text{m}$ ]	[pF]
NMOS-Bias	18	0.15	15	0.06	2.37
PMOS-Bias	18	0.15	30	0.06	2.37

Table 5.2: NMOS cross-coupled LC VCO dimensions

### 5.1.2.3 PMOS LC VCO

As mentioned in the previous chapter, the cross-coupled topology can be optimized by using proper transistors in the bias circuit. In the following part, the sizing of the transistors and phase noise analysis are shown in detail.

PMOS LC Oscillator	PMOS		Reference Current		Capacitance
	W[ $\mu\text{m}$ ]	L[ $\mu\text{m}$ ]	W[ $\mu\text{m}$ ]	L[ $\mu\text{m}$ ]	[pF]
NMOS-Bias	48	0.15	10	0.06	1.97
PMOS-Bias	48	0.15	20	0.06	2.1

Table 5.3: PMOS cross-coupled LC VCO dimensions

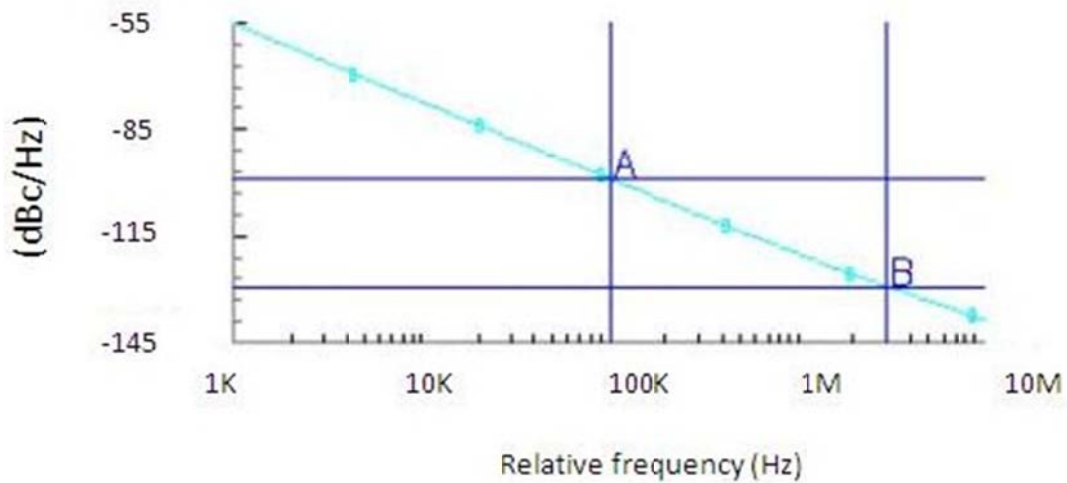


Figure 5.14: Phase noise of PMOS VCO with NMOS bias circuit

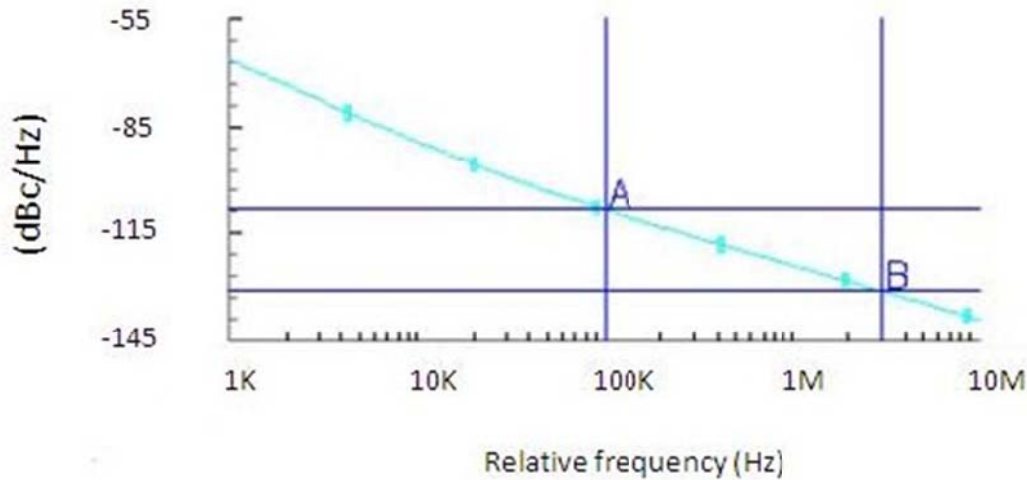


Figure 5.15: Phase noise of PMOS VCO with PMOS bias circuit

### 5.1.3 Comparison of Different VCO Topologies

Generally, the cross-coupled topology using NMOS and PMOS pair is preferred mostly among designers due to its phase noise performance. However, it is not always the case. In some designs, the CMOS topology puts some constraints on the supply voltage. Therefore, the optimum phase noise performance cannot be met by CMOS cross-coupled topology all the time. To solve this problem, the sizing of the transistors and the W/L ratio are increased. Consequently, we will have a large transconductance. Therefore, it will worsen the thermal noise of switching transistors. Additionally, the output suffers from a large harmonic distortion due to the nonlinearity of the transistors. On the other hand, low  $V_{gs}$  causes the oscillator to function improperly.

As it is observed in simulation results, the PMOS bias circuit exhibits better phase noise performance than its NMOS counterpart. However, at high frequency offsets, this improvement does not persist. This difference can be analyzed in different aspects. PMOS bias transistor has a larger width than its NMOS counterpart. On the other hand, in the 65nm technology, it is observed that PMOS transistor has the least flicker noise. Therefore, it is much logical to use the PMOS bias circuit in the design.

Generally, the PMOS topology is more practical in LC VCO design. However, it has some drawbacks that should be taken into account. The main disadvantage is that the output transistor is biased at  $V_{SS}$  so it is prone to noises on ground. In practice, this can degrade the function of PLL in some cases. For instance, when accompanying with a digital circuit on the same  $V_{SS}$ , the functionality of the whole circuit will be affected.

In the following table, we have compared the different LC VCO topologies regarding the phase noise and power consumption.

Architecture	Phase Noise at 100kHz [dBc/Hz]	Phase Noise at 3MHz [dBc/Hz]	Supply Voltage [V]	Bias Current [mA]
NMOS-Nbias	-103	-129	1.2	2.65
NMOS-Pbias	-107	-132	1.2	2.68
PMOS-Nbias	-100	-130	1.2	2.68
PMOS-Pbias	-109	-131	1.2	2.7
CMOS-Nbias	-106	-127	1.2	2.4
CMOS-Pbias	-111	-128	1.2	2.47
CMOS-Self-bias	-107	-133	1.2	2.6

Table 5.4: Comparison of different VCO topologies regarding the phase noise and power consumption

## 5.2 Bias Circuitry Design

In LC VCO design, the sizing of the current mirror has an effect on selecting the proper value for supply voltage. The current is related to  $V_{ds}$  in saturation region. The drain to source voltage should be considerably large to pave the way for the desired value of current.

Simply,  $V_{ds}$  should be equal to  $V_{gs}$  in 65nm technology. Theoretically,  $V_{supply}$  is equal to  $V_{ds} + (V_{gs} - V_{th})$ . Here, the transistors transconductance is larger than the inductor loss. The sizing of the transistors should be chosen properly to maintain the desired  $V_{gs}$ . In our simulations, we have increased the size of bias transistors to observe their effect on the phase noise performance. As described in previous chapters, one of the main sources of the phase noise in  $1/f^3$  region is the flicker noise upconversion of the bias transistors.

## 6. COMPLEMENTARY SIMULATIONS AND RESULTS

### 6.1 Introduction

In this chapter, we verify our previous results by a more detailed analysis. Here, we do the final integration of VCO sub-blocks to approach the state-of-the-art phase noise and power consumption. To meet the design specifications precisely, we have tested VCO performance for varying temperature, supply voltage and tuning range. Additionally, a wider comparison is made between different VCO topologies regarding the phase noise and power consumption. As a result, we have obtained a deeper understanding of different VCO topologies regarding their applications and frequency range of oscillation.

### 6.2 Phase Noise and Frequency vs. Control Voltage

In this section, to verify the frequency range of our designed QVCO, the tuning voltage is swept from 0.2 V to 1.2 V. From the simulation results, the frequency range is observed from 2.25 GHz to 2.55 GHz. The center frequency is 2.4 GHz which matches our specification requirements. Moreover, due to control voltage and frequency variations, the phase noise changes correspondingly.

In Fig. 6.1, the blue plot demonstrates the frequency variation controlled by tuning voltage while the red curve shows the phase noise variation versus frequency and tuning voltage.

As understood from the red plot, the phase noise is considerably high at low tuning ranges. At low tuning voltages, the quality factor of the varactor is quite small. Therefore, the overall quality factor of the resonator reduces and this leads to higher phase noise. However, as the tuning range increases, the phase noise improves and finally it reaches to our desired value at the center frequency.

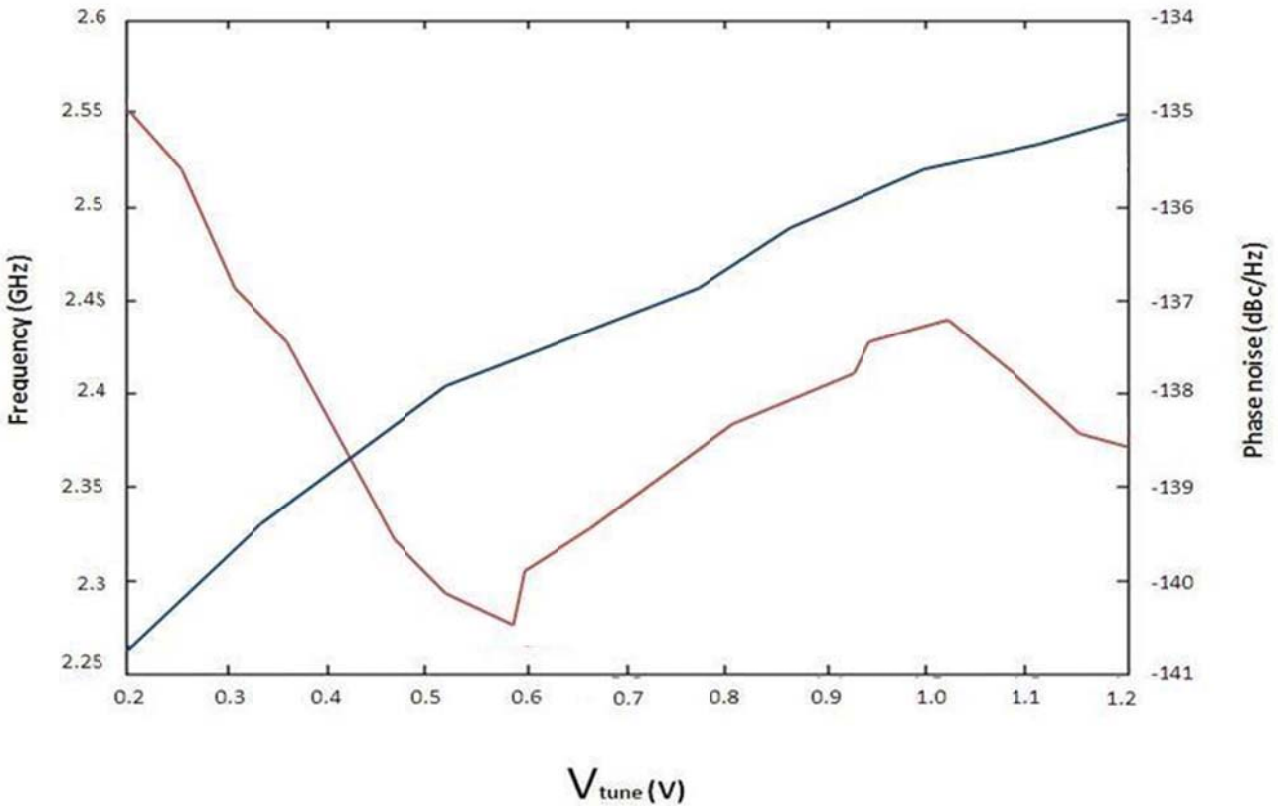


Figure 6.1: QVCO phase noise (red) and frequency (blue) versus control voltage

### 6.3 Reference Current Source Variation

In this section, we have analyzed the impact of reference current source variation on the center frequency. The supply voltage is set at 1.2 V while the reference current is swept from 150 $\mu$ A to 210 $\mu$ A.

As observed from Fig. 6.2, there is a small deviation from the center frequency when the reference current is swept from 150 $\mu$ A to 210 $\mu$ A.

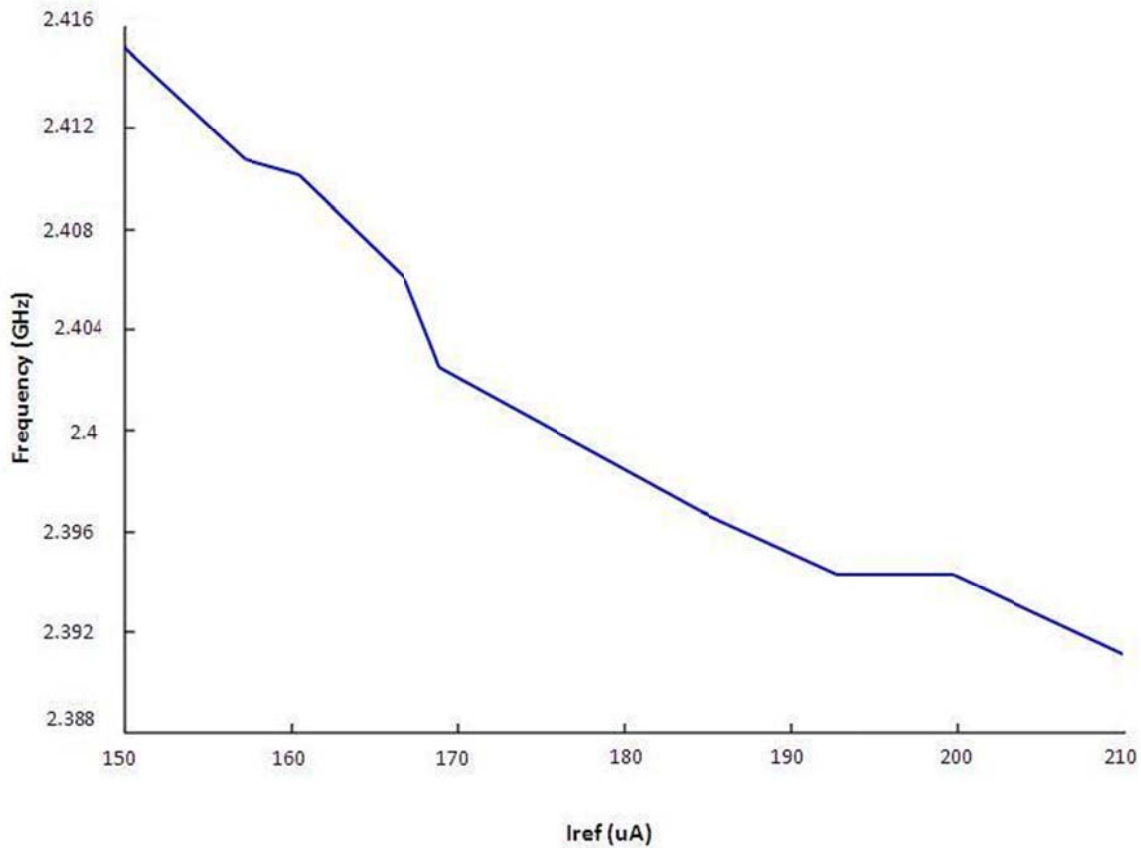


Figure 6.2: Impact of reference current source variation on QVCO center frequency

## 6.4 Phase Noise and Frequency vs. Temperature

In this section, we have analyzed our proposed QVCO performance versus temperature variation. The tail current is set at 3 mA while the supply voltage is 1.2 V. Applying a tuning voltage of 0.6 V, the temperature is swept from -50°C to 175°C.

The Fig. 6.3 demonstrates the phase noise dependency on temperature. As we know, the thermal noise is directly proportional to temperature and this leads to poor phase noise performance as the temperature increases.

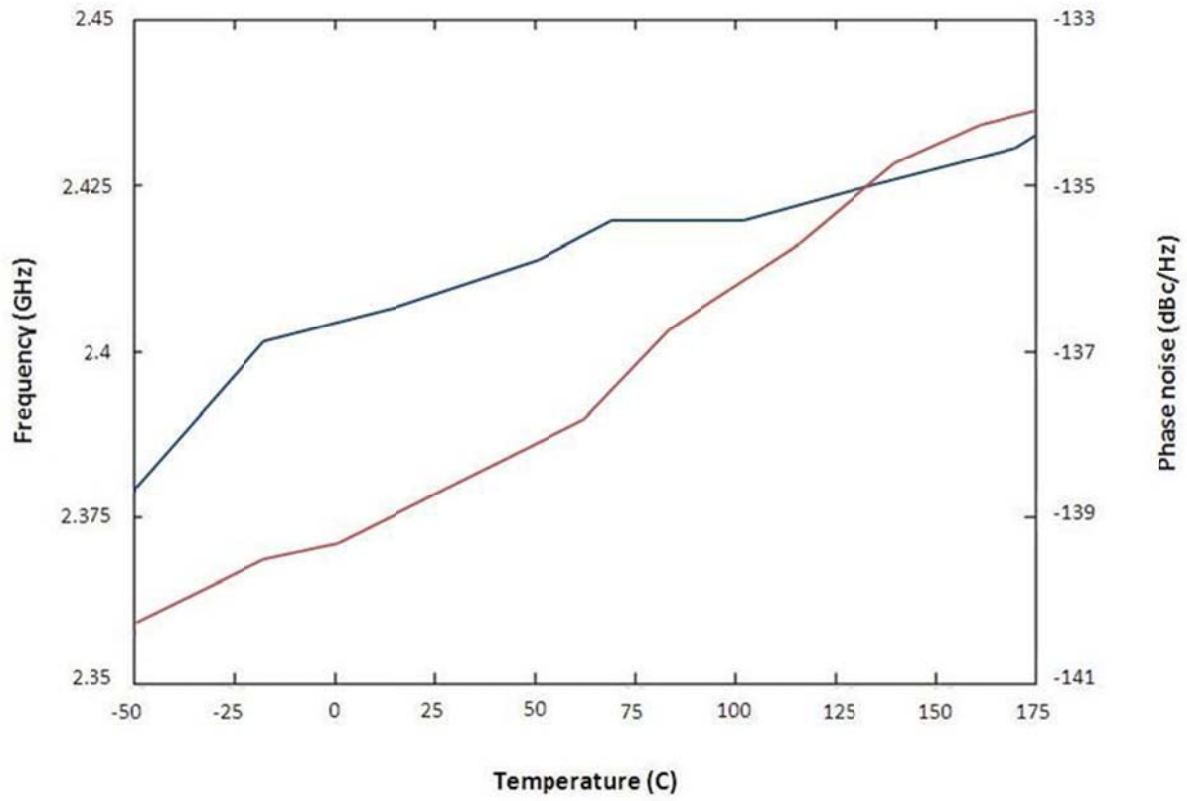


Figure 6.3: Impact of temperature variation on QVCO phase noise (red) and frequency (blue)

## 7. CONCLUSION

### 7.1 Summary

At the beginning of the project work, we studied the basic theory of an oscillator. In the following sections, the noise contributors affecting the VCO performance are identified. Furthermore, different models interpreting the noise impact on a voltage-controlled oscillator are presented. The main purpose of this project is to implement a state-of-the-art design considering optimal phase noise and power consumption. Initially, to achieve a high performance VCO, we have designed different high performance LC VCO architectures. Moreover, a wide comparison is carried out regarding the VCO specifications such as phase noise at different offset frequencies, power consumption, FOM and so forth. As a result, a suitable LC VCO topology is chosen for further analysis. Afterwards, we have improved our design to a Quadrature VCO with back-gate coupling and source resistive degeneration.

The designed QVCO oscillates at the center frequency of 2.4 GHz. The phase noise estimated by simulation at 1MHz offset frequency is -140dBc/Hz. The circuit consumes a power of 3.6mW which is less than conventional QVCO architectures.

Finally, to verify our design, process, temperature, and reference current variations were tested. As a result, the specification requirements have been met in our design.

## 7.2 State-of-the-Art Comparison

Here, the performance of the designed LC QVCO circuit is compared with other reported LC VCOs. As we see, the implemented QVCO performance is in line with the state-of-the-art designs in terms of power consumption and phase noise.

Topology	Technology	Center frequency (GHz)	Phase Noise at 1MHz (dBc/Hz)	Power consumption (mW)	Supply Voltage (V)	FOM (dBc/Hz)
[1]	90 nm	2.42	-119.7	0.515	1.8	-190.26
[2]	0.25 $\mu\text{m}$	2.45	-113.3	3.1	1.8	---
[3]	0.18 $\mu\text{m}$	5.47	-122.4	5	1.2	-190.2
[4]	0.25 $\mu\text{m}$	2.07	-124.4	3	1.5	-186
[5]	0.18 $\mu\text{m}$	1.87	-111	0.5	0.9	-180
[6]	0.18 $\mu\text{m}$	3.5	-116.5	4.7	1.8	---
[7]	0.18 $\mu\text{m}$	5.37	-123	18	1.8	-185
[8]	0.18 $\mu\text{m}$	3.2	-133	4.4	1	-196.6
[9]	0.18 $\mu\text{m}$	2.4	-134	4.6	1	-195
This work	65 nm	2.4	-140	3.6	1.2	-197

Table 7.1: State-of-the-art comparison

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