Characterization of Dielectric Layers for Passivation of 4H-SiC Devices

Ph.D. thesis by

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The pictures shown on the cover are a photo of a sample with 30 silicon carbide MESA diodes prepared for passivation experiments (left) and a scanning electron micrograph of a cross-section of one of the diodes but after AlN passivation (right). The thickness of the AlN layer is 200 nm. The detailed description of the diodes structure and of the picture to the right is done in Chapter 5.1 and in Fig. 5.1 on pages 27 and 28 in the thesis, respectively.

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Thesis submitted to Royal Institute of Technology (KTH), Stockholm, Sweden in partial fulfilment of the requirements for the degree of Doctor of Philosophy (Ph.D.).

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Abstract

Silicon carbide rectifiers and MESFET switches are commercially available since 2001 and 2005 respectively. Moreover, three inch SiC wafers can be purchased nowadays without critical defects for the device performance, four inch wafers are available and the next step of technology is set to be the six inch substrate wafers. Despite this tremendous development in SiC technology the reliability issues, like bipolar device degradation, passivation, or low MOSFET channel mobility still remain to be solved.

This thesis focuses on SiC surface passivation and junction termination, a topic which is very important for the utilisation of the full potential of this semiconductor. Five dielectrics with high dielectric constants, $\text{Al}_2\text{O}_3$, $\text{AlN}$, $\text{AlON}$, $\text{HfO}_2$ and $\text{TiO}_2$ have been investigated. The layers were deposited directly on SiC, or on the thermally oxidized SiC surfaces with several different techniques. The structural and electrical properties of the dielectrics were measured and the best insulating layers were then deposited on fully processed and well characterised 1.2 kV 4H-SiC PiN diodes. For the best Al$_2$O$_3$ layers, the leakage current was reduced to half its value and the breakdown voltage was extended by 0.7 kV, reaching 1.6 kV, compared to non-passivated devices. Furthermore, AlON deposited on 4H-SiC at room temperature provided interface quality comparable to that obtained with the thermally grown SiO$_2$/SiC system.

As important as the proper choice of dielectric material is a proper surface preparation prior to deposition of the insulator. In the thesis two surface treatments were tested, a standard HF termination used in silicon technology and an exposure to UV light from a mercury or deuterium lamp. The second technique is highly interesting since a substantial improvement was observed when UV light was used prior to the dielectric deposition. Moreover, UV light stabilized the surface and reduced the leakage current by a factor of 100 for SiC devices after 10 Mrad $\gamma$-ray exposition. The experiments show also that the measured leakage currents of the order of pA are dominated by surface leakage.
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Appended papers

A. Influence of bulk and surface defects on electrical characteristics of SiC diodes with zone termination in the temperature range from 300K to 623 K.
Maciej Wolborski and Mietek Bakowski
Submitted to Journal of Applied Physics

B. Analysis of bulk and surface components of leakage current in 4H-SiC PiN MESA diodes.
Maciej Wolborski, Mietek Bakowski and Adolf Schöner
Microelectronics Engineering 83 (2006) pp. 75-78

C. Reduction of leakage current of 4H-SiC PiN diodes after UV light exposition.
M. Wolborski, M. Bakowski and A. Schöner
Submitted to Electronics Letters (Nov. 2006)

D. Electrical characterisation of gamma and UV irradiated epitaxial 1.2 kV 4H-SiC PiN diodes
M. Wolborski, M. Bakowski and W. Klamra
Summary of the appended papers

Paper A focuses on electrical characterisation of the 1.2 kV 4H-SiC PiN diodes in a temperature range from room temperature up to 350° C. It concerns mostly the investigation of the extracted activation energies from the current-voltage characteristics both for forward and reverse bias, and statistical comparison of the diodes with the same design, but with epitaxial or implanted p-type emitter. The contribution to the work is performing the measurements of the diodes and partial manuscript writing and interpretation of results.

Papers B and C present electrical characterisation of SiC diodes after different surface treatments including dry etching, exposure to UV light with different photon energies and variation of leakage current with time. The main conclusion is that the total leakage current measured on the devices is surface dominated. The author’s contribution to the articles is data analysis, manuscript writing and partial interpretation of the results.

Paper D shows experiments proving impressive resistance of SiC to gamma irradiation. More interesting result from the point of SiC surface passivation is our first indication on the leakage current reduction after exposure to UV light. The author’s contribution to the paper is performing most of the measurements (except statistical IV), data analysis, to some extent interpretation of the results and manuscript writing.
| --- | --- |

**Not appended in the thesis:**

Paper E concerns Al₂O₃ and TiO₂ deposited by atomic layer deposition technique. For the Al₂O₃ layer the leakage current of a PiN diode at 500 V was reduced by half compared to a non-passivated device. The TiO₂ material showed very high leakage currents most probably caused by a low energy offset to SiC bands.

Paper F is a full characterisation of Al₂O₃, the most promising alternative to SiO₂ insulator for SiC. In the paper, materials deposited by atomic layer deposition and ultrasonic spray pyrolysis techniques are compared and the influence of the two different surface preparations prior to the deposition process is indicated. The paper also proposes surface coating for SiC using a stack of two insulators; the first one with a large energy offset to SiC bands and then a thicker top layer with a high dielectric constant.

Paper G is a brief and introductory experiment which employs polycrystalline AlN layers as the passivation material. UV surface pre-treatment reduced the leakage as compared to HF terminated samples. The leakage current of PiN diodes increased after deposition, but AlN coating stabilises the devices and prevents premature breakdown in air.

Papers H and I present superior performance of stacked passivation layers that consist of a dielectric with high dielectric constant and a thin SiO₂ interface layer that provides good interface properties to SiC. AlON/SiC interface quality strongly depends on oxygen content in AlON material and at best was comparable to SiO₂/SiC interface. Significant contribution to the interface charge is identified to come from polarization phenomenon in AlON. HfO₂ material was unstable at 400 °C degrees, however, it extended diodes breakdown at least by 20%.

Papers from E to I are investigations of SiC passivation by insulators with high dielectric constants. The author’s contribution to these papers is similar to papers A-D and covers experiment planning, most of the measurements (CV, AFM, XRD, 50% of IV), the data analysis including simulations, and manuscript writing.
Acknowledgements

Most people while reading this thesis would see dry results and (useful or not) descriptions of scientific issues. However, only I am the lucky one who knows what was behind every experiment or idea. That is amazing but while writing or updating those chapters I do not see the graphs or tables but passing by faces or situations that happened within the last 4 years… This is it, the road is finished, but the journey still continues as I (luckily) see in front of me many paths I can choose from …

I would like to start my acknowledgements with Prof. Mietek Bakowski, whom I had a chance to meet on a very special conference in the Polish mountains in 2000. He showed me “the road” by giving me the opportunity to visit Sweden as an exchange student and, after a year, as a PhD student. I still remember long evenings on empty corridors in Acreo, when he was answering all my questions regarding SiC and microelectronics. Despite a constant overload at work, he has always time and a new idea for experiment. Mietek also planned, designed and controlled all the device processing.

The second person I owe my gratitude is Doc. Anders Hallén, my second supervisor who with impressive patience is directing me towards the precise goals, as for example (for the second time!) this thesis. Besides having always a good advice he also did RBS measurements of every sample I asked for. Thank you.

“The road” was sometimes bumpy or uphill, but I was well prepared for that thanks to my Parents, Wojciech and Anna, who always believed in me and supported me during all my life. The best companion I could ever dream about for “the journey” is my wonderful wife Dorotka, thanks to whom every bad news was always halved and the good one multiplied by two. For us it is still the beginning.

Another person I am grateful to is our secretary Marianne Widing. Her warm personality and readiness to help is always impressive. Thank you for the friendly atmosphere you create for the FTE, MSP, again FTE, MAP, ICT or whatever we are called right now or at the time the dissertation takes place.

I would also like to thank all the persons who cooperated in our project or helped me with many scientific issues that came up during this study. Out of the many I thank Dr Adolf Schöner from Acreo for doing endless measurements on diodes, Dr Torbjörn Åkemark for XPS measurements and PLD depositions, Viljami Pore, Prof. Mikko Ritala and Prof. Markku Leskelä from Helsinki University for ALD depositions, Jon Andersson and Prof. Ulf Helmersson from Linköping University for MSE depositions, Dr Armando Ortiz from Autonomous National University of México for USP
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Last but not least thanks to Prof. Ulf Karlsson for securing the financial support for my work from the Swedish Foundation for Strategic Research and Prof. Jan Linnros for valuable assistance.
**Abbreviations and Symbols**

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
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<tbody>
<tr>
<td>AFM</td>
<td>Atomic force microscope</td>
</tr>
<tr>
<td>ALCVD</td>
<td>Atomic layer chemical vapour deposition, also called atomic layer deposition (ALD)</td>
</tr>
<tr>
<td>ALD</td>
<td>Atomic layer deposition, also called atomic layer chemical vapour deposition (ALCVD)</td>
</tr>
<tr>
<td>AlN</td>
<td>Aluminium nitride</td>
</tr>
<tr>
<td>AS</td>
<td>Admittance spectroscopy</td>
</tr>
<tr>
<td>BJT</td>
<td>Bipolar Junction Transistor</td>
</tr>
<tr>
<td>BRT</td>
<td>Base Resistance MOS-Controlled Thyristor</td>
</tr>
<tr>
<td>C</td>
<td>Carbon</td>
</tr>
<tr>
<td>CC-DLTS</td>
<td>Constant capacitance deep level transient spectroscopy</td>
</tr>
<tr>
<td>CVD</td>
<td>Chemical vapour deposition</td>
</tr>
<tr>
<td>CV</td>
<td>Capacitance voltage measurement</td>
</tr>
<tr>
<td>DLTS</td>
<td>Deep level transient spectroscopy</td>
</tr>
<tr>
<td>E</td>
<td>Electric field (V/cm)</td>
</tr>
<tr>
<td>ESAVD</td>
<td>Electrostatic spray assisted vapour deposition</td>
</tr>
<tr>
<td>EBIC</td>
<td>Electron beam induced current</td>
</tr>
<tr>
<td>EC</td>
<td>Relative energy of the conduction band edge [eV]</td>
</tr>
<tr>
<td>ECR</td>
<td>Critical field (MV/cm)</td>
</tr>
<tr>
<td>El</td>
<td>Semiconductor bandgap (eV)</td>
</tr>
<tr>
<td>EST</td>
<td>Emitter switched thyristor</td>
</tr>
<tr>
<td>ε0</td>
<td>Vacuum permittivity (8.85·10(^{-14}) F/cm)</td>
</tr>
<tr>
<td>εr</td>
<td>Relative dielectric constant</td>
</tr>
<tr>
<td>εi</td>
<td>Dynamic dielectric constant</td>
</tr>
<tr>
<td>FIB</td>
<td>Focused ion beam</td>
</tr>
<tr>
<td>φb</td>
<td>Potential barrier (eV)</td>
</tr>
<tr>
<td>φmi</td>
<td>Potential barrier between metal Fermi level and conduction band of insulator(eV)</td>
</tr>
<tr>
<td>GaAs</td>
<td>Gallium arsenide</td>
</tr>
<tr>
<td>GaN</td>
<td>Gallium nitride</td>
</tr>
<tr>
<td>Ge</td>
<td>Germanium</td>
</tr>
<tr>
<td>h</td>
<td>Planck's constant (6.63·10(^{-34}) Js)</td>
</tr>
<tr>
<td>H</td>
<td>Hydrogen</td>
</tr>
<tr>
<td>HF</td>
<td>Hydrofluoric acid</td>
</tr>
<tr>
<td>IGBT</td>
<td>Insulated gate bipolar transistor</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
</tr>
<tr>
<td>--------</td>
<td>-------------</td>
</tr>
<tr>
<td>IV</td>
<td>Current voltage measurement</td>
</tr>
<tr>
<td>J</td>
<td>Current density (A/cm²)</td>
</tr>
<tr>
<td>JFET</td>
<td>Junction field effect transistor</td>
</tr>
<tr>
<td>JTE</td>
<td>Junction termination extension</td>
</tr>
<tr>
<td>k</td>
<td>Boltzmann's constant (1.38·10⁻²³ J/K)</td>
</tr>
<tr>
<td>κ</td>
<td>Thermal conductivity (W/cmK)</td>
</tr>
<tr>
<td>LED</td>
<td>Light emitting diode</td>
</tr>
<tr>
<td>LPCVD</td>
<td>Low pressure chemical vapour deposition</td>
</tr>
<tr>
<td>MESFET</td>
<td>Metal semiconductor field effect transistor</td>
</tr>
<tr>
<td>MIS</td>
<td>Metal insulator semiconductor</td>
</tr>
<tr>
<td>MISFET</td>
<td>Metal insulator semiconductor field effect transistor</td>
</tr>
<tr>
<td>MOCVD</td>
<td>Metal organic chemical vapour deposition</td>
</tr>
<tr>
<td>MOS</td>
<td>Metal oxide semiconductor</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal oxide semiconductor field effect transistor</td>
</tr>
<tr>
<td>MSP</td>
<td>Merged Schottky and PiN rectifier</td>
</tr>
<tr>
<td>MSE</td>
<td>Magnetron sputtering epitaxy</td>
</tr>
<tr>
<td>µn</td>
<td>Electrons mobility (cm²/Vs)</td>
</tr>
<tr>
<td>µp</td>
<td>Holes mobility (cm²/Vs)</td>
</tr>
<tr>
<td>OBIC</td>
<td>Optical beam induced current</td>
</tr>
<tr>
<td>PD</td>
<td>Plasma deposition</td>
</tr>
<tr>
<td>PECVD</td>
<td>Plasma enhanced chemical vapour deposition</td>
</tr>
<tr>
<td>PFC</td>
<td>Power factor control</td>
</tr>
<tr>
<td>PVD</td>
<td>Physical vapour deposition</td>
</tr>
<tr>
<td>PWM</td>
<td>Pulse width modulation</td>
</tr>
<tr>
<td>q</td>
<td>Electronic charge (1.6·10⁻¹⁹ C)</td>
</tr>
<tr>
<td>RBS</td>
<td>Rutherford backscattering spectrometry</td>
</tr>
<tr>
<td>RIE</td>
<td>Reactive ion etching</td>
</tr>
<tr>
<td>ρ</td>
<td>Density (g/cm³)</td>
</tr>
<tr>
<td>ρs</td>
<td>Surface charge density (cm⁻²)</td>
</tr>
<tr>
<td>SEM</td>
<td>Secondary electron microscopy</td>
</tr>
<tr>
<td>Si₃N₄</td>
<td>Silicon nitride</td>
</tr>
<tr>
<td>SBD</td>
<td>Schottky barrier diode</td>
</tr>
<tr>
<td>SiC</td>
<td>Silicon carbide</td>
</tr>
<tr>
<td>SiO₂</td>
<td>Silicon dioxide</td>
</tr>
<tr>
<td>T</td>
<td>Absolute temperature (K)</td>
</tr>
<tr>
<td>TiO₂</td>
<td>Titanium dioxide</td>
</tr>
<tr>
<td>XPS</td>
<td>X-ray photoelectron spectroscopy</td>
</tr>
<tr>
<td>XRD</td>
<td>X-ray diffraction</td>
</tr>
</tbody>
</table>
1. Introduction

The usage of semiconductors in high power electronics is nowadays mostly limited to silicon devices. Gallium arsenide (GaAs), introduced to power components almost two decades ago, does not exceed dramatically theoretical silicon limitations. As the number of power electronics applications is still expanding, new semiconductors are considered as a replacement of the fully developed silicon. The main competitors today to silicon are silicon carbide (SiC) and gallium nitride (GaN), where SiC material quality is in a much more mature state. The new materials should also allow for an introduction of unipolar devices (MESFETs and Schottky diodes) instead of silicon bipolar components (IGBT and PiN Si diodes) in medium and high voltage applications.

The work presented in this thesis is devoted to surface passivation and electric field termination of SiC devices. Three issues that are of particular interest are the design of the device, SiC surface preparation before the dielectric deposition and the choice of dielectric material together with the deposition technique applied, all of which are vital for commercial applications.

To motivate this choice of the topic one should realise, that nowadays SiC passivation, termination and design are based on solutions and dielectric materials developed for silicon components [1]. This situation creates difficulties as the physical properties of SiC outperform those of Si. As an example one can take the critical breakdown field which is about 2.2 MV/cm for SiC while for Si it is only 0.3 MV/cm, almost an order of magnitude lower. Another very pronounced difference is the maximum operating temperature of the device. While Si can operate up to about 150 °C, SiC gas sensor was reported to operate at 600 °C [2]. Those two examples show that to gain the benefit of advantageous SiC features regarding higher critical field strength and higher operating temperature it is necessary to introduce new dielectric materials with sufficiently good properties not to limit the maximal utilization of the semiconductor itself. The review of SiC properties and the development stage of passivation and termination technology is done in Chapter 2 of the thesis.

The most popular dielectric in microelectronics is silicon dioxide (SiO2), the natural oxide of both silicon and SiC. Beside many advantages its usage is expected to be limited due to degradation at high temperatures and under high voltage stress. A large drawback of SiO2 is its low dielectric constant, which is about 2.5 times lower than that of SiC. This causes a proportionally large electric field enhancement in the insulator compared to that in the semiconductor, which is a reason why new insulators with dielectric constant at least similar to that of SiC are desired [1]. Only recently, alternative dielectrics like aluminium nitride (AlN) [3], [4], hafnium dioxide (HfO2) [5], [6], aluminium oxide (Al2O3) [7], [8], [9],
lanthanum oxide (La$_2$O$_3$) [11] and gadolinium oxide [12] have been attempted in SiC technology. Many of these novel alternative dielectrics are presented in this thesis. The materials tested and described here as potential new dielectrics for SiC are Al$_2$O$_3$, AlN, aluminium oxynitride (AlON), titanium dioxide (TiO$_2$) and HfO$_2$. Some tests were also performed with the exotic lithium fluoride (LiF) and calcium fluoride (CaF$_2$). The review of the published experiments and results for each of the investigated dielectrics is done in detail in Chapter 3.

In our studies the best results were obtained for Al$_2$O$_3$ passivation, which reduced the leakage current by a factor of two and extended breakdown voltage from 0.9 kV up to 1.6 kV compared to the non-passivated diodes. On the other hand AlON deposition yielded comparable interface state density to that of thermal SiO$_2$ and reduced leakage current of the rectifiers by a factor of two.

A novel approach tried in our studies was to introduce a thin SiO$_2$ interface layer on SiC samples prior to the deposition of high dielectric constant dielectrics HfO$_2$ or AlON. The stacked structures extended breakdown fields and provided very good SiC interface properties as compared to the samples without SiO$_2$ buffer. The influence of the interface between the alternative dielectric and SiO$_2$ is analysed in both cases.

Another issue of interest is surface preparation techniques prior to dielectric deposition. The standard process in Si technology is wet etch in hydrofluoric acid (HF). Unfortunately, this procedure does not provide satisfactory results in the case of SiC [13]. An alternative method tested here is “cleaning” of the SiC surface with UV light, which has a sufficient energy to break carbon clusters that are present on the SiC surface after device processing. The procedure tried in our experiments decreased the surface charge in the AlN/SiC system and also substantially decreased the leakage current of the non-coated diodes. Both HF etch and RCA1 clean gave poorer results.

All the results regarding alternative dielectrics and surface preparations are described in detail in Chapter 6 and further referred to publications attached at the end of the thesis.

The suppression of the surface generated leakage current is a crucial issue in SiC devices as illustrated by many results obtained in this thesis. The leakage current level is used in the studies as a measure of the passivation quality. To better understand the origin of the leakage current, PiN diodes with different shapes and designs were manufactured and revealed that most of the leakage is driven through the edges of MESA structures, the regions where electric field in the devices has the highest value. The devices and structures used in this study are described in Chapter 5.
2. Silicon carbide properties and devices

Silicon carbide is today the most advanced wide bandgap semiconductor with a potential usage for high power and high frequency applications. Outstanding mechanical features like 9.5 hardness in Mohs scale, corrosion resistance and good thermal conductivity, made a polycrystalline SiC a perfect material for tool coating, an abrasive, for production of wear resistive components (e.g. automotive industry) and even for armour fabrication [14].

2.1 SiC material properties and electronic applications

SiC crystals exist in many crystalline forms (polytypes), with differences occurring only along one axis (polymorphism). The variation is obtained by a periodicity of diatomic (C and Si) layers with only 3 possible C-Si atoms positions named for simplicity A, B and C [15], as shown in Fig. 2.1 and Fig. 2.2.

The only existing cubic (zinc-blende) SiC crystalline structure with the bilayer sequence of ABCABC… is also named as 3C-SiC or α-SiC. The other two polytypes of technological interest as semiconductors are hexagonal (wurtzite) or β-SiC crystals with the stacking sequence of ABACAB… and ABCACBABC… for 4H-SiC and 6H-SiC, respectively. In this thesis all experiments were carried out on 4H-SiC polytype using the Si face.

![Fig. 2.1: Positioning of Si-C atoms in 3 possible SiC diatomic layers, A, B and C. On the right side of the picture, schematic 3D view on Si-C atom positions in the 3C-SiC crystal.](image-url)
Fig 2.2: 3C-SiC, 4H-SiC and 6H-SiC crystal structures after [13]. The grey rectangles are crystal lattice cells. The 3C-SiC structure is made only of cubic bonds, while 6H-SiC and 4H-SiC have 2:1 or 1:1 of hexagonal to cubic bonds ratio, respectively. The [0001] surface is corresponding [111] Si surface and the bottom [000-1] surface is similar to the diamond [111] surface for both hexagonal orientations.

The main electrical properties of SiC crystals and other common semiconductor materials are grouped in Table 2.1. Many of the parameters grouped in this table must be taken as an approximation due to the anisotropy of hexagonal polytypes of the SiC crystals (3C-SiC is isotropic). Variation of some other parameters like mobility depends for instance on dopants and their concentrations.

Clean-room processing of SiC and silicon is to some extent similar, which is sometimes stated as one of the reasons for SiC success. Thanks to the similarities, costs reduction is obtained by sharing much of the Si process equipment like lithography, dry etching or ion implantation. The lack of good quality large wafer size of SiC was for many years one of the main problems for SiC development. The situation is changing nowadays as CREE Research Inc. provides on-axis 4 inch wafers and further development is pushed towards 6 inch wafer standard [16]. Another large obstacle is the high stability and inertness of SiC which prevents for example an implementation of most wet etching techniques, or the usage of diffusion for semiconductor doping. The techniques used for a p-n junction formation are epitaxy or implantation. These technologies require temperatures in the range from 1500 °C to 1700 °C.

Silicon and SiC have the common native oxide, SiO₂, which is one of the best developed dielectrics in microelectronics. Unfortunately, the low dielectric constant of SiO₂ may cause difficulties in its applicability in the presence of the high fields that are possible in SiC. One of the reasons why SiO₂ is still used in SiC processing is that this insulator provides a SiC interface with the best known quality needed for MOS transistors and additionally, the SiO₂ layer can be used as a mask during device fabrication.
Table 2.1 Comparison of electrical and mechanical properties of common semiconductors

<table>
<thead>
<tr>
<th></th>
<th>Ge</th>
<th>Si</th>
<th>GaAs</th>
<th>3C-SiC</th>
<th>6H-SiC</th>
<th>4H-SiC</th>
<th>GaN</th>
<th>AlN</th>
<th>C Diamond</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap $E_g$ [eV]</td>
<td>@0.66</td>
<td>@1.12</td>
<td>@0.142</td>
<td>@0.240</td>
<td>@3.02</td>
<td>@3.26</td>
<td>@3.39</td>
<td>@6.1</td>
<td>@5.45</td>
</tr>
<tr>
<td>Critical field $E_{cr}$ [MV/cm]</td>
<td>0.1</td>
<td>0.3</td>
<td>0.4</td>
<td>2.12</td>
<td>2.5</td>
<td>2.2</td>
<td>3.3</td>
<td>11.7</td>
<td>5.6</td>
</tr>
<tr>
<td>Electron mobility $\mu_e$ [cm$^2$/Vs]</td>
<td>3900</td>
<td>1500</td>
<td>8500</td>
<td>800</td>
<td>400</td>
<td>1000</td>
<td>900</td>
<td>1100</td>
<td>1900</td>
</tr>
<tr>
<td>Hole mobility $\mu_p$ [cm$^2$/Vs]</td>
<td>1900</td>
<td>450</td>
<td>400</td>
<td>40</td>
<td>101</td>
<td>115</td>
<td>1800</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dielectric constant $\varepsilon_r$</td>
<td>16</td>
<td>11.9</td>
<td>13.1</td>
<td>9.72</td>
<td>9.66</td>
<td>The same as 6H-SiC</td>
<td>9.5</td>
<td>8.5</td>
<td>5.5</td>
</tr>
<tr>
<td>Thermal cond. $\kappa$ [W/cmK]</td>
<td>0.6</td>
<td>1.5</td>
<td>0.46</td>
<td>3.2</td>
<td>4.9</td>
<td>3.7</td>
<td>1.3</td>
<td>2</td>
<td>20</td>
</tr>
<tr>
<td>Melting temp $T_m$ [°C]</td>
<td>937</td>
<td>1415</td>
<td>1238</td>
<td>2830</td>
<td>2830</td>
<td>&gt;2500</td>
<td>3000</td>
<td>4440</td>
<td>12.4 GPa</td>
</tr>
<tr>
<td>Density $\rho$ [g/cm$^3$]</td>
<td>5.33</td>
<td>2.33</td>
<td>5.32</td>
<td>3.21</td>
<td>3.21</td>
<td>3.21</td>
<td>6.15</td>
<td>3.26</td>
<td>3.51</td>
</tr>
<tr>
<td>Hardness [Mohs scale]</td>
<td>6</td>
<td>7</td>
<td>4.5</td>
<td>9.2-9.3</td>
<td>Similar to 3C-SiC</td>
<td>Similar to 3C-SiC</td>
<td>10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lattice</td>
<td>diamond</td>
<td>diamond</td>
<td>cubic</td>
<td>cubic</td>
<td>hexag.</td>
<td>hexag.</td>
<td>hexag.</td>
<td>hexag.</td>
<td>diamond</td>
</tr>
<tr>
<td>Lattice const.</td>
<td>a [Å]</td>
<td>5.32</td>
<td>5.43</td>
<td>5.65</td>
<td>4.36</td>
<td>3.08</td>
<td>3.07</td>
<td>3.189</td>
<td>3.112</td>
</tr>
<tr>
<td></td>
<td>b [Å]</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>15.12</td>
<td>10.05</td>
<td>5.185</td>
<td>4.982</td>
</tr>
</tbody>
</table>

a) evaporation, no liquid phase  (i) indirect bandgap  (d) direct bandgap
1) ref. [17], 2) ref. [18], 3) ref. [19], 4) ref. [20], 5) ref. [21], 6) ref. [22], 7) ref. [23]
The largest part of the SiC material that is produced today finds the application as substrates for high brightness GaN blue LEDs. Beside that, electronic devices of SiC were recently introduced to a large scale fabrication. Silicon carbide Schottky diodes are commercially produced by Infineon, Germany (production started in 2000) and CREE Research Inc., USA (production started in 2001). The best diodes produced can block 600 V or 1200 V and can conduct up to 12 A and 20 A for Infineon [24] and CREE Research Inc. [16] devices, respectively. The main areas where these products find applications are power supplies and active power factor control circuits, PFC. A unipolar Schottky diode has a maximum theoretical blocking voltage up to 5000 V for SiC and only 200 V for Si diodes [25]. 5 kV is a comparable value to a bipolar Si PiN device, but the unipolar diode eliminates minority carrier recovery time, which allows improving the efficiency by boosting switching frequency. The problem of high leakage current for Schottky junction is solved by introduction of additional parallel PN junction, the solution applied in technology called thinQ\textsuperscript{TM} 2G (second generation SiC Schottky diode) at Infineon.

The future potential of SiC products is far more promising when high power switches like MOSFETs or BJTs will reach the market. The most important applications are expected to be electric engines in hybrid and plug-in hybrid cars [26], power lines or high power high frequency applications like mobile phones base stations and radars. Moreover SiC can find application as a gas sensor in hazardous environments [2], [27], durable room temperature radiation detector [28], combustion engines cylinder pressure sensor [29], and many others [30]. The example of potential savings that might be achieved in the case of 400 V, 15 A module unit with pulse width modulation (PWM) with different power semiconductor devices (including SiC) and operating at different frequencies are shown in Fig. 2.3.

![Fig. 2.3: Power losses of the 400 V, 15 A PWM unit for different switches (IGBT, BRT, EST) and rectifiers (PiN and MPS) taken from [31]. Unfortunately, there is no data presented for the combination of Si switches with SiC Schottky diodes – the combination that is implemented nowadays.](image-url)
2.2 Device termination

The maximum blocking voltage and the maximum current density are the two key parameters of power electronics components. Termination techniques modify the first one i.e. they prevent premature breakdown at the surface of the device. The proper termination design distributes electric field evenly by enlarging the space charge region at the edge of the p-n junction.

All termination techniques used in SiC devices were developed initially for silicon applications. Junction termination extension (JTE) is the most efficient termination method obtained by implantation or diffusion of the floating p-n junctions in the form of rings or more uniform surface plates around the emitter. Another very popular technique is based on bevelling of the edge of the junction used mainly for the devices of large diameter. Those and many other techniques are described in detail by B.J. Baliga in [32].

Very low diffusion of dopants into SiC or defects induced by ion implantation and high temperature annealing (1500 °C) make it difficult to utilise these mentioned termination techniques in SiC technology. Even though, different variants of implanted JTE are the best developed SiC termination method described for example in [33], [34], [35] and [36]. Implantation gives very good control over the charge distribution in the terminated region. The other approach to form termination (such devices are used in this thesis) are MESA structures where the epitaxially grown stack of SiC with different dopants concentrations is etched in such a way that JTE region surrounds the emitter in the form of one or many rings[37].

Additionally, a very important issue that is not discussed in literature so extensively is the existence and influence of the surface charge on the performance of the devices [38] and the right choice of the dielectric material for passivated SiC components [39]. Those topics will be discussed in the Chapter 3 entitled “Dielectrics”.

2.3 Surface properties

Due to the presence of both hexagonal and cubic bonds in hexagonal SiC polytypes there might be many different surfaces present even for one (silicon or carbon) face of the crystal. As an example one can look at the structure of 6H-SiC shown in Fig. 2.4, where the six possible surfaces named as S1, S2, S3, S1*, S2* and S3* are shown. The existence of all those structures on a single wafer is enhanced by the terrace like surface of the off-axis orientated wafers.

To make things even more complex, due to composition of Si and C atoms the cubic SiC unit cells show spontaneous ionic polarization along [0001] axis [40]. For a hexagonal structure, spontaneous polarization is much stronger and originates from cubic and hexagonal bonds in a single unit cell. Quantitative computations are difficult, nevertheless in [40] the ionic polarization is estimated to 25% of total spontaneous polarization. However, it is also shown that the polarization charge is screened by the electronic charge distribution and is neither affecting polytype stability nor the surface of the crystal.
2.4 Surface processing

SiC [0001] and Si [111] surfaces have many similarities. This is the reason why, from the very beginning of SiC processing, a number of standard surface treatments was tested. Surface cleaning can be divided into two main steps: the first one is the removal of surface contaminations like organics, metals, oxides to basically bring it back to state shown in Fig. 2.4, and the second one is passivation of free dangling bonds of the atoms on the wafer surface. The goal of the passivation is to control the oxidation in air and to eliminate electronic traps on the surface of the wafer. While the first step in the surface treatment seems to be common for Si and SiC wafers [41], surface passivation is much more challenging for SiC and lack of systematic studies of the charge present on the SiC surface after different surface processing is of large concern for devices stability.

The most commonly used method for Si passivation is attaching hydrogen atoms, H, to Si dangling bonds. This standard procedure in Si technology is carried out by dipping in hydrofluoric acid solution, HF, or buffered HF. Unfortunately, a similar procedure performed on SiC surfaces is unsuccessful. X-ray photoelectron spectroscopy, XPS, studies performed on SiC surfaces after HF processing reveal the existence of both oxygen and fluorine [13]. The conclusion is that Si atoms are passivated by the OH groups instead of H. As a result charged surface states at the dielectric-SiC interface can pin the Fermi level. Another attempt for SiC surface termination is applying hydrogen plasma process, but again an oxygen monolayer is detected on the Si surface. Still another attempt to clean the surface from oxygen contamination is annealing in ultra high vacuum, UHV. Unfortunately, detailed studies of SiC wafers after annealing revealed clean but reconstruct surfaces [42].

A promising way of SiC surface termination proposed recently is annealing of SiC samples at 1000 °C in pure hydrogen atmosphere, first proposed by Tsuchida et al. [42]. According to [13] this technique yields a stable silicon face, i.e. does not oxidise in air, for 4 days and carbon face remains unchanged for 2 days. The technique seems to be a promising surface treatment prior to dielectric deposition, but 1000 °C annealing step causes difficulties in case of a limited thermal budget for processing.
3. Dielectrics

Dielectrics or insulators are a group of materials that do not conduct current in the presence of an electric field. Their applications in microelectronics are very broad, from gate oxides, a key element that allows silicon CMOS utilisation, through passivation of the semiconductor surfaces, up to the insulation between metallization layers and packaging.

The electronic parameters of insulators taken under consideration in this work are the relative dielectric constant ($\varepsilon_r$), the critical field that the dielectric can sustain ($E_{cr}$), the dielectric bandgap ($E_g$) and the potential offset between dielectric and semiconductor conduction band edges ($\varphi_b$). Additionally, one always has to check how stable the insulator is in an aggressive chemical environment and at high temperatures, typically larger than 300 °C. Some of the dielectrics considered as a SiC passivation material are grouped in Table 3.1.

The dielectric constant is the main motivation to search for a replacement of SiO$_2$, which has a relative dielectric constant of 3.9. According to Gauss law, this causes the electric field in SiO$_2$ to be about 2.5 times larger than that in SiC, where the dielectric constant is 10. This is schematically shown in Fig. 3.1. It implies that the SiO$_2$ layer is the weakest point of the whole system. All new dielectrics should have a dielectric constant of at least 10.

For passivation applications the critical field of the dielectric is an important parameter. The important reliability issues for insulator are high temperature or radiation induced degradations that might cause lowering of the $E_{cr}$ or increase leakage current. Injection and trapping of hot carriers in the dielectric may also cause instability of the system. For the passivation application one should consider only the fraction of the critical field measured on the bulk material e.g. only 20% of the bulk $E_{cr}$ is often used for SiO$_2$ applications.

The bandgap of a dielectric material and the band offsets in relation to the semiconductor band edges are correlated. Often the measured leakage current at lower fields is dominated by the Fowler-Nordheim (FN) tunnelling current expressed by Formula (3.1) [17]. This is also shown in Paper F. The key factor is the energy difference between the SiC and the insulator conduction bands, the potential barrier, $\varphi_b$. Expression (3.1) shows that the higher $\varphi_b$, the lower is the leakage current caused by FN as shown in the schematic picture, Fig. 3.2. A barrier of 1.7 eV was enough to prevent detectable FN tunnelling up to 3 MV/cm in the Al$_2$O$_3$/SiC system. Since the electric field is similar in both SiC and Al$_2$O$_3$ due to the same value of dielectric constant, the FN current will not
be a major contribution to the leakage current of the passivated devices up to the breakdown field of SiC.

\[ J_{\text{FN}} \sim E^2 \cdot \exp\left(\frac{-b}{E}\right) \]  
\[ b = \frac{8 \cdot \pi \cdot \sqrt{2} \cdot m^* \cdot (q \cdot \phi_b)^{3/2}}{3 \cdot q \cdot h} \]  

where:

- \( J_{\text{FN}} \) is the current density due to Fowler-Nordheim tunnelling
- \( E \) is the electric field
- \( m^* \) is an effective mass of the charge carrier
- \( q \) is the electronic charge \( 1.6 \times 10^{-19} \text{C} \)
- \( h \) is the Planck’s constant \( 6.63 \times 10^{-34} \text{Js} \)

**Fig. 3.1:** Two cases of Gauss law, for the electric field vectors perpendicular (left) or parallel (right) to the interface of the isolator and semiconductor, \( \rho_s \) is the interface charge.
The dielectric bandgap has a correlation to a leakage current through the band edge offset. Wider bandgap means a better chance for a larger conduction or valence band offsets between the semiconductor and the dielectric. In a situation when theoretical calculations of band diagrams are not available, nor there are measured differences between insulator and SiC energy bands, the size of the bandgap allows for a rough estimation of the potential usability of the dielectric. Assuming ideal, symmetrical offsets for electrons and holes of the order of 2 eV, the bandgap of the insulator should be at least 7 eV.

The structure and mechanical properties of an “ideal” insulator are as important as its electronic features. The most stable and defined form of the materials are monocrystalline structures but those are often grown at high temperatures and pressures. In case of passivation, when the dielectric material is considered to be deposited as the last processing step at low temperatures, the material should have an amorphous composition. This would prevent a possible current conduction through the grain boundaries of the polycrystalline material. Moreover, a lot of research is oriented towards nanocrystalline structures and application of those could provide materials with e.g. larger bandgap, modified by small grains dimension.

Other mechanical features like surface roughness, purity, or right stoichiometry of insulators implies that a good control over the deposition process and correct film uniformity is achieved. To eliminate the mechanical stress caused by device operation at high temperature, the thermal expansion coefficient and thermal conductivity of the dielectric and SiC should be similar. The insulator should also be hard, resistant to cracks and should not be influenced by the surrounding atmosphere.
In this thesis we have investigated Al₂O₃, AlN, AlON, HfO₂, TiO₂, LiF and CaF₂. The main parameters of these dielectrics, together with the other insulators are summarised below in Table 3.1.

### Table 3.1 Values of dielectric constant, bandgap, conduction (CB) and valence (VB) band offsets, breakdown voltage and thermal conductivity for various materials.

<table>
<thead>
<tr>
<th>Material</th>
<th>εᵣ/εᵢ</th>
<th>Bandgap [eV]</th>
<th>CB offset from Si/4H-SiC [eV]</th>
<th>Breakdown electric field [MV/cm]</th>
<th>Thermal conductivity [W/cmK]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al₂O₃</td>
<td>8 ¹/3.4 ²</td>
<td>8.8 ²</td>
<td>2.8 ²/1.7 ³</td>
<td>&gt;5 ⁴</td>
<td>0.02 # ⁵</td>
</tr>
<tr>
<td>CaF₂</td>
<td>6.8 ⁵/ -</td>
<td>12.3 ⁷</td>
<td>-/-</td>
<td>14.44 ⁸</td>
<td>0.1 ⁹</td>
</tr>
<tr>
<td>HfO₂</td>
<td>~30 ⁶/4 ²</td>
<td>6 ²</td>
<td>1.5 ²/1.6 ³</td>
<td>8.5 ⁹</td>
<td>0.015 # ⁵</td>
</tr>
<tr>
<td>LiF</td>
<td>9 ⁶/ -</td>
<td>11.6 ¹⁰</td>
<td>-/-</td>
<td>12.24 ⁸</td>
<td>0.15 # ⁶</td>
</tr>
<tr>
<td>Si₃N₄</td>
<td>7.4 ¹¹/3.8 ²</td>
<td>5.3 ²</td>
<td>2.4 ²/-</td>
<td>10 ¹¹</td>
<td>0.3 ¹²</td>
</tr>
<tr>
<td>SiO₂</td>
<td>3.9 ¹³/2.25 ²</td>
<td>9 ²</td>
<td>3.5 ²/2.7 ³</td>
<td>10 ¹¹</td>
<td>0.015 # ⁵</td>
</tr>
<tr>
<td>TiO₂</td>
<td>24-57 ¹⁴/7.8 ²</td>
<td>3.05 ²</td>
<td>0 ²/-</td>
<td>2.7 ¹⁴</td>
<td>0.07 # ⁵</td>
</tr>
<tr>
<td>ZrO₂</td>
<td>15 ¹⁵/4.8 ²</td>
<td>5.8 ²</td>
<td>1.4 ²/1.6 ³</td>
<td>15-20 ¹⁵</td>
<td>0.02 ²</td>
</tr>
<tr>
<td>Si</td>
<td>11.7/ -</td>
<td>1.12</td>
<td>-</td>
<td>0.3</td>
<td>1.5</td>
</tr>
<tr>
<td>AlN</td>
<td>9.14/ -</td>
<td>6.03</td>
<td>2.2*/1.7 ¹⁵</td>
<td>1.2-1.8</td>
<td>11.7</td>
</tr>
<tr>
<td>4H-SiC</td>
<td>9.66/ -</td>
<td>3.23</td>
<td>-</td>
<td>3.5</td>
<td>3.7</td>
</tr>
</tbody>
</table>

1) ref. [43], 2) ref. [44], 3) ref. [45], 4) ref. [46], 5) ref. [47], 6) ref. [23], 7) ref. [48], 8) ref. [49], 9) ref. [50], 10) ref. [51], 11) ref. [17], 12) ref. [52], 13) ref. [53], 14) ref. [54], 15) ref. [55], εᵣ – static dielectric constant, εᵢ – dielectric constant at high frequencies
# - thermal conductivity data for sputtered material, otherwise for bulk
### Silicon dioxide

As previously mentioned, silicon dioxide is the most popular dielectric applied in Si microelectronics technology, being at the same time the native oxide of SiC. This situation produced a lot of effort into the implementation of SiO₂/SiC interface, especially for MOS transistor. Unfortunately, the complexity of this system, in comparison to the SiO₂/Si-system, still causes severe problems and the mobility is only about 5% of the theoretical value. The measured maximum and average effective mobilities are both about 50 cm²/Vs for [0001] n-type 4H-SiC [58] and 229 cm²/Vs for n-type 3C-SiC [59], respectively.

Silicon dioxide can be obtained with many techniques developed during 30 years of silicon supremacy in semiconductor industry. This insulator can be both grown by thermal oxidation of silicon under dry or wet conditions, or it can be deposited by means of different variants of chemical vapour deposition (CVD), such as liquid phase CVD (LPCVD), plasma enhanced CVD (PECVD) or atomic layer deposition (ALD). The best
Characterization of Dielectric Layers for Passivation of 4H-SiC Devices

Oxide quality is obtained by dry oxidation done at temperatures of about 1000 °C in oxygen atmosphere. Oxide growth on silicon is dominated in this case by oxygen diffusion through SiO₂ towards the SiO₂/Si interface. This process faces difficulties in SiC system where, beside Si atoms that form SiO₂, there are also C atoms. How the SiO₂ is influenced by C atoms is not well understood at present. Hypotheses propose migration of free C atoms in almost every direction. The most probable is out-diffusion of CO₂ or CO through the grown silicon oxide but also formation of carbon clusters at the SiO₂/SiC interface and even diffusion of C into bulk SiC are possible. Song et al. [60], presents a model of the thermal oxide growth on hexagonal SiC. The work assumes two competitive processes influencing SiO₂ formation, one is the in-diffusion of oxygen towards the interface and the other one is the out-diffusion of CO. However, by experimental data one cannot prove that some of the carbon atoms do not stay at the interface and form very stable carbon cluster [61]. Further investigation of thermal oxidation and re-oxidation with different oxygen isotopes seem to confirm that unknown carbon structures exist at the interface [62].

An alternative method of SiO₂ formation by growth is deposition on a well prepared, terminated, SiC surface. Comparing various methods for materials deposition, atomic layer deposition has a large potential [63]. With this technique very well controlled growth, almost atomic layer by atomic layer, of the desired species from gaseous precursors is possible. Unfortunately, very few publications report efficient SiO₂ deposition with ALD like in [64], and only one work describes very good properties of the SiO₂ film obtained with ALD on 4H-SiC [65]. Still another technique for SiO₂ formation is deposition of Si on SiC surface and later thermal oxidation of the Si layer. X-ray photoelectron spectroscopy (XPS) study of such an attempt on 6H-SiC is presented in [66] and the material formed by overlayer oxidation shows less Si and C related species in comparison with thermally oxidized samples, suggesting a less complex interface structure for the first case.

An electronic study of SiO₂/SiC interface was presented by V.V. Avanas'ev et al. [67] in 1997 and the proposed origin and interface states distribution presented in Fig. 3.3 is a result of this work. The interface traps may come from three main sources, carbon clusters with wide band gap, graphite-like carbon, and oxide traps. One could have expected that after the disclosure of the problems with the SiO₂/SiC interface, the improvements would be on the way. However, a very similar paper was presented by the same author in 2005 [68]. The point is that during 8 years of intensive studies this complex problem is still unsolved.

Beside all the investigations aimed at the SiO₂ formation one has to also consider applicability of this material during high temperature and high field exposures. Up to date Si and SiO₂ form a very useful system, but electric fields in SiC can reach values 10 times higher than those observed in Si, resulting in degradation of the gate oxide by hot carrier injection, which is well known in Si MOS devices [69]. In SiC the potential barrier height between SiO₂ and semiconductor is even smaller making this degradation process more pronounced. Additionally, SiC can operate at many hundreds of Celsius degrees (Si cannot reach 200 °C without turning intrinsic), but problems with SiO₂ interface on 6H-SiC appear already at 300 °C [70]. Moreover, applications in space or radiation detectors will, most probably, suffer from problems caused by the oxide reliability and not the semiconductor itself [71].
Fig. 3.3: The origin and distribution of interface states density of SiO$_2$ and Si, 3C-SiC, 4H-SiC and 6H-SiC semiconductors taken from [67]: a) the traps from the wide energy gap carbon clusters, b) graphite-like carbon clusters and c) near-interfacial oxide defects. The valence band energy is placed on the same level for all SiC semiconductors. Interesting issue is the fact that oxide traps, part c), should be present only in the 4H-SiC band gap, which might result in better quality of the SiO$_2$/6H-SiC or SiO$_2$/3C-SiC interfaces.

Fig. 3.4: Interface state density distributions in the bandgaps of 3C-SiC, 4H-SiC and 6H-SiC [67]. The measurements were taken for both n- and p-type semiconductors by admittance spectroscopy (AS) and constant capacitance deep level transient spectroscopy (CC-DLTS). The scattered results might suggest different origin of the defects.
3.2 Aluminium oxide

Aluminium oxide ($\text{Al}_2\text{O}_3$) is intensively investigated in recent years as a potential gate oxide in Si MOS technology. Its main advantages are a wide bandgap of 8.8 eV and a high potential barrier to Si conduction band, 2.8 eV, which is only 0.7 eV smaller than that for $\text{SiO}_2$/Si system, according to Table 3.1. The calculated $\text{Al}_2\text{O}_3$ conduction band offset to 4H-$\text{SiC}$ is 1 eV smaller than the one measured on Si but still the value of 1.7 eV is high enough to effectively prevent carrier injection.

$\text{Al}_2\text{O}_3$ can take a crystalline form called sapphire, or $\alpha$-$\text{Al}_2\text{O}_3$ with the rhombohedral symmetry. This material has a wide usage in microelectronics industry and it is commercially available in single crystal wafers. The use of sapphire for passivation of $\text{SiC}$ is difficult due to crystalline mismatch and deposition of polycrystalline material may cause leakage through grain boundaries. Nevertheless, amorphous aluminium oxide seems to be an interesting candidate as a dielectric for $\text{SiC}$ devices.

$\text{Al}_2\text{O}_3$ may be deposited with many different techniques such as sputtering [72], plasma deposition [73], thermal oxidation of AlN films [74], ultrasonic spray pyrolysis, where ultrasonic waves are used to decompose the precursor [75] and atomic layer deposition, ALD, with the sequential gaseous inlet of the precursors [76], [77], [78], where the last one seems to have the largest interest. Very good results are presented by K.Y. Gao et al. [76] where post deposition annealing of $\text{Al}_2\text{O}_3$ in $H_2$ at 500 °C reduced interface states density to the level of $10^{11}$ cm$^{-2}$eV$^{-1}$ in the mid gap of the 6H-$\text{SiC}$ band gap, but formation of a $\text{SiO}_2$ buffer layer after annealing was also indicated. Only recently the $\text{Al}_2\text{O}_3$/SiC interface properties gain interest [7], [8], [9] and the first 4H-$\text{SiC}$ MESFET with $\text{Al}_2\text{O}_3$ as a gate dielectric was demonstrated [10].

Previous investigations of the defects and reliability of crystalline $\text{Al}_2\text{O}_3$ are summarised in [79], but a large spread of the conductivity data as a function of temperature can be observed. Additionally, it was reported that radiation enhances the leakage current in aluminium oxide [79] and Si diffusion is possible in aluminium oxide for temperatures over 1000 °C [78]. Nevertheless, up to date, the potential of the $\text{Al}_2\text{O}_3$/SiC system was only tried and further investigations are needed to confirm its usability in high power, high temperature electronics.

3.3 Aluminium nitride

The other proposed dielectric material for $\text{SiC}$ is aluminium nitride ($\text{AlN}$). Its lower bandgap of 6 eV in comparison with $\text{Al}_2\text{O}_3$ or $\text{SiO}_2$ might be disappointing, but a lattice mismatch to $\text{SiC}$ of only 1%, almost the same thermal expansion up to 1000 °C [80] and a high dielectric constant are more encouraging.

Aluminium nitride is often used as a buffer layer for GaN structures grown on SiC substrates and for that reason the largest number of studies concern epitaxial growth at high temperatures, e.g. [81]. Other techniques that are of interest for low temperature deposition of passivation layers like sputtering [82], atomic layer deposition [83], physical vapour deposition [84] and pulsed laser deposition [85] were also applied.
There are not many studies concerning electrical characterisation of AlN layers on SiC [3], [81], [86], [87], [88], [89]. The results, however, show good insulating properties with leakage currents of the order of $10^{-9}$ A/cm$^2$ and a breakdown field of around 4 MV/cm for monocrystalline material [81]. R.D. Vispute et al. [86] describe thermal stability of AlN/SiC system. The leakage current of MIS structures at a field of 2 MV/cm shows 5 orders of magnitude increase, from $10^{-8}$ A/cm$^2$ to $10^{-3}$ A/cm$^2$, for measurements done from room temperature to 450 °C. Charge trapping in AlN/SiC interface is an important issue as presented in [88], [89], however HCl pre-treatment of SiC results in a tremendous improvement of the insulating properties of AlN grown afterwards [81], and provides interface quality sufficient for MISFET fabrication [3].

The results of nanocrystalline and amorphous AlN material deposited on Si at low temperatures by means of physical vapour deposition are presented in ref. [84] by F. Engelmark et al. The data shown in the report confirm a high dielectric constant of 10 for both materials and their stability up to frequencies of 5 GHz. On the other hand the work presented by T. Adam et al. in [82] shows unsatisfactory quality of magnetron sputtered AlN films on Si.

The conclusions regarding AlN for passivation are that the material is sensitive to the deposition technique and the surface preparation procedure. Very promising are measured results of amorphous and nanocrystalline AlN, as the material was deposited at room temperature. Introduction of SiO$_2$ buffer layer between SiC and AlN as an additional barrier to prevent electron injection from semiconductor to dielectric should further decrease leakage current. Such an attempt of the stack of AlN/SiO$_2$/6H-SiC was presented in [4] and reveals a low charging effect when 100 Å SiO$_2$ layer was used.

3.4 Titanium dioxide

Another dielectric that was tested as a passivation layer for SiC material in this thesis is titanium dioxide (TiO$_2$). The motivation of the experiment was to try an insulator characterised by a high dielectric constant, which is given in the literature to be between 24 for amorphous composition [90] up to 170 for the parallel direction to the optical axis of the rutile crystal [91]. Such a high value of dielectric constant would allow a relatively low reported TiO$_2$ breakdown field of about 2.7 MV/cm, as indicated in Table 3.1.

TiO$_2$ film can be deposited with many techniques, some of which can be classified as electrostatic spray assisted vapour deposition (ESAVD) [92], photo-induced chemical vapour deposition [93], metal-organic chemical vapour deposition (MOCVD) [94], chemical vapour deposition (CVD) [95], RF sputtering [96], or plasma spraying [97].

Dielectrical characterisation of RF sputtered TiO$_2$ reported by M.D. Stamate in [96] shows large variations in the relative dielectric constant depending on temperature ($\varepsilon_r=20$ and $\varepsilon_r=70$ at 250 K and room temperature, respectively), film thickness ($\varepsilon_r=70$ and $\varepsilon_r=50$ for the thicknesses 0.3 µm and 0.6 µm, respectively) and measurement frequencies ($\varepsilon_r=70$ and $\varepsilon_r=10$ for the frequencies 100 Hz and 100 kHz, respectively). On the other hand working Si MOSFET transistors with TiO$_2$ gate insulator were presented by S.A. Campbell et al. [98], where the dielectric was obtained by decomposition of titanium tetrakis-isopropoxide annealed at 750 °C. The TiO$_2$ dielectric constant reported was 31,
stable in the range from 100 Hz to 1 MHz, the critical breakdown field was 3 MV/cm, and the potential offset to silicon conduction band equal to 1 eV. Those examples show how crucial for the film quality is the right choice of deposition technique. In the present studies we characterised films prepared by atomic layer deposition. The technique offers good control of stoichiometry and a low growth rate, the two important deposition parameters needed to obtain a material of good quality.

### 3.5 Hafnium dioxide

Hafnium dioxide, HfO$_2$, and its silicate, HfSi$_x$O$_y$, are candidate dielectrics to replace SiO$_2$ as a gate material in a scaled down MOS technology. Backed by the industry, the research of this material is substantially advanced compared to other high-k dielectrics [99], [100]. HfO$_2$ is also very promising insulator in SiC passivation due to its high dielectric constant (the highest tried in this thesis) and very large breakdown voltage of about 8 MV/cm, which provides a lot of reliability margin for device operation.

The control of HfO$_2$ film thickness and its good and uniform quality are key technological issues, due to the future HfO$_2$ application in MOS transistors. The deposition technique of choice that satisfies those requirements is ALD. However, the task is not trivial and to exemplify commitment and problems that emerge during the HfO$_2$ deposition process optimisation in ALD, one can reference to [101] where 18 different precursors combinations are described or further referenced. In another work published by the same authors [102], large variations in dielectric constant, crystalline phase, growth rate and fixed charge are presented for HfO$_2$ deposited on silicon with different surface pretreatments.

The issues of vital importance in the reliability of HfO$_2$ deposition is its interface stability. Here one can find confusing and contradictory reports of stable HfO$_2$/Si interface [103] or SiO$_2$ formation at the interface during deposition process on silicon [104]. Further input to this discussion might be found in Paper I, where degradation of SiO$_2$ buffer layer on SiC substrate after HfO$_2$ annealing was observed.

As HfO$_2$ is considered to be applied in SiC technology, its thermal stability at elevated temperatures is a must. This condition seems to be satisfied when the precursor is chlorine component and the deposition is done at 370 °C on Si substrate [105], where both crystalline monoclinic phase and electrical properties are stable up to 900 °C, for the films deposited at lower temperatures the performance was reported to improve already after 500 °C annealing. However, films deposited with iodine precursor (applied also in this thesis) at 225 °C [106], had their breakdown field reduced from 7 MV/cm to less than 2 MV/cm during 500 °C annealing process. In the same process the relative dielectric constant of the films increased from 10 to 18.

Unfortunately, there was only one publication found where HfO$_2$ was deposited by means of ALD on SiO$_2$/4H-SiC stack [5]. The process was based on Hf(NO$_3$)$_3$ precursors and the deposition was done at 300 °C. The films had good dielectric properties and were stable after annealing at 800 °C.

Lack of further investigations of HfO$_2$ compatibility with SiC encouraged us to further investigate this insulator.
3.5 Lithium fluoride and calcium fluoride

Lithium fluoride and calcium fluoride are used in optics as materials for high transparency windows. One can purchase those dielectrics in a form of wafers, which can transmit light down to the wavelength of 120 nm.

The main reason why those two exotic materials drew our attention was their large bandgaps (>10 eV) and good bulk electrical properties, summarized in Table 3.1. Unfortunately, no LiF/SiC or CaF$_2$/SiC study was found in literature and it is even difficult to find publications describing the electrical performance of the two dielectrics deposited on silicon (except [107] for CaF$_2$). The most often used technique for LiF deposition is laser ablation described e.g. in [108], [109], evaporation [110] or reactive gas magnetron sputtering [111], CaF$_2$ can be obtained by evaporation [110], molecular beam epitaxy [112], RF magnetron deposition [113]. In our experiments laser ablation at room temperature was used to deposit both dielectrics.
4. Characterization techniques

In this thesis several characterization techniques have been utilized. The main techniques are: X-ray diffraction (XRD), Rutherford backscattering spectrometry (RBS), X-ray photoelectron spectroscopy (XPS), atomic force microscopy (AFM), current-voltage measurements (IV) and capacitance-voltage measurements (CV).

These characterization techniques might be sorted into two groups: the methods to investigate structural material features (XRD, RBS, XPS, SEM, AFM) and methods for electrical properties (IV, CV) analysis. All techniques listed above are non-destructive and all except RBS are available in the laboratories located in the department building.

4.1 X-ray diffraction (XRD)

The principles of XRD were applied in 1912 by the German physicist Max von Laue, who showed diffraction pattern of X-rays on a crystal of copper sulphate [114]. During almost a century the technique has matured and nowadays allows investigation of lattice structure, lattice dimensions and atom positions, orientation of crystalline films, grain size or residual stress in thin films and also many other features not mentioned here.

The method is based on the interference of scattered X-rays from a crystal lattice (see Fig. 4.1). The strongest signal is recorded, when the angle of the incident beam fulfils the condition described below,

\[ n \cdot \lambda = 2 \cdot d \cdot \sin \theta \]  \hspace{1cm} (4.1)

Where:
- \( n \) – is an integer number
- \( \lambda \) – is the wavelength of the incident beam [m]
- \( d \) – is the distance between the crystalline planes [m]
- \( \theta \) – is the angle between the incident beam and crystal surface [deg]

In this thesis the XRD analysis is mainly focused on verification whether the dielectric layer is amorphous or polycrystalline. Such information is important since leakage current in dielectrics might be dominated by leakage through grain boundaries. Such a situation is presented in the Chapter 6.2.1, in Fig. 6.12, where the and IV characteristics of AlN films deposited by plasma deposition method on p-type Si substrates are presented.
4. Characterization techniques

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Fig. 4.1: Schematic presentation of the principles of the Θ-2Θ scan. The symbols are the same as in formula (4.1)

4.2 Rutherford backscattering spectrometry (RBS)

The fact that accelerated helium particles (α radiation) are scattered by matter was described by a famous scientist from New Zealand, Ernest Rutherford in 1911. This phenomenon allowed at those times to understand the structure of the atom. Nowadays RBS is very elegant and non-destructive technique that allows measurement of the sample composition i.e. elements present, and stoichiometry. For a known thickness of the analysed film a density calculation is possible. Additional information that can be obtained from RBS analysis is the abruptness of the interface, element migration or verification of the existence of unintended contamination. The sensitivity of the method is better for heavier elements.

All RBS measurements were done at the 5 MV tandem accelerator at Ångstrom Laboratory, Uppsala University. The energy of He atoms during measurement was 2.0 MeV and simulations of the spectra were performed by SIMNRA 5.1 software [115]. A typical plot and simulation are presented in Fig. 4.2 for 150 nm thick layer of TiO₂ on a Si substrate. One can see a very good fit of the measurement and calculations. The interface between Si and ALD-deposited TiO₂ seems to be abrupt.
Fig. 4.2: Recorded RBS spectrum and RBS simulation of a 150 nm thick TiO$_2$ film deposited on Si. The channel represents the energy of the backscattered He particles (energy is rising to the right side of the axis), while the intensity is the strength of the measured signal.

### 4.3 X-ray photoelectron spectroscopy (XPS)

XPS is a technique used to study the chemical composition of the top surface layer up to a depth of about 5 nm. In this method X-rays are focused on the surface and the energies of the scattered photoelectrons are recorded. The electrons emitted are non-valence electrons so that the measurement is not so sensitive to the binding energies of the atoms. Nevertheless, the result can be compared with reference tables to obtain specific bond signatures.

In this thesis XPS was used mainly for the studies of Al$_2$O$_3$ deposited by laser ablation and also investigation of the SiC surface after UV treatment. In the equipment $h\nu = 1486.6$ eV for $K_\alpha$ of an Al source was used. Typically, electrons from the silicon 2p (Si$_{2p}$) and oxygen 1s states (O$_{1s}$) are used to monitor the presence of Si and O, respectively. As an example of the XPS investigation of SiC surfaces, the changes in Si$_{2p}$ and O$_{1s}$ for various surface treatments are shown in Fig. 4.3. The figure shows three spectra, the first after standard solvent cleaning procedure (acetone, propanol and deionised water in succeeding 5 min. ultrasonic baths) and HF dip, the second after UV-cleaning in air and the third after UV-cleaning in N$_2$. In Fig. 4.3, the left picture is the O$_{1s}$ peak and the right one is Si$_{2p}$. O$_{1s}$ signature suggests the existence of two oxygen compounds after UV treatment in air. The spectrum for the same energies after UV in N$_2$ and HF dip also show at least two types of oxide compounds, but the peak at a higher binding energy is different and shifted towards the dominant O$_{1s}$ peak if compared to those after UV in air. The change in Si$_{2p}$ peak is not that much pronounced but after UV in N$_2$ the shape of the
spectrum is more symmetric, suggesting less contaminated surface than after UV exposition in air.

Fig. 4.3: XPS spectra taken from the 4H-SiC sample after 5% HF dip, UV treatment in air and UV treatment in N₂ atmosphere.

4.4 Atomic force microscopy (AFM)

The principle of scanning probe microscopy (SPM) is very simple. It is based on scanning the surface with a very small tip at a close distance while monitoring for example tip deflection, current or voltage between the tip and the sample. There are many variants of the SPM technique depending on the measured property, for example atomic force microscopy (AFM) measures forces between the tip and the surface atoms by monitoring the tip deflection, scanning spreading resistance microscopy (SSRM) measures resistance distribution on the surface using a conducting tip, scanning tunnelling microscopy (STM) measures tunnelling current, etc. The equipment available for this thesis is a Nanoscope 3100, which was mainly used for roughness measurements and imaging of surface structures. One example of such a measurement is presented in Fig. 4.4, where the surface of the 150 nm thick TiO₂ deposited on Si substrate is shown. The surface RMS roughness, 5.3 nm, was almost one order of magnitude larger than for the Al₂O₃ film obtained with the same technique. This suggests that the TiO₂ film could be deposited too fast.
Fig.4.4: The amplitude variation of a 1 µm² scan of TiO₂ surface deposited on Si with the ALD technique. The origin of the surface structures is unknown. However, the roughness of 5.3 nm was almost one order of magnitude higher than for Al₂O₃ film deposited with the same ALD technique. This suggests too fast deposition of the titanium compound. One can add that XRD analysis of the material did not reveal any TiO₂ peaks what indicated an amorphous structure of the material.

4.5 Current-voltage measurements (IV)

Current voltage measurements allow an estimation of the leakage current characteristics and the critical breakdown field of the dielectric material. The IV measurements performed at different temperatures allow also better understanding of the mechanism of the leakage current. The characterisation was performed both on metal-insulator-semiconductor (MIS) structures, see Fig. 4.5, and diodes with and without passivation layers. All the MIS structures had a nickel top metallization and a backside ohmic contact consisting of Al for all Si samples and nickel silicide and Ti/Au metallization for SiC. The measurements were performed both on a manual probe station at KTH SSD laboratory and for statistical analysis by Dr Adolf Schöner on a Carl-Suss automatic probe station at Acreo. An example of the leakage current characteristics of an AlN film is presented in Fig. 6.12.
Fig. 4.5: Typical MIS structure used for electrical measurements in the thesis. The top electrode is Ni deposited by electron beam sputtering; the semiconductor is silicon with Al backside metallization, or silicon carbide with Ti/Au backside metallization. The smallest or largest circular electrode can have 100 µm or 700 µm in diameter, respectively.

4.6 Capacitance-voltage measurements (CV)

Capacitance voltage measurement of semiconductors and their interfaces is a very sensitive and powerful technique for electrical characterisation of semiconductor-dielectric interface. The method is based on monitoring capacitance for varying DC voltages. The capacitance measurements utilize a small AC bias signal super imposed on the DC bias. In these measurements the top contact of a MIS structure was always used. The DC voltage creates inversion (minority carriers accumulation), depletion (no mobile carriers) or accumulation (of majority carriers) in the semiconductor underneath the dielectric, while the AC signal is sampling the charge variations. The method allows an estimation of the fixed charge in the dielectric, measurement of trap distribution in the oxide and also estimation of the dielectric constant if the thickness of the dielectric is known. An example of measurement result is presented in Fig. 4.6, where the difference between the Al₂O₃ deposited on p-type Si substrates with or without 5% HF dip after UV pre-treatment is shown.

As can be seen in Fig. 4.6, the sample etched in HF prior to the deposition (the right set of curves) does not create an inversion region, whereas the non-etched sample does. Moreover the visible horizontal shift between the set curves measures the different concentration of the interface charge, 2.8·10¹² cm⁻² and 2.5·10¹² cm⁻² for etched and non-etches samples, respectively. The charge difference, 3·10¹¹ cm⁻², is located at the surface as both samples were prepared by the same deposition process. The CV characteristics also show good quality of the films, as they have no hysteresis (charging), no AC frequency dependence, they have stable capacitance in accumulation, and an expected value of the calculated dielectric constant.
Fig. 4.6: CV characteristics of 200 nm Al₂O₃ deposited by ultrasonic spray pyrolysis on p-type Si after different surface pre-treatments, with or without 5% HF dip after UV cleaning. The dielectric constant equal 9 is obtained from the capacitance value in the accumulation (for lower positive voltages in the plot) while the horizontal shift is due to fixed charge in the oxide. An interesting feature is the lack of inversion region for the sample etched in 5% HF before deposition, indicated by not stabilized capacitance at high positive potentials.
5. Device structures

The devices used in the thesis are grouped into two main sets. The first set consists of epitaxial PiN diodes (Master of Science diploma work, FTE/2002-2) and these are the double etched MESA diodes manufactured by Acreo. The second group of devices, designed especially for the passivation investigation, are sets of PiN diodes with different device periphery to surface ratio. An addition to these rectifying structures are MIS capacitors used for CV and IV characterisation of the dielectrics.

5.1 1.2 kV 4H-SiC double etched MESA PiN diodes

The first set of diodes was designed for blocking 1.2 kV and a detailed description is given in [116] where their performance was compared with implanted devices having the same structure. The components were also investigated electrically in a temperature range from room temperature up to 350 °C and part of those results is enclosed in Paper A.

The diodes were manufactured on n-type 4H-SiC substrate wafers with a doping of 8·10^{18} cm^{-3} purchased from CREE Research Inc. The same company also prepared 10 µm thick epitaxial layer with a doping of 4·10^{15} cm^{-3}. The termination layers were done by Acreo with an aluminium dopant concentrations of 1·10^{17} cm^{-3} and 7·10^{20} cm^{-3}, and thicknesses 2.8 µm and 0.5 µm, respectively. A cross section of the device is shown in Fig. 5.1. The diode process used four mask steps. The circular anode contacts were 400 µm in diameter and the circular field termination rings were 50 µm or 100 µm from the anode contact edge. In the studies presented in this work, only the devices with 100 µm terminations are used. The diodes were arranged in the form of 9 sectors, each containing 4 groups of 30 diodes, see Fig. 5.2. Each of the device termination design was prepared on 4 sectors, totally 16 groups of 30 diodes for one design. The last 9th sector had a lithography failure and was discarded from the analysis.
The cross-section of the investigated 4H-SiC diodes and the SEM picture of cross-section of the top MESA edge. White coating at the SiC surface is 200 nm thick AlN passivation layer.

The largest advantage of MESA PiN diodes design is the relative easiness of the processing. The component can be obtained with a minimum of one mask for anode contact metallization and utilizing self aligned etching. The disadvantage of the concept is the existence of the corner between device surface and MESA slope, where the highest electric fields are expected. Double MESA design has two such regions and, in theory, the peak electric field intensity should be lower than in a single MESA device. The difficulty is in the proper doping of the first MESA layer, the lower doped p-type region in Fig. 5.1, because too low dopant concentration will cause higher field intensity in the upper corner, while too high doping will cause the first MESA region to be not fully depleted and the electric field will be increased in the lower corner.

Fig. 5.2: The layout of the 1.5 inch wafer with the epitaxial diodes.
Fig. 5.3: ISE TCAD simulations used to optimise the thickness of the p-type region in the double MESA structure. The decrease of the electric field for higher effective doses creates the failure point at the lower MESA edge, while too low dose exceeds electric field on the upper edge.

A set of simulations performed on the device, presented in Fig. 5.3 using ISE TCAD software [117] resulted in a range of effective doping concentration given in units of cm$^{-2}$. The effective doping is a product of the p-type region doping and the thickness of that region. As seen in Fig. 5.3, the optimum effective doping concentration is in the range of $9 \times 10^{12}$ cm$^{-2}$ to $1.1 \times 10^{13}$ cm$^{-2}$, which correspond to the thicknesses of the p-type region 0.9 µm and 1.1 µm, respectively.

Electric field surface distribution at the edge of the diodes in the blocking mode was visualized by electron beam induced current (EBIC) measurements [118], where the electron beam of a SEM microscope is used to generate electron-holes pairs that can be detected by current meter. The example of such a measurement is shown in Fig. 5.4.

![Figure 5.4](image_url)

Fig. 5.4: SEM picture (to the left) of the bonded 1.2 kV SiC diode used in the tests, metallization and the two edges of MESA structure are visible. EBIC image (to the right) of the same diode taken for the acceleration voltage of electrons of 25 kV, the sample is not biased. The uniform distribution of depletion region is visible; the other edge is not visible due to low lifetime of the carriers. The measurements were done at Uppsala University [118].
The influence of the passivation on the diodes voltage blocking capabilities is shown in Fig. 5.5, where are presented the reverse characteristics of the best non-passivated and Al2O3 passivated devices. The breakdown voltage of the passivated diode was extended by about 80%.

Fig. 5.5: Breakdown characteristics of the non-passivated and Al2O3 passivated devices. The 200 nm thick passivation layer was deposited with USP technique.

In conclusion the data presented in this chapter suggest that the device passivation studies should focus on the MESA corner passivation and deposition technique should provide as good coverage of the vertical walls and eliminate shadow effects of e.g. bonding wires.

5.2 SiC MESA diodes of different periphery to area ratio

The second set of devices used in the thesis consisted of MESA diodes with different periphery to area ratio, to measure surface and edge components of the leakage currents. The components were processed on the 2 inch 4H-SiC n-type (5·10\(^{18}\) cm\(^{-3}\)) commercial Cree substrate. A 5 µm thick n\(^+\) buffer (5·10\(^{16}\) cm\(^{-3}\)), 25 µm thick n\(^−\) drift region (6·10\(^{15}\) cm\(^{-3}\)), 1 µm thick p-type buffer (1.5·10\(^{17}\) cm\(^{-3}\)) and 0.5 µm thick p\(^+\) emitter (5·10\(^{19}\) cm\(^{-3}\)) were epitaxially grown at Acreo. The layout of the diodes is shown in Fig. 5.6.

The devices consist of two types of PiN structures:

a) The standard circular MESA diodes with different top metallization diameters, namely 250 µm, 450 µm and 650 µm.

b) Two MESA structures in a shape of rings with area and periphery lengths matching some of the circular diodes. The larger diode had outer and inner diameters 922 and 650 µm, respectively, and the smaller ring diode 480 and 170 µm, respectively.
Fig. 5.6: Schematic cross-section of the circular MESA diodes and layout of one sector of the circular- and ring- shaped MESA diodes, used for leakage current studies.

The MESA structures were measured after different surface treatments (reactive ion etching or exposure to UV light), and different depths of the mesa etch from 2 to 3.5 µm (from the top electrode). The main conclusions of the experiment was that all the leakage current of the MESA components was through device periphery, diodes processing was introducing surface charge which was unstable within a period of days and months. Annealing at 200 °C stabilized the charge at the surface. The results of the investigation are described in detail in Paper B.

5.3 Metal insulator semiconductor structures (MIS)

MIS is a basic structure used for dielectrics electrical characterisation. The cross section of the device is shown in Fig. 4.5. The mask used in lithography process has four sizes of circular capacitors, 100 µm, 300 µm, 500 µm and 700 µm.

The semiconductor material used for depositions are n-type 4H-SiC CREE substrate with a $6 \cdot 10^{15}$ cm$^{-3}$ epilayer grown at Acreo, p-type (100) Si ($0.75-1.25 \ \Omega$cm) and n-type (100) Si (1-10 $\Omega$cm). Additionally, in the Papers H and I, n-type SiC samples with 8 nm or 13 nm thermal oxide thicknesses, and epitaxial layers nitrogen doped at $1 \cdot 10^{15}$ cm$^{-3}$ or $2 \cdot 10^{14}$ cm$^{-3}$ were used, respectively. The backside ohmic contact for both silicon substrates was obtained by sputtered Al, but prior to n-type Si metallization a phosphorus implantation and annealing was done. The contact for SiC was nickel silicide and Ti/Au metallization.

After dielectric deposition, a 140 Å thick nickel layer was sputtered and a positive lithography process was used for photoresist patterning. The process was finished by nickel etch and photoresist removal. The main problems in the process were caused by the small samples size, usually not larger than 1 cm$^2$. Nevertheless, there were always at least 50, 100 µm diameter devices available for measurements on each sample.
6. Results from dielectric films and surface passivation

The problem of SiC passivation is not only related to the choice of a proper dielectric material, but also to the surface preparation and growth or deposition techniques.

6.1 Aluminium oxide

In this thesis aluminium oxide, Al₂O₃, was the most intensively studied dielectric alternative to silicon dioxide. The techniques used for deposition are:

- ultrasonic spray pyrolysis (USP) done at the Materials Research Institute at Autonomous National University of México (UNAM),
- atomic layer deposition (ALD) done at the Department of Chemistry at Helsinki University
- magnetron sputtering epitaxy (MSE) done at the Department of Physics at Linköping University
- pulsed laser deposition (PLD) done at the Department of Microelectronics and Information Technology at the Royal Institute of Technology
- physical vapour deposition (PVD) done at the Thin Films Group at Uppsala University

The work in this thesis does not involve the deposition techniques themselves. To obtain the desired films we have relied on collaboration with the expert groups mentioned above. The techniques are further described in the appended papers, and here we concentrate on the evaluation of the film properties.

6.1.1 Ultrasonic spray pyrolysis and atomic layer deposition

Out of the five methods tried, only ALD and USP techniques are successful in producing good quality passivating films. Both materials have critical breakdown fields of more than 6 MV/cm and dielectric constants between 9 and 11 as obtained from Si MIS capacitors. The positive effect of UV irradiation is seen for the USP process when two different surface treatments were tested, with and without UV exposure as the last process prior to dielectric deposition. The PiN diodes used in both experiments had breakdown voltages of 1.6 kV and 0.9 kV for the USP and ALD passivated devices, respectively. The non passivated diodes have a breakdown at 0.5 kV and 0.9 kV, without surface coating.
and covered with liquid suppressing electric discharge in air, respectively. There were two 
Al₂O₃ depositions done by USP and one by ALD. The aluminium oxide deposited in 
the second experiment by USP is of poorer quality compared to the first one, which raises the 
question regarding the process reliability. The breakdown tests on diodes were done for 
devices with the later deposited USP film. The detailed results from this comparison are 
the contents of Paper F.

6.1.2 Magnetron sputtering epitaxy

The goal of the experiment, done together with Plasma and Coating Physics from 
Linköping University was to test the aluminium oxide deposited both with and without 
chromium oxide, (Cr₂O₃), interfacial layer. The deposition technique is fully described by 
the group in [119]. Additionally, different surface treatments were applied before 
depositions, namely with and without 5% HF dip after UV exposure. The electrical 
measurements performed on all the samples reveal high leakage levels compared to the 
material obtained from other sources, see Fig. 6.1. The only exception is the sample with 
no HF pre-treatment and no chromium oxide layer, Fig. 6.1b, where the dielectric strength 
reaches 7 MV/cm on the Si sample and about 6 MV/cm on the SiC material (Fig. 6.1b). 
Unfortunately, the large differences in dielectric properties of the film, measured on the 
samples prepared during the same deposition indicate problems during the deposition 
process. Capacitance measurements of the best film resulted in relative dielectric constant 
of about 10 and large hysteresis. Unfortunately, the characterisation was only possible to 
conduct on the smallest MIS capacitors (100 µm in diameter) on silicon samples deposited 
without Cr₂O₃ layer, Fig. 6.3.

Fig.6.1: IV characteristics for Al₂O₃ layers on silicon and SiC obtained from Linköping University. 
Sample “b” with no Cr₂O₃ layer and without HF pre-treatment reached a breakdown field of about 
7 MV/cm. The difference between samples “b” and “c” is very large and cannot be caused only by 
the HF dip. Most probable reason for differences was a problem during the deposition process. The 
same conclusions can be drawn from the measurements done on SiC.
The structural XRD analysis did not confirm the presence of crystalline structures of aluminium oxide or chromium oxide. The RBS spectra, Fig. 6.4, were recorded from three samples, excluding the one without Cr$_2$O$_3$ layer and with HF pre-treatment. The results show many differences, such as varying stoichiometry and layer thicknesses, proving incoherent sample structures. For that reason no conclusive comparison could be done between the electrical results.

Fig.6.2: IV characteristics for Al$_2$O$_3$ layers on SiC obtained from Linköping University.

Fig.6.3: The capacitance-voltage results obtained for Al$_2$O$_3$ material deposited by magnetron sputter epitaxy. The results suggest unrealistically different dielectric constants for two surface pretreatments before the depositions. The assumed films thickness is 200 nm and the top electrode is 100 µm in diameter. Arrow indicates increasing frequency of the AC component, from 1 kHz to 1 MHz.
6. Results from dielectric films and surface passivation

Fig.6.4: RBS spectra taken for the Al₂O₃ samples prepared by magnetron sputter epitaxy. The only proper profile is obtained for the sample without Cr₂O₃ interfacial layer. Both aluminium and oxygen peaks are clearly visible with stoichiometry of 35% of Al and 65% of O, according to simulations. For the other samples the aluminium and chromium thicknesses differ between the samples. Also the oxygen peak is indicating non-uniform oxygen distribution.

6.1.3 Pulse laser deposition

Pulsed laser deposition (PLD) was tested as an in-house technique for aluminium oxide deposition. The method is based on sputtering of aluminium oxide from a target material. The material is released from the target due to high energy, 5.0 eV, laser pulses from KrF Eximer laser. The laser pulse energy is 200 mJ. The deposition can be done in vacuum, or with a desired pressure of oxygen, nitrogen, argon or hydrogen gases. The equipment also allows for heating the substrate and rotation of both the target and the substrate. Here only the main insulator features will be discussed, since the detailed characterisation of the material obtained by PLD was done elsewhere [120].

The material obtained from the laser ablation was deposited at three different deposition temperatures: room temperature, 510 °C and 640 °C. The films were studied by XRD, RBS, AFM, SEM, XPS, CV and IV. Out of three samples, only the one deposited at room temperature was eventually acceptable for electrical characterisation. Current-voltage measurements suggested the existence of short circuit regions of the top nickel metallization with the p-type silicon substrate, caused by holes in the insulator. Such holes could be also seen by AFM. For that reason the yield of the the largest (400 µm in diameter) MIS structures is much poorer than for the smallest (100 µm in diameter) ones, Fig. 6.5. Unfortunately, the insulating film properties investigated with capacitance-voltage measurements, shown in Fig. 6.5, have large hysteresis, revealing a fixed oxide charge
varying between $1 \cdot 10^{12}$ to $2 \cdot 10^{12}$ cm$^{-2}$. Additionally, the effective charge is dependent on the AC frequency. Interesting result is also obtained by the SEM investigation, where many electrically active defects are shown on the dielectric surface. Those defects are not visible by means of AFM, or any other technique used. An example of such observations is shown in Fig. 6.6, where the dark spots are thought to be electrically conducting.

As a consequence, the PLD technique was found not appropriate for device passivation. Film non uniformities, unrealistic dielectric constant of more than 15 and large oxide charge discarded the deposition technique from further studies. Moreover, the reproducibility of the method for passivation is problematic, due to target degradation caused by the laser pulses. This causes decreasing of Al$_2$O$_3$ deposition rate with time.

![Fig. 6.5](image)

**Fig.6.5:** Leakage current density as a function of voltage for the best sample with the laser ablated aluminium oxide. The plot on the left side is for the smallest capacitors of 100 µm in diameter and the right plot corresponds to the largest structures of 400 µm in diameter. The difference in yield is clearly visible.
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Fig. 6.6: Capacitance-voltage measurements of one of the best Al₂O₃ layers deposited by PLD. All the capacitors suffer from a very large hysteresis. In the picture it is seen that during the measurement (1 MHz curve was measured first) the film becomes more negatively charged. Capacitor diameter is 200 µm and film thickness is 37 nm.

Fig. 6.7: SEM picture of the sample deposited at room temperature by PLD. Many black points on the surface might be the indication of defects as the contrast in SEM is such that a darker region is more conductive then a brighter one.
6.1.4 Physical vapour deposition

The principle of operation of the physical vapour deposition system used at Uppsala University is the same as for the magnetron sputtering epitaxy used by Linköping University; therefore it was very interesting to characterize Al₂O₃ obtained from both collaborators.

The goal of the PVD deposition was to test AlON material but during the RBS test on the films no trace of nitrogen was found and aluminium to oxygen ratio was found to be 40% to 60%, respectively, which is exactly the stoichiometry of Al₂O₃. The example of the RBS spectra is shown in Fig. 6.8, together with an example of the AlN spectra.

Fig. 6.8: RBS spectra recorded for the Al₂O₃ films, for comparison an example of the spectrum recorded for the AlN material deposited on SiC substrate is added. The stoichiometry of the Al₂O₃ was 40% and 60% for aluminium and oxygen, respectively.

The surface of the Al₂O₃ films was very smooth (0.2 nm variation from the region of 1 µm²), but the holes of the depth of at least 3 µm were observed on n- and p-type samples. The surface of the 4H-SiC sample did not reveal any structures except the terraces due to the off-axis orientated substrate. XRD measurement did not reveal any crystalline forms in the samples (except substrates) which indicated, together with the smooth surfaces, that the films were amorphous.

The samples were characterised electrically (IV, CV) both before and after one hour 400 °C anneal in a forming gas atmosphere. The IV characteristics did not change during annealing, they were scattered and could block up to 25 V and 60 V on a n- and p- type silicon samples, respectively, in accumulation regimes. The blocking capability on SiC was much better and yielded up to 140 V in accumulation. This large difference in the values of a breakdown voltage is most probably caused by the holes in the dielectric on silicon samples.
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CV measurements showed very large improvement in films quality after annealing, Fig 6.9. The hysteresis visible at different AC frequencies was reduced for silicon samples, and for SiC sample the CV characteristics could be obtained, that was not a case before the annealing.

After those encouraging measurements, the decision was taken to continue tests with Al₂O₃. At the time when the thesis are written (September 2006), the samples are not annealed yet, but 200 nm thick films, have the roughness of 0.6 nm, can block up to 8 MV/cm, have comparable spread of CV characteristics and have average dielectric constant of 6.95. No holes in the films were observed.

Fig.6.9: Capacitance voltage measurements on Al₂O₃ insulator deposited on p-type silicon (left plot) and n-type SiC (right plot). After forming gas anneal less charging is observed in case of the silicon sample, CV plot was possible to extract on SiC sample only after anneal. The origin of the different capacitance levels in accumulation might be caused by the difference in thickness, which is unknown.

6.2 Aluminium nitride (AlN)

Aluminium nitride is another potential insulator for SiC material. AlN layers were acquired from two research groups, namely: Department of Material Sciences, and Solid State Electronics, both from Uppsala University.

- plasma deposition (PD) done at Plasma Group
- physical vapour deposition (PVD) done at Thin Films Group

6.2.1 Plasma deposition

There were two attempts for AlN deposition by the PD method. The deposition is done at low pressure and temperature. The reactive plasma obtained from the gaseous precursors is created by a horizontal electric field not interacting with the sample holder with the substrate attached. The deposition is done through a second, vertical electric field, which accelerates the ions from the plasma towards the substrate.
In the first run, AlN deposition was accomplished with different plasma power (400 W, 500 W and 600 W) and different film thicknesses (200 and 500 nm). Unfortunately, as presented in Fig. 6.10, all the samples were characterised by a high leakage current and the breakdown field was less than 1 MV/cm. Additionally, the RBS spectrum revealed an unidentified element in the film material with a mass similar to Ti, which could indicate a Ti contamination in the process chamber. The composition was 0.40 and 0.60 parts for aluminium and nitrogen, respectively, which is different from the expected 0.50 to 0.50 (see Fig. 6.11).

![Fig. 6.10: The current-voltage measurements performed on the first batch of AlN films deposited by PD technique. All the films are of poor quality](image-url)
The second batch of AlN material deposited by PD was more successful. In the experiment all the process parameters were constant and two samples were obtained for grounded and floating substrate potential. As a result two different leakage current dependencies were obtained, suggesting a polycrystalline structure of the material deposited with the grounded sample holder, Fig. 6.7. The RBS analysis confirmed again the existence of a contamination and also allowed for density calculations yielding 1.78 g/cm$^3$ for the less crystalline film and 1.92 g/cm$^3$ for the polycrystalline material. The stochiometry obtained was also better than in the first batch resulting in atomic contents of 0.44 and 0.56 for aluminium and nitrogen, respectively. These improved layers also allowed for capacitance voltage measurements, although they showed very large charge trapping in the insulator, Fig. 6.13.

Fig. 6.11: RBS spectra of the four AlN samples deposited by PD in the first batch. Sample of the largest thickness, 500 nm, did not show any AlN material. Contamination signature is also pointed out by Ti and an arrow.
Fig. 6.12: Current-voltage measurements of the 200 nm thick AlN MIS capacitors from the second batch of the PD grown samples. The XRD results (not shown here) indicate the presence of AlN grains in the sample named UII2 (sample holder grounded during deposition) while the sample UII1 is assumed to be amorphous. The large difference in leakage currents is indicated by the leakage through grain boundaries. XRD measurements are done by the Plasma Group at Uppsala University.

Fig. 6.13: Examples of the capacitance-voltage characteristic for AlN material deposited with the floating substrate potential. The film suffers very large charging seen as hysteresis. The CV curves are also AC frequency dependent. The top metallization is nickel, the substrate is p-type silicon, the film thickness is 200 nm and the capacitor diameter is 300 µm.
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6.2.2 Physical vapour deposition

The second AlN material source was physical vapour deposition (PVD) done at the Thin Films Group at the Dept. of Material Sciences, Uppsala University. The dielectric analyses were performed on two batches and good results after the preliminary tests encouraged us to verify the insulator performance as SiC diodes passivation. In this thesis only the results from the second batch will be mentioned, the detailed description of the experiment can be found as Paper G.

AlN was deposited on two sets, each containing n- and p-type silicon substrates and n-type SiC substrates. Additionally, 1.2 kV SiC diodes described in Chapter 5.1.1 were included. All the samples were exposed to UV light from a mercury lamp in nitrogen atmosphere and the same AlN material was deposited on both sets with the only difference that one set was dipped in 5% HF prior to the deposition procedure. The SiC diodes were not HF-etched.

The structural XRD analyses of the insulator showed a polycrystalline material with a dominant [002] orientation. The stochiometry from the RBS studies was 0.40 and 0.60 for aluminium and nitrogen respectively, and the calculated density was 3.27 g/cm³ for materials from both sets. A soft electrical break down, defined at a current density of 0.1 A/cm², was observed at about 3 MV/cm for the accumulation regimes on both n- and p-type silicon substrates. The same data for SiC samples showed an influence of the pre-treatment and a higher breakdown field of about 3 MV/cm was measured for the sample without 5% HF dip. The other SiC sample had a breakdown at about 2 MV/cm.

The CV characterisation was only possible to perform on silicon samples and resulted in a dielectric constant of 8.8 on capacitors with 500 µm diameter. The samples with no HF treatment prior to the deposition showed smaller hysteresis. The CV measurement on SiC samples was unsuccessful due to too high leakage observed already at 5 V (0.25 MV/cm).

The diode passivation resulted in a slightly higher leakage current after passivation than for as-processed devices. Nevertheless, the leakage level of 10 pA at 500 V was still a low value and the most probable failure mechanism of the diodes, breakdown at the MESA edge, was suppressed by the AlN dielectric material.

6.3 Silicon dioxide

Silicon dioxide applied in this thesis was not used as a passivation layer. Its function was to provide an additional potential barrier to prevent carrier injection from semiconductor into the insulator with a high dielectric constant. The schematic picture of the band diagram of the metal/dielectric/SiO₂/4H-SiC stack with the applied electrical field is shown in Fig. 6.14. The situation presents n-type 4H-SiC material in accumulation where letter “A” is for the electrons at lower electric fields, when the SiO₂ layer is seen as an additional potential barrier. Letter “B” corresponds to the case when at higher electric fields the electrons are injected by FN tunnelling.
Two n-type (0001) SiC wafers were processed on CREE substrates with epilayers nitrogen doped to the level of $4 \cdot 10^{15}$ cm$^{-3}$ and $1-2 \cdot 10^{15}$ cm$^{-3}$, marked as W1 and W2 respectively. The oxide was obtained by thermal oxidation at 1100 °C for 5 or 30 minutes and proceeding wet oxidation at 950 °C for 3 hours. Wafer W1 had 8 nm of SiO$_2$ (estimated by CV measurements) and wafer W2 had 13 nm thick (estimated by ellipsometry) SiO$_2$ layers.

The wafers were cut into pieces and were characterized electrically before usage in AlON and HfO$_2$ depositions. The breakdown voltage measured on both SiO$_2$ layers yielded 7 MV/cm. The CV characteristics revealed good interface properties with small hysteresis and the fixed interface charge equal to $2.5 \cdot 10^{12}$ and $1.2 \cdot 10^{12}$ cm$^{-2}$, for samples W1 and W2, respectively, Fig. 6.15.
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Fig. 6.15: Typical CV measurements of the 8 and 13 nm thick SiO₂ layers grown on 4H-SiC wafers. The shifts of the characteristics dependent on the AC frequency are marked by arrows.

6.4 Aluminium oxynitride

The idea to mix the properties of aluminium oxide (breakdown voltage of 8 MV/cm) and aluminium nitride (comparable thermal expansion coefficient to SiC, good interface properties to SiC) lead us to the experiment where AlON films were deposited with the two different oxygen contents, 8% and 10%. The depositions were done with PVD technique, the same as was used for AlN depositions. The experiment details are presented in Paper H.

Six sets of samples were used, each consisting of n- and p- type silicon, 4H-SiC and 1.2 kV SiC diodes (in only two sets of samples), and additional two pieces of 4H-SiC samples with 8 or 13 nm thick thermal SiO₂ to introduce additional potential barrier to prevent carriers injection from SiC into AlON. Surface preparation procedure included solvent clean; etch in 5% HF (except samples with SiO₂ layers) and exposition to the standard UV procedure (except samples with SiO₂ layers). As mentioned, two different types of films with different oxide content were deposited, each on three sets of samples that differed in film thickness (100 nm thick or 200 nm thick) and surface treatment (100 nm thick film with one additional 10 min. RCA1 clean prior to the deposition).

XRD analyses were done by our collaborators at Uppsala University. The measurements revealed that the film with 8% oxygen content contain preferential [002] AlN orientation perpendicular to the surface. The samples with 10% oxygen had 5 times lower intensity of that peak.

The oxygen content difference of only two percent (verified by XPS also done at Uppsala University and by RBS) influenced substantially AlON CV properties. The film
with 8% of oxygen deposited without SiO₂ buffer provided the similar shift at flatband voltage as the SiO₂ layers before the AlON depositions. As the measured CV hysteresis is not proportional to the thickness of the insulator films its origin is assumed to be due to polarization in AlON. Electron trapping at the SiC interface is discarded by the direction of the hysteresis loop. The films with 10% of oxygen, compared to material with 8% of oxygen, yielded in larger hysteresis and had much worse AlON/SiC interface quality, which is believed to originate from the presence of oxygen at the semiconductor interface. The SiO₂ buffer layers provided sufficient barrier (up to 3 MV/cm electric field in SiO₂) to limit electrons injection from SiC into AlON and did not limit the breakdown voltage of the whole AlON/SiO₂ stack.

The RCA1 clean (H₂O, NH₃ and H₂O₂ in the ratio of 5:1:1, at 60 °C) prior to the deposition introduced additional negative charge at the AlON/SiC interface, also believed to be caused by oxidation of the SiC surface. CV measurements on the SiC sample with the thin (8 nm) SiO₂ layer were unsuccessful. The same measurements on the SiC sample with the thick (12.9 nm) SiO₂ layer revealed higher dielectric constant of the whole stack, what can be explained by the partial reduction of the SiO₂ thickness to 7 nm.

6.5 Hafnium dioxide

Hafnium dioxide depositions were done by ALD technique at the Department of Materials Chemistry at Uppsala University. All the results obtained from the HfO₂ investigation are included in Paper I, and only the most interesting ones will be pointed out in this section.

The choice of the material and the deposition technique were very encouraging, as HfO₂ is well characterized for usage in silicon technology, and ALD provides very good quality of the material. The samples used in our deposition included n- and p- type silicon, SiC, two samples with different thickness of thermally oxidized SiC and 1.2 kV SiC diodes. The samples before deposition were solvent cleaned, dipped in 5% HF and exposed to UV (last two steps without oxidized samples). Just prior to the deposition the samples were again solvent cleaned. Electrical characterization was performed before and after 1 hour annealing at 400 °C in a forming gas.

Structural characterization before annealing did not provide clear diffractionograms to identify which phase of the HfO₂ is present in the film. It was assumed that the film is polycrystalline with a mixture of different phases. The RBS measurement revealed unintended presence of the iodine (3%) and zirconium (2%), both of which are present in the precursor gas HfI₄.

Electrical CV measurements proved bad quality of the HfO₂/SiC interface while the introduction of the SiO₂ buffer layer was very beneficial. The flatband voltage shift that corresponds to the fixed interface charge was reduced by a factor 10 and two different thicknesses of the SiO₂ layers allowed to estimate the charge present at the HfO₂/SiO₂ interface. Breakdown tests of the dielectric stacks showed that the thicker SiO₂ layer limited the breakdown electric field of the whole stack, and reduced it by a factor of 2, to 4MV/cm. The calculated electric field present in the SiO₂ yielded 7 MV/cm, close to its performance limit. The breakdown voltages of the samples with 8 nm thick buffer layer
and without any buffer layer were very similar, what indicated that thin oxide did not prevent the injection of electrons and only provided a good SiC interface quality.

Annealing of all the samples resulted in a reaction between HfO$_2$ and SiO$_2$. Since it was impossible to measure any CV characteristics on the SiC sample with the thin SiO$_2$ layer, it was assumed that the compound of Hf, O and Si consumed the entire 8 nm thick SiO$_2$ buffer layer. That is in agreement also with a fact that CV characteristics could be measured on the SiC sample with the thick SiO$_2$ layer, what was explained by only partial consumption of SiO$_2$. The measurement also revealed that annealing increased the relative dielectric constant from 15.4 to about 21.

The diodes with HfO$_2$ termination had much higher leakage current compared to as processed devices; however the breakdown voltage was extended by 20%, compared to non-passivated components.

As a conclusion, HfO$_2$ is an interesting candidate for SiC termination. The quality of the film was good, but unfortunately unrepeatable due to limited source of precursors. Further tests would be needed to check the stability of the HfO$_2$ films after annealing.

6.6 Titanium dioxide

As described in Chapter 3.5 regarding dielectric materials, titanium dioxide is potentially a good dielectric for surface passivation. Unfortunately, the small bandgap of TiO$_2$ of about 3 eV, made the potential barrier too small to prevent injection of electrons from the semiconductor into the insulator, and very high leakage current of the MIS structures are measured as presented in Paper E. Further experiments with this dielectric were not performed, although the material could be used as a second dielectric layer with an intermediate insulator having a high barrier offset to SiC conduction band.

6.7 Lithium fluoride and calcium fluoride

Both LiF and CaF$_2$ dielectrics were deposited by the PLD technique at the Institute of Experimental Physics, University of Wroclaw, Poland. Both layers were deposited at 100 °C and had a thickness of 350 nm and 360 nm, for LiF and CaF$_2$ samples, respectively.

The RBS measurement revealed contamination with no uniform distribution along the thickness of the CaF$_2$ films, Fig. 6.16. The stoichiometry of the samples differed from the expectations and yielded 40% and 60% of lithium and fluoride atoms in LiF, respectively. CaF$_2$ layer was composed 28%, 65% and 7% of calcium, fluoride and an unknown contamination, respectively.
Fig. 6.16: Rutherford backscattering spectra recorded on n-type silicon and SiC samples. Uneven distribution of contamination can be observed.

XRD analysis did not show crystalline phases of the investigated films. This is in contradiction to the AFM measurements. Large roughness and structures of the size of tenths of nanometers were observed on the films surface indicating polycrystalline structure, Fig. 6.17.

Electrical measurement of the LiF and CaF$_2$ films were limited to IV breakdown test, shown in Fig. 6.18. CV analysis was impossible to perform due to too large electrical leakage.
Further investigations of the LiF/SiC or CaF₂/SiC systems were not carried on due to their poor electrical performance and difficulties in the processing as both films were soluble in water. The MIS structures were obtained by evaporation of metal through metal grid.

6.8 Gamma irradiation hardness

As mentioned in the introduction, one of the main future applications of SiC are devices with large resistance against irradiation, needed for example in space electronics. The typical dose of radiation the non shielded electronic components acquire on the Earth’s orbital is about 1 Mrad during the period of one year. The radiation hardness of silicon components is only 7 krad or up to 50 krad for flash memories or CMOS devices, respectively [121]. The defects are induced in the lattice of semiconductor and as charge trapping centres in the gate oxides or at their interfaces with semiconductors where the last one is the main reason of the failure. Therefore all electronic devices used in the space need to be shielded - typically put into a box made of aluminium.

Hardness against radiation was one of the main driving forces to develop SiC technology. Here only two experiments that prove the outstanding SiC radiation hardness will be referred. The first one is the exposure of the nickel Schottky diodes to 600 Mrad gamma irradiation dose [122]. As stated in the article the main change observed in the performance of the exposed device was the increase in resistance due to a degradation of metal electrode. The breakdown voltage decreased only by 10% and the rectifiers were still working properly. The other example is the exposure of SiO₂/SiC system and Schottky diodes to 4 Mrad irradiation [123]. After exposure, no change in the Schottky barrier was observed and the breakdown voltage of the rectifiers was even extended due to negative charge generated on the SiO₂/SiC interface. Based on those two examples one can see that SiC components would not need any shielding to be send out into space, which would compensate the high price of the development of SiC components.
In this thesis experiments performed on gamma irradiated SiC PiN diodes are described in Paper D. The measurements verify the impressive radiation hardness of SiC and a huge dose of 10 Mrad did not destroy the devices. SiC radiation hardness is not included as a topic in this thesis, but it is important for our studies because it drew our attention towards UV treatment of the SiC surface. The point is that UV exposure of the diodes radiated with the highest $\gamma$ dose reduced the leakage current by two orders of magnitude, suggesting that the whole leakage current originates from charged surface defects, which also agrees with the observations in [123].

Further gamma irradiation tests were conducted, where DLTS was used to monitor the possible bulk defects. The same 1.2 kV PiN SiC diodes were used as in the first experiment. The DLTS confirmed the irradiation immunity of up to a total dose of 4 Mrad, as no signal from bulk defects was identified.

### 6.9 Surface treatments

Three main surface treatments prior to the dielectrics deposition were tried in the thesis:

1. 5% HF dip
2. RCA1 clean ($\text{H}_2\text{O}, \text{NH}_3$ and $\text{H}_2\text{O}_2$ mixture in the ratio of 5:1:1, at 60 °C)
3. UV irradiation of the sample using a mercury lamp with a power density of 28 mW/cm² prior to the dielectrics deposition. The main intensity of the lamp occurs at 253.7, 184.9 and 282.1 nm and the respective intensity ratio are 10:2:1.

There are only two published studies of the electronic properties of SiC surface after exposure to UV irradiation, both conducted in ozone atmosphere [124], [125]. However, the results obtained by both groups are different as Avanas'ev et al. in [124] measured reduced charge at the SiO$_2$/SiC interface after exposure to the light with a wavelength of 147 nm and Zetterling et al. in [125] indicate very minor changes of the charge at the interface of the same materials, but after exposure to the lamp with the highest intensity at 254 nm. The other application of UV light in SiC technology is to enhance the rate of the electrochemical etching of the semiconductor [126], [127], [128], but no indication was done to any interaction of UV light to surface states. By now there are no data published regarding UV treatment of any SiC devices.

The author’s experiment with UV pre-treatment is submitted to publication as Paper D. In this work the 30 standard 1.2 kV PiN SiC diodes were characterised electrically before and after the following surface treatments:

- IV measurement after processing of unpassivated diodes.
- IV measurement after solvent clean and 5% HF dip
- IV measurements after UV irradiation in N$_2$
- IV measurements at RT and 150 °C after more powerful UV irradiation up to 10 eV photon energy.
- IV measurements after 5% HF dip
The results are presented in Fig. 6.19 and reveal that the lowest leakage occurs after high energy UV exposure. Instability of the surface at 150 °C might be probably avoided by deposition of the dielectric layer.

Fig. 6.19: The leakage current characteristics of SiC PiN diode after different surface treatments. The measurements are done after solvent cleaning and HF etch (1), an exposition to a mercury UV lamp in nitrogen atmosphere (2), an exposition to high power UV lamp measured at room temperature (3), at 150 °C (4) and again at room temperature (5) and as the last step, the measurement after HF etch (6).

In addition, the UV treated surfaces have been investigated by X-ray photoelectron spectroscopy, XPS. The analyses were done on 4H-SiC substrates after UV exposure in air or nitrogen atmospheres. More samples were tested after an exposure to high energy KrF Eximer pulsed laser in vacuum, nitrogen, oxygen or argon atmospheres. XPS measurements done after the laser exposures did not show any differences because of the SiC surface annealing effect caused by the laser beam. The differences between the samples after UV irradiation in air or nitrogen are more pronounced. The O 1s peak after the UV exposure in air shows clearly two oxygen compounds on the surface, Fig. 4.3, while after the UV exposure in nitrogen the O 1s shows a different signature. The less pronounced surface peak of the oxygen compound is shifted more towards the main SiO2 peak. Moreover, the Si2p peak is more symmetric for the UV exposure in nitrogen than for the UV exposure done in the air.

The main problem during XPS measurements was the fact that samples were prepared and analysed at different in-house laboratories, which caused the need to transport them in air atmosphere. This caused surface contamination like carbon or water adsorption, and the experiment should be repeated under more controlled conditions. UV exposure may be a promising alternative to HF or H2 annealing as a surface treatment process.
7. Summary

The Ph.D. thesis is focused mostly on characterisation of dielectric materials deposited on SiC. Finding the right dielectric for future devices is very important, but also surface preparation techniques and electric field termination are highly important.

Electrical and structural characterisation results from insulating layers of aluminium oxide (deposited by ALD, USP, MS, PLD and PVD), aluminium nitride (deposited by PD and PVD), aluminium oxynitride (deposited by PVD), titanium dioxide and hafnium dioxide (both deposited by ALD), lithium fluoride and calcium fluoride (both deposited by PLD) on low doped SiC epitaxial layers are presented in this thesis. Many of the dielectrics are novel in SiC technology.

Of all the investigated dielectric materials, aluminium oxide is especially interesting as it reduced the leakage current of rectifiers by a factor of two and extended breakdown voltage by 80% compared to the non-passivated diodes. Its electrical breakdown field of 6 MV/cm, relative dielectric constant of about 10 and the highest extracted conduction band offset to 4H-SiC of 1.7 eV makes it a suitable material for device passivation. The only drawbacks of the material are surface states and a large negative fixed charge measured at the SiC interface.

The quality of aluminium oxynitride with 8% oxygen content deposited by PVD technique was also very good and yielded a relative dielectric constant of 8.4, electrical breakdown field more than 6 MV/cm and a fixed interface charge comparable to that measured for the reference SiO$_2$/SiC system. The polarisation charge was identified as the reason of the measured hysteresis. The dielectric processing in PVD equipment must, however be optimised since in our experiments only 2% increase in the oxygen content induced large negative interface charge at the SiC interface and increased the hysteresis measured by CV technique.

Hafnium dioxide is also very promising passivation material, with a dielectric constant of 15 and electrical breakdown field of 6 MV/cm. The insulator deposited on PiN diodes increased leakage current by two orders of magnitude but at the same time extended their breakdown voltage by 20%.

Passivation made of two layers of dielectrics, namely silicon dioxide and hafnium dioxide or aluminium oxynitride were also investigated in the course of the studies. The stacked structures with a thin thermally grown SiO$_2$ buffer layer closest to the SiC proved their superior performance. In particular the structures showed extended breakdown voltage, improved interface quality to SiC and reduced leakage current (measured on MIS structures) compared to single passivation layers with a high dielectric constant deposited
directly on the semiconductor. However, thermal stability was a problem for the hafnium dioxide layer in our study, since the 400 °C anneal in a forming gas caused a chemical reaction between hafnium dioxide and silicon dioxide buffer layer.

MESA devices designed for an investigation of the origin of the leakage current and to separate the bulk and surface contributions of the leakage were also characterized. The edge of the MESA etch was identified as a place where most of the total measured leakage current comes from. SiC leakage characteristics were, however, stabilized after 250 °C annealing. Surface induced leakage current was also dominating the total leakage of the 1.2 kV PiN diodes with one zone termination (double MESA structure).

The “cleaning” of the SiC surface with the UV light of photon energies extending up to 10 eV dramatically reduced the leakage current of the SiC diodes. The origin of that phenomenon is not clear, but, the reduction of the carbon clusters present on the SiC surface may be responsible for the promising result.

The direction of further research should be to identify the leakage current mechanisms on the devices with the JTE and to analyse their performance with the passivation made of stacked dielectrics. Exposure of SiC devices to high energy UV light done at different ambients could also help to understand the SiC surface passivation mechanisms.
8. References


8. References


Characterization of Dielectric Layers for Passivation of 4H-SiC Devices


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