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Manufacture and Characterization of Elastic Interconnection Microstructures in Silicone Elastomer

Doctoral Thesis by
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Elastic Interconnection Microstructures in Silicone Elastomer
by Slavko Dejanovic

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Abstract

The subject of this thesis is a new chip to substrate interconnection technique using self-aligning elastic chip sockets. This work was focused on the technology steps which are necessary to fulfill in order to realize the suggested technique. Elastic chip sockets offer a solution for several assembly and packaging challenges, such a thermo-mechanical mismatch, effortless rework, environmental compatibility, high interconnection density, high frequency signal integrity, etc.

Two of the most challenging technology aspects, metallization and etching of the silicone elastomer were studied, but also, air bubble free casting of the silicone elastomer was taken into consideration.

Elastic chip sockets and single elastic micro-bump contacts of different shapes and sizes were manufactured and characterized.

The contact resistance measurements revealed that the elastic micro-bump contacts manufactured by using the developed methods require less than one tenth of the contact force to achieve the same low contact resistance as compared to commercial elastic interconnection structures.

The analysis and measurements of the high frequency properties of the elastic micro-bump structures have shown that they can operate up to several tens of GHz without a serious degradation of the signal quality.

The same methods were applied to manufacture very high density contact area array (approximately 80000 connections/cm^2), which until now was achieved only using so called chip-first techniques.

The low contact resistance, the absence of environmentally harmful materials, no need of soldering, easy rework as well as capability of very high interconnecting density and very high frequency compatibility, indicates a high potential of this technique for assembly and packaging.

Moreover, the presented technology of the silicone elastomer micromachining (metallization and RIE in particular) can be used for manufacturing of other microstructures, like chemical or biological micro reactors.

Keywords: silicone elastomer, packaging, assembly, elastic interconnection, chip socket, metallization, RIE of silicone elastomer, contact resistance, micro contact, high density interconnection.

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List of Appended Papers

1. **Sputter Deposing of Chromium, Gold and Copper on Silicone Elastomer**, Slavko Dejanovic, Hjalmar Hesselbom and Gunnar Norberg, submitted to *IEEE Transaction on Components and Packaging Technologies.*
2. **CF_4/O_2 versus SF_6/O_2 RIE of Silicone Elastomer – Characterization and Comparison**, Slavko Dejanovic, Hjalmar Hesselbom and Gunnar Norberg, submitted to *IEEE Transaction on Components and Packaging Technologies.* Editor in Chief rejected with suggestion to be combined with Paper 4.
3. **Metal Covered Elastic Micro-Bump Contacts as an Alternative to Commercial Elastic Interconnection Techniques**, Slavko Dejanovic, Gunnar Norberg, Hjalmar Hesselbom and Daniel Haglund, submitted to *IEEE Transaction on Components and Packaging Technologies*.
4. **Manufacturing of Via Holes in Silicon Elastomer**, Slavko Dejanovic, Gunnar Norberg, Rickard Olsson, and Hjalmar Hesselbom, submitted to *IEEE Transaction on Components and Packaging Technologies*. Accepted with major revisions. Suggested to be combined with Paper 2.
5. **Elastomer Chip Sockets for Reduced Thermal Mismatch Problems and Effortless Chip Replacement, Preliminary Investigations**, Gunnar Norberg, Slavko Dejanovic, and Hjalmar Hesselbom, *IEEE Transaction on Advanced Packaging.* Vol. 26, NO.1, February 2003.
6. **Very High Density Interconnect Elastomer Chip Sockets**, Gunnar Norberg, Slavko Dejanovic, and Hjalmar Hesselbom, accepted June 2005 for publication in *IEEE Transaction on Advanced Packaging*.
7. **High Frequency Signal Transmission Properties of Elastomer Chip Sockets**, Gunnar Norberg, Slavko Dejanovic, U. Persson and Hjalmar Hesselbom, submitted to *IEEE Transaction on Components and Packaging Technologies*. Accepted with major revisions.
8. **Solder and Adhesive Free Chip Assembly Using Elastic Chip Sockets: Concept, Manufacture and Preliminary Investigation**, Hjalmar Hesselbom, Gunnar Norberg, Slavko Dejanovic, and Daniel Haglund, *Asian Green Electronics Conference*, Jan 2004.
9. **Method for Making Micro/Nano-Liter Pools and Channels with Hydrophilic Bottom in Silicone Elastomer on Glass**, Slavko Dejanovic and Hjalmar Hesselbom, submitted to *IEEE Transactions on Biomedical Engineering.*

10. **Contact Resistance of Thin Film Metal Contacts,** Gunnar Norberg, Hjalmar Hesselbom, and Slavko Dejanovic, accepted Oct 2005 for publication in *IEEE Transaction on Components and Packaging Technologies*.

Acronyms

PDMS	Polydimethylsiloxane
MCM	Multi Chip Module
TAB	Tape Automated Bonding
I/O	Input/Output
WEEE	Waste Electrical and Electronic Equipment
JEDEC	Joint Electronic Device Engineering Council
JEIDA	Japanese Electronic Industry Development Association
EUELVD	European Unit End of Life Vehicles Directive
CSP	Chip Scale Package
PCB	Printed Circuit Board
LEGO	Large Exposure Gap Optics
RBS	Rutherford Back Scattering Spectroscopy
μBGA	Micro Ball Grid Array
RF	Radio Frequency
RIE	Reactive Ion Etch
HF	High Frequency
DC	Direct Current
FEM	Finite Element Method

1. Introduction

1.1. Background

Development of the electronics is driven mostly by the requirements on the reduction of size and weight and the increase of speed, functionality and signal frequency, but also, the reduction of waste pollution and reduced usage of environmentally harmful materials is becoming a strong demand from the market and authorities.

In order to make electronics which occupy less volume, is faster, can perform more per unit of time, volume and weight and consumes less power than its ancestors, it is necessary to make components smaller and faster. Fortunately, smaller components are, as rule of thumb, faster [1] and can handle signals at higher frequencies [2] and scaling down their physical dimensions provides electronic industry with a great opportunity to satisfy the growing technical (faster with larger functionality) and physical (less volume and weight and more mobility) requirements from the market. Also, due to reduced size, the quantity of used toxic and environmentally hostile materials can be reduced.

According to [3] and [4] the chip size increase is expected to level off and remain constant while the pin-count will continue to increase. This will require a finer on-chip and off-package pitch. In order to be able to handle components with finer pitch and higher interconnection density, tools and methods with appropriate precision have to be used or, if non-existent, developed.

The costs of assembly and packaging according to [3] and [4] are expected to decrease over the time on a cost per pin basis, but, the chip and package pin-count is expected to increase faster than cost per pin is decreasing. This will consequently not only increase absolute cost of assembly and packaging but even costs of substrate and system level packaging.

The off-chip frequency has been constantly increased and that trend seems to be continued ([3] and [4]) which will require new solutions with improved packaging signal integrity properties.

The different materials used in the same package have, as thumb of rule, different CTE (Coefficient of Thermal Expansion) which cause thermo-mechanical stress related problems and this has to be taken into consideration during the design process due to its influence on the reliability of the package.

In many market segments packaging technology is now a critically competitive factor, as it affects operating frequency, power, complexity, reliability and cost. The development of new component technologies, applications and environment issues are driving the requirements and innovation for assembly and packaging too.

A lot of research in the field of packaging were and are still conducted to meet the above mentioned requirements and trends. The previous more or less clear borders between semiconductor technology, packaging technology and system technologies are getting blurred and neither of these technologies should be developed without taking the other two into consideration.

The work presented in this thesis is one of the many intellectual and practical efforts around the world focused on finding packaging solutions which can satisfy the requirements stated above, i.e. offer:

- very high interconnection density, i.e. small pitch of high density area array interconnection,
- good HF properties, low latency and good signal integrity,
- good thermo-mechanical properties, i.e. good reliability,
- easy rework, i.e. cheep and fast rework with minimized risk to damage the chip or substrate,
- low load on the environment, i.e. non or limited use of environmentally harmful materials.

This thesis is organized in seven chapters. In section 1.2. after a brief overview of the tasks which packaging is intended to fulfill and the problems which it can introduce, the three dominating assembly and packaging techniques of today are described briefly with their advantages and shortcomings. Some of the alternative techniques are mentioned as well. Moreover, in order to give a more complete picture of the "packaging world" the environmental, rework and test concerns are shortly discussed. In section 1.2.7. the new chip-to-substrate assembly concept (Elastic Chip Socket) is introduced. The practical realization of that concept has been in focus in this work. Chapter 2 deals with the methods and materials which were used in this work for a practical realization of the suggested concept. In Chapter 3 measurements and results are presented and discussed. Chapter 4 describes achieved connecting densities with the techniques used in this work. The methods for micromachining of the silicone elastomer could be used in other fields of technology, thus, in Chapter 5, one possible use is presented. In Chapter 6 the future challenges are discussed and finally a summary and some conclusion remarks are given in Chapter 7.

1.2. Packaging

In order to meet and satisfy the technical and environmental requirements stated above several component and MCM (Multi Chip Module) packaging techniques were developed ([5] and [6]). Packaging usually includes assembly with bonding and sealing/encapsulation steps. Some of these steps can be conducted simultaneously like attachment and bonding in the case of flip chip or even skipped, e.g. if the passivation layer on the chip is considered capable to protect it from attacks from the environment where it will operate, sealing/encapsulation step could be unnecessary.

Generally speaking the package is intended to:

- provide mechanical support for the components,
- provide protection from the environment to the components,
- provide or house the interconnections from the component to other components (in the case of MCM) or the outer world,
- provide thermal path for cooling down the heat generating components,
- may provide confinement of electromagnetic fields to their desired configurations,
- may provide distribution of power and ground currents,
- may provide desired impedances at the signal terminals,
- may provide interface for testability.

But, the package can also significantly:

- introduce resistance to ground and power distribution,
- introduce degradation of signal quality and integrity,
- add weight and occupy space,
- introduce thermal resistance into cooling down paths,
- introduce mechanical stress to the components,
- constitute a source of contamination,
- increase price of the system.

The performance requirements put on packaging techniques include both adequate operational performance (electrical, mechanical and thermal) and long-term reliability under various environmental stress condition. There are also cost factors that include materials choices (plastic, ceramic, metal), design configurations (peripheral leads, array pins, array pads, array bumps) and environmental durability (low-cost non-hermetic and high-reliability hermetic). Design success is a careful balance between meeting customers' requirements for package and performance and achieving a cost that is affordable to the customer, yet provides the packaging manufacturer a reasonable profit.

An overall packaging procedure with advantages and disadvantages of specific techniques is considered in the following text.

1.2.1. Assembly

Single or MCM assembly includes the mechanical attachment and electrical interconnection of semiconductor devices, passives and mechanical components on the substrate. They can be conducted as separate operations e.g. as in the case of epoxy chip attach and wire bonding or some of them can be accomplished simultaneously, as in the flip chip assembly technique.

Attachment

The most common method for the chip assembly is attachment of the chip to the substrate with epoxy adhesives followed by subsequent wire bonding. This method has the advantage of needing no special processing of the chip and this increases the number of different kinds of devices that this technique is suitable for. Aside from epoxy other materials like polyimide, thermoplastics and metals are used. The polyimide is a high temperature stable polymer and is suitable when the assembly has to be exposed to the temperatures which exceed 350°C for e.g. subsequent assembly. The primary advantage of thermoplastics is the ability of reheating and removal of the device during e.g. rework operation. Solder chip attach methods provide good thermal conductivity and thus cooling of the devices but requires the appropriate back side metallization in order to secure good solderability.

Chip Interconnect

The three dominant chip interconnect methods are wire bonding, TAB (Tape Automated Bonding) and flip chip [5].

Historically, wire bonding was the first chip interconnect technique that was widely adopted by the electronic industry, and it still is continuing to be the dominant method for making the electrical connection between the contact pads on the top of the semiconductor and the MCM or package substrate metallization or the leads in the package. In the wire bonding process, the wire is brought into contact with the metallized contact pad. The wire and the contact pad metallization are deformed, producing a shearing action at the interface - some times enhanced by applying ultra sonic relative motion. The shearing action removes contaminants from the wire and the contact pad. When sufficient cleaning has occurred the metallurgical bonding is initiated between the wire and the contact pad.

The limitations of wire bonding are parasitic inductance of the wire, the requirement for perimeter pads on the chip, and the slow, sequential nature of the process. The parasitic inductance of wires can limit the performance of high-speed electronics. The wire inductance on power and ground pins contributes to switching noise. Integrated circuit designs are becoming limited by the number of perimeter I/Os. The rapid reduction of wire bonding pitch will cause the reduction in wire diameter, the capillary of the bonding equipment and affect solutions for wire sweep, signal integrity and contact pad design, all which will require significant materials improvement and material process innovation beyond which are available today.

Another bonding technique that was developed in the mid-1960s is TAB. First Au bumps have to be made onto the chips. This is accomplished before the chips are separated by first sputter depositing an adhesion and diffusion barrier layer using a Ti/W mixture onto the wafer. Next a thin Au seed layer is sputtered after which a thick resist is deposited. Holes for the bumps are generated by photolithographic methods and the bumps are electro plated. The photo-resist is dissolved and the thin Au and Ti/W layers are removed and the wafer diced. The chips are then bonded to a polymer tape containing a Cu lead pattern, and once bonded, the chip can be automatically handled in a tape-and-reel format. Probe pads can also be patterned in the Cu leads to allow test and burn-in of the chip prior to assembly. That is the primary advantage of TAB. The TAB tape, while expensive, can be designed with a ground plane, or as multilayer, to provide controlled characteristic impedance or can be designed to access an area array of contact pads.

The disadvantages of TAB include the need for the pre-bumped chip, the need to custom design a tape for each chip and the need to redesign for chip-shrink. The limited availability of bumped chip has severely limited the use of TAB.

Flip chip technology was first introduced by IBM in 1964 and is based on direct bonding of pre-bumped chip, similar as for TAB, but using solder ball bumps instead, and when it is flipped down attaching it directly on to the substrate [5]. The short length of the solder bump has a minimal parasitic inductance and capacitance, and the area array connections can improve electrical performance and meet the need for the ever increasing number of I/Os. However, the pad pitch on the substrate has to be the same as that on the chip, limiting the availability of suitable substrates.

Although flip chip technique from the point of view of signal integrity properties is superior to wire bonding and TAB, there are some serious problems. One particular problem when using solder based flip chip methods is the thermal expansion mismatch between the silicon chips and conventional substrates, leading to thermo mechanical stress related fatigue in the peripheral solder balls, the more so the smaller the balls, the larger the chip and the wider the temperature excursions. This can be partially resolved by using under-fills, but this increases the difficulties associated with the chip replacement. The reliability of flip chip on board technologies has been studied among others in [7], [8] and [9].

Other Types of Chip Interconnect

Aside from the above mentioned chip interconnect methods, there are e.g. techniques which use isotropic and anisotropic conductive adhesives.

One example is the technique which uses the epoxy resin loaded with the dielectric coated silver particles. The chip is gold-bumped prior to the assembly. Assembly is done by alignment and pressing the chip down to the substrate. The pressure raptures the dielectric coating on the particles, which are between the bump and substrate pad, providing a gold bump-to-silver particle-to-substrate pad electrical path. Particles between the pads are not exposed to the high pressure and the insulating coating remains intact preventing the electrical contact in the lateral direction. Finally, the epoxy adhesive is cured and the electrical paths are preserved on the desired places.

Anisotropic conductive films can be used to assembly the chip without the bumps. The films are made by loading polymers by conductive particles below the limit where it becomes conductive. The adhesive film is designed to have distributed conductive particles which are suspended in the polymer matrix. During the assembly process the chip is pressed down to the substrate and the electrical contact is achieved in the vertical direction, but due to there is no pressure in the lateral direction and larger separations between the pads than the distance to the substrate, the contact between the conductive particles is not established, and thus the desired electrical path between the chip contact pad and the substrate contact pad has been isolated from those adjacent.

There are also compliant interconnection techniques which use metal particle filled elastomers for making conductive elastic bumps. Here, the electrical contact is achieved when the micro-bumps are compressed and the metal-particles have come into close contact, both to each other and the contact pads on the chip and the substrate.

Previously mentioned metal-particle loaded polymer based interconnection techniques are suffering of the serious reliability problems if the chip contact pads are made of the aluminum, which still is very present in the electronic industry. Aluminum has tenacious native oxide which forms rapidly at room temperature. It is insulating and has to be removed or penetrated in order to establish electric contact. To avoid the aluminum oxide to form again it is necessary to prevent the oxygen to come in to the contact with aluminum surface which is not easy. Even if the initial electrical contact is achieved, the polymers do not provide a hermetic seal, and the aluminum oxide will form over the time causing worsening and even loss of the electrical contact. These reliability problems can be evaded if the contact pads on the chip and substrate are made of gold, because gold does not oxidize.

Also, there is a diversity of other suggested techniques which relies on e.g. use of elastic membranes provided with suitably placed conductive bumps or use of nonconductive adhesives in combination with mechanical gold stud bums etc.

1.2.2. Encapsulation and Sealing

After the device is assembled, it is usually mechanically and environmentally protected. That is done by encapsulation or sealing. Encapsulation provides an economical way to protect devices by isolating them from environmental pollutants, and at the same time it offers mechanical protection by structural coupling of the device to the constituent packaging materials into a robust package.

The protection can be an organic overcoat, in which case it is called encapsulation, or inorganic in which case it is called sealing. Organic over-coatings are cheap but neither permanent nor hermetic in contrast to e.g. glass sealing which is permanent and hermetic but an expensive method.

1.2.3. Chip-First Technique

Previously mentioned techniques are also called chip-last methods. That is the substrate is completely manufactured with its signal and power/ground layers and the chip(s) is attached as the last part of the assembly.

However, there is the so called chip-first technique where the chip is first attached onto the bare support substrate, or sometimes, substrate that contains power and/or ground layers, with the chip contact pads up. The layers of organic dielectric with metal signal and power/ground patterns are built above the top of the chip. Electrical contact between the chip and the signal or power/ground patterns is achieved by making via holes in the dielectric layers. The via holes can be made by e.g. using photolithographic methods which can provide interconnection with the same density as the contact pad density on top of the chip.

The chip-firs technique turned out to be extremely robust when it is exposed to thermal and mechanical shock and stress, because the chip is completely encapsulated by the support substrate and the subsequently built covering layers of dielectric and metal layers. This solution, however, implies the disadvantage of not enabling chip replacement without total rework.

The chip-first technique has electrical properties as good as or even better than flip chip attachment methods.

1.2.4. Environmental Concerns

Because of the mining technologies and the use of toxic materials, the mining and manufacture of raw materials used in the electronic industry, as well as the materials themselves, are sources of environmental pollution, and they can be a potential health hazard. Also, the electronic industry, itself, uses a diversity of poisonous materials which very often ends up in the electronic equipment (e.g. lead, mercury, cadmium, flame retardants etc.) or land on the scrap-heap as technological by-products.

The steady expansion of the diversity of application fields have resulted in a massive consumption of electronics. Small, low-weight, mobile and cheap electronic equipment have become more and less confection – buy it, wear it out and waste it. The scrap-heaps containing so called E-Waste is growing and is considered as a more and more significant load on the environment and constitute a risk for human health.

In order to protect the environment from the electronic pollution the European Union issued: “The Directive on Waste Electrical and Electronic Equipment” (WEEE) (expected to be in effect as of August 13, 2005) which regulates manufacturers’ responsibility for E-Waste, and the “Directive on the restriction of the use of certain hazardous substances in electrical and electronic equipment”. That will, after July 1, 2006, restrict the use of materials such as Pb, Cd, hexavalent Cr, Hg, and polybrominated diphenyl ethers. Similar directives were suggested by other councils and associations like JEDEC (Joint Electronic Device Engineering Council), JEIDA (Japanese

Electronic Industry Development Association) and EUELVD (EU End of Life Vehicles Directive) ([10], [11] and [13]).

Such directives put requirements on electronic industry to find new materials and technologies which can cost-effectively substitute those banned ([10], [16] and [17]). Of course, packaging is also affected both concerning choice of materials and methods. For example, BGA, flip chip etc. technology will not be allowed to use lead in solder balls. Various lead-free compositions have been put forward; Sn/Ag, Sn/Ag/Cu, Sn/Bi, as replacement for lead but they also result in worsened wetting, raised reflow temperature, enlarged thermal shock etc. ([12], [13], [14], [15], [18] and [19]). Moreover, the potential threats to the environment from these, in some cases so far not much used materials, is unclear.

1.2.5. Rework Concerns

All of those techniques mentioned above (see 1.2) are suffering from severe problems when rework is needed [5]. That operation is costly, time consuming, can be harmful for the chip, the substrate or the socket, and the final result is usually uncertain.

1.2.6. Test Concerns

Regardless of which interconnection technique is used, knowing that the semiconductor chip that is to be assembled is good (is a so called Known Good Die - KGD) is of crucial importance. Assembling a bad or faulty chip usually leads to the loss of an entire module since the rework of the module is difficult, costly and often even impossible. Thus several methods for testing chip on wafer were suggested and developed [5]. They can be sorted in two main groups. The first is pressure contacts, i.e. miniaturized probes, chip sockets, or temporary carriers that employ a variety of contacting interfaces including metal alloy bumps, membrane contact, conductive films or conductive adhesives. The second is metallurgical connections, e.g. solder, thermo-compression, thermo-sonic, electrochemical, or welded low-impedance connections in a wide variety of forms including bumped chip, TAB, bonded chip carriers, CSP (Chip Scale Packages) etc [5].

Most of already existing techniques for chip test are fitted to measuring instruments using relatively long cables. When operational frequency is high, particularly in the micro-wave region, losses and dispersion will be more severe the higher the frequency. Likewise, the differences in physical length of cables, and thus the signal paths, are of very high importance. Unwanted difference in signal path length can introduce phase error and jeopardize entire tests and diagnostics. To avoid these problems it is recommended to move the test circuitry as close as possible to the test object.

1.2.7. Concept of Elastic Chip Sockets

The new concept of elastic chip sockets invented by Hjalmar Hesselbom et al. [20] is aiming to offer a packaging technique with good HF properties, significantly reduced thermal expansion mismatch related fatigue problems, and to relax the requirements on having the high precision chip placement equipment. If the chip has turned out not to be functional, its replacement will be essentially effortless when this concept is used.

Figure 1 shows a cross-section of the elastic chip socked as intended in actual use.

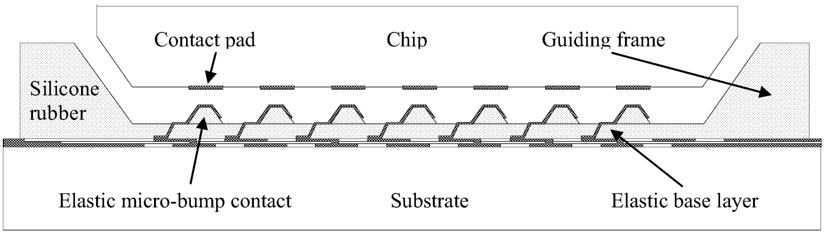


Figure 1 Cross section of intended elastic chip socket and chip under placement.

The sockets are intended to have an array of Au-metallized elastic micro-bump contacts, which corresponds to the array of chip contact pads, and an elastic guiding frame which will assist an easy and accurate chip placement. They should be made by precision casting of silicone elastomer in micro machined silicon molds. The sockets are subsequently Au-metallized and then metal patterned. The elasticity of silicone elastomer would comply with any reasonable CTE mismatch without severe strain while the Au to Au contact, which is a good electrical contact, requires no solder or adhesive, only that force is applied to the back of the chip to keep it in place. This pressure would be applied via some kind of spring-loaded heat sink.

If replacement of the chip is needed, then the spring-loaded heat sink could be easy removed, the chip replaced with new one and the spring-loaded heat sink put back.

The signal path from the chip down to the substrate should be established by making via holes through the thin elastic base layer. That will diminish parasitic inductances and capacitances and prevent degradation of the signal.

The elastic chip sockets are made from silicone elastomer and Au and thus could be considered to be environmentally friendly. There is, however, also some infinitesimal amount (~1 nm) of Cr or Ti serving as metal adhesive layers.

The author of this thesis and his co-workers intended to practically realise the above suggested concept. They were put in front of challenges related to especially metallization and micromachining of the silicone elastomer. The four most important manufacture steps which were recognized are: casting of the body of the elastic chip sockets, alternatively the single micro-bumps, metallization of the surface of the elastic microstructures, Au patterning and control of the characteristic impedance and making via holes down to the substrate. The methods and recipes for particular steps were treated and suggested in the Appended Papers.

2. Manufacture of Elastic Interconnection Structures

A successful manufacture of good elastic chip sockets requires skills of:

- controlled casting of the silicone elastomer, i.e. air bubble free body of elastic micro-bumps and underlying elastic base layer. For the case when the structure has to operate at very high frequencies (tens of GHz) and when the electric lines are patterned on the underlying elastic base layer it has to be of predefined thickness in order to avoid degradation of the signal quality due to mismatch in the characteristic impedance. This is an additional requirement which casting operation has to satisfy.
- metal deposition with good coverage of sharp corners and steep surfaces with good adhesion to the silicone elastomer,
- making via holes through the silicone elastomer layer in order to reach substrate and electric lines on it,
- well defined patterning of the electric lines conducted over a topography of several tens of µm.

This chapter deals with manufacturing process flow and technologies that were applied for making a single micro-bump contact as well as for manufacture of the elastic chip sockets.

A coarse overview of the manufacturing process flow is shown in Figure 2. The first step in the manufacturing process (Figure 2 a)) is design and fabrication of the mold followed by design, manufacture and alignment of the substrate to be followed by casting of the silicone elastomer (Figure 2 b)). After completed cure of the silicone elastomer the structure is separated from the mold and the RIE mask is deposited and patterned (Figure 2 c)), followed by RIE of the silicone elastomer, mask strip, Au deposition and the final patterning of electrical lines (Figure 2 d)).

Those sub-steps which required special technology recipes were developed during this work, and the most important of them, are presented in more detailed separate papers (appended to this thesis) submitted to science magazines. When needed they are referred to in this text.

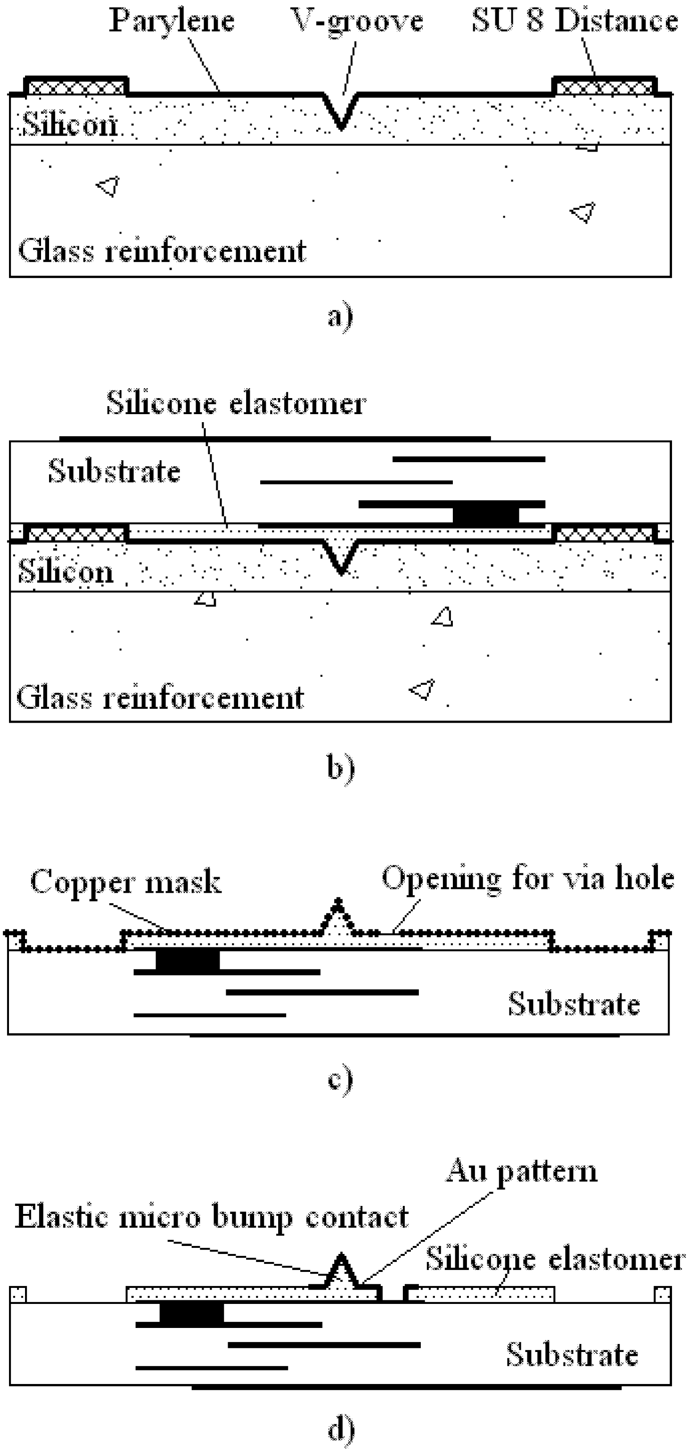

Parylene
V-groove
SU 8 Distance
Silicon
Glass reinforcement
a)
Silicone elastomer
Substrate
Silicon
Glass reinforcement
b)
Copper mask
Opening for via hole
Substrate
c)
Au pattern
Elastic micro bump contact
Silicone elastomer
Substrate
d)

Figure 2 Manufacturing flow for making elastic micro-bump contact as well the entire elastic chip sockets.

2.1. Materials and Methods

2.1.1. Requirements on and Selection of Materials

In order to fulfill their particular tasks the decision was to use the following materials:

- mono-crystalline silicon wafer can be anisotropically etched exactly along the crystalline planes [21] opening the possibility of making molds with precisely predefined size of the cavities for the future elastic micro-bumps and trenches for the future elastic guiding structure for assistance during the self-alignment of the chip. Silicon wafers with crystal orientation <100> were chosen for the purposes of the manufacture of the molds. The same was suggested also by the concept presented by P. Bodö, H. Hesselbom and H. Hentzell [20],
- the body of the elastic chip sockets and elastic micro-bump contacts has to be elastic, geometrically well defined, without any voids in it and made of dielectric material. The elastic material of which the elastic chip sockets as well as single elastic micro-bump contacts have to be made (cast) must have following physical and electrical properties:
  - ✓ its wettability must bee so good that it can fill cavities of the size of µm (see Figure 3) and its viscosity has to be such, that it can flow at sufficiently low speed that air has enough time to escape, preventing trapping air bubbles especially in the v-grooves intended for casting of elastic micro-bumps,
  - ✓ its curing must be anaerobic and without any gases or vapors developed during curing (see 2.2.4.),
  - ✓ after curing the material must be of such firmness that it can secure sufficient contact force which can guarantee good electrical contact between the chip contact pad and the elastic micro-bump contact,
  - ✓ be a good dielectric.

  The material which was believed to bee capable to fulfill these requirements is the silicone elastomer Sylgard® 184 (Dow Corning).
- for the prevention of sticking of the silicone elastomer to the mold, a thin film of a release agent is to be conformally deposited on the mold,
- in order to prevent degradation of the electrical properties, i.e. increase of the contact resistance due to oxidation of the metal, Au, as a good conductor and noble metal, was selected to be deposited for metallization of elastic micro-bumps. Also, knowing that the elastic-micro bumps will be deflected when pressed into physical contact with the contact pads on the chip, and that Au is plastic, i.e. a ductile metal, it is particularly suitable for the issues of metallization and patterning of the elastic micro-bump contact. The metal layer for the signal,

power and ground traces, on the top of the silicone elastomer layer, and the via holes should be deposited and patterned at the same time as the elastic micro-bump contacts. Thus Au was the obvious selection for these issues.

- after evaluation of several techniques it was established that CF_4/O_2 plasma is suitable to etch the silicone elastomer (see **Paper 2** and **Paper 4**),
- because Cu can withstand CF_4/O_2 plasma, a thin Cu film could be and was used as a RIE (Reactive Ion Etch) mask (see **Paper 2** and **Paper 4**),
- for the issue of metal patterning over large topographies, which is the case for elastic chip sockets and elastic micro-bump contacts, an electroplated photo-resist had to be used (see 2.5).

2.1.2. Selection of Methods and Equipment

The following methods and equipment were used:

- casting of the silicone elastomer had to be done either by injecting it through a hole in the center of the substrate or pouring it into the mold (see 2.2.4.),
- due to availability of the equipment in this work, deposition of the metal was conducted by sputtering in a Von Arden S730CS sputtering/etching cluster system (see 2.3),
- opening of via holes was carried out by RIE in a Von Arden S730CS sputtering/etching cluster system (see 2.4),
- in order to get good and accurate definition of the metal lines the exposure of the photo-resist had to be conducted using an exposure system with highly collimated light. In this work mask aligner with LEGO (Large Exposure Gap Optics), MA 6, manufactured by Karl Süss was used (see 2.5).

2.2. Manufacture of the Elastic Structures

The easiest way to get the silicone elastomer to assume some particular shape is to cast it in the suitable mold. Due to silicon’s crystal lattice of diamond type, by using proper etchants, it is possible to anisotropically etch pyramid-shaped cavities and strait grooves along its crystallographic planes ([21] and [22]) with high precision. Such cavities and grooves can be used as molds for casting entire self-aligning elastic chip sockets.

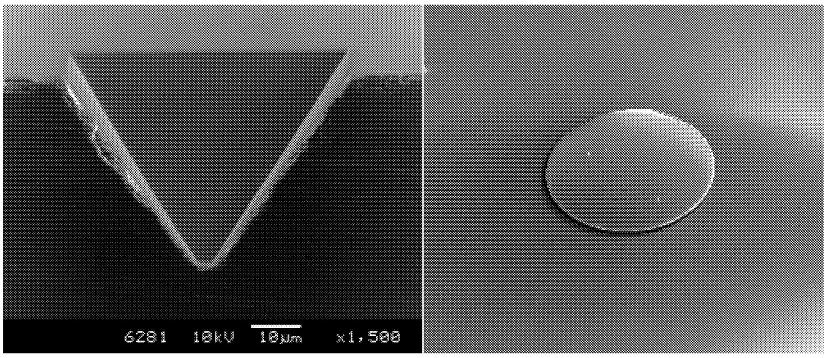
The elastic chip sockets are cast on the substrate or the PCB (Printed Circuit Board). That means that the silicone elastomer or other suitable substance is placed between the mold on one side and the substrate or the board on the other side. The two component silicone elastomer cross-linking (addition type) occurs through the entire volume simultaneously and anaerobically without generating waste products ([23] and [24]) which can be a source of forming unwanted voids like gas bubbles or uncured regions.

Sylgard® 184 (Dow Corning) is one of the silicone elastomers which belong this group.

The silicone elastomers stick quite well to metals and rough surfaces. In order to prevent its adhesion to the mold, especially to the bottom of the cavities which can be rough, a release agent is deposited. In order to maintain the shape of the mold the release agent has to cover it conformally.

2.2.1. Manufacture of Mold

The molds used for casting silicone elastomer were <100> Si wafers anisotropically etched in hot KOH with SiO_2 as a mask that was previously made using conventional photolithographic methods (see **Paper 3, Paper 5** and **Paper 6**). Because KOH etches Si anisotropically [22], and the photo mask was properly oriented, the mold contained v-grooves defined by <111> crystalline planes. Small, pyramid-like v-grooves were etched at the positions where the elastic-micro bumps were intended to be and long, wide and deep, v-trenches were etched where the guiding elastic structures were intended to be. Figure 3 a) shows a SEM (Scanning Electron Microscope) image of the cross section of one v-groove intended for casting of an elastic micro-bump.



a) b)

Figure 3 a) SEM image of v-grove in Si wafer etched in KOH solution intended for casting elastic micro-bump, b) SEM image of SU 8 stand-off.

2.2.2. Thickness Control

In order to be able to control the thickness of the underlying elastic base layer, a group of relatively large diameter columns were made at suitable positions on the surface of the mold. Their function was to keep the substrate at proper distance from the surface of the mold during casting and curing of the silicone elastomer. These columns were made of SU 8 photo-resist using conventional photolithographic methods. Figure 3 b) shows a SEM image of one SU 8 stand-off.

2.2.3. Sticking Problem

As a release agent a 5 µm thick Parylene layer was deposited over the mold. Parylene is especially suitable for these purposes because the process of coating with Parylene results in a conformal layer over the entire mold and thus the original shape will not be disturbed. Although the Parylene layer is quite conformal, there still appeared small particles created during the Parylene deposition process (see Figure 5). This was probably due to non-optimized process parameters.

2.2.4. Casting and Curing of the Silicone Elastomer

The silicone elastomer that was chosen was Sylgard® 184 manufactured by Dow Corning. It was assumed to have quite good mechanical and electrical properties [25]. Its wettability and viscosity are such that it can fill very small cavities and sufficiently slow that air has enough time to escape from them, and thus trapping of gas (air) bubbles was diminished.

The silicone elastomer was mixed according to recommendations obtained from Dow Corning. During mixing of Part A and Part B of silicone elastomer it is hardly possible not to introduce any air bubbles into the mixture (except if it is done in vacuum).That unwanted air content was easy to remove by placing the silicone elastomer mixture in a vacuum chamber and pumping out the air. Some occasional rising of the pressure to one atmosphere is recommended and speeds up the degassing process.

The casting operation was conducted by injecting the degassed silicone elastomer mixture through the hole drilled in the center of the circular 4 inch milled substrate (see Figure 4) or by simply pouring the silicone elastomer onto the mold followed by careful placement of the substrate and pressing it down (see **Paper 3** and **Paper 5**).

By injecting the silicone elastomer through the hole in the center of the substrate the thickness of the underlying elastic base layer will be exactly as the height of the SU 8 stand-offs, i.e. well defined.

During the casting and curing (for one week at room temperature) of the silicone elastomer, it was necessary to put a couple of kilograms weight on top of the substrate, to prevent it from lifting, especially during injection of the silicone elastomer mixture. After finished cure of the silicone elastomer, the weight was removed and the mold was separated from silicone elastomer by inserting e.g. knife blade. Figure 5 a) shows image of a cast and cured elastic micro-bump

If the silicone elastomer was poured into the mold, the thickness of the elastic base layer depended on its viscosity, the applied weight, dimensions of the substrate and SU8 stand-offs etc., and was not easily controlled. The risk of getting air bubbles trapped between the substrate and the mold was also considerably increased.

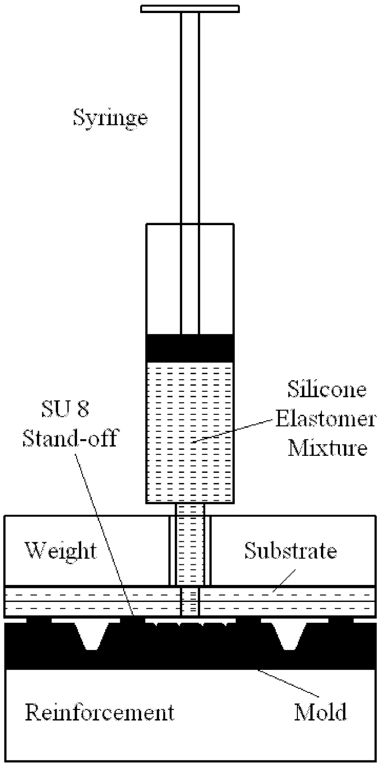
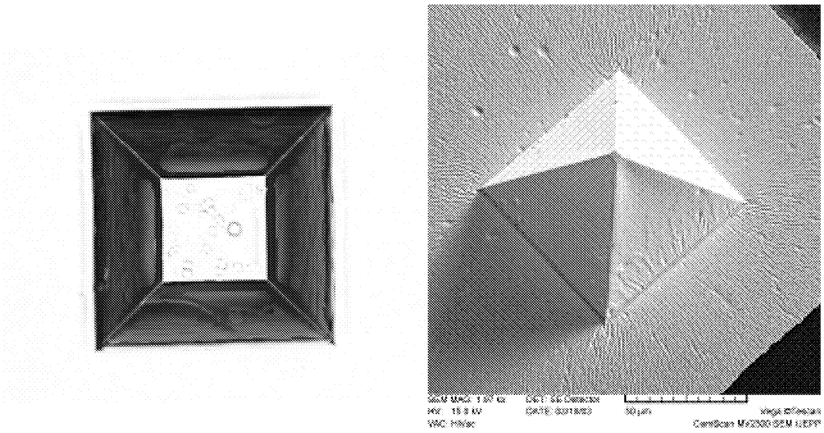

Syringe
Silicone
Elastomer
Mixture
SU 8
Stand-off
Weight
Substrate
Reinforcement
Mold

Figure 4 Principle for casting of the elastic micro-bumps.



a) b)

Figure 5 a) Image of one typical elastic micro-bump after separation from the mold; obtained by optical microscope, and b) metallized (and patterned) elastic micro-bump.

Due to that, especially, silicone oil (Part B) is easily spread around and difficult to remove from contaminated surfaces, the molding operation should be conducted in separate room from that where e.g. the semiconductors are made.

2.3. Metallization of Elastic Structures

As explained in 2.1.1. Au is the suitable metal for contacts and serves well as signal and power/ground traces on the silicone elastomer. Cu is suitable for making the RIE mask. The metal deposition was carried out by using the sputtering equipment Von Ardenne CS730S. Sputter deposition on the silicone elastomer is not trivial task. The deposition rate is dependent on the process gas pressure, applied RF (Radio Frequency) or DC (Direct Current) power, system geometry etc. It is known that Au does not have a good affinity to other materials, so it is necessary to deposit an adhesion layer on the surface of the silicone elastomer prior to depositing the Au layer. During this work the metallization of the silicone elastomer was comprehensively studied and it was, among other things, established that Cr is suitable as adhesion layer (see **Paper 1**). A successfully conducted metallization of the silicone elastomer is of vital importance both for patterning of the electric lines and the RIE mask for making via holes. In **Paper 1** a recipe for sputter deposition of Cr, Au and Cu is suggested. In that paper the metallization was assumed as good if the metal layer was smooth and adhered well to the entire surface of the silicone elastomer. To achieve such a result with sufficiently thick metal layers, several hours will be spent, which is not realistic to expect that the industry will accept in a large-scale production. But if that request is relaxed a little bit, i.e. a reasonable small amount of wrinkle formation is tolerated, a good metal layer will be deposited much faster.

Figure 5 b) shows a SEM image of a successfully metallized elastic micro-bump. There is still some wrinkle formation at the sharp corners at the bottom of the elastic micro-bumps but they can be ignored.

2.4. Via Hole

It is very likely that the substrate will not act only as the carrier but also as a multi-layer PCB in the concept described in [20]. According to [3] package pin count for single chip packages for high performance applications will reach 8450 year 2018. Such large number of terminals is not possible to route and fan out from the chip without having via holes through silicone elastomer down to the substrate where that amount of fan out is feasible using several layers.

Because making via hole is an absolute imperative for implementation of the concept [20], punching, mechanical drilling, laser drilling and RIE were considered in this work and the results are presented in **Paper 4**.

2.4.1. RIE of Via Holes

RIE is the technique that was found to be suitable for making via holes in the silicone elastomer. RIE of the silicone elastomer as such is treated in **Paper 2** where different gas mixtures were tried and their etch rates characterized.

The procedure for making vial holes is the following:

- ***making Cu mask***

Cu is suitable for making etch masks for CF_4/O_2 plasma (see **Paper 2**, **Paper 4**), and thus it was sputter deposited over the silicone elastomer to a thickness of approximately 1μm. Opening in the Cu mask was made by conventional photolithographic methods (see **Paper 4**).

- ***RIE of silicone elastomer***

A relatively good anisotropy of the RIE process was observed. When via holes were etched their final diameter was established to be larger than the initial one of the RIE mask. RIE in the lateral direction is one reason, but also the erosion of RIE mask, i.e. the gradual expansion of the holes in the RIE mask can contribute to the via holes expansion (see **Paper 4**). That slow but steady erosion of the RIE mask can be advantageous for obtaining a preferable slope of the sidewalls (as those shown in Figure 6 b)) and thus improved metallization coverage. The surface of the etched silicone elastomer is rough and can be a serious problem concerning yield and reliability of metallization of the via holes. This problem is discussed in 6.3.

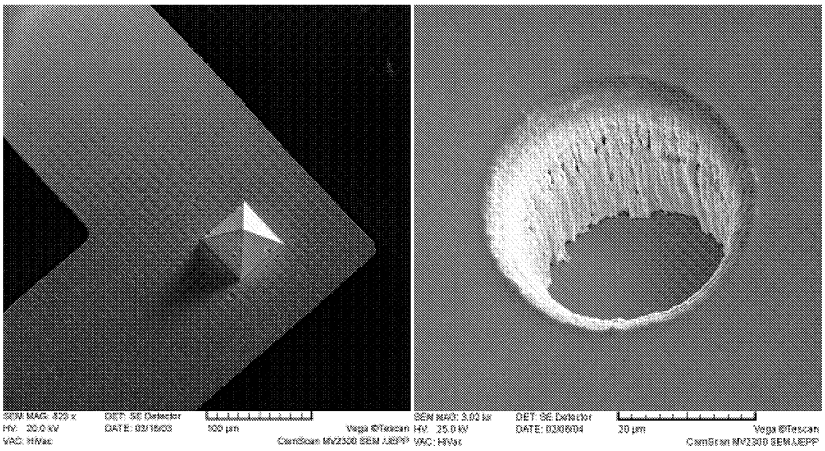
- ***removal of etch residues***

During this process there are etch residues created both on the sidewalls and bottoms of the via holes. The etch residues constitute problems during subsequent metal deposition. They are loose and a deposited metal layer on top of the residues will detach easily. It was found that most of them are easy to wash away in water, especially when an ultrasonic bath is used. Despite that the ultrasonic bath is quite efficient, some etch residues will always remain both on the sidewalls and at the bottom. They are not easily removed and those at the bottom are a serious problem due to their obstruction of good electrical contact between the pads on the substrate and subsequently deposited final Au layer. In order to remove the etch residues from the bottom it is recommend to first deposit one thin layer of Au and then a layer of Cu on the top of the metal layer on the substrate prior to metal patterning and subsequent cast and cure of silicone elastomer. After washing away loose etch residues, that Cu layer can be etched away, by using suitable Cu wet etch chemicals, and thus lift-off the remaining etch residues from the bottom. The Cu layer works as etch stop for RIE and the Au layer works as the etch stop for Cu etch. The result is a clean Au surface at the bottom of via hole as in Figure 6 b).

2.5. Patterning

Due to that the mold is manufactured by antistrophic etch of mono - crystalline Si the position and the tilt of the sidewalls of the cavities in the Si wafer are strongly defined by the position of <111> crystalline planes [22]. This cause the corners of the elastic micro-bumps to be very sharp both before and after the metallization step and thus the deposition of conventional photo-resist by spinning is not suitable as sharp corners of the elastic micro-bumps will cut through it and the corners will not be covered. The solution to this problem is electroplating of photo resist. This was done using PEPR® 2400 (SHIPLEY) photo-resist (see e.g. **Paper 3** and **Paper 5**). For ultra violet light exposure of the photo-resist a very low divergence light, Karl Süss MA6 mask aligner with LEGO optics was used.

After development of the photo-resist the Au layer was wet etched. A subsequent Cr wet etch had to be applied too, in order to ensure that the very tin Cr layer was removed from the surface of the silicone elastomer. The typical result is shown in Figure 6 a).



a) b)

Figure 6 a) Patterned elastic micro-bump contact (its basis 40X40 µm) with associated micro strip line and b) successfully etched, metallized and patterned (pad perimeter outside picture) via hole.

Metallization of via holes is a much more uncertain business. Probably, due to uneven erosion of the etch mask, non-uniformity of the bulk of the silicone elastomer and remaining etch residues, the sidewalls are quite rough. Furthermore, the sidewalls are quite steep especially near to the bottom (see Figure 6 b)). It is also known that the thickness of sputter deposited metal layers on sidewalls and bottoms of steep via holes is considerably less compared to the metal deposited on the top surface [26]. These facts give us reason to believe that metal layers down through the via holes are quite thin and uneven. Some vortices on sidewalls can cause shadowing effect for sputter deposition and thus further reduce or even totally prevent deposition below them. Even in this case of patterning of metal in via holes, an electroplated photo resists is necessary to secure good coverage of via holes. It is naturally the case that patterning elastic micro-bump contacts and associated via holes will occur simultaneously so the same photo-resist could be used. Despite all obstacles stated above, via holes were made and one successfully metallized and patterned via hole is shown in Figure 6 b).

3. Characterization of Processes and Elastic Interconnection Structures

In this chapter the characterization techniques which were used during this work are briefly listed. Measurements of the metal thickness were performed both by using RBS (Rutherford Back Scattering) method and a stylus profiler. The RIE rate was also measured with a stylus profiler. The characterization of the contact resistance was mostly focused on the measurements on one single elastic micro-bump contact. Daisy chain resistance measurements for entire elastic sockets was also conducted, and reported in **Paper 5** and **Paper 6**.

Visual inspection was done by using optical and scanning electron microscopes.

3.1. Metal Thickness Measurements

The metal thickness measurements were carried out after a good result of the metallization was reached, i.e. after a good adhesion was established by using tape-pull method and achieved sufficiently good smoothness of the surface. The main goal with these measurements was to estimate for how long period of time it is necessary to deposit, first of all Au, in order to achieve desired thickness of the metal lines, but also to estimate the thickness of the Cr layer which is sufficient to secure good adhesion but will not crack during and after the metallization process.

3.1.1. Chromium Thickness Measurement

Cr thickness measurement was conducted by the RBS method. In order to be able to receive large enough signal (number of counts) originating from Cr layer, it is necessary that Cr layer is either uncovered, or that the subsequently deposited Au layer is thin enough, to prevent that Cr signal will be disguised by the Au signal and noise. Therefore, silicone elastomer was spun and cured on a wafer and then Cr was sputter deposited with the same process parameters as when good metallization result is achieved, and in order to prevent the oxidation of the Cr layer Au was deposed with the same process parameters as for good metallization, but only for roughly 15 s (see **Paper 3**). The RBS spectrum was recorded from the Tandem accelerator at the Ångström Laboratory of Uppsala University and fed into the software SimNRA v5.01. This software is intended for simulation and analysis of RBS spectra received from different materials, their compounds and different number of layers and combinations of them for arbitrary energy, incident, exit and scattering angle of ion beam etc. By choosing the same calibration data, ion energy, angles etc. as they were during measurements in the accelerator and simulating a sample with the same material composition as the examined sample the simulated RBS spectra was fitted to the spectra received from the accelerator. Figure 7 shows SimNRA fitted spectra. Thickness t' of Cr layer received from SimNRA is expressed in 10^{15} atoms per cm^2 and has to be converted to actual thickness by applying the formula $\text{thickness} = \frac{t'M}{N_{\text{Avogadro}}\rho}$ where M is relative atomic mass of Cr and ρ is mass density. From the matched spectra it was calculated that Cr layer was approximately 1 nm thick.

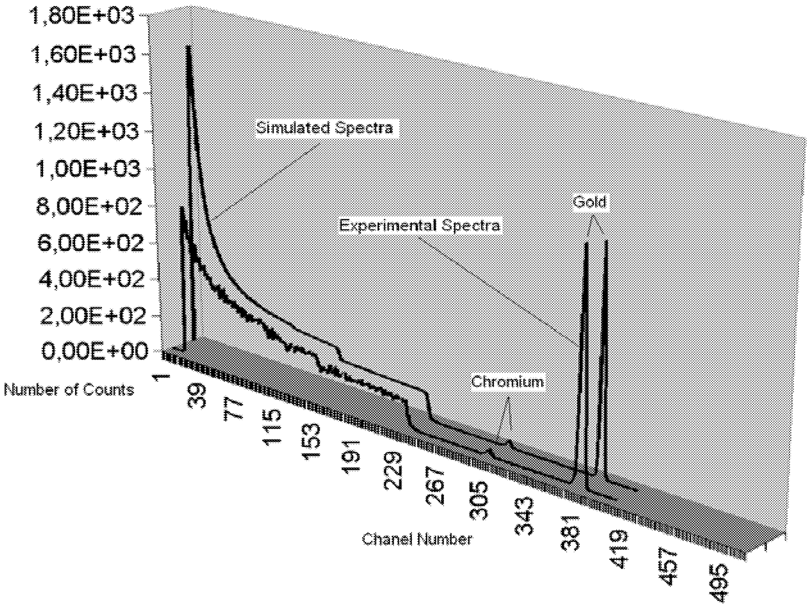


Figure 7 3D view of plots of RBS energy spectra received from accelerator and achieved by running SimNRA software.

3.1.2. Gold Thickness Measurement

Au was sputter deposited over a wafer using the “good” parameters, and by using the profiler DEKTAK V200 Si, the deposition rate was estimated to be approximately 1 μm/h (see **Paper 6**).

3.2. RIE Rate

One of the most important issues in the realization of the elastic chip sockets is efficient and controlled removal of the silicone elastomer in order to make the via holes. In this work the RIE technique was recognized as suitable and thus much effort was spent to find the optimum recipe which will give maximum etch rate. These measurements were conducted with stylus profiler Dektak 6M. Figure 8 shows a comparison between etch rate for different fractions of O_2 in CF_2/O_2 and SF_6/O_2 plasmas. RIE of the silicone elastomer is studied and presented in **Paper 2**.

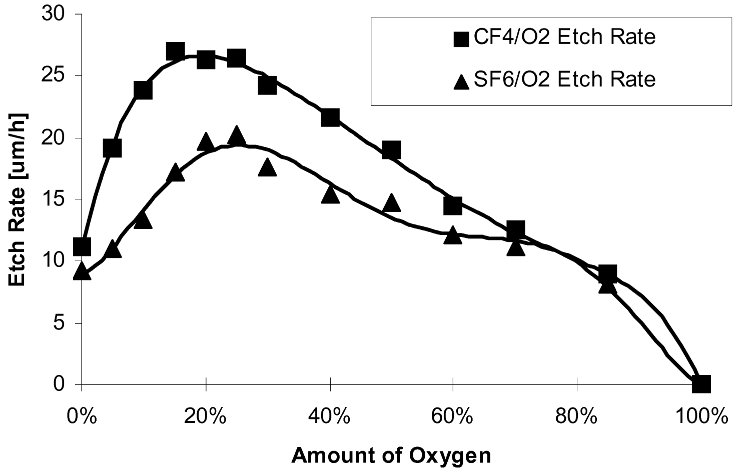


Figure 8 RIE rate as function of amount of oxygen in the gas mixture.

3.3. Contact Resistance

A mechanical force has to be applied to press the chip onto the elastic micro-bump contacts or into the elastic chip socket in order to create physical contact and thus establish an Au to Au electrical contact as well. Contact between the elastic micro-bump contact and the chip can be achieved in the three following ways:

- by applying constant mechanical force. This method is very dependent on deflection and creep of the elastic micro-bump contact. Namely, with applied constant force deflection of the elastic micro-bump contact is believed to be a relatively rapid visco-elastic deformation in the beginning and is succeeded by a very slow creep. This deflection affects the size of the contact area and thus the value of the contact resistance (see Figure 9)
- by fastening the chip to make the chip position be constant. This method needs some initial mechanical force for establishing good electrical contact, but it is expected that the elastic micro-bump contact will creep back and thus the contact force will be reduced. How much it will affect the value of the contact resistance is not investigated, but probably it will get higher.
- by combining the two above. First applying some constant mechanical force, and then when the deflection curve is flattened (see Figure 9) and the

initial deformation can be assumed to have finished, finally fixing the chip position.

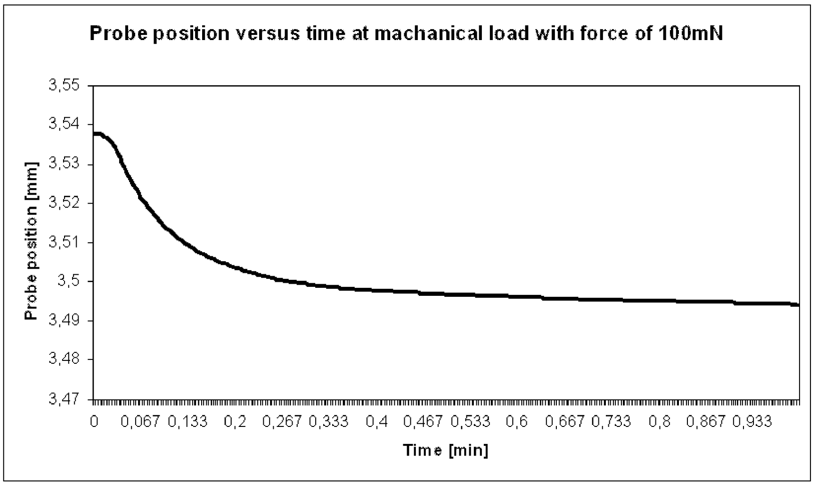


Figure 9 Change in probe position when one elastic micro-bump contact was exposed to 100 mN mechanical force during 1 minute.

3.3.1. Measurement of Contact Resistance

When discussing the contact resistance, questions arise as to how it is composed. This is discussed to some extent in **Paper 10**. For small contacts to semi-infinite bodies the well known Holm formula [27] applies. This describes in principle a three-dimensional spreading resistance from a contacting area of some size. However, when contacting a not semi-infinite body but a film of infinite lateral dimensions and of a thickness comparable to the size of the contacting spot, the situation is more complex. Further more, if the film is also limited in its lateral dimensions and in particular when it is again contacted with a small spot, many different kinds of current distributions exist. In the last case there is initially a three-dimensional spreading resistance which gradually evolves into a two-dimensional spreading resistance which evolves into a linear resistance which evolves into a two dimensional etc. As the change-over is gradual there is no easy way to formulate a formula that describes the situation. Therefore, FEM analysis was applied to study these situations in detail in **Paper 10**. The results from these simulations show that simply applying the Holm formula, which is frequently the case in many reports, easily results in errors of several hundred percent. In **Paper 10** correction factors are given for a number of typical thin film cases to obtain correct results from simple formulas.

Measurement of the contact resistance of one single elastic micro-bump contact was conducted by using a Kelvin Bridge. It was measured over one single elastic micro-bump, so that in reality, this contains resistance of the Au layer over the elastic micro-bump contact, spreading resistance outside the elastic micro-bump, contact resistance between the elastic micro-bump contact and the probe and spreading resistance in the body of the probe (see **Paper 3**). Figure 10 shows the measurement set-up.

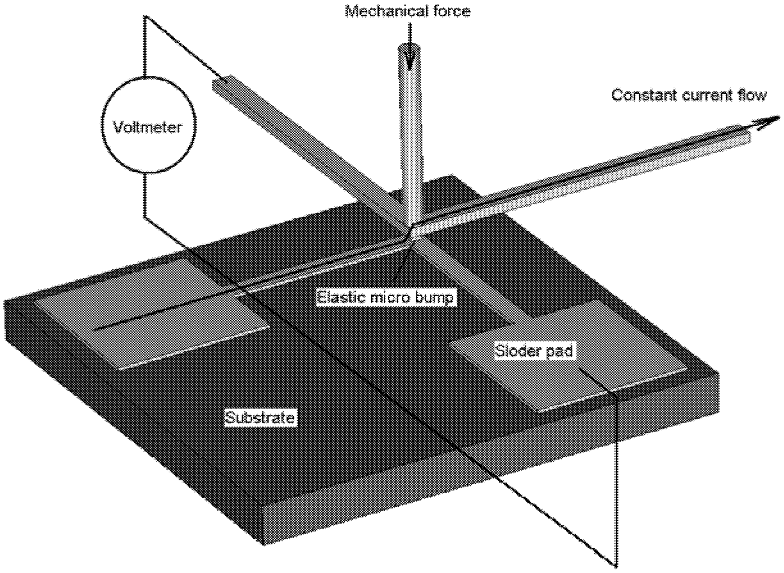


Figure 10 Kelvin Bridge used for precision measurements of contact resistance for single elastic micro-bump contact.

The measurement set-up was connected to a four wire Ohm meter (HP 3459A), and is symmetric from the point of view of the thermoelectric electromotive forces, i.e. they cancel each other, and thus do not introduce any error in the measurements.

This set up was put in DMA (Dynamic Mechanical Analyzer, Perkin Elmer DMA 7e) and then the mechanical force was applied. This gave plots that depicted contact resistance versus the probe position (i.e. deflection) (see Figure 11) and applied mechanical force (see Figure 12) received from measurements on the elastic micro-bump shown in

Figure 13.

Comparing this contacting technique with already existing elastic contact technique which uses metal-particle loaded elastomer bumps such as that treated in [28], it is obvious that in order to achieve the same low contact resistance, the applied force per elastic micro-bump contact is approximately twenty times larger for the structure discussed in [28], than for those presented in this work. For example, to achieve a contact resistance less than 10 mΩ it is necessary to apply a force of ca 200 mN/contact for the structure in [28], but the force of ca 10 mN/contact is sufficient for the contact structure discussed here.

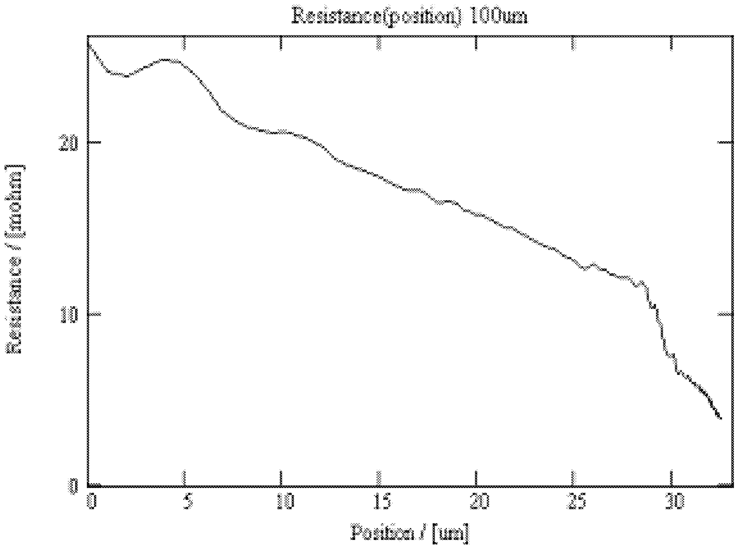


Figure 11 Contact resistance versus probe position.

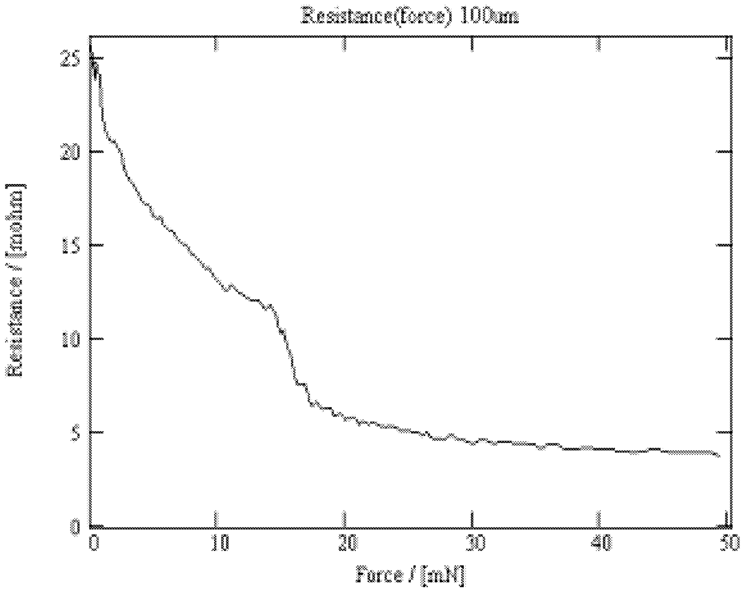


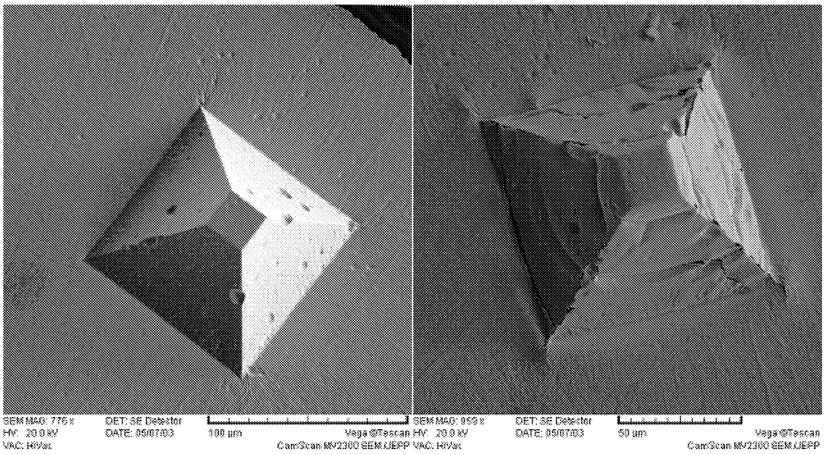
Figure 12 Contact resistance versus applied mechanical force.

This fact can be of great interest when the amount of I/Os on chip, that has to be contacted, is large. For example, for contacting 1000 I/Os, the contact load that has to be applied is tens of kg for the structure in [28]. Under such circumstances, the localized stress may be a potential cause of bowing of the

PCB or even more serious problems, such as cracking, breaking lines etc. If the concept described in this work is used, that load will be kilograms for the same number of I/Os.

The measured resistance over the micro-bump contact structure will not be a serious problem in an electronic system signal path, and is fully competitive with present elastic contacting techniques ([28], [29], and [30]).

Figure 13 shows a truncated elastic micro-bump contact before and after measurement.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DET: SE Detector
HV: 20.0 kV
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50 µm
VAC: HiVac
Vega ©Tescan
CamScan MV2300 SEM UEPP

Figure 13 Elastic micro-bump contact (100X100 µm base) before and after contact resistance measurement.

3.4. HF Properties

Although limited, but still valuable HF measurements on the structure consisting of micro-strip line to the elastic micro-bump – elastic micro-bump to the chip – from the chip to the elastic micro-bump – from the elastic micro-bump to the micro-strip line signal path were carried out and reported in **Paper 7**.

As a complement to conducted measurements, 3-D simulation of the HF behavior of the same structure was run and compared to the measured results.

Despite some difference between the measured and simulated results, one could say that the considered structure with elastic micro-bump contacts in the signal path will work quite well up to a couple of tens of GHz, i.e. having the elastic micro-bumps in the signal path will not affect signal quality significantly. It revealed also that the elastic micro-bump contact based interconnection technique is, if not better, then at least equally good as the flip chip and chip-first techniques. Its advantage of the reduced thermo-mechanical stress and effortless rework with good HF properties makes this technique a potentially attractive solution for chip interconnects.

4. Scaling

The initial results presented in **Paper 5** indicated the possibility to scale the structures down to achieve extreme density of I/O. Therefore, an attempt was made to fabricate daisy chains in elastic chip sockets and test chips of 7 by 7 mm (see **Paper 6**).

Table 1 describes the attempted densities.

Array size	Pitch	Bump Base	Bump Height	I/O Density
200 x 200	36 μm	26 μm	18 μm	80000 / cm^2
150 x 150	48 μm	36 μm	25 μm	45000 / cm^2
100 x 100	72 μm	48 μm	34 μm	22500 / cm^2

Table 1 Attempted densities by applying techniques described in this paper.

The 22500 contacts per cm^2 worked well and it was possibly to temperature chock cycle these structures multiple times without failure as reported in **Paper 6**. Also 45000 and 80000 contacts per cm^2 worked for several samples. Due to not perfect dimensions, these, however, lost alignment when temperature cycling. This is a remarkable result for a chip last scheme, which has previously only been possible using chip-first techniques, and dramatically increases the available number of the I/O pads for the given chip size compared to peripheral contact pad assemblies and also to conventional flip chip assemblies.

If an area array of I/Os on the top of the chip is planned during its design, the chip can be optimized to maximize the benefits of area array. For example, the power/ground and signals can be distributed where they are required, eliminating the need to route all the connections to the periphery of the chip, reducing parasitics and delays. There is also the opportunity of reducing the size of the chip contact pads which consequently reduces their parasitic capacitances which can affect the quality of the signals. The increased number of I/Os available also allows a design with an increased number of parallel-transferred signals which can increase the total data rate significantly, which is in contrast to today's trend toward higher bit-rate I/Os, due to more and more limited number of available I/Os on the chips.

5. Using the developed techniques for another application: manufacture of micro reactors

The presented methods for micromachining of the silicone elastomer, particularly metallization and RIE can be interesting in other fields of use where the silicone elastomer is considered as a suitable material. The silicone elastomer is chemically quite stable and does not react with the most of chemicals. Several authors have reported having made micro-reactors from silicone elastomer (e.g. [31] and [32]). The common idea for all of them is that they consist of groups of cavities and channels cast in the silicone elastomer. The silicone elastomer is a hydrophobic material and as such does not force the liquid droplets to stay on the predefined place. That can be improved if the bottom of the channels and cavities are made hydrophilic by which the surface forces will result in highly improved wettability and holding of the liquid at desired locations. The methods and techniques considered in the previous chapters of this work are suitable for achieving that goal. Namely, if the substrate is made of hydrophilic material, e.g. glass, and the silicone elastomer layer of desired thickness is spun and after curing selectively removed, e.g. using RIE, from desired positions, it is possible to make micro-reactors with arbitrary size and shape. The procedure for making micro/nano-pools in silicone elastomer on the glass substrate, which have a potential to be used for making hydrophilic-bottom structures with the arbitrary shape, is presented in **Paper 9** and example of such a micro-pool is shown in Figure 14.

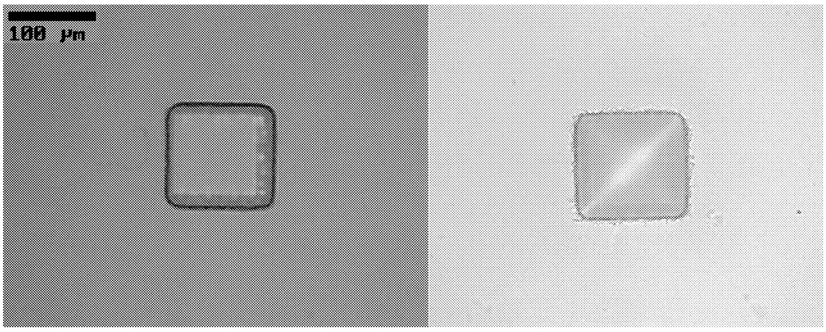

Figure 14 The micro-pool empty (left) and filled (right) with water. The pure glass is visible at the bottom (left) after RIE protection layer is removed.

6. Future Work

During this work the most vital process steps for manufacturing elastic chip sockets was investigated and recipes are presented. However, further investigation and improvement of these recipes and use of other similar materials and methods should be performed.

6.1. Material Concerns

Due to the characterization was conducted on structures (both single elastic micro-bump contacts and entire elastic chip sockets) made of one kind of silicone elastomer, it should be conducted on other types of silicone elastomer in order to find out the optimal viscosity, stiffness, electrical properties etc. for given field of use. Also, when changing silicone elastomer, it is possible that the recipes especially for metallization and RIE will be affected and thus need to be modified.

The other issue in finding the optimum silicone elastomer is finding one which is, if not totally, then maximally clean-room compatible because of its emission of silicon oil which is easily spread and quite difficult to remove.

A particular problem with the silicon oil can be worsened or even lost electrical contact between the chip and elastic micro-bump(s), but also changing long term mechanical properties of the silicone elastomer, which can affect the contact resistance. Also, the “normal” expected creep of the silicone elastomer will probably cause the contact resistance to change during time. These aspects have to be taken into consideration during future research.

6.2. Cracking and Adhesion of Metal Film

By comparing SEM image of the elastic micro-bump contact prior and after contacting (see

Figure 13) one can see two major problems: cracking and lack of adhesion of the metal film.

The cracking of the metal film is most prominent at sharp corners which are stress collectors. That stress can be diminished by e.g. proper rounding the corners. Another way could be to remove the metal film from the corners and let them expand/deform freely and thus preserve the metal film from unnecessary mechanical stress.

Even thought the tape-pull test established quite good adhesion it can still be insufficient as evidenced in

Figure 13.

These two problems should be further investigated in order to optimize the type of silicone elastomer and the shape of the elastic micro-bumps regarding stress related cracking and poor adhesion of the metal film, and also regarding the applied force which guaranties low contact resistance for the used metallized silicone elastomer. Simultaneously, the metallization recipe which will give optimum result should be found.

6.3. Via Yield – Complete Elastic Chip Socket

In order to achieve a final product it is necessary to conduct all the steps shown in Figure 2. It has been established that the via hole metallization and patterning are the most uncertain of all the processes. Although functioning via holes have been achieved, their yield is not high due to the roughness and steepness of their sidewalls.

In Figure 15 an attempt of making a complete elastic chip socket is shown. The via holes have steep and very rough sidewalls which gave us reason to believe that sputter deposition of the metal is not the optimum solution for metallization of these via holes.

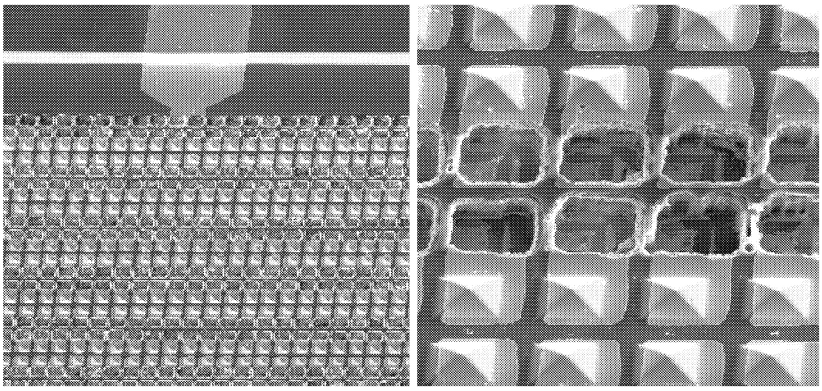

Figure 15 An attempt making a complete elastic chip socket.

The possible solution could be electroplating the metal, which can be for example Cu, from the bottom up to the top level of the via holes. In that case neither the roughness nor the slope of the sidewalls of the via hole should be important, but it is necessary to secure electrical contact to the bottom of every via hole. The problem with via hole metallization can force this concept to move more towards manufacture of elastic chip sockets not directly on PCB/substrate, but on a carrier, fan-out substrate with μBGA (Micro Ball Grid Array) on one side and elastic chip socket on the opposite side. Under-bump metallization of the μBGA could be used to assist electrical contact to the bottom of the via holes, making it possible to electroplate metal through them. Then, such elastic chip sockets will be supplied with solder balls and attached onto the PCB/substrate and the chip will be placed into it afterwards. The properties of the basic concept still will be retained, but the manufacturing procedure will be more complicated; but probably with much higher yield.

The step of metallization of the via holes has to be developed to be a high yield step like those previous, but also the modification of the original concept [20] towards μBGA elastic chip sockets, if not more, is equally worth investigating.

7. Summary and Conclusions

Manufacturing of electronics involves a diversity of different materials that most often have different CTE. This leads to an inherent thermo mechanical stress that can directly affect the reliability of the system. One of the latest interconnecting techniques to be used on a major scale is the flip chip technique. That is considered until now as one of the best solutions from the point of view of high frequency properties and interconnection density. Due to the fact that small solder balls are positioned between chip and the substrate, they are exposed to thermo mechanical stress that can cause them to crack either after a short time after some temperature excursion or later due to fatigue caused by temperature excursion cycling or elevated constant stress.

The new suggested concept of elastic chip sockets is treated in this work as it is considered as a potential solution which can offer high density interconnection, much reduced thermo-mechanical stress and the reliability problems accompanied with it, and effortless rework. That concept proposes use of the silicone elastomer, Au and an tiny metal adhesive layer (Ti or Cr) and is considered as not harmful for the environment.

Cast molds for the elastic chip sockets and the single micro-bums were made in Si by antistrophic etch in KOH. This technology is well known and described in literature [22]. In order to achieve control over the thickness of silicone elastomer it is recommendable to make stand-offs on suitable places on the mold. For this purpose SU 8 negative photo-resist was successfully used.

Metal deposition can be tricky and during this work a recipe was developed (see **Paper 1**). If some other sputtering equipment or silicone elastomer is used, it could be necessary to modify some parameters in the recipe.

Patterning have to be done by electroplating of photo-resist as conventional spin coater deposited photo resists will not work because the sharp corners of the metallized elastic micro-bumps will cut through the photo-resist and it is not certain that via holes sidewalls will be entirely protected against the Au wet etch chemicals.

Making via holes is necessary in order to reach through silicone elastomer layer to the lines patterned on the underlying substrate. RIE of silicone elastomer has shown a good potential when making via holes. The majority of the RIE residues can be relatively easily removed by washing the substrate in the ultrasonic bath with DI water and using the lift-off process reported in this work. The roughness and inclination of the sidewalls were found to be a serious obstacle for the successful metallization by sputtering of Au. As an alternative to sputtering, the electroplating of the metal, which does not necessarily have to be Au from the bottom up to top of the via holes, is suggested.

Mixing, casting and curing of the silicone elastomer should be done carefully and not in the same clean-room where semiconductors are made, because of the risk of contamination with silicon oils which are very difficult to remove from contaminated surfaces.

From the resistance measurements that were done on both single elastic micro-bump contacts (see **Paper 3**) and complete elastic sockets (see **Paper 5** and **Paper 6**) it is clear that the mechanical force per contact for this concept is less than one tenth (ca 1/20) of that of commercial elastic interconnection structures. This can be a great advantage when the number of contacts is large, i.e. this technique reduces applied mechanical force by at least ten times and thus the risk for e.g. bowing of the substrate is significantly reduced. Another great advantage of this interconnection technique is the size of elastic micro-bump contacts. The elastic contacts (buttons) that were treated in [28] have a size of 0.5 but the elastic micro-bump contacts reported in this work are of size of 0.1 mm and less. This means that by applying this technique it is possible to reach much higher contact density (see **Paper 6**) than with the technique treated in [28]. Contacts area array densities of 22500/cm^2 were accomplished and endured severe temperature cycling which was previously achieved only by the chip-first techniques.

As pointed out in Future Work, several issues remain to be investigated to ascertain acceptance of the elastic chip socket concept from the electronic industry. Mechanical creep of the silicone elastomer can cause severe problems after prolonged time of use. To minimize this problem the most suitable elastomer material has to be determined and so far only one silicone elastomer has been tried. This may, however, cause reduced metal adhesion etc. which will require further changes etc. In order to truly prove the concept, full sockets including via connections to the metal pattern on the substrate have to be manufactured and evaluated.

So far we achieved elastic chip sockets which could be used only in applications where the fan-out is possible to conduct at the top of the elastomer layer, but when reliable via holes have been developed, this technique probably will be fully competitive versus the flip chip and chip-first technique considering interconnection density and HF properties. Regarding rework this technique has shown its potential to be superior to most of any invented chip interconnect techniques. No heating, cleaning or similar operations are needed – just physical removal of the old chip and placement of the new.

The absence of any solder, under fills or glues, and use of, so far considered, environmentally harmless materials (the silicone elastomer and Au) and a tiny Cr layer, makes the elastic chip sockets or the single elastic micro-bump contacts a very small potential risk for the environment.

Summary of Appended Papers

The papers included in this Thesis are dealing with manufacture of single elastic micro-bump contact and elastic chip socket concept introduced by Professor Hjalmar Hesselbom et al. [20]. Main focus was put on micromachining and metallization of the silicone elastomer which were recognized as key problems in practical realization of the treated concept. The measurements and some theory concerning contact resistance are also presented in the appended papers. Several other important properties of the single elastic micro-bump contacts as well as the entire chip sockets are considered in these papers.

Paper 1

Sputter Deposition of Chromium, Gold and Copper on Silicone Elastomer

This paper deals with the sputter deposition of metals needed for patterning of Au lines and bump-pads on silicone elastomer and also for making RIE masks for dry etch of the silicone elastomer. Wrinkle formation and cracking are investigated and discussed and a recipe for avoiding them is suggested.

Authors' contributions: The author planned and conducted all of the experiments, as well as most of the analysis of the observed phenomena, and finally wrote the manuscript.

Paper 2

CF_4/O_2 versus SF_6/O_2 RIE of Silicone Elastomer – Characterization and Comparison

In this paper RIE rate of the silicone elastomer by using CF_4/O_2 versus SF_6/O_2 plasma was investigated, characterized and compared to each other regarding the fraction of O_2 in the gas mixtures, pressure in the process chamber, temperature and the location on the processed wafer.

Authors' contributions: The author planned and conducted all of the experiments and all the measurements as well as most of the analysis of the observed phenomena and wrote the manuscript.

Paper 3

Metal Covered Elastic Micro-Bump Contacts as an Alternative to Commercial Elastic Interconnection Techniques

This paper studies single elastic micro-bump behavior. In this work sharp-tipped and truncated elastic micro-bump contacts with different size of the base were manufactured and characterized regarding contact resistance versus contact force and deflection. A comparison to existing commercial elastic interconnection structures was also considered.

Authors' contributions: The author planned and conducted most of the experiments, as well as all the measurements and wrote the manuscript.

Paper 4

Manufacturing of Via Holes in Silicone Elastomer

Making via holes in the silicone elastomer was investigated. Several techniques like punching, laser drilling and RIE were taken in consideration. RIE has been recognized as a suitable method and vias with diameter of 30 µm were achieved. Removal of the etch residues from the bottom was suggested to be conducted by using a lift-off process. Inclination and roughness of the sidewalls, as well as under-etch during lift-off process, were established as serious problem for successful metallization.

Authors' contributions: The author planned and conducted most of the experiments, as well as all the measurements and wrote the manuscript.

Paper 5

Elastomer Chip Sockets for Reduced Thermal Mismatch Problems and Effortless Chip Replacement, Preliminary Investigations

The first prototype of the elastic chip socked with 216 peripheral contacts was presented in this paper. Heat cycling between room temperature and dipping into the liquid nitrogen was conducted and indicated promising thermo-mechanical properties of the concept. Allowing for low contact force for achieving low contact resistance was also established. The first theories regarding the contact resistance of thin film contacts was introduced in this paper.

Authors' contributions: The author assisted in the test vehicle design process, some test vehicles processing and participated in general discussions.

Paper 6

Very High Density Interconnect Elastomer Chip Sockets

Area array elastic chip sockets with densities as large as 80000 connections per cm^2 were presented. Daisy chain tests were conducted on well working samples with up to 22500 serial connected contacts. The thermo-mechanical behavior during temperature cycling was monitored and presented in this paper.

Authors' contributions: The author assisted in the test vehicle design process, some test vehicles processing and participated in general discussion.

Paper 7

High Frequency Signal Transmission Properties of Elastomer Chip Sockets

A HF characterization of the specially designed elastic chip sockets for these purposes was performed. It was established that the measurements correlate well to full field electromagnetic simulator results on the same structures and that the elastic chip socket concept should work sufficiently up to 30 GHz. A comparison of the simulated results for solder bump geometries to the elastic micro-bump geometries is also presented.

Authors' contributions: The author assisted in the test and HF calibration structure design process, some test vehicles processing and participated in general discussion.

Paper 8

Solder and Adhesive Free Chip Assembly Using Elastic Chip Sockets: Concept, Manufacture and Preliminary Investigation

In this paper a general review and the most significant achievements in the development of the elastic chip socket concept were presented as a conference presentation given by Prof. Hjalmar Hesselbom.

Authors' contributions: The author assisted with collecting the data of interest and critical reading the drafts.

Paper 9

Method for Making of Micro/Nano-Liter Pools and Channels with Hydrophilic Bottom in Silicone Elastomer

In this paper a method for making micro/nano-liter pools with hydrophobic bottom and surrounding areas was presented. The technique is based on the same methods and recipes as those used in previous papers, and their potential usefulness has been shown not only within electronic but also e.g. bio-medical and chemical equipment manufacture.

Authors' contributions: The author planned and conducted all of the experiments, as well as all the measurements and wrote the manuscript.

Paper 10

Contact Resistance of Thin Film Metal Contacts

A model for approximation of the contact resistance of thin film metal contact based on Maxwell/Holm contact resistance theory extended with a cylindrical spreading resistance was presented in this paper. FEM simulations were used as a base for weight functions. Error plots are also presented.

Authors' contributions: The author participated in discussions concerning current spreading within the thin film contact structures.

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