SiGeC
Heterojunction Bipolar Transistors

Doctoral Thesis
by
Erdal Suvar
Stockholm, 2003
Sweden

Laboratory of Solid State Devices,
Department of Microelectronics and Information Technology (IMIT),
Royal Institute of Technology (KTH)
SiGeC Heterojunction Bipolar Transistors
by Erdal Suvar

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Babam Ömer için,
annem Aslım için,
kardeşlerim Elif ve Ersan için,
sevdiklerim, dostlarım ve yakınlarım için
ve Temam için.
I would like to thank Professor Mikael Östling for giving me the opportunity to fulfill a dream. Working with research and pursuing a Ph.D. has been a life long ambition of mine. This part of my life is now ending to make way for the remaining of a new life. I am forever grateful for your support.

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Thank you Temam.

Thank You all.

Erdal Suvar, Stockholm, November 2003
Heterojunction bipolar transistors (HBT) based on SiGeC have been investigated. Two high-frequency architectures have been designed, fabricated and characterized. Different collector designs were applied either by using selective epitaxial growth doped with phosphorous or by non-selective epitaxial growth doped with arsenic. Both designs have a non-selectively deposited SiGeC base doped with boron and a poly-crystalline emitter doped with phosphorous.

Selective epitaxial growth of the collector layer has been developed by using a reduced pressure chemical vapor deposition (RPCVD) technique. The incorporation of phosphorous and defect formation during selective deposition of these layers has been studied. A major problem of phosphorous-doping during selective epitaxy is segregation. Different methods, e.g. chemical or thermal oxidation, are shown to efficiently remove the segregated dopants. Chemical-mechanical polishing (CMP) has also been used as an alternative to solve this problem. The CMP step was successfully integrated in the HBT process flow.

Epitaxial growth of $\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$ layers for base layer applications in bipolar transistors has been investigated in detail. The optimization of the growth parameters has been performed in order to incorporate carbon substitutionally in the SiGe matrix without increasing the defect density in the epitaxial layers.

The thermal stability of npn SiGe-based heterojunction structures has been investigated. The influence of the diffusion of dopants in SiGe or in adjacent layers on the thermal stability of the structure has also been discussed.

SiGeC-based transistors with both non-selectively deposited collector and selectively grown collector have been fabricated and electrically characterized. The fabricated transistors exhibit electrostatic current gain values in the range of 1000-2000. The cut-off frequency and maximum oscillation frequency vary from 40-80 GHz and 15-30 GHz, respectively, depending on the lateral design. The leakage current was investigated using a selectively deposited collector design and possible causes for leakage has been discussed. Solutions for decreasing the junction leakage are proposed.

Key words: Silicon-Germanium-Carbon (SiGeC), Heterojunction bipolar transistor (HBT), chemical vapor deposition (CVD), selective epitaxy, non-selective epitaxy, collector design, high-frequency measurement, dopant segregation, thermal stability.
### Symbols & Acronyms

<table>
<thead>
<tr>
<th>Symbol/Acronym</th>
<th>Meaning</th>
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<tr>
<td>As</td>
<td>Arsenic</td>
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<tr>
<td>B</td>
<td>Boron</td>
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<tr>
<td>C</td>
<td>Carbon</td>
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<td>Ge</td>
<td>Germanium</td>
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<tr>
<td>Si</td>
<td>Silicon</td>
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<td>P</td>
<td>Phosphorous</td>
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<tr>
<td>SiGe</td>
<td>Silicon-Germanium alloy</td>
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<tr>
<td>Si$_{1-x}$Ge$_x$</td>
<td>Silicon-Germanium alloy</td>
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<td>SiGeC</td>
<td>Silicon-Germanium-Carbon alloy</td>
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<tr>
<td>Si$_{1-x-y}$Ge$_x$C$_y$</td>
<td>Silicon-Germanium-Carbon alloy</td>
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<tr>
<td>SiC</td>
<td>Silicon-Carbon alloy</td>
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<tr>
<td>Si$_{1-y}$C$_y$</td>
<td>Silicon-Carbon alloy</td>
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<tr>
<td>BJT</td>
<td>Bipolar Junction Transistor</td>
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<tr>
<td>HBT</td>
<td>Heterojunction Bipolar Transistor</td>
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<tr>
<td>SIC</td>
<td>Selective Implanted Collector</td>
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<tr>
<td>CVD</td>
<td>Chemical Vapor Deposition</td>
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<tr>
<td>RPCVD</td>
<td>Reduced Pressure Chemical Vapor Deposition</td>
</tr>
<tr>
<td>SEG</td>
<td>Selective Epitaxial Growth</td>
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<tr>
<td>NSEG</td>
<td>Non-Selective Epitaxy Growth</td>
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<tr>
<td>SIMS</td>
<td>Secondary Ion Mass Spectrometry</td>
</tr>
<tr>
<td>AFM</td>
<td>Atomic Force Microscopy</td>
</tr>
<tr>
<td>TEM</td>
<td>Transmission Electron Microscopy</td>
</tr>
<tr>
<td>HRXRD</td>
<td>High-Resolution X-Ray Diffraction</td>
</tr>
<tr>
<td>HRRLM</td>
<td>High-Resolution Reciprocal Lattice Map</td>
</tr>
<tr>
<td>CMP</td>
<td>Chemical Mechanical Polishing</td>
</tr>
<tr>
<td>HF</td>
<td>High Frequency</td>
</tr>
<tr>
<td>$f_{\text{max}}$</td>
<td>Maximum oscillation frequency</td>
</tr>
<tr>
<td>$f_T$</td>
<td>Cut-off frequency</td>
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This Ph. D. thesis describes research work was carried out at Department of Microelectronics and Information Technology (IMIT), Laboratory of Solid State Devices, Royal Institute of Technology (KTH). This thesis includes an introduction and the following papers,

1. *Phosphorus profile control in low-temperature silicon epitaxy by reduced pressure chemical vapor deposition.*
   E. Suvar, H. H. Radamson and J. V. Grahn

2. *A base-collector architecture for SiGe HBTs using low-temperature CVD epitaxy combined with chemical-mechanical polishing.*
   E. Suvar, E. Haralson, M. Forsberg, H. Radamson, Y.-B. Wang, and J. V. Grahn

3. *Growth of high quality epitaxial Si_{1-x-y}Ge_xC_y layers by using chemical vapor deposition.*
   J. Hållstedt, E. Suvar, P. O. Å. Persson, L.Hultman, Y.-B. Wang and H. H. Radamson

4. *Influence of doping on the thermal stability of Si/SiGe/Si heterostructures.*
   E. Suvar, J. Christiansen, A. Kusnetzuv and H. H. Radamson

5. *High Frequency Performance of SiGeC HBTs with Selectively & Non-Selectively Grown Collector.*
   E. Suvar, E. Haralson, H. H. Radamson, Y.-B. Wang, B. G. Malm, and M. Östling,
   Physica Scripta (2003), accepted for publication.

   E. Haralson, E. Suvar, G. Malm, H. Radamson, Y.-B. Wang, M. Östling,

7. *Characterization of leakage current related to a selectively grown collector in SiGeC Heterojunction Bipolar Transistor structure.*
   E. Suvar, E. Haralson, H. H. Radamson, Y.-B. Wang, J. V. Grahn, B. G. Malm, and M. Östling,
The following papers are related to the work to this thesis but have not been included;

8. *Formation of As- or P-doped polycrystalline Si layers grown by RPCVD for emitter application in SiGeC-based Heterojunction Bipolar Transistors.*
   E. Suvar, E. Haralson, J. Hållstedt, H. H. Radamson and M. Östling,
   Physica Scripta (2003), accepted for publication.

9. *Methods to reduce the loading effect in selective and non-selective epitaxial growth of SiGeC layers.*
   J. Hållstedt, E. Suvar, C. Menon, P.-E. Hellström, M. Östling and H. H. Radamson,
   Materials Science & Engineering B, (2003), accepted for publication.

10. *Formation of shallow junctions by isotropic Si etch followed by selective epitaxy of SiGe in RPCVD.*
    C. Isheden, H. H. Radamson, E. Suvar, P.-E. Hellström, and M. Östling,
SUMMARY OF THE APPENDED PAPERS

1. *Phosphorus profile control in low-temperature silicon epitaxy by reduced pressure chemical vapor deposition;*
   Phosphorous incorporation in silicon epitaxial layers grown by reduced pressure chemical vapor deposition has been studied. Strong segregation of phosphorous towards the surface was observed and different methods to solve this problem have been investigated. It was shown that *ex-situ* chemical or thermal oxidation of these layers followed by HF-dip can remove the segregated phosphorous atoms at the surface. After the surface treatments, HBT structures with well-controlled dopant concentration were grown. In this study, SIMS and HRRLM were applied as main characterization tools. The author of this thesis has grown all samples and performed all material characterizations.

2. *A base-collector architecture for SiGe HBTs using low-temperature CVD epitaxy combined with chemical-mechanical polishing;*
   CMP method has been integrated in HBT structures with selectively grown collector layers. It was shown that CMP can remove effectively the segregated phosphorous atoms and SiGe layers with high quality can be grown on the CMP-processed phosphorous-doped Si layers. AFM, SIMS and HRRLM were used in this article. The author of this thesis has grown all samples and performed all material characterizations.

3. *Growth of high quality epitaxial Si$_{1-x}$Ge$_x$C$_y$ layers by using chemical vapor deposition;*
   Implementation of carbon in non-selectively and selectively deposited Si$_{1-x}$Ge$_x$C$_y$ layers has been studied. The interaction of Ge with C in Si matrix covering the growth rate behavior and defect generation has been discussed. This C incorporation in SiGe has been explained by the growth rate and the chemical effect. Electrical behavior of Si$_{1-y}$C$_y$ has also been investigated. A decrease in electron mobility by increasing carbon concentration was interpreted by the presence of carbon interstitials. HRRLM, TEM, SIMS, and Hall measurements were applied in this study. The author of this thesis has contributed to the material characterization.
4. Influence of doping on the thermal stability of Si/SiGe/Si heterostructures;
The thermal stability of Si/SiGe/Si transistor-like structures grown by chemical vapor deposition is discussed. The thermal stability of npn and pnp structures exhibit significant improvements compared to undoped structures. This high thermal stability was explained by dopant diffusion/precipitation as competitive phenomena to the formation of misfit dislocations in these heterojunction structures. SIMS and HRRLMs have applied in this study. The author of this thesis contributed to the growth of samples and material characterizations.

5. High Frequency Performance of SiGeC HBTs with Selectively & Non-Selectively Grown Collector;
A quasi-self aligned heterojunction bipolar transistor process using a non-selective deposition for the SiGeC base is presented. Both a traditional non-selective high temperature collector and a low temperature selectively grown collector were studied. Good electrostatic and high frequency performance for the fabricated transistors are demonstrated. The author of this thesis has prepared the mask design and contributed to the processing and electrical characterization of the devices.

6. The Effect of C on Emitter-Base Design for a Single-Polysilicon SiGe:C HBT with an IDP Emitter;
A SiGeC heterojunction bipolar junction transistor design featuring an in-situ doped poly-crystalline emitter is reported. This design is used to study the effect of carbon, the thickness of intrinsic emitter layer, and rapid thermal anneal temperature on emitter/base junction formation. In addition, the effect of lateral design parameters on electrostatic and high frequency performance was also studied. It was observed that the intrinsic emitter thickness under the influence of the carbon had a strong impact on the device performance. The author of this thesis has prepared the mask design and contributed to the processing of the devices.

7. Characterization of leakage current related to a selectively grown collector in SiGeC Heterojunction Bipolar Transistor structure;
Sources of leakage currents in a SiGeC-based heterojunction bipolar transistor with a selectively grown collector are discussed. Electrical measurements have been performed to investigate the leakage current behavior. Transmission electron microscopy results have demonstrated that edge-located defects generated by selective epitaxy process are the origin of the junction leakage. The author of this thesis has prepared the mask design, processed the devices, and performed the electrical characterization of the devices.
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While there exist many semiconductor materials that outperform silicon-based devices in a number of applications, silicon has been the dominant semiconductor on the market place since the invention of the integrated circuit. There are many reasons one may put forward to explain this position, but the ability to produce low-cost systems ensures that silicon will keep this position for some time.

Whilst most other semiconductors are non-compatible with silicon process technology, SiGe and SiGeC are easily incorporated into a silicon production line with little negative effect but considerable benefits at low investment cost. This ensures that both SiGe and SiGeC will have a clear position on the market. Recent reports [5-8] using SiGe(C) technology have also demonstrated devices with high-frequency performance that was only accessible with expensive III-V compound semiconductor devices. SiGe based devices with 350 GHz cut-off frequency and 170 GHz maximum oscillation frequency [9] will ensure that the position of silicon based technology will even expand in the future.

Two important applications of SiGe(C) are in Heterojunction Bipolar Transistors (HBTs) and Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs). In HBT structures, the high frequency performance can be improved by minimizing the parasitic series resistances and capacitances [10]. These goals are achieved by downscaling the lateral dimensions [11], applying base-link engineering [9, 12] and optimizing both vertical and lateral profile including the dopant diffusion after device processing [13].

The progress in the epitaxy techniques has provided an opportunity to grow layers with well-controlled vertical dopant profiles in monolayer scale and low defect density [14-17].

In the fabrication of SiGe-based transistors, a low temperature budget process is demanded. This limitation is due to diffusion of dopants to the adjacent layers and also strain relaxation after thermal treatments [10]. Both these undesired effects degrade the HF performance of HBTs. A totally self-aligned transistor design is the preferable way to decrease the junction capacitances [18]. An industrial approach is integration of selective implanted collector (SIC) layers [19]. However, there is a serious barrier in this type of designs, which is mainly due to transient enhance
diffusion (TED) of boron [19, 20]. This makes it almost impossible to have the freedom to create a desired doping profile. It has recently been shown that implementation of carbon in SiGe layer reduces TED of boron. This decreases in fact the boron out-diffusion and creates the possibility to extend the thermal budget of processing [21-23]. The presence of carbon in SiGe layers also relieves strain in the lattice, resulting in an increase of the critical thickness and thermal stability of the layers [24, 25]. This makes SiGeC based heterojunction structures the most attractive material for high-speed device applications [26].

The primary motivation for the research presented in this thesis was to investigate two high-frequency SiGeC HBT architectures with different collector designs. In both designs, the collector were grown epitaxially. Chapter 2 will present some relevant material properties of Si, Ge, SiGe, and SiGeC. This is followed with a short discussion on the basic operation of a bipolar transistor. Chapter 3 will introduce chemical vapor deposition used for the formation of the epitaxially grown collector and SiGeC base layers. Issues such as dopant incorporation and growth of high quality SiGeC are considered. Chapter 4 will introduce the different device designs and the process flow for the fabrication of the HBTs. Chapter 5 will present comparative electrical results for the different HBT architectures. Finally, a summary and future outlook will conclude this thesis.
The principal advantage of SiGe and SiGeC based heterojunction bipolar transistors over the traditional silicon based bipolar junction transistor technology arises from the possibility of band-gap engineering. This allows an improved high frequency performance without sacrificing the gain, as it will be discussed in this chapter.

This chapter will present some relevant material properties of Si, Ge and Si$_{1-x-y}$Ge$_x$C$_y$ layers e.g. bandgap and strain relaxation. Furthermore, an introduction of the basic structure and principal of operation of a heterojunction bipolar transistor (HBT) is presented. A quantitative analysis is performed where the current gain, cut-off frequency, and maximum oscillation frequency are also presented.
2.1 Material properties

Si, Ge & Si$_{1-x}$Ge$_x$

Both silicon and germanium are elements of group IV and they have diamond structure with band-gap energies of 1.12 eV and 0.66 eV at 300K, respectively [Fig. 2.1]. The valence-band of silicon has maximum at $\Gamma$-point and it consists of light hole (lh), heavy hole (hh) and spin-orbit (so) hole bands. The lh and hh are degenerate at $\Gamma$-point while the so has 44 meV split from the others bands. The conduction-band minima is located near X along $\Gamma$-X direction (denoted $\Delta$) and it is six-fold degenerate. Germanium has a valence-band structure similar to silicon but spin-orbit split is larger (290 meV). On the other hand, the conduction-band minimum is located at L-point and consists of eight degenerate states. Similar structural and chemical properties of these materials allow a binary alloy of Si$_{1-x}$Ge$_x$ that is continuously variable from pure silicon ($x=0$) to pure germanium ($x=1$). The band-structure of Si$_{1-x}$Ge$_x$ is silicon-like for $0 \leq x < 0.85$ and germanium-like for $0.85 < x \leq 1$ [27]. Though, the band-gap energy is a non-linear relation depending strongly on germanium amount and temperature [28, 29]. Empirical result of the band-gap reduction ($\Delta E_g$) for a strained Si$_{1-x}$Ge$_x$ layer grown on silicon substrates with the germanium content in a technologically interesting range [30, 31] is given by the following relation

$$\Delta E_g = E_g(Si) - E_g(Si_{1-x}Ge_x) = 0.896x - 0.396x^2, \text{ for } x < 0.3$$

(Eq. 2.1)

Although desirable, it is not possible to grow thick strained layers with much higher germanium content than 30% in a device structure due the lattice mismatch between

Figure 2.1 Band-diagram of (a) silicon and (b) germanium. Figure from [3].
silicon and germanium. The lattice constant $a(Si_{1-x}Ge_x)$ for unstrained $Si_{1-x}Ge_x$ is given by the following empirical relation [32]:

$$a(Si_{1-x}Ge_x) = a(Si)(1-x) + a(\text{Ge})x - 0.02393x + 0.01957x^2 + 0.00436x^3,$$

for all $x$(Eq. 2.2)

This makes it difficult to deposit thick $Si_{1-x}Ge_x$ layers with high germanium content without introducing defects into the material due to high induced strain in the lattice [33]. The strain in $Si_{1-x}Ge_x$ layers is released by formation of dislocations above a certain critical thickness ($h_C$) [34]. This thickness is also growth temperature dependent and $h_C$ becomes thinner for high growth temperature. A practical growth temperature range for $Si_{1-x}Ge_x$ layers is 550-750 °C.

In the literature, Matthews and Blackeslee (MB) model [34] is one of the earliest theories about strain relaxation of SiGe layers and it shows a diagram of critical thickness versus germanium amount. MB model calculates critical thickness values, $h_{\text{C,eq}}$ for $Si_{1-x}Ge_x$ layers based on the equilibrium between two competing forces; the force exerted by the misfit strain and the tension in the dislocation line. Later it was demonstrated that MB equilibrium model predictions were not consistent with the experimental data of critical thickness and $Si_{1-x}Ge_x$ layers with thickness above $h_{\text{C,eq}}$ could be grown. The reason for the failure of MB model is that it is too simple and it has not considered nucleation, propagation, and interaction of dislocations. Fig. 2.2 shows the experimental data for $h_C$ and $h_{\text{C,eq}}$ for different Ge amounts. $Si_{1-x}Ge_x$ layers with thickness above $h_{\text{C,eq}}$ line are called meta-stable and strain relaxation occurs by post-annealing treatment. More accurate theories were proposed afterwards to estimate $h_C$ for SiGe layers based on non-equilibrium approach [35].

Recent reports have shown that the critical thickness diagram in Fig. 2.2 cannot be applied directly for SiGe layers grown on the patterned substrates. Thicker strained layers can be grown selectively\(^1\) whereas the meta-stable region shrinks for $Si_{1-x}Ge_x$

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\(^1\) See chapter 3 for definition of selective and non-selective growth.
layers grown non-selectively [36-38]. The discrepancy of the experimental data in the later case is due to injection of defects from the polycrystalline layer into the epitaxial part. The increase in $h_C$ for the selectively grown $\text{Si}_{1-x}\text{Ge}_x$ layers is due to strain distribution of these layers leading to a more strain relaxation closer to the edge of the oxide [39].

The other results about the strain relaxation of thin $\text{Si}_{1-x}\text{Ge}_x$ layers demonstrate that the strain relaxation does not occur through formation of misfit dislocations but through creation of surface roughening [40-42].

$\text{Si}_{1-y}\text{C}_y \& \text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$

Incorporation of carbon in SiGe offers several attractive possibilities that will be explored in this section. Similar to the $\text{Si}_{1-x}\text{Ge}_x$ heterojunction, a band-gap reduction occurs for the diamond structured $\text{Si}_{1-y}\text{C}_y$ alloy. In contrast to SiGe materials where most of the band-gap reduction as described in (Eq. 2.1) occurs in the valence band, $\text{Si}_{1-y}\text{C}_y$ materials shows the major reduction in the conduction band [43]. The exact nature of the band-gap offset for the ternary alloy $\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$ is not known yet. Initial results [44-48] shows a large discrepancy between the reported values though they suggest the total band-gap reduction for this material is mainly accommodated by a valence band offset and a minor off-set in the conduction band.

Another important property of $\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$ is the improved thermal stability of a strained layer deposited on silicon. This originates from the reduced strain in $\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$ [49] compared to $\text{Si}_{1-x}\text{Ge}_x$ as indicated in Fig. 2.3.

However, the most relevant property of $\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$ in the context of this thesis is the influence of carbon on diffusion of boron. It has been demonstrated that diffusion

![Figure 2.3 Schematic representation of the lattice distortion in (a) Si/Si$_{1-x}$Ge$_x$/Si, (b) Si/Si$_{1-y}$C$_y$/Si, and (c) totally strain compensated Si/Si$_{1-x-y}$Ge$_x$C$_y$/Si heterojunction.](image-url)
of carbon, boron, and phosphorus atoms in silicon [50-53] are predominantly assisted by silicon self-interstitials via the following reaction [Fig. 2.4]:

\[ A_S + I \leftrightarrow A_I \]  

(Eq. 2.3)

where A stands for a certain atom, I for silicon self-interstitial, and the subscripts S and I indicate substitutional and interstitial positions. This reaction is known as kick-out (KO) mechanism and it occurs when silicon interstitial pushes an immobile substitutional impurity atom to an interstitial site where they can diffuse. The diffusion coefficient (D) of carbon and boron can be described in the general form

\[ D = D_0 \cdot \exp\left(\frac{E_a}{kT}\right) \]  

(Eq. 2.4)

The activation energy \( (E_a) \) of both species are around 3 eV whereas the pre-exponential diffusivity factor \( (D_0) \) is more than 10 times higher for carbon than boron [20]. This implies that, in a lattice with carbon and boron the carbon atoms will consume the interstitials in higher rate than boron and thereby reducing the boron diffusivity. The reduction of the boron diffusivity in Si\(_{1-y}C_y\) and Si\(_{1-x-y}Ge_xC_y\) compared to samples without carbon has been experimentally verified by several groups [22, 54-56]. This makes implementation of carbon very attractive for many device structures, most notably where steep boron profile and/or high temperature annealing treatment are required, but also where an implantation process is requested. It is a well-known fact that implantation causes injection of point defects such as silicon interstitials which may significantly enhance dopant diffusion. This phenomenon is known as transient enhanced diffusion (TED) and may in the case of boron, result in diffusivity that is enhanced more than one order of magnitude [20]. However, carbon will suppress TED.

Fig. 2.5 shows secondary ion mass spectrometry (SIMS) results from two fabricated HBTs with and without carbon in the boron doped base layer after a thermal anneal at 925°C for 10 s. The sample with carbon in the base resulted in functioning devices with only a minor boron out-diffusion from the SiGe layer. In contrast to this, the sample without carbon in the base resulted in a device with a
significant boron out-diffusion and severely degraded performance.

2.2 Basic Device Physics, The bipolar transistor

Bipolar junction transistors (BJTs) are three-terminal electronic devices, which mainly are used for ultra fast switching, current and voltage amplification. Only the n-p-n silicon based transistors designed for current amplification in a common-emitter configuration will be considered in this discussion.

Current gain

The basic principle of operation of a BJT is based on the formation of depletion regions at the pn-junctions. Due to the potential difference over the depletion regions, electrons and holes will experience a barrier blocking a current flow at the emitter/base and base/collector junctions. Fortunately, the height of the barriers can be altered by the applied bias over the pn-junctions such that electrons from the emitter can flow into the collector and thereby contribute to a current. This function can be understood by first considering the base/collector junction; by reverse biasing this junction by $V_{CB}$ free electrons close the junction in the base region will be swept by the electric field to the collector [Fig. 2.6]. However, with only intrinsic electron concentration in the base there would only be a small saturation current ($I_{Cn0}$, $I_{Cp0}$) in the device. Now consider applying a small forward bias $V_{BE}$ at the emitter/base junction, supplying electrons to the base ($I_{E0}$). In the base, the electrons respond to the reverse biased base/collector junction and continue to the collector and thereby

Figure 2.5 Boron profile in two fabricated HBTs after a rapid thermal anneal at 925°C for 10 s. Sample 1 (broken line) has no carbon in the base while sample 2 (thick solid line) is doped with $1 \times 10^{20}$ cm$^{-3}$ carbon in the SiGe layer. No substantial difference was observed for the P and Ge profile between the samples.
giving raise to a collector current \( (I_C) \). In an ideal transistor all of the electrons supplied by the emitter would have continued to the collector. However, due to the finite recombination lifetime of the electrons some of them will recombine with holes in the emitter-base depletion region \( (I_{rg}) \) and in the base \( (I_{En}-I_C) \). Furthermore, in a real device some of the holes in the base will diffuse to the emitter and recombine with electrons \( (I_{Ep}) \). Both these current contribute to the base current \( (I_B) \) and for most practical transistors \( I_B \) is much smaller than \( I_C \). The emitter current \( (I_E) \) is defined as the sum of \( I_B \) and \( I_C \).

The transistor action as described above is such that by applying a certain electric potentials on the terminals, a small current between the base and emitter contacts results in a large current between the emitter and collector terminals, yielding a current amplification. The current amplification, also known as electrostatic common-emitter forward current gain \( (\beta) \) is the most fundamental characteristics of bipolar junction transistors. It is defined as following

\[
\beta = \frac{I_C}{I_B} \sim \frac{\text{emitter doping}}{\text{base doping}}
\]  

(Eq. 2.5)

This feature of the transistor is directly related to the total emitter and base doping. In a modern bipolar transistor with an in-situ doped poly-crystalline (IDP) emitter, the doping level in the emitter is limited by dopant activation to \(~1-2\times10^{20} \text{ cm}^{-3}\). Thus, the easiest way to increase the gain is by reducing the total base doping. However this has a negative effect on the high frequency performance of the device as will be shown below. A common strategy to overcome this dilemma has been by

Figure 2.6 Schematic representation of the current-flow in bipolar transistor in common-emitter configuration. The depletion regions are represented by dashed regions.
implementing SiGe base to increase the gain. The benefit of using heterojunction bipolar transistors with band-gap reduction ($\Delta E_g$) in the base is recognized as an improvement to the gain as following

$$\beta \sim \beta_0 \cdot \exp(\Delta E_g/kT) \quad (Eq. 2.6)$$

where $\beta_0$ is gain for a BJT, $k$ is the Boltzmann’s constant and $T$ is the temperature. As seen, even a small reduction in the band-gap [Eq. 2.1] renders a large improvement in the gain.

**High frequency behavior**

This section will introduce the frequency response of a transistor to a small-signal excitation on the base terminal. This is strongly coupled with the small-signal current gain, which in its general form is defined as

$$h_{21} \equiv \frac{\partial I_C}{\partial I_B} = -2 \cdot \frac{s_{21}}{(1-s_{11})(1+s_{22})+s_{12} \cdot s_{21}} \quad (Eq. 2.7)$$

where $s_{11}, s_{12}, s_{21},$ and $s_{22}$ are the measured scattering parameter components. The scattering parameters, S-parameters for short, are a set of parameters that relates to the travelling waves that are scattered or reflected when a transistor is inserted into a transmission line.

At low frequencies, the current gain is independent of the frequency. However, above a certain frequency it starts to decline with slope of 20 dB/decade in an ideal case. The cut-off frequency ($f_T$) is defined as the frequency at which no current amplification is obtained, i.e.

$$|h_{21}(f_T)| = 1 \quad (Eq. 2.8)$$

In conjunction to this definition, the maximum oscillation frequency ($f_{max}$) is defined as the frequency at which no power amplification is obtained, i.e.

$$|U(f_{max})| = 1 \quad (Eq. 2.9)$$

where $U$ is the unilateral power gain given by the measured scattering parameter components as [57]

$$U = \frac{|s_{21}/s_{12}-1|^2}{2k \cdot |s_{21}/s_{12}| \cdot -2\text{Re}(s_{21}/s_{12})}, \quad \text{where} \quad k = \frac{1-|s_{11}|^2-|s_{22}|^2+|s_{11}s_{22}-s_{12}s_{21}|^2}{2 \cdot |s_{12}| \cdot |s_{21}|} \quad (Eq. 2.10)$$

In bipolar transistors these two frequencies are related by the following relation

$$f_{max} = \sqrt{\frac{f_T}{8\pi \cdot R_B \cdot C_{BC}}} \quad (Eq. 2.11)$$

where $C_{BC}$ is the base/collector capacitance and $R_B$ is the base resistance, which is related to the total base doping.
In order to analyze the limiting factor of the cut-off frequency, a related quantity $\tau_F$ is normally defined as following

$$\frac{1}{2\pi f_T} = \tau_F + \frac{kT}{q} \cdot \frac{C_{EB}}{I_E} + \frac{kT}{q} \cdot \frac{C_{BC}}{I_C} \sim \tau_F + \frac{kT}{q} I_C \cdot \left( C_{EB} + C_{BC} \right)$$  \hspace{1cm} (Eq. 2.12)

Where $\tau_F$ is often denoted as the forward transit time and the second and third terms are referred to as the capacitance charging times for the emitter/base and base/collector depletion regions, respectively. Normally, the forward transit time is divided up in several contributing parts, which in turn can be divided in two groups. First are the transit times for each quasi-neutral region emitter ($t_E$), base ($t_B$), and collector ($t_C$). Secondly, there are the depletion region transit times $t_{EB}$ and $t_{BC}$ for the emitter-base and base-collector depletion regions, respectively. Other parasitic capacitances and resistances also exist but these are not considered in this context.
CHAPTER 3
EPITAXIAL GROWTH

The word epitaxy comes from a Greek root meaning “arranged upon” and it refers to the concept of arranging atoms in single-crystalline form upon a single crystalline substrate. Reduced pressure chemical vapor deposition is one of many technological solutions to grow epitaxial thin films. It is a versatile technique that allows growth of high quality in-situ doped Si, SiGe, and SiGeC films.

This chapter will start by describing the chemical vapor deposition reactor used for depositing all the epitaxial layers in this thesis. The relevant chemical reactions in epitaxy are also explained. This will be followed by a brief discussion of non-selective and selective deposition modes, loading effect during deposition, and incorporation of phosphorus in silicon. This is followed up with a concluding discussion of implementing carbon in SiGe epitaxial layers.
3.1 Chemical Vapor Deposition

CVD Reactor

The epitaxy steps in the device processing were performed in a single-wafer reduced pressure chemical vapor deposition (RPCVD) ASM Epsilon 2000 reactor [Fig. 3.1]. The reactor is divided in three main parts, load-locks, wafer handling and the process chamber. The wafers are transferred from the load-locks to the process chamber onto a silicon carbide coated graphite susceptor by a quartz wand arm. The susceptor compromises of two parts; an inner rotating part where the wafer is positioned during processing and an outer fixed part. The reactor can be converted for deposition on 100, 150 and 200 mm wafers. There are two lamp sets, which radiantly heat up the susceptor. The wafer handling chamber and the load-locks are always purged with nitrogen in order to avoid oxygen contamination.

Reactant gases, which are connected to the reactor, are pure sources of SiH₄, SiH₂Cl₂, HCl, and diluted sources of 10% GeH₄, 1% SiH₃CH₃, 1% B₂H₆, 1% AsH₃ and 1% PH₃ in H₂. In this reactor, H₂ is used as carrier gas. The reactor pressure during deposition can be varied from atmospheric to practically 15 torr.

A scrubber is placed at the exhaust part of the processing chamber to neutralize most of the by-products of the reaction. The remaining gases are burned in a burner.

Figure 3.1 Schematic illustration of an ASM Epsilon 2000 RPCVD reactor [1].
Wafer cleaning

Epitaxial deposition is highly sensitive and easily disturbed by surface contamination. Therefore, the wafers need to be cleaned prior to any deposition. The standard *ex-situ* substrate cleaning procedure used in this thesis is as follows;

1. A solution of H$_2$SO$_4$:H$_2$O$_2$ (5:2) is used to chemically oxidize organic contamination on the surface for 5 minutes and then rinsed in di-ionized (DI) water for another 5 minutes.
2. This is followed by an oxide wet-etch consisting of DI H$_2$O:HF(50%):C$_3$H$_7$OH (100:1:1) for 100 seconds.
3. Finally they are rinsed for another 5 minutes in DI water before they are spin-dried and loaded into the load-locks.

An *in-situ* cleaning is also performed to remove native oxide on the wafer by annealing in a hydrogen flow at 1050°C for 2 minutes and 950°C for 20 minutes for the blanket and patterned substrates, respectively.

Chemical Reactions

The basic reactions for the silicon precursors are as following:

For silane (SiH$_4$) based epitaxy [58]

\[
\text{SiH}_4(g) + 2_\text{M} \rightarrow \text{H} + \text{SiH}_3
\]

\[
\text{SiH}_3 + _\text{M} \rightarrow \text{H} + \text{SiH}_2
\]

\[
2\text{SiH}_2 \rightarrow \text{H}_2(g) + 2\text{SiH}
\]

\[
2\text{SiH} \rightarrow \text{H}_2(g) + 2\text{Si(film)} + 2_\text{M}
\]

For dichlorosilane (SiH$_2$Cl$_2$) based epitaxy [59]

\[
\text{SiH}_2\text{Cl}_2(g) \rightarrow \text{SiCl}_2(g) + \text{H}_2(g)
\]

\[
\text{SiCl}_2(g) + 2_\text{M} \leftrightarrow \text{Si(film)} + 2\text{Cl}
\]

\[
\text{Cl} + \text{H} \rightarrow \text{HCl}
\]

where "_" and M represent an incorporation site and a species absorbed on an incorporation site, respectively.

Germane (GeH$_4$) and/or methylsilane (SiH$_3$CH$_3$) are then introduced into the chamber to grow Si$_{1-x}$Ge$_x$, Si$_{1-y}$C$_y$ or Si$_{1-x-y}$Ge$_x$C$_y$ layers. The germane radicals are created analogously to the SiH$_4$ reactions, while the main radical for carbon incorporation is created through the following reaction [60];

\[
\text{SiH}_2 + \text{SiH}_3\text{CH}_3(g) \rightarrow \text{SiH}_4(g) + \text{SiCH}_4
\]

In the above reaction, a certain amount of SiH$_2$ is essential to produce the SiCH$_4$ molecules. SiCH$_4$ is the main radical required for incorporating of carbon, which is extremely sensitive to the fraction of SiH$_3$CH$_3$ or SiH$_2$. A high partial pressure of methylsilane will lead to carbon radicals that cannot be frozen into substitutional sites and nano-crystallites will be formed and acting as defects [60, 61]. Furthermore,
if the partial pressure of SiH$_4$ is too low the reaction will be distorted creating defects in the layer (see paper 3).

**Non-selective & Selective Epitaxial Growth**

Non-selective epitaxial growth (NSEG) of Si, SiGe, or SiGeC is a deposition process where a film will be deposited all over the substrate [Fig. 3.2b), independent of the exposed areas are single-crystalline, poly-crystalline, or amorphous (e.g. oxide). However, the deposited film will only be single-crystalline if the exposed area has a single-crystalline structure and the deposition temperature is sufficiently high. Film deposited on poly-crystalline area will be poly-crystalline while film characteristics deposited on oxide will depend on the source gases. In the case of silane-based epitaxy, a poly-crystalline film will be deposited on the oxide while germane and dichlorosilane-based [62] epitaxy promote the formation of nucleation on the oxide. Therefore, in order to deposit the non-selective SiGeC layers fabricated in this thesis a 10 nm thick poly-crystalline seed layer was deposited using silane as source gas prior to SiGeC layer. Furthermore, the thickness of the deposited single- and poly-crystalline films are generally not equal. For films deposited at higher pressure, the poly-crystalline film is normally significantly thicker than the single-crystalline film. However, by lowering the pressure in CVD chamber the poly-crystalline layer thickness becomes thinner and the difference vanishes at 20 torr.

Selective epitaxial growth (SEG) of Si, SiGe, or SiGeC is a deposition process where a film will only be deposited on exposed crystalline areas and not on oxide (or nitride) [Fig. 3.2c]. This type of growth can be obtained by introducing HCl to the process gases in order to suppress the formation of nucleation sites on the oxide. However, the presence of HCl will also cause a low deposition rate for the single crystalline silicon, thus it is preferable to apply high growth temperatures. On the other hand, high temperature SEG results in a defect-rich area close to the sidewall oxides [63]. The main reason of these defects is a mismatch between the coefficient of thermal expansion (CTE) of silicon and oxide (CTE$_{SiO2}$=6.0×10$^{-6}$ °C$^{-1}$< CTE$_{Si}$=2.6×10$^{-6}$ °C$^{-1}$< CTE$_{Si3N4}$=3.2×10$^{-6}$ °C$^{-1}$). There are two possible alternatives to reduce the thermal stress:

*Figure 3.2* Schematic illustration of different deposition modes in a RPCVD reactor where (a) represent initial substrate before deposition, (b) represent substrate after a non-selective deposition, and (c) after a selective deposition.
a) Decreasing the mismatch in CTE by nitridization of the thermal oxide (it brings the coefficient closer to nitride) [63].

b) Using low deposition temperature, typically around 770 °C.

Another type of problem, in selective epitaxy is facet formation. These facets are (311) oriented and arise at early stage after deposition of few monolayer. During the epitaxy, the silicon atoms on the (311) planes have a longer diffusion length compared atoms on (100) planes in the middle of the oxide openings [39]. Consequently, a flow of atoms from the edges towards the central part is established. However, due to the limited diffusion length, these atoms cannot cover the whole opening and pile up at edges. Thus, applying a low temperature epitaxy causes a larger pile-up at the edges. Thus, a compromise growth temperature has to be taken to reduce both the pile-up and sidewall defects. Our studies have been shown that growth temperatures around 800°C is an appropriate choice to have a high quality layer with low edge defects.

**Loading effect during CVD**

Previous studies have shown that the growth during CVD on oxide patterned substrates differs from growth on blanket wafers [64, 65]. This effect is denoted by global loading effect and it displays itself as doping, composition, and thickness differences between layers deposited on patterned and blanket wafers under similar conditions. A second related phenomenon denoted as local loading effect occurs within one single wafer such that large and small structures will have different film characteristics. This pattern dependency poses a serious problem in device technology.

It has been demonstrated that the loading effects originate mainly from two factors; thermal and chemical. The thermal effect depends essentially on the emissivity of the substrate, whereas the chemical effect is generated by the difference in diffusion length of the species as well as surface reaction mechanisms. In principle, the global effect can be measured by having a test chip on the patterned wafer with a large opening for SIMS or x-ray measurement. Local loading effect is a more critical subject since the device openings are significantly smaller than the test opening. Introducing a polycrystalline silicon seed layer with thickness of 10-30 nm on the oxide can change both the emissivity and the lateral diffusion of the species. This layer reduces significantly both global and local loading effect [66].
3.2 Results of epitaxy studies

Dopant incorporation in CVD

During CVD, dopant atoms from the precursor gases are adsorbed and dissociated on the substrate surface. These adsorbed atoms will migrate on the surface before they are incorporated into the silicon crystal. In this process, not all atoms will be located in the crystal but some will float on the surface. These surface atoms will act as a dopant source long after the precursor gases have been turned off and this will limit the dopant profile control. This phenomenon is known as segregation and it is a major issue with n-type doping during low temperature chemical vapor depositions at reduced pressure.

The origin of this behavior can be explained by non-equilibrium segregation theory [67]. This theory is mainly based on two principles, namely the chemical and size effect of the dopant atom. The chemical effect can be correlated with the heat of sublimation while the size effect is related to the difference of the covalent radius between dopant and silicon atoms. Table 1 shows these data values for different dopant elements in silicon. Segregation is favored either if the heat of sublimation of dopant atoms is lower than for silicon, i.e., bond-breaking of Si-dopant is easier than that of Si-Si or the dopant covalent radius is larger than silicon. A simple conclusion from this theory indicates that the most common n-type dopants show high segregation during CVD. However, this is strongly temperature dependent since the incorporation is temperature controlled.

<table>
<thead>
<tr>
<th>Element</th>
<th>Covalent radius $[10^{-10} \text{m}]$</th>
<th>Heat of sublimation [Kcal/mole]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>1.1</td>
<td>40</td>
</tr>
<tr>
<td>B</td>
<td>0.82</td>
<td>130</td>
</tr>
<tr>
<td>P</td>
<td>1.06</td>
<td>3</td>
</tr>
<tr>
<td>As</td>
<td>1.2</td>
<td>8</td>
</tr>
<tr>
<td>Sb</td>
<td>1.4</td>
<td>47</td>
</tr>
</tbody>
</table>

*Table 1 Data from [67].*

Our studies have been focused on this issue and also methods to reduce the segregation problem [see paper 1]. Fig. 3.3 illustrates the SIMS profiles of three different samples deposited at 660, 700, and 750°C using SiH₄ and PH₃. The doping profiles in all the cases are 100 nm thick box-like profiles with constant phosphorous doping level followed by a nominally undoped cap layer. As seen, segregation of phosphorous is manifested in all the samples. Similar results have been reported for arsenic-doped silicon layers at these growth temperatures [68]. The figure indicates strong temperature dependence but also that segregation would reduce even further at lower deposition temperatures. However, reducing the deposition temperature
would result in extremely low growth-rate. It is also shown that the segregation is affected by introducing HCl during the growth of the cap layer.

An effective way to remove the segregated atoms from the substrate surface is by ex-situ oxidation followed by a HF dip. This oxidation can be performed either by chemical solutions (e.g. using H$_2$SO$_4$:H$_2$O$_2$ (3:1)) or thermally at low temperatures (e.g. 750°C for 30 min). SIMS results [Fig. 3.4] show the segregated atoms have been removed after such ex-situ surface cleaning procedures. This process has been integrated as a collector in a SiGe HBT structure [Fig. 3.4b].

![Figure 3.3](image_url)

**Figure 3.3** Phosphorous doping profiles with nominal box profile at different growth temperatures using silane as silicon precursor. The sample in (a) are deposited without HCl and samples in (b) with HCl during the deposition. The SIMS curves are plotted so that the turn-on of the profiles coincides.

![Figure 3.4](image_url)

**Figure 3.4** (a) P profiles of ex situ oxidized (chemical or thermal) wafers grown using SiH$_2$Cl$_2$ under SEG conditions with a non-treated wafer for comparison. (b) Epitaxial NSEG Si/SiGe:B/Si profile grown on a thermally oxidized SEG collector profile.
Another way to remove the segregated atoms is applying chemical-mechanical polish (CMP). However, this method is only applicable for SEG of n-type layers. Fig. 3.5a shows AFM top view images and surface profile of the as-deposited collector SEG. There is a significant growth rate difference between the central region and the edge due to pile-up in SEG as previously discussed. Thus, an epitaxial overgrowth is required to efficiently fill oxide windows and insure no voids are formed at the edges of the oxide opening after CMP.

Fig. 3.5b presents the AFM examination of the SEG collector after the CMP procedure. The silicon surface coincides with the surrounding oxide with no apparent defects. Generally, the CMP results in a uniform and planar structure for all device window sizes.

![AFM Image and Surface Profile](image)

**Figure 3.5** AFM image and surface profile of sample after (a) SEG with approximately 40 nm overgrowth, (b) applying a CMP step, (c) depositing a non-selective stack of Si/SiGe/Si structure on the top of sample in (b), and (d) SIMS results from sample in (c).
This sample has been shown after the CMP and NSEG Si/SiGe:B deposition in Fig. 3.5c. The surface profile shows the SiGe:B layer is planar and the epitaxial quality of the active base region appears to be of high quality with no visual defects. Furthermore, a definite boundary between the epitaxial and polycrystalline SiGe regions clearly are distinguished. The SIMS profile of the collector/base stack is presented in Fig. 3.5d. As seen, excellent doping control is achieved for both p-type as well as n-type doping. This indicates that the CMP procedure does not have a significant negative effect on the growth of the SiGe layer.

**Thermal stability of npn and pnp Si/SiGe/Si structures**

Thermal stability and diffusion of dopants are two major problems in the design of SiGe based HBTs. A poor thermal stability of the SiGe layer will lead to strain relaxation and the generation of misfit dislocations. Si/SiGe/Si structures doped in sequences of npn and pnp (transistor-like) have been grown and their thermal stability have been investigated (paper 4). The thermal stability of these structures can be significantly improved by doping the SiGe layer with boron, phosphorus, or arsenic. Moreover, doping the silicon layers adjacent to the SiGe also enhances the thermal stability of the structures. These results have been attributed to a competition between the phenomena of dopant diffusion/precipitation and the misfit dislocation network development in the doped SiGe. The highest thermal stability was obtained in n-Si/p-SiGe/n-Si structures. Furthermore, the thermal stability of these structures were decreased by applying intrinsic silicon spacers grown in presence of HCl between the doped layers. This is connected to the surface roughness caused by HCl. Meanwhile, HCl decreases segregated phosphorus concentration and this consequently results in a less precipitation at the Si/SiGe interface.

**Growth of SiGeC layers**

In epitaxial growth of $\text{Si}_{1-y}\text{C}_y$, the dissociation of the silicon precursor (SiH$_4$ and SiH$_2$Cl$_2$) provides SiH$_2$ or SiCl$_2$ species, which react with the carbon source, SiH$_3$CH$_3$. This chemical reaction generates SiCH$_4$ molecules, which is the main radical for carbon incorporation as described above. A sufficient amount of SiH$_4$ or SiH$_2$Cl$_2$ is thus necessary to obtain optimal carbon incorporation (see paper 3). Moreover, the growth temperature is an extremely sensitive parameter when carbon is incorporated in silicon or SiGe. The Si/C phase-diagram show that the only thermodynamically stable Si-C compound is stoichiometric silicon-carbide. Additionally the bulk solubility of carbon in silicon is relatively low, around $3\times10^{17}$ at the melting point [69]. During growth of thin $\text{Si}_{1-y}\text{C}_y$ films, the bulk solubility is not the critical limitation but rather surface solubility and this can be several orders of magnitude higher. Therefore alloys with substitutional carbon amount exceeding the bulk solubility will be in a meta-stable regime. This means that the growth has to be performed at low temperatures, around 600°C to avoid transformation to the equilibrium state. However once the film is deposited it is thermally stable for temperatures above 1000°C depending on germanium and carbon concentrations and annealing time [23].

Fig. 3.6 illustrates TEM micrographs of a SiGeC multilayer sample deposited at 625°C using constant partial pressure of silane ($P_{\text{Si}}$) and methylsilane ($P_{\text{C}}$) and
increasing partial pressure of germane ($P_{Ge}$). In this figure, the layer thickness are below the critical thickness given in Fig. 2.2. As seen, no extent defects are visible in the first two SiGeC layers while the last SiGeC layer shows clear evidence of defects. These defects are believed to originate from carbon precipitates. A main goal in this investigation has been to minimize defects such as dislocations, precipitates, and carbon interstitials. The defect generation is a result of non-substitutional carbon atoms with minor effect on the strain. Thus, the strain compensation amount between a Si$_{1-x-y}$Ge$_x$C$_y$ sample and Si$_{1-x}$Ge$_x$ reference sample presents a representative picture of the amount of substitutional carbon incorporation in Si$_{1-x-y}$Ge$_x$C$_y$ layers.

The influence of $P_{Ge}$ on the incorporation of substitutional carbon in the silicon matrix has been studied as illustrated in Fig. 3.7a. For low germane partial pressure, the incorporation of carbon was enhanced with $P_{Ge}$ due to increased surface solubility (chemical effect). However, higher amounts of germanium resulted in higher growth rates which lead to an increase in defect density (kinetic effect).

The impact of methylsilane partial pressure on the epitaxial quality was also investigated. Fig. 3.7b shows the influence of $P_{C}$ on the strain compensation of carbon in the Si$_{1-x-y}$Ge$_x$C$_y$ matrix. In this case, both the growth rate and the germanium content were found to be unaffected by carbon integration. The region with defects has been marked in the figure.
Figure 3.6 Transmission electron microscopy of multilayer Si/Si_{1-x-y}Ge_{y}C_{x} stack with different germanium content but constant carbon amount.

Figure 3.7 Impact of germane and methylsilane partial pressure on the strain compensation amount (carbon incorporation). Each data value in the figure represents the amount of strain difference between Si_{1-x-y}Ge_{x}C_{y} and Si_{1-y}Ge_{x} layers.
This chapter will present two SiGeC heterojunction bipolar transistors designs with different collector architectures. In these transistors, the collector layers either were grown selectively or non-selectively by reduced pressure chemical vapor deposition. In both designs, the base region is formed by a non-selective deposition of SiGeC while the emitter is formed by an in-situ phosphorous-doped polycrystalline silicon deposition.

Initial studies to verify the concept and operation of the device were performed by process- and device simulations with the Silvaco VWF tools. After the numerical verification, a nine-mask process was developed in Framework II LayoutPlus environment by Cadence Design Systems to experimentally demonstrate the operation of the device.

The fabrication aspect of these designs will be described in detail.
4.1 Design

Collector design

The collector has to be low resistive to improving high frequency characteristics [70-72]. Another essentiality for the collector is low base-collector capacitance [Eq. 2.12], which requires low collector doping at the depletion edge on the collector side. The industrial approach of dealing with these requirements has been by implementing a selectively implanted collector (SIC) of phosphorus or arsenic beneath the intrinsic base region. By using multiple implantations, the collector profile can be optimized for the desired application. However, this method creates some of its own problems. Namely, the creation of implantation defects which can enhance dopant diffusion [19, 20] and jeopardize the stability of the strained base layer. A potentially superior method for fabricating a desired collector doping profile is by epitaxial techniques.

In this thesis, two epitaxial methods are investigated for the collector region. The first alternative is based on selective epitaxial growth (SEG) of phosphorous-doped silicon in a pre-defined oxide window. The phosphorous doping is $2 \times 10^{18} \text{ cm}^{-3}$ and the collector is approximately 200 nm thick in the transistor structure. Arsenic can be used as an alternative dopant but this is limited to higher deposition temperatures due severe surface roughness of arsenic doped SEG [68]. A common problem with n-type doping during RPCVD is segregation but this problem was solved in chapter 3 by *ex-situ* surface cleaning techniques. Beside segregation, selective growth of silicon also exhibits non-flat topography, e.g. facets are formed during SEG [Fig. 4.1]. This requires that the collector is grown substantially thicker than the surrounding oxide thickness in order to prevent the formation of voids near the periphery of the collector. In the fabricated HBTs, the collector overgrowth was about 100 nm, which provides sufficient lateral epitaxial overgrowth. This overgrowth along with the segregated phosphorous atoms is removed by a chemical mechanical polish process.

![Figure 4.1 Scanning electron microscopy (SEM) image of (a) phosphorous doped SEG with facets and (b) this layer after chemical mechanical polish to remove facets and segregated atoms.](image-url)
The second alternative for the collector is based on high-temperature non-selective epitaxial growth (NSEG) of arsenic doped silicon on blanket wafers. In this case the arsenic doping is $1 \times 10^{18} \text{ cm}^{-3}$ and the collector thickness is approximately 200 nm. This is a relatively high thermal budget process since the LOCOS oxidation process is performed after the collector deposition. This limits the dopant source to arsenic since phosphorous will diffuse significantly during the high-temperature oxidation. Even arsenic will diffusion during the oxidation step, thus the oxidation step needs to be optimized by process simulations. A well-known issue with LOCOS isolation is generation of strain due to encroachment of the oxide into the active device region. This limits LOCOS isolated device structures to relatively large collector widths.

Base design

A requirement for the base is a thin highly doped layer to improve high frequency characteristics [73, 74]. Another requirement for BJTs lies in the fundamental nature of current amplification. This feature of the transistor is directly related to the total base doping level where an increased base doping leads to a decreased collector current and gain [Eq. 2.5]. Reducing the base doping will result in an increased base resistance and reduced maximum oscillation frequency [Eq. 2.11]. A common strategy to overcome this dilemma is by implementing a SiGe base to increase the gain [Eq. 2.6] without reducing the doping level. To increase the cut-off frequency the boron doped SiGe layer has to be as thin as possible in order to reduce the forward transit time [Eq. 2.12]. However, this requirement is inhibited by process issues concerning boron diffusion. For a thin base layer even a small out-diffusion of the boron has a relatively large impact. It has been shown [Fig. 2.5] that a carbon content of 0.2% is sufficient to reduce the boron out-diffusion. Furthermore, the carbon will also have a strain compensation effect, which results in enhanced thermal stability of the strained base layer.

A highly doped thin non-selectively deposited SiGeC base was implemented in the fabricated HBTs in order to reduce the base resistance and obtain a high current gain. The boron doping level is constant $4 \times 10^{19} \text{ cm}^{-3}$, 15 nm thick, and centered in the $20 \text{ nm Si}_{0.818} \text{Ge}_{0.18} \text{C}_{0.002}$ layer. A 10 nm thick silicon seed layer is deposited non-selectively prior to the deposition of the SiGeC layer. This creates the possibility for applying higher growth pressures in RPCVD chamber (20-60 torr) in order to obtain a thicker polycrystalline layer on the oxide compared to epitaxial layer in the oxide opening. The thick polycrystalline layers have lower resistance yielding to higher $f_{\text{max}}$.

Emitter design

The emitter is required to be highly conductive for electrons and designed to provide sufficient barrier for holes injected from the base. Therefore, the highest doping level in a silicon based bipolar transistor for analog applications is normally found in the emitter.

The deployed emitter design in the fabricated HBTs is the common in-situ doped polycrystalline (IDP) emitter. In this case, phosphorous was used as the emitter doping. The presence of carbon in base may interfere with the phosphorous drive-in
process. Thus, the thickness of the intrinsic emitter and anneal temperature has been optimized in order to obtain the designed emitter-base junction [Fig. 2.5]. The optimum thickness of the intrinsic emitter, which is deposited together with the SiGeC base deposition was 15-20 nm and the anneal temperature were 925°C for 10 seconds.

**Device Design**

Two different device designs were fabricated. The major difference between the designs was in the formation of the collector. The first alternative designated as design A has a selectively deposited collector. In this design, the collector was formed after the formation of the field oxide, which was a patterned TEOS oxide. The alternative design designated as design B has a non-selectively deposited collector. In these transistors, the collector layer was formed prior to the formation of the field oxide, which in this case was a standard LOCOS isolation. Fig. 4.2 illustrates a schematic cross-section of the SiGeC heterojunction bipolar transistors with above-mentioned designs.

### 4.2 Device Fabrication

The fabrication of both designs consists of over 50 steps. A summary of the major phases for design A and B is found in Fig. 4.3 and 4.4, respectively and is described below.

1. The process starts with alignment mark definition on p-type Si(100) substrates by a 120 nm dry etch into the silicon. This step is not necessary for design B, as will

![Figure 4.2 Schematic cross-section of (a) designs A and (b) design B HBTs, respectively. In these figure, the NSEG SiGeC layer represent a single non-selective deposition of Si(10 nm) / SiGeC(20nm) / Si(15-20 nm). The following device parameters are defined in the sketch; the emitter width (we), the collector width (wc), the emitter-poly overlap (b). The position of the extrinsic base implantation is also indicated.](image)
be clarified below.

2. This was followed by a dry oxidation step at 900°C to form a 20 nm thick screen oxide for the succeeding arsenic buried collector implantation for both designs. After the buried collector definition the wafers were implanted with arsenic at a dose and energy of $3 \times 10^{15}$ cm$^{-2}$ and 50 keV, respectively. The photoresist was used as the implantation mask.

3. Subsequently, a 260 nm thick TEOS layer replaced the thin screen oxide for design A wafers. After the deposition of the TEOS, the wafers were annealed at 1100°C for 30 min to cure implantation damages. The ambient during the annealing were 5 minutes in dry oxygen and 25 minutes in pure nitrogen.

For design B wafers, the screen oxide was removed and the wafers were wet oxidized at 900°C for 15 minutes and then annealed at 1100°C for 30 minutes and once again, all oxide was removed by a wet etch. The reason for the wet oxidation is to create a height difference between the implanted and non-implanted regions caused by doping enhanced oxidation. The step height, which will be used as alignment mark is approximately 100 nm on the substrate.

4. The next step for design A wafers is to define the collector window by a combination of reactive ion etch (RIE) and wet etch. The bulk of the field oxide was removed by RIE to obtain a vertical etch profile. The remaining part, approximately 30 nm was removed by a 5% dilute HF dip to avoid etch-damages.

For design B wafers were chemically cleaned and loaded into the chemical vapor deposition (CVD) reactor for the collector deposition. A 300 nm non-selective deposition of arsenic doped silicon was performed at 1050°C and 40 torr using chemistry based on SiH$_2$Cl$_2$ and AsH$_3$. The doping level was calibrated by 4-point probe resistivity measurements and SIMS to be $1 \times 10^{18}$ cm$^{-3}$.

5. For design A, the patterned wafers was chemically cleaned and loaded into the CVD reactor for the deposition of the collector. A selective deposition of phosphorous doped silicon was performed at 830°C and 40 torr using chemistry based on SiH$_2$Cl$_2$, HCl, and PH$_3$. Approximately 350 nm of phosphorous doped silicon was deposited with a doping level of $2 \times 10^{18}$ cm$^{-3}$. In order to simplify the process, the collector plug is also deposited during this relatively low doping deposition; however this region will be etched away during the extrinsic base definition [step 9].

The design B wafers was oxidized at 900°C to form a 20 nm thick screen oxide for the succeeding device isolation implantation, also known as junction isolation. The wafers were patterned and implanted with boron at 30 keV and $3 \times 10^{15}$ cm$^{-2}$. The photoresist was used as the implantation mask.

6. Design A wafers was processed by a silicon CMP to remove overgrown silicon, segregated phosphorous atoms, and obtain global planarization.
Design B wafers was striped from the screen oxide and re-oxidized at 1000°C to form a 50 nm thick pad-oxide for the subsequent LOCOS oxidation. The oxidation was followed by 100 nm thick nitride deposition and LOCOS window definition.

7. After the CMP, design A wafers were patterned and implanted with boron at 50 keV and $3 \times 10^{15}$ cm$^{-2}$ to form the junction isolation. The photoresist was used as the implantation mask.

The other design was wet oxidized at 900°C for 8.5 hours to form the 700 nm thick LOCOS field oxide. The pad-oxide and the nitride layer were wet-etched.

From this step both designs have same process flow.

8. After a chemical cleaning procedure all the wafers were returned to the CVD reactor and a stack of Si(10 nm)/SiGeC(20 nm)/Si(15-20 nm) was deposited non-selectively at 625°C and 20 torr. The 10 nm thick undoped silicon layer was used a seed layer for the SiGeC layer. The germanium and carbon content in the SiGeC layer was aimed at constant 18% and 0.2%, respectively. The active base of the device constitutes of 15 nm thick boron layer in the middle of the SiGeC layer with constant concentration of $4 \times 10^{19}$ cm$^{-3}$. The 15-20 nm thick undoped silicon layer will form the intrinsic emitter region after the drive-in process [Step 14].

9. Next, the extrinsic base-poly was defined and etched. This etch step also removed the bulk of the relatively low-doped collector-plug region described in step 5.

10. This was followed by multiple depositions to form the following stack; TEOS(30nm)/nitride(40nm)/TEOS(200nm).

11. After the depositions, the emitter along with collector-plug window was defined by a combination of RIE and wet etch.

12. The IDP emitter was formed by depositing an amorphous phosphorous doped silicon layer at 480°C by using Si$_2$H$_6$ and diluted PH$_3$ (1% in H$_2$) source gases. This layer was crystallized during a one hour anneal at 650°C in O$_2$ ambient.

13. The IDP layer was patterned to form the poly contacts for the emitter and collector. This step was immediately followed by an extrinsic base implantation with the photoresist still on the emitter- and collector-poly. The boron implantation dose and energy were $3 \times 10^{15}$ cm$^{-2}$ and 30 keV, respectively.

14. At this stage, the wafers were deposited with a 300 nm thick oxide and annealed at 925°C for 10 seconds in oxygen to form the intrinsic emitter, and patterned for the contact holes.

15. Finally, a single layer TiW/Al-metallization stack and a forming gas anneal (FGA) at 400°C in an ambient of 10% H$_2$ diluted N$_2$ completed the process.

Cross-sectional transmission-electron microscopy (TEM) of the two fabricated transistor designs and secondary ion mass spectrometry (SIMS) of design A transistors can be seen in Fig. 4.5.
Figure 4.3 Schematic process flow for design A.
Figure 4.4 Schematic process flow for design B.
Figure 4.5 (a) TEM image of device with a selectively deposited collector. (b) TEM image of device with a non-selectively deposited collector. (c) Top-view of transistors. (d) SIMS result of a device with selectively deposited collector.
The primary motivation for the research presented in this thesis was to integrate new collector architectures and a SiGeC base in heterojunction bipolar transistors. Furthermore, to investigate the potential use of such transistors in future high frequency HBTs. During the course of fabrication, several obstacles such as segregation of n-type dopants and the epitaxial quality of the SiGeC were encountered and finally solved. This allowed us to integrate the different modules into a functioning bipolar transistors ready for electrical characterization.

This chapter will initially introduce the electrical characterization methods carried out on the fabricated HBTs. This will be followed by a short discussion of the obtained results from these measurements and their implications.
5.1 Characterization methods

A typical starting point for device characterization is electrostatic measurements to determine the current gain ($\beta$). The current gain is obtained by measuring the collector ($I_C$) and base current ($I_B$) as a function of the forward base-emitter voltage ($V_{BE}$) in a common-emitter configuration. The measurement set-up [Fig. 5.1] to determine this figure-of-merit was such that the base terminal, i.e. $V_{BE}$ was swept by a bias ranging from 0.2 to 1.2 V while the collector was synchronized to the base bias, i.e. $V_{CB} = 0$. The emitter terminal was grounded. Each of the terminal biases was supplied by a high-resolution source/monitor unit (HRSMU), which also allows monitoring of the resulting current at respective terminal. A typical output known as Gummel plot of such a set-up is also shown in the same figure. The Gummel plot, i.e. plot of $I_C$ and $I_B$ versus $V_{BE}$ with the currents plotted on a log scale, is an exceptionally useful tool in device characterisation because it reflects on the quality of several important aspects of the device. First, the electrostatic current gain is defined as the ratio of $I_C$ and $I_B$. Secondly, it reflects on the quality of the emitter-base and base-collector depletion regions with resulting collector ($n_{IC}$) and base ($n_{IB}$) ideality factors differing from unity due to recombination-generation centers [75].

The small-signal high frequency measurements were performed with a HP8510 Vector Network Analyzer (VNA) calibrated by a standard Full SOLT 2-Port technique to remove the influence of the set-up equipment including the waveguides and measurement probes. However, this calibration does not remove the capacitive and resistive influence of the on-wafer pads connecting to the active device. In order to accommodate for this parasitic influence special pad-compensation structures [76] where measured and accounted for in the high frequency measurements.

![Figure 5.1](image)

Figure 5.1 Measurement set-up in a common-emitter configuration to determine Gummel characteristic with a typical output.
The measurement set-up [Fig. 5.2] to determine the high frequency characteristics of a transistor was such that the small signal frequency at port 1 & 2 was swept from 500 MHz to 26.5 GHz at 17 different $V_{BE}$ ranging from 0.8 to 1.0 V and $V_{CB}$ equal to 0 or 0.5 V. The emitter terminal was grounded.

A typical output from a high frequency measurement is seen in Fig. 5.3, where the measured scattering parameters have been converted to the small signal current gain [Eq. 2.7] and the unilateral power gain [Eq. 2.10]. The cut-off frequency ($f_T$) was estimated from extrapolating the maximum current gain down to 0 dB as shown in Fig. 5.3a. Similarly, the maximum oscillation frequency ($f_{max}$) is extrapolated from maximum power gain [Fig. 5.3b]. These extracted $f_T$ and $f_{max}$ frequencies are the maximum available values. A more common figure to present is the collector current dependency of these frequencies; this is obtained by extrapolating these frequencies for each $V_{BE}$ curve in the figure.

**Figure 5.2** Measurement set-up in a common-emitter configuration to determine the high frequency characteristics.

**Figure 5.3** Typical high frequency characteristics with the small-signal current gain presented in (a) and the unilateral power gain is presented in (b). These gain curves are initially increasing with $V_{BE}$ but they will eventually decrease after the maximum available frequencies have been reached.
5.2 Characterization

DC Measurements

Fig. 5.4 shows the Gummel plots of two transistors with a selective (design A) and a non-selectively deposited (design B) collector design, as described in the previous chapter. In order to make a comparison of the influence of the collector design, both transistors were chosen to have identical emitter and base design. In the high bias region, both transistors exhibit similar behavior. Especially, the base current curves for both designs demonstrate a so-called base-current-kink feature at $V_{BE} \sim 1$ V. In the low to medium bias region, the collector currents for both designs exhibit a near ideal behavior with the collector current ideality below 1.02 at $V_{BE} = 0.6$ V and a current gain exceeding 1000. The high gain suggests that the emitter-base junction is formed in the strained SiGeC layer.

The base currents for the two different designs exhibit a small difference in the same region (small to medium bias). The base current ideality factors were calculated to be 1.15 and 1.25 at $V_{BE} = 0.7$ V for design A and B, respectively. This indicates a small surface recombination current and/or a recombination-generation current in the emitter-base depletion region [75] for the transistor with a non-selectively deposited collector. A possible explanation to this non-ideal base current at small biases is an increased defect-density in the SiGeC layer. Transmission electron microscopy (TEM) images [Fig. 5.5] confirms the presence of defects in the collector and base region close to the tip of the LOCOS oxide for design B. Formation of defects in the collector during LOCOS oxidation is a well-known phenomena [77]. These defects in the collector will probably disturb the subsequent growth of the

Figure 5.4 Gummel characteristic at $V_{BC} = 0$ V for transistors with (a) a selectively deposited collector, (b) a non-selectively deposited collector.
strained SiGeC layer. TEM image of design A indicates an increased SiGeC thickness close to the edge of the collector opening, manifesting traces of defects.

These problems are believed to influence the device performance. Therefore, variation of the Gummel characteristics as a function of the collector width ($w_c$) was studied in detail for both designs. In Fig. 5.6, the collector width was allowed to vary between 0.7 $\mu$m and 1.9 $\mu$m. As seen, the collector current for the two designs demonstrates considerable differences. In design A, the collector currents exhibit a near ideal behavior for all collector widths. This is expected for a well-designed collector since the collector current is mainly dependent on emitter and base features [75]. However, there is a decrease in the collector current for the smallest collector width 0.7 $\mu$m, which can be explained by reduced collector efficiency [78] and a smaller effective emitter area due to misalignment of the emitter to the collector window, as seen in the TEM images. In design B, a non-ideal collector current behavior is displayed at smaller collector widths. This verifies the presence of LOCOS induced defects in the collector periphery.

Furthermore, Fig. 5.6 indicate that the base current for the designs A and B has a similar dependency on the collector width, where a non-ideal characteristic is observed for transistors with small collector widths. However, the non-ideal behavior is expected since the emitter-base depletion region extends into the defect-rich extrinsic base-poly region due to misalignment and emitter-undercut. Nevertheless, there is a small difference in the base current at small biases between the designs, which are seen in Fig. 5.7.

![Cross-sectional TEM images for transistors](image)

*Figure 5.5 Cross-sectional TEM images for transistors with (a) a selectively deposited collector, (b) a non-selectively deposited collector.*
Figure 5.6 Typical Gummel plots at $V_{BC} = 0$ V for (a) design A and (b) design B transistors with identical base and emitter design ($w_e = 0.7 \mu m$, $b = 0.3 \mu m$) but varying collector widths ($w_c$). The filled markers represent the base current while open markers represent the collector current.

Figure 5.7 Base current at $V_{BE} = 0.3$ V for (a) design A and (b) design B transistors as a function of $w_c$ and $b$. 
AC Measurements

High frequency measurements were performed as described previously in order to investigate the cut-off frequency and maximum oscillation frequency characteristics of the fabricated devices. Fig. 5.8 shows the high frequency results for two similar transistors with identical vertical doping profile but they are differentiated by the collector design A and B. Both transistor designs demonstrate similar performance with \( f_T \) above 70 GHz at \( V_{CB} = 0 \) V. A significant increase in \( f_T \) is observed at \( V_{CB} = 0.5 \) V, which is attributed to the high collector doping. An additional effect of the collector doping is the observed peak \( f_T \) of 79 GHz occurs at a high collector current density \( J_C \) of 7.9 mA/\( \mu \)m².

The observed low \( f_{max} \) values for the fabricated devices are due to several reasons that include relaxed lateral dimensions, high extrinsic-base resistance, and high base-collector capacitance due to the collector doping level. All of these weaknesses can be solved by using smaller lateral dimensions, applying silicided extrinsic base, and adopt the collector doping for the specific application.

Similar to the electrostatic analysis, the variation of the high frequency characteristics with respect to lateral design was studied in detail for design A. Fig. 5.9 illustrate the maximum available \( f_{max} \) and \( f_T \) as a function of the collector width and emitter design. A significant influence of the lateral design variation is observed for both \( f_{max} \) and \( f_T \). The general trend in these variations is improved device performance as the collector width and the emitter-poly overlap (\( b \)) decrease. For transistors with \( b = 0.2 \) \( \mu \)m, it is observed that \( f_T \) and \( f_{max} \) are linearly proportional to the collector width. This indicates that the limiting factor for these transistors is the base-collector capacitance (\( C_{BC} \)), i.e. the forward transit time \( \tau_F \) [Eq. 2.12] is limited by the base-collector depletion region charging time. For transistors with \( b = 0.7 \) \( \mu \)m, the limiting factor is the extrinsic base resistance (\( R_{Bx} \)).

![Figure 5.8](image)

**Figure 5.8** High frequency results measured at \( V_{CB} = 0 \) V (○) and \( V_{CB} = 0.5 \) V (□) for transistors with (a) selectively deposited collector, and (b) non-selectively deposited collector.
Figure 5.9 High frequency characteristics at $V_{BC} = 0$ V for design A transistors with (a) maximum oscillation frequency and (b) cut-off frequency.
This thesis has focused on design, processing, and characterization of high-frequency SiGeC-based heterojunction bipolar transistors (HBTs). The important five issues presented in this thesis are as following:

- **Epitaxy of collector layers**
  Integrating n-type epitaxially grown silicon layers as collector in HBT structures has been difficult due to high segregation of dopants to the surface during epitaxy. Our results demonstrated that the incorporation of phosphorous increases as the growth temperature is decreased. Introducing HCl to the process gases also improved the dopant profile. However, only thermal or chemical oxidation methods of these n-type layers could effectively remove the segregated atoms at the surface. In case of selectively deposited collector layers, chemical-mechanical polishing method was also used as an alternative to oxidation for eliminating the segregated surface atoms. Our results illustrated that integration of chemical-mechanical polishing does not significantly increase the defect density of the transistor structures.

- **Epitaxy of SiGeC layers**
  Implementation of carbon in selectively and non-selectively deposited Si$_{1-x}$Ge$_x$C$_y$ layers has been studied. It has been shown that the carbon content in silicon increased by decreasing the silane partial pressure or the growth temperature. The quality of the Si$_{1-x}$Ge$_x$C$_y$ epitaxial layers had a strong dependency on the fraction of SiH$_4$ and SiH$_3$CH$_3$ partial pressures. Carbon incorporation was increased with increasing germanium amount (for low amounts). This was saturated at higher germanium levels, which lead to the formation of precipitates and dislocations. The incorporation of carbon in SiGe was explained by the growth rate (kinetic effect) and the chemical effect (surface solubility).

- **Thermal stability of Si/SiGe/Si heterojunction structures:**
  Boron-, phosphorus-, or arsenic-doped SiGe layers showed higher thermal stability compared to intrinsic layers. Moreover, doping the silicon layers adjacent to the SiGe also enhances the thermal stability of the transistor structures. These observations have shown that a competition between the phenomena of dopant
diffusion/precipitation and the misfit dislocation network development in the doped SiGe.

• **Electrical characterization of SiGeC HBTs**
  SiGeC heterojunction bipolar transistors with different collector designs were fabricated and electrically characterized. In these transistors, the different collector designs were grown either by selective or non-selective chemical vapor deposition. The DC characterizations showed base and collector ideality factors of 1.15 and 1.02, respectively, indicating low defect density in the transistor structure with selectively grown collector. High current gain values in the range of 1000-2000 were measured in these transistors. These values showed that the phosphorus drive-in process was performed successfully and the emitter-base junction was formed in the SiGeC base. The HF characterization of the transistors demonstrated $f_T$ and $f_{\text{max}}$ values in range of 40-80 GHz and 15-30 GHz, respectively, depending on lateral design relations. Both $f_T$ and $f_{\text{max}}$ have increased by decreasing the dimension of devices. This is remarkable since the SiGeC layer was grown non-selectively and in the small openings the poly/epi- transition can act as a strong defect source into the intrinsic part of the device. Meanwhile, by fabricating smaller devices the parasitic resistances, which have dominant role in the high frequency behaviour of the transistor were decreased.

• **Leakage current in SiGeC HBTs**
  Source of emitter-base and base-collector junction leakage of the SiGeC transistors with SEG collectors followed by CMP method was investigated. The base-to-collector leakage, which dominates the base current at small biases was found to be size independent. TEM results illustrated the presence of defects near the base/collector poly- and single-crystalline transition region. On the other hand, the emitter-base leakage current decreases as collector width increases, indicating that this leakage originates from the single crystalline SiGeC base periphery. These defects at small collector widths cause an overlapping of the emitter-base depletion region into the defect rich extrinsic base region at the emitter edge.
SiGeC-based technology has still many un-touched or partially-touched topics which can be investigated. A totally self-aligned HBT structure is extremely attractive for high frequency devices. This can be obtained by either selective epitaxy or by an advanced device design. Carbon is definitely a necessary element for decreasing the out-diffusion of boron in the thin SiGe base layer meanwhile it is interesting to investigate its presence in other layers of the device. Diffusion engineering can be achieved by choosing a certain dopant in interaction with carbon since out diffusion of arsenic and antimony is increased in contrary to phosphorous or boron in presence of carbon.

Base-link has the key role for decreasing the parasitic base resistances. In the present transistor designs, the extrinsic base implantation cannot response properly to the demands e.g. the low defect density in the intrinsic base layer. A new extrinsic architecture is needed in this field. The recent approach [9] of forming a selective highly B-doped poly contact is very desirable. This can be applied together with down-scaling of the transistor for improving high frequency performance.

Integration of silicides is always required in these devices to decrease the resistances.
APPENDIX A
MASK DESIGN

The mask layout was developed in Framework II LayoutPlus environment by Cadence Design Systems. It consists of transistors and diodes for electrical measurements, pad compensation structures for calibration of high frequency measurements, structure to determine the base link resistance, Transfer Length Method (TML) structures and Cross Bridge Kelvin structures to measure sheet and contact resistances, SEM lines for cross-sectional imaging, SIMS squares for dopant profiling, and several other structures for the operation of the XLS stepper.

An illustration of the chip design can be seen in Fig. A1.

Figure A1 Schematic of mask layout.
High-resolution x-ray diffraction (HRXRD)

HRXRD technique is a non-destructive method that has been used to characterize the crystal quality, material composition (carbon, germanium), layer thickness, strain amount and relaxation in SiGeC layers. This technique is based on the scattering of an x-ray beam by a crystal sample and analyzing the diffracted beam. The Bragg’s law provides a relation among the distance between parallel crystal planes (d), the x-rays wavelength (λ) and the angle of the incoming beam (θ):

\[ 2d \cdot \sin(\theta) = n \cdot \lambda \] (where n is an integer)

High-resolution one- or two-dimensional x-ray scans were performed by using an Philips X’Pert instrument with Cu Kα1 (λ = 0.1504 nm) x-ray radiation from a four-crystal (220) Ge monochromator [Fig B1]. There is an aperture system after the monochromator in order to adjust the spot size of the incident beam in the range of 100*100 µm² to 1*1 cm². The sample holder can shift along the three directions (x, y, z). In this set-up, the incident and diffracted angles are ω and 2θ, respectively. Φ and Ψ angles are the rotations in- and perpendicular-to-plane.
In these measurements, the diffracted beam can be collected in following two modes:

1) Receiving-slit mode with a slit in front of the detector in order to decrease the acceptance angle of ≈4°

2) Triple axis mode by using a two-crystal collimator in front of the detector to decrease the acceptance angle to 12 arcsec to obtain very high resolution.

Scanning the incident angle, \( \omega \) with fixed 2\( \theta \) (\( \omega \) scan) probes different orientations of planes with a given plane separation, while a simultaneous scan of \( \omega \) and 2\( \theta \) with a rate ratio of 1:2 (\( \omega \)-2\( \theta \) scan) probes different orientations of planes with a given direction. A \( \omega \) or \( \omega \)-2\( \theta \) scan is called a rocking curve. By scanning epitaxial layers e.g. Si/SiGe(C), the Bragg condition will be satisfied for Si and SiGe(C) layer generating two peaks. In these scans some optical fringes also appear, which are originated from interference of x-ray beam in the thin film. The composition can be obtained from the split angle of the layer peak from the substrate and the layer thickness from split of two neighbouring fringes. By applying a mirror in the primary optics the beam intensity is increased remarkably. By decreasing the spot size, a narrow beam with high intensity can be obtained to measure on an array of devices. This creates the possibility to measure directly the Ge or C content and the defect density in the transistor structures.
A two-dimensional high-resolution reciprocal lattice mapping (HRRLM) [79] can be obtained by performing several \( \omega - 2\theta \) scans for a range of incident angle \( \omega \pm \Delta \omega \) as the starting value. In these maps, from the position of the layer peak relative to the substrate peak provides the mismatch parameters and the feature of the peaks illustrate the defect density. The perpendicular and parallel lattice mismatches can be calculated from data obtained from HRRLMs:

\[
\begin{align*}
    f_\perp &= \frac{\Delta a_\perp}{a_\perp} = \frac{a_\text{lay} - a_\text{sub}}{a_\text{sub}} = \frac{\sin \theta_\text{sub} \cos(\omega_\text{sub} - \theta_\text{sub})}{\sin \theta_\text{lay} \cos(\omega_\text{lay} - \theta_\text{lay})} - 1 \\
    f_\parallel &= \frac{\Delta a_\parallel}{a_\parallel} = \frac{a_\text{lay} - a_\text{sub}}{a_\text{sub}} = \frac{\sin \theta_\text{sub} \sin(\omega_\text{sub} - \theta_\text{sub})}{\sin \theta_\text{lay} \sin(\omega_\text{lay} - \theta_\text{lay})} - 1
\end{align*}
\]

where “\( a \)” is a lattice parameter and the indices “\( \text{sub} \)” and “\( \text{lay} \)” stand for the substrate (Si) and the layer (SiGe), respectively. The symbols \( \perp \) and \( // \) refer to in-plane and normal components, respectively.

Then the total mismatch is given by:

\[
f = (f_\perp - f_\parallel) \frac{1 - \nu}{1 + \nu} + f_\parallel \quad \text{where } \nu = 0.278 \text{ for } \text{Si}_{1-x}\text{Ge}_x \text{ and } \text{Si}_{1-x-y}\text{Ge}_x\text{C}_y
\]

and the lattice constant of the compound semiconductors can be obtained from Vegard’s law.

\[
a_\text{layer} = a_{\text{Si}_{1-x}\text{Ge}_x} = (1-x) \cdot a_{\text{Si}} + x \cdot a_{\text{Ge}} \text{ therefore } f = x \cdot \left(\frac{a_{\text{Ge}}}{a_{\text{Si}}} - 1\right) = 0.0418 \cdot x
\]

In fact, this is reliable for low germanium fractions \((x<0.2)\). However, a deviation has been observed from the Vegard’s law and in this case a non-linear variation represent a better approximation [80].

\[
f = 3.67 \cdot 10^{-2} x + 5.03 \cdot 10^{-3} x^2
\]

HRRLM at (113) reflection is very sensitive to reveal the defect generation [81]. The incident beam in these HRRLMs is 2.81°, which provides the possibility to measure a large volume of the layer revealing any minor defects (or relaxation). It makes this type of measurement very attractive for performing an accurate optimization of the growth parameters in a state-of-the-art epitaxial process compared to the ordinary rocking curve measurements.
Secondary Ion Mass Spectrometry (SIMS)

A focused beam of high-energy ions (~15 keV) called primary ions, e.g. $\text{Ar}^+$, $\text{Cs}^+$, $\text{O}^-$ is sent on the surface of the sample to be analyzed. Those ions pull out ions, called secondary ions, from the sample and a small fraction of the secondary ions are analyzed by a mass spectrometer. Concentration can be determined with accuracy ±10%. It is essential to apprehend that this method gives total concentration. In other words, this method does not permit to discriminate substitutional and interstitial atoms.

Atomic Force Microscopy (AFM)

AFM was used in order to study the surface morphology of the samples. The technique is based on the Coulomb force between the probe and the atoms on the investigated surface. The images are generated by sensing the forces on a sharp tip, which is scanned in contact with, or in close proximity to the surface. The tip is located at the end of a thin elastic cantilever, which bends under the forces acting on it. The deflection of the cantilever is monitored by focusing a laser beam on its back surface. The laser beam is reflected via a mirror to a photodiode which detects the position of the laser spot and thereby the cantilever deflection. Three-dimensional positioning of the tip is achieved with a piezo-elements, which elongates or retracts in the z-direction and bends in the x- and y-directions when voltages are applied in different directions across it. A feedback loop is applied to control the z-position of the tip while it is scanned over the surface [82].

Transmission electron microscopy (TEM)

In order to study the crystal quality and defects in the epitaxial layers, cross-sectional TEM has been used. An electron beam with 120 keV energy (medium resolution) passed through a thinned patterned sample. Focused ion beam (FIB) technique was applied to thin the area of sample with the actual device.
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APPENDED PAPERS