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5. Epitaxial growth on on-axis substrates

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Abstract. SiC epitaxial growth using the Chemical Vapour Deposition (CVD) technique on nominally on-axis substrate is presented. Both standard and chloride-based chemistry have been used with the aim to obtain high quality layers suitable for device fabrication. Both homoepitaxy (4H on 4H) and heteroepitaxy (3C on hexagonal substrate) are addressed.

Introduction

Silicon carbide (SiC) is a strong candidate to fulfill the severe demands for several kinds of high functional semiconductor devices such as high temperature, high power and/or high frequency electronic devices. Bulk material can be prepared with e.g. sublimation. However, the quality and purity of the crystal is not at a level requested for the active layers of devices. An epitaxial technique is thus needed for the realization of such layers. The most advanced technique today to achieve the various types of high quality SiC layers needed in all electronic applications is *Chemical Vapour Deposition* (CVD). Already in the end of the sixties, before the invention in bulk growth of the seeded sublimation technique [1], epitaxial growth on small Lely platelets demonstrated the possibility of homo-epitaxy but only at temperatures higher than 1750 °C [2]. This was reported only when using 6H

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polytype as substrate, to the best of our knowledge. At lower growth temperatures (typically below 1500 °C) the 3C polytype of SiC is more thermodynamically stable [3] and twinned crystalline 3C epilayers were obtained during epitaxy. When large area 6H-SiC crystals obtained with seeded sublimation became available, homo-epitaxy could be performed in the temperature range 1400-1500 °C using 3° - 6° off-oriented substrates. This technique named “step-controlled epitaxy” [4, 5] was a breakthrough for the SiC technology. The high density of steps on the surface increases the probability for incoming atoms to maintain the desired stacking sequence [4]. Epilayers of very high quality and with controlled doping suitable for device fabrication were obtained. Substrates of the 4H polytype became available later and rapidly showed better properties than 6H for many applications, the epitaxial growth was found to be more sensitive to defects and polishing damages. A slightly higher growth temperature as well as a larger off-angle (typically 8°) to reduce the terrace widths, was proposed to decrease the possibility of 3C nucleation; this is mainly due to the fact that larger terrace width characterizes the 4H polytype compared to the 6H and this fact increases the probability to get 3C formation on the terraces through a two-dimensional nucleation. A complete review regarding “step-controlled” epitaxial growth can be found in ref [5].

However, as it will be described more in detail below (section 3), the growth on those off-oriented substrates leads to severe problems when used for the fabrication of SiC bipolar devices. Thus the possible “re-introduction” of epitaxy on *nominally on-axis substrate* today gathers researcher’s interest.

Homoepitaxial growth on on-axis C-face 4H-SiC was achieved with good yield when using low C/Si ratio over a whole 2 inch diameter wafer [6]. Compared with Si-face, the C-face material has better polytype stability. However, higher n-type background level and difficulty to control very high p-type doping are the main drawbacks and therefore epilayers grown on C-face are not suitable for device applications. The first attempt to re-investigate the use of Si-face on-axis material for homo-epitaxy was done with 6H polytype and the substrates were only “nearly” on-axis since the off-angle was typically 0.2 - 0.3° [7]. Few works where Si-face 4H polytype was used as substrate, for our knowledge, using CVD technique, are found in the literature; the first presented a study on mesa growth, thus very thin layer on very small area [8] and in a second study morphology after epitaxial growth was reported using different SiC polytypes [9]. In both cases the minimal off-axis was 0.2°. Growth of thicker epitaxial layers has also been successfully shown on 4H C-face and 6H Si-face, while attempts on the 4H Si-face showed large problem with polytype stability and only about 50% stable area was achieved [10].

The first large scale 100% 4H on-axis homoepitaxial growth on Si-face was shown on 2-inch 4H-SiC substrate [11]. In-situ surface preparation in Si-rich conditions prior to the epitaxial growth on mechanically polished substrates together with slightly higher growth temperature was shown to be the key process to avoid the formation of 3C-inclusions [12].

Regarding hetero-epitaxy (growth on 3C on 4H substrate) and using CVD, the main reported investigation was again on mesa [13]; other works used 6H as substrates [14, 15].

After a description of the experimental techniques the growth of nominally on-axis will be presented and discussed both using the standard chemistry during the CVD process and with the chloride based chemistry. This will be discussed first for the homoepitaxy of the 4H polytype. However the growth of 3C on hexagonal Si-face substrate will also be addressed. At the end of this chapter we present the first device results obtained using epilayers grown on on-axis substrate and propose future aspects for the epitaxial growth of SiC.

Experimental

In the Hot-Wall Chemical Vapor Deposition (HWCVD) [16, 17] process reactive compounds (precursors) are transported by a carrier gas (typically hydrogen) to a hot zone (growth temperature as high as 1550-1600 °C) where the precursors will thermally decompose into atoms or radicals of two or more atoms which may diffuse down onto a substrate and produce an epitaxial film. In this process there are several complications: the precursors and carrier gas must be correctly chosen, the flow of the gases must be laminar and the material used for the hot part of the reactor must be chosen with great care in order not to contaminate the system. The growth is performed at reduced pressure typically 100 or 200 mbar. In our case the hot zone is a graphite susceptor coated with SiC which is first heated to about 1200 °C with only the carrier gas as ambient and then a second temperature ramp to the growth temperature is made which can differ depending on the chemistry used, as described in the next sections. No-rotation of the substrate is used in our CVD reactors. We use propane (C_3H_8) or ethylene (C_2H_4) as carbon precursor and silane (SiH_4) for the silicon. Doping can be achieved by adding suitable gas during growth to obtain n-type or p-type conductivity. Control of conductivity (doping level and uniformity over the growth surface) is a key factor for the performance of electronic devices made from epitaxial layers. For the experiments with the standard chemistry a small addition of argon to the hydrogen carrier gas was used and propane was the carbon precursor [16, 17]. When using the chloride based chemistry ethylene

was the carbon precursor; chlorine can be added to the CVD process in various ways as recently reviewed [18]. In our case HCl was added to the standard precursor (SiH_4 and C_2H_4) or methyltrichlorosilane (MTS, CH_3SiCl_3) in the CVD process.

Homo epitaxy on nominally on-axis substrates

The degradation of SiC *p-i-n* junction is now well documented and has shown to be due to the expansion of Shockley-type stacking faults along the off-axis basal plane in the part of the devices reached by the electron-hole plasma [19, 20]. The origins of the stacking faults are basal plane dislocations that are replicated from the substrate into the epitaxial layers due to the off-axis basal plane which is used to maintain the polytype stability during epitaxial growth [21]. Different approaches have been investigated to enhance the conversion of the basal plan dislocations into threading edge dislocations [22] at the epilayer/substrate interface; however those dislocations could also be harmful for devices. In addition, those approaches will introduce additional steps in the device processing including buffer layer growth which could affect cost and yield. An alternative way of avoiding bipolar degradation and epitaxial defects along the basal plane is to abandon off-cut substrates and instead grow epitaxy on on-axis substrates, where there will be no replication of dislocations or other defects along the basal plane [23]. A second aspect will be the lower cost of large-area substrates considering that the boule growth is done on on-axis material and an off-axis angle contributes to a large loss of material after cutting.

Nominally on-axis (0001) substrates as supplied from manufacturers should not have any tilt from the basal plane, therefore epitaxial growth should in principle occur only via three-dimensional growth (islands formation at screw dislocation, and their expansion through lateral step growth at the islands walls). Indeed it often happens that on-axis substrates are not cut out of the crystal boule with no off-angle, even not intentionally, resulting in substrates with small off-cut varying from 0.05 to 0.5°. Besides, due to the growth process of SiC crystals which occurs at very high temperature, a crystal bending during the growth commonly occurs, resulting in a variation of the basal plane angle across the whole wafer area. Substrates often show tiny differences of the off-angle over the wafer area. This will affect growth mechanism as shown below and is evidenced by the morphology of the epitaxial layer [24].

When using on-axis substrates the polytype stability is thus difficult to maintain and typically can result in high concentration of 3C polytype inclusions. The origin of the 3C nucleation can be randomly distributed on

the substrate and thus lower the effective usable area of the 4H material. At the growth temperature (typically 1500-1650 °C) the low diffusion length of the adatoms will favor the formation of 3C inclusions. The 3C formation is mainly due to surface damage from polishing [23] showing the importance of the in-situ preparation of the surface prior the growth. Fig.1.a shows a typical micrograph image of a small 3C inclusion as highlighted by the white circle (the other features observed are due to the various growth mechanisms of the 4H polytype as presented below). This type of inclusion can also be investigated by high resolution synchrotron white beam X-ray topography as shown in Fig.1.b [24]. High density of basal plane dislocations (BPDs) is revealed at the interface between the 3C and the 4H polytype; BPDs are suggested to appear during epitaxial growth in order to compensate the lattice mismatch between the both polytypes [23]. A simple and rapid technique to visualize polytype inclusions in materials is UV emission imaging. The wafer is illuminated with UV excitation using a defocused UV laser line in a liquid nitrogen bath. An example is shown in Fig.2.a for an early epitaxial layer where the black areas correspond to 3C-inclusions while the remaining clear areas are 4H polytype. Fig.2.b shows the possibility to obtain 100% 4H polytype on full wafer. A very important part of this achievement beside the probable improvement of the substrate polishing by the supplier, is the in-situ surface preparation prior to the epi growth on nominally on-axis 4H-SiC substrates and the control of the growth parameters. Depending on the growth process (possibility or not to have chloride in the system) different approaches have been tested.

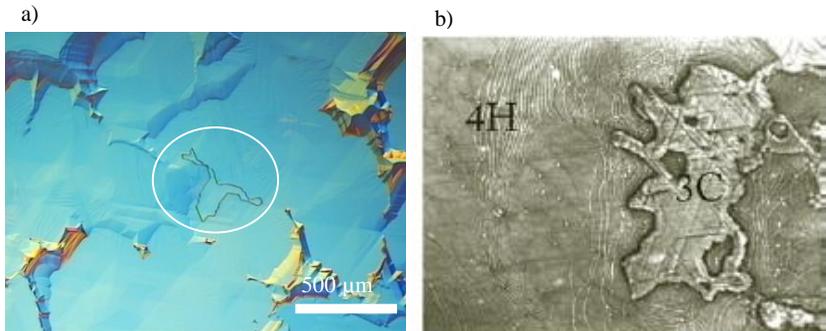


Figure 1. a) Optical image from an as-grown epitaxial layer grown on Si-face nominally on-axis 4H-SiC substrate showing 3C inclusion highlighted in the white circle. The thickness of the layer was 10 μm . b) SWBXT image (corresponding to $2 \times 3 \text{ mm}^2$) showing an inclusion of 3C in a 4H-SiC epitaxial layer. The network of lines around the 3C inclusion shows basal plan dislocations.

Homo-epitaxy with standard chemistry

In situ surface preparation

As received epi-ready substrates are known to have surface damages which could be related to polishing or bulk imperfections. This is confirmed by careful investigation of the substrate surface with atomic force microscopy (AFM) in tapping mode showing damages in form of shallow or deep pits and scratches on the surface [12]. Most of the studies reported in the literature for *in-situ* etching have been done using off-axis substrates. Etching at high temperature with pure hydrogen, which is used as carrier gas, has served as pre-treatment of the substrate prior to the growth to remove surface imperfections. Moreover optimal *in-situ* etching conditions are generally obtained by adding propane to the hydrogen flow when using 8° off Si-face 4H-SiC substrates. This leads to the removal of polishing scratches without leaving any traces of silicon droplets [25]. For on-axis 4H-SiC surface, C-rich condition did not help to avoid the formation of 3C inclusions and resulted in mixed polytypes [23] as illustrated in Fig.2.a.

A systematic study comparing the effect of various etching conditions has been carried out including *in-situ* etching under i) pure hydrogen ambient, ii) C-rich condition ($H_2 + C_3H_8$) and iii) Si-rich ($H_2 + SiH_4$) on Si-face 4H-SiC [12]. Both tapping mode AFM and Normarski imaging were used to characterize the surfaces. The optical images obtained on treated SiC surfaces at $1560^\circ C$ and 200 mbar for 20 minutes are displayed in Fig.3. The

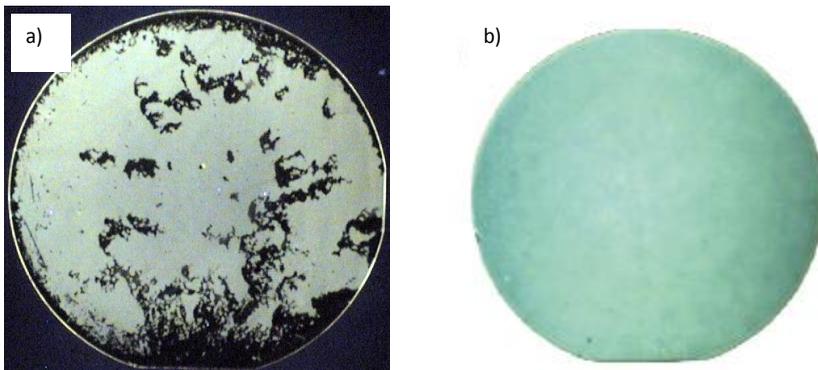


Figure 2. UV polytype maps taken under UV illumination at 77K from two full 50 mm diam. epi-wafer with a) early CVD process and b) improved *in-situ* and CVD process. The black areas visualize the 3C inclusions, whereas the clear areas are from 4H-SiC material.

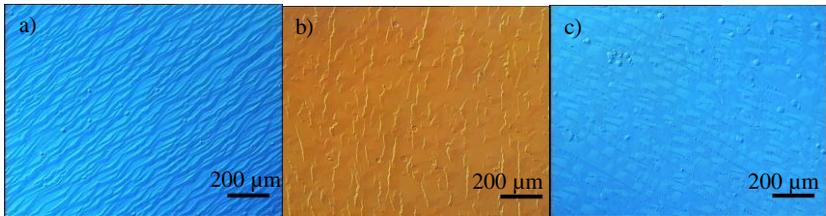


Figure 3. Optical images taken from Si-face (0001) substrate after etching for 20 min at 1560 °C in a) pure hydrogen, b) C-rich and c) Si-rich conditions.

polishing related damages are removed by these processes. Heavy step-bunching and preferential etching at defects originated from the substrate are observed and are due to the high surface energy of the Si-face. In addition the surface step structure is found to be dependent on the ambient etching. Pure H_2 etching results in irregular, zig-zag macro-step structure. Using *in-situ* etching with C-rich conditions irregular macro-steps are also observed, but with discontinuity and rather high surface roughness.

For on-axis 4H-SiC surface *in-situ* etching with Si-rich conditions is found to be the most effective way of obtaining low surface roughness and linear, uniform and periodic macro-step structure [12]. As mentioned before small local tilts in the basal plane or off-angles exist on the surface and are suggested to be the origin of the observed macro-steps. Furthermore, micro-steps with unit cell heights are observed on the surface. Threading screw dislocations (TSDs) can intersect on the surface being the main source for the micro-steps. These micro-steps extend far away from the dislocation providing a continuous distribution of steps at the surface. In addition, Si-droplets which are expected when using *in-situ* etching with Si-rich conditions due to high over pressure of Si containing species in the gas phase were never observed in this study [12].

Starting growth conditions

After the *in-situ* etching, the condition at the beginning of the growth is another very important parameter to understand and control. Most of the epilayer defects as the 3C inclusions nucleate at the interface substrate/layer and they continue to evolve during the epilayer growth [24]. An abrupt change in the gas phase can enhance defect formation. During the surface preparation a negative growth mode (etching) occurs which should be changed to positive growth mode by adding the precursor. This step may cause the formation of defects if not done in a proper way. A very slow and

gradual change in the gas phase has to be applied. Supersaturation is the driving force for both nucleation and layer growth. Moreover it should be as low as possible in the case of homo-epitaxy of 4H-SiC on on-axis substrate. This is to avoid the two dimensional nucleation of the unwanted 3C polytype. The precursors have to be introduced into the growth chamber with very small flows which slowly and progressively are increased to the desired value for the growth. This operation, starting of the growth, typically takes 20 minutes [11]. The initial growth rate is thus extremely low but allows the nucleation of only 4H material (few hundred of nm), and it can be increased to about 3-4 $\mu\text{m/h}$ for the main part of the epilayer growth. The C/Si is, in our case, always very close to 1 during this operation.

Growth mechanism

Epitaxial growth occurs always at steps, when it is not due to a two dimensional nucleation. On the same substrate we could observe for the first time two different types of growth mechanism [11]. Both of them appear at steps but having different heights. When the substrate is nearly on-axis the only steps available are related to the TSDs, as described before. It is on those steps that the growth will occur and it defines as spiral growth. Illustrations are given in the inset of Fig.4.a and Fig.4.c which are tapping mode AFM images taken from a Si-face epilayer grown on on-axis substrate. The spiral growth mode is characterized by the observation of smooth islands (Fig.4.a) and even large terraces (Fig.4.c) where the density of TSDs is supposed to be low. However when the basal planes are slightly off, with probably a very small angle as only 0.3° , the growth turns to step growth mode as for the intentional off-cut material, and large irregular steps, step-

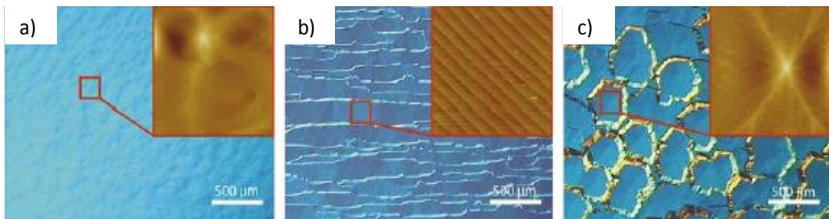


Figure 4. Optical images taken on three different locations on the same 10 μm thick epilayer grown on nominally on-axis substrate showing a) very smooth morphology with spiral growth mechanism, b) rough surface due to step growth mechanism and c) very rough morphology with high step due to spiral/columnar growth. The insets show tapping mode AFM $100 \times 100 \mu\text{m}^2$ area with associated roughness of a) 4 nm, b) 1 nm and c) 40 nm.

bunched surface, are observed. However on those large steps the surface is very smooth and covered with macro-steps (see inset of Fig.4.b). Mixing of these two growth modes is also observed. We observed that the surface roughness as measured with AFM increased with the thickness of the layer; typically for a 40 μm thick epilayers, macro-step height could reach over 100 nm.

Temperature effect

As described before the 3C nucleation is favored by the low diffusion length of the adatoms on the grown surface. Increasing the growth temperature helps to enhance the mobility of the adatoms on the surface, lowering the probability for a two dimensional nucleation of 3C. Typically when the growth temperature used in our reactor was 1580 $^{\circ}\text{C}$ for epitaxy on 8 $^{\circ}$ off-axis substrate, it was increased to 1620 $^{\circ}\text{C}$ for the growth of homo-epitaxial layer on nominally on-axis substrate.

Using the in-situ etching to obtain micro-steps on the surface together with a slightly higher growth temperature and an initial low growth rate, we were able to grow thick epitaxial layer with complete 4H polytype replication on a nominally on-axis substrate using the standard non chlorinated chemistry. This has been both on 50 and 75 mm diameter wafers (the latest corresponding to the maximum growth area on our reactor) and for 12 μm thick epilayers. For the smallest diameter substrates, epilayers with thicknesses up to 40 μm have been demonstrated with 100% 4H polytype (Fig.2.b as example).

C/Si ratio and growth rate effect

After in-situ etching better surface morphology, meaning lower roughness of the surface, is achieved when using Si-rich conditions (see section 3.1.1). This behavior could indicate that Si-rich conditions during growth could also help to obtain lower surface roughness. The effect of the C/Si ratio on the surface morphology has thus been studied; homoepitaxial growth was performed using various C/Si ratio in the range 0.8 - 1.2. Outside this range 3C formation was easily observed in the epitaxial layer. Within this range of C/Si ratio, the roughness was found to decrease when decreasing the C/Si ratio. For an area of 100 x 100 μm^2 , roughness of less than one nm was obtained for 10 μm thick epilayers, whereas for thicker layer (35 μm) the roughness was around 2 nm. The roughness was thus found to increase with the epilayer thickness [26].

Low supersaturation at the beginning of the growth and thus very low growth rate were found to be necessary for polytype stability. With low

growth rate increased probability of growth process related problem such as down falls from the susceptor ceiling is expected. This could give rise to perturbation of the growth and thus to 3C inclusions. As on-axis homoepitaxy is intended for high voltage bipolar devices, very thick (more than 50 μm) and low-doped (less than 10^{15} cm^{-3}) layers are requested. High growth rate is simply needed. We succeeded to increase the growth rate from 3 $\mu\text{m/h}$ to 10 $\mu\text{m/h}$ by increasing the silane flow but also by decreasing slightly the process pressure, keeping 100% 4H homoepitaxy with roughness of 2 nm for a 100 x 100 μm^2 area [26]. Higher growth rates led to very rough surfaces and 3C nucleation.

Chlorine based homoepitaxy for nominally on-axis material

The importance of adding chlorine into a CVD reactor for the growth of SiC on on-axis substrates was investigated by Xie *et al* in 2000 [27]. Although 6H (0001) substrate was used, homo-epitaxy was demonstrated at 1475 °C; the addition of HCl during the growth (and not only prior the growth) was suggested to provide stepped surface where the step-controlled epitaxy could occur. The growth rate was found to slightly decrease (from 1.8 to 1.3 $\mu\text{m/h}$) when adding HCl to the process with a high HCl/Si ratio of 50. HCl was also reported to etch preferentially 3C- over 6H-SiC. However surprisingly, no work regarding 4H homo-epitaxy has been reported by the same author's group or other, to the best of our knowledge.

More recently chloride-based CVD for SiC has been proposed and used to achieve high growth rate on off-axis substrates [see a recent review in Ref.18]. The presence of chlorine is necessary at high growth rate to prevent silicon cluster nucleation in the gas phase, which usually occurs at high Si/H₂ ratios. Various chloride based chemistries have been used for SiC: i) adding HCl gas to the standard chemistry, ii) replacing the silane by a chlorinated silane molecule, iii) replacing the carbon precursor by a chlorinated carbon molecule, or iv) using a precursor which contains both chlorine, silicon and carbon (see ref [18]). Chlorine has been successfully used to achieve homoepitaxial growth of SiC also on on-axis substrates at rates of 100 $\mu\text{m/h}$ as described below. Besides it has been found out that chlorine addition in the CVD process widens the operating window of parameters allowing such homoepitaxial process. Below follows a description of the main parameters which could be tuned to achieve a chloride-based process for the homoepitaxial growth of 4H- or 6H-SiC on (0001) substrates: *in situ* treatment; temperature; Cl/Si ratio; C/Si ratio; precursors, substrates off-angle and growth rate.

In situ surface preparation

The two most successful surface preparations suitable for the chloride-based process are based either on heating up in pure hydrogen atmosphere followed by very silicon rich growth conditions [28], or on the silicon rich in situ etching [29], similar to the case using non-chlorinated CVD process as described before [12].

In the first case ramping up in pure hydrogen is necessary simply to promote desorption of contaminations or oxide formed on the surface. Experiments with HCl *in situ* etching have been performed as well, but they have not been proved to be really beneficial for our process, contrarily to various reports in the literature [30]. In such a case, where no special surface treatment is performed, the growth parameters at the very beginning of the growth are critical for a successful homoepitaxial process. Since this process requires very silicon rich conditions in order to suppress those nuclei which could start the formation of any 3C inclusion, a very low C/Si ratio (down to 0.3), and very high Cl/Si ratio (up to 30) were required when growing at 1600 °C. A slow ramp up of the precursors ($\text{SiH}_4 + \text{C}_2\text{H}_4 + \text{HCl}$ in H_2) while keeping the proper ratios was mandatory to keep polytype control either on 4H or 6H-SiC (0001).

In the second case SiH_4 has been used for *in situ* etching of the on-axis surface. 10 minutes etching with a Si/ H_2 ratio of 0.12 % at the growth temperature of 1600 °C was performed. Such a preparation probably renders the surface silicon terminated, and modifies it in a way that promotes only two-dimensional growth starting from steps existing on the surface, due to either a small off-angle or to the presence of screw dislocations. In this way it is possible to use a wider range of C/Si- and Cl/Si-ratios, which are important to tune the growth mode, and to allow raising the precursor concentration in order to get a higher growth rate.

Comparing the two etching procedures and the related growth conditions, the first procedure keeps a growth environment permanently silicon rich, but the high amount of chlorine produces a parallel etching, which is competitive to the growth. The second procedure creates the proper silicon rich condition at the very early stage of the process, making such conditions less critical during the growth process itself.

Temperature effect

When silicon *in situ* etching is not used, very high Cl/Si ratios up to 30 are needed at 1600 °C to obtain homoepitaxial growth. At a higher temperature this ratio can be reduced (Cl/Si = 20 at 1680 °C) while still

obtaining a 100% 4H homoepitaxial layer free of 3C inclusions, thanks to the increased polytype stability. With such conditions and a C/Si of 1.5 we demonstrated the growth of a 100 μm thick 4H-SiC epilayer. The high quality of this layer can be easily inferred from the low temperature photoluminescence (LTPL) spectrum showed in Fig. 5. The near-band gap emission was the dominant luminescence and contains mainly intrinsic (free-exciton) related lines and from this spectrum a net carrier concentration in the low 10^{13} cm^{-3} was determined.

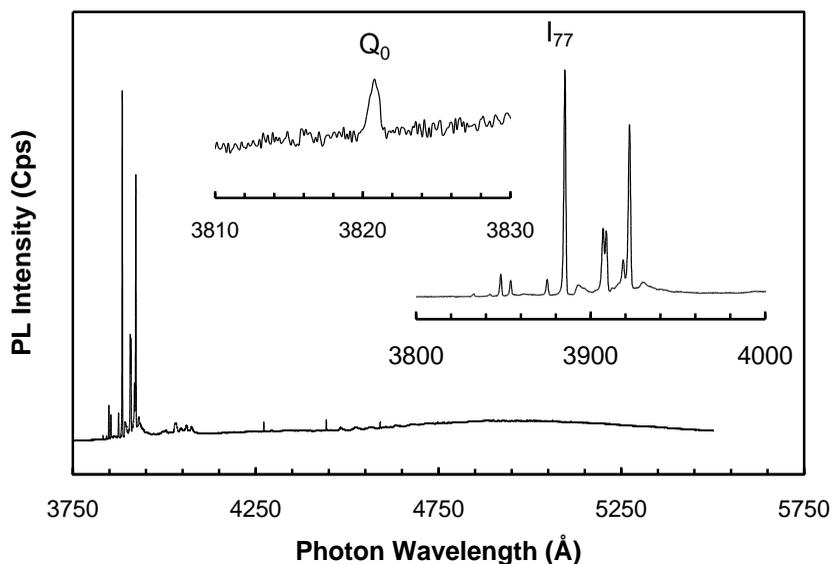


Figure 5. Photoluminescence spectrum a 100 μm thick 4H-SiC epitaxial layer grown at 1680 $^{\circ}\text{C}$ with a growth rate of 25 $\mu\text{m}/\text{h}$. The insets show first the near band gap emission with free-exciton lines as dominant (as p.e. I_{77}) and then the nitrogen bound exciton related lines Q_0 to be negligible (intensity increased with a $\times 100$ scale compared to the rest of the spectrum). The measurement was done at 2K with a 244 nm excitation laser. In the extended spectrum weak luminescence from the D_1 is also observed as well as from Ti related lines, Ti incorporation being due to crack in the susceptor coating.

Cl/Si ratio influence

Epitaxial growths performed without special surface preparation or any low C/Si ratio process, have put in evidence how an increased amount of chlorine reduces the formation of 3C inclusions formed on an epilayer. As

shown in Fig. 6, higher amount of HCl added to SiH_4 and C_2H_4 reduces 3C inclusions, and even the use of a chlorinated precursor, such as CH_3SiCl_3 (MTS), added with HCl can give 100% 4H-SiC homopolytypic growth [31].

This trend has been confirmed in several growth conditions on on-axis substrates, and it is explained by the change in gas-phase chemistry due to the presence of chlorine. Thermodynamic and kinetic calculations demonstrated that higher amount of chlorine lead to an increased formation of SiCl_2 , which is the key silicon precursor formed in the gas phase to contribute to the growth.

As discussed above, the main advantage of chloride-based CVD is the feasibility of achieving higher growth rates. Combining this process with the silicon-rich *in situ* surface preparation, a growth rate up to $100 \mu\text{m/h}$ was obtained [29].

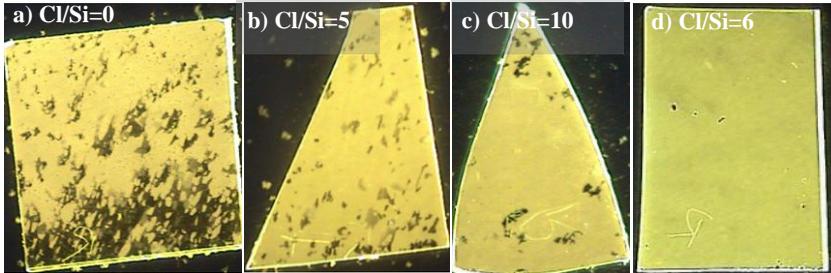


Figure 6. $20 \mu\text{m}$ thick epitaxial layers at 77 K illuminated by UV-light. Growth at 1600°C with $\text{C/Si} = 1$ and a) $\text{Cl/Si}=0$; b) $\text{Cl/Si}=5$; c) $\text{Cl/Si}=10$; using $\text{SiH}_4+\text{C}_2\text{H}_4+\text{HCl}$ and d) MTS precursor with HCl addition and $\text{Cl/Si}=6$. 3C-SiC inclusions appear as dark spots on the samples. The samples have an area of about $20 \times 20 \text{ mm}^2$.

C/Si ratio effect

As it happens for the epitaxial growth on off-axis substrates, the C/Si ratio is a determining parameter for the epitaxial growth since it affects directly the growth mode, and therefore the doping incorporation. Its required value to get an on-axis homoepitaxial layer depends on the other growth conditions but, as a rule of thumb, generally silicon rich conditions are usually preferred for the growth on on-axis substrates, since the 3C-SiC polytype is favoured by high carbon partial pressure.

When higher growth rates are desired, the C/Si ratio should be generally kept below 1, unless chlorinated precursors such as MTS are used. The background doping is affected by this ratio as explained by the site-

competition epitaxy theory, according to which higher C/Si ratios reduce n-type dopants incorporation [32].

The choice between various precursors

The various chlorinated precursors can have a very different gas-phase chemistry, which has been demonstrated both from an experimental and theoretical (simulations) [18] point of view. For off-axis epitaxial growth MTS was found to be the most efficient precursor. Similar behaviour has been demonstrated for epilayers grown on on-axis substrates while keeping a total control of the polytype. As mentioned above, a growth rate of 100 $\mu\text{m/h}$ has been demonstrated for the growth on 4H-SiC (0001) substrates, using MTS as precursor. The other parameters were: *in situ* etching with SiH_4 , $T = 1600\text{ }^\circ\text{C}$, $\text{C/Si} = 1$, $\text{Cl/Si} = 3$, $\text{Si/H}_2 = 0.66\%$. The same result could not be achieved when using $\text{SiH}_4 + \text{C}_2\text{H}_4 + \text{HCl}$.

Growth rate influence

As a final example of the great potential of chloride-based CVD on on-axis SiC substrates, it is worth mentioning the outstanding results obtained in a vertical hot-wall CVD reactor using such a process [33] as an example of process tuning for high growth rates. Selecting as precursors either $\text{SiH}_4 + \text{C}_2\text{H}_4 + \text{HCl}$ or $\text{SiHCl}_3 + \text{C}_2\text{H}_4 + \text{HCl}$, the chloride-based process has made possible to grow up to 1 mm thick epilayer on 4H or 6H on-axis substrates with growth rate up to 350 $\mu\text{m/h}$ at temperature of 1850 $^\circ\text{C}$. At such high growth rates polytype stability gets more challenging; high Cl/Si ratio (5 – 10) and low C/Si ratio (0.3 – 0.5) were employed in this process, but difficulties with etching effect and 3C inclusion were eventually solved. In fact the amount of 3C inclusions increases with higher growth rates, but keeping a low C/Si ratio and increasing the Cl/Si proportionally helped to avoid them. Yet etching effect occurs at Cl/Si ratio of 10 or higher, therefore at moderate Cl/Si of 7, the use of a chlorinated precursor such as SiHCl_3 was the key to get growth rate at 350 $\mu\text{m/h}$.

Hetero-epitaxy on nominally on-axis substrates

The growth of structures consisting of different SiC polytypes is a challenge for new applications such as resonant tunneling, but remains to be experimentally explored. The growth of 3C on on-axis grown 4H epitaxial layers could give device benefits with respect to MOSFETs (superior inversion channel mobility and reliability). In addition two-dimensional

electron gas (2DEG) was predicted [34] to be formed at the hetero-junction 4H/3C or 6H/3C SiC due to abrupt change in spontaneous polarization between the cubic and the hexagonal SiC. However this challenge needs to resolve the problem with high defect level resulting from the hetero-polytypical growth, such as twin-boundaries and, the growth of such structures demands different nucleation conditions for each of the polytype forming the structure. 3C layers can be grown on the most common SiC hexagonal-polytype substrates, which has been demonstrated by vapor-liquid-solid (VLS) [35], sublimation epitaxy [36] and chemical-vapor-deposition (CVD) [14, 15]. However, those studies have used mainly nominally on-axis 6H-SiC as substrate. The use of the 4H polytype seems thus to be an additional challenge. We will here describe the recent work using 6H as substrate and the chloride based chemistry as growth technique and then the standard chemistry using 4H Si-face on-axis substrate.

Hetero-epitaxy using 6H as substrate with chloride based CVD

One of the main potential of chloride-based CVD is to prevent silicon nucleation in the gas phase which can occur either at high precursor concentration, or at low growth temperatures (below 1400 °C) [37]. This has been proved to be beneficial also for the growth of good quality 3C-SiC on hexagonal SiC substrates [38]. As discussed above, 3C-SiC is more thermodynamically stable at lower temperature (below 1500 °C), therefore it can be grown at temperatures lower than those used for 4H and 6H-SiC. In order to get 100% 3C-SiC on hexagonal SiC substrates, on-axis material is preferred, in order to favor islands growth.

Chloride-based CVD has been tested mainly on 6H-SiC (0001) [39]. In our group we have found an optimal temperature window to grow 3C on 6H (0001) which is between 1300 and 1400 °C [38]. A higher temperature makes very likely the formation of 6H, while lower temperatures lead to lower crystal quality. Different surface preparations have indicated the importance of using carbon rich conditions, as already done when growing 3C on silicon substrates in the so-called carbonization process. Using other gases for the surface preparation, such as silane or pure hydrogen, brings more chance to get 6H, while HCl seems to be more favorable to 3C. Growths with different C/Si ratios and Cl/Si ratios have indicated that silicon rich conditions are ideal to get higher quality 3C. Cl/Si ratios between 3 and 6 were optimal for such process; higher values were detrimental from a growth rate and quality point of view. C/Si ratios from 0.6 to 0.9 were more suited to the process, because higher carbon inputs gave rise to defects, while lower carbon amounts gave rise to very high background doping levels. A final

improvement to the process, necessary to favor single domain 3C to be formed, instead of the very common double-position-boundaries (DPB), was to add some nitrogen in the gas mixture, since it seems to stabilize one domain. 3C-SiC epitaxial layers almost completely single domain were grown at a rate of 10 $\mu\text{m/h}$ using: C_2H_4 flow during temperature ramp up; $T = 1365^\circ\text{C}$; $\text{C/Si} = 0.75$; $\text{Cl/Si} = 6$; and a small nitrogen flow. Small addition of nitrogen during the growth was proposed to help to stabilize the 3C-SiC polytype even when the growth conditions were not favoring the formation of 3C [40].

The material grown in this way was characterized optically and electrically. Electron back scattering diffraction (EBSD) was used to evaluate the presence of DPBs, indicating that the layers grown at the best conditions were 90% made of a single domain, as illustrated in Fig. 7.

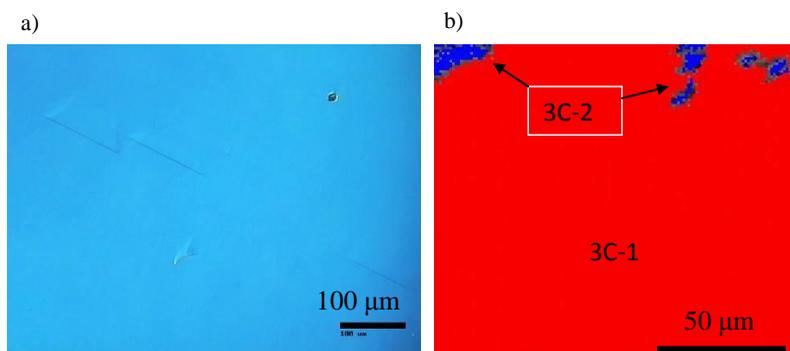


Figure 7. a) Optical microscope image and b) EBSD image of a 3C epilayer grown on on-axis 6H-SiC at 1365°C . 3C-1 and 3C-2 indicate the domains with two possible orientations tilted with 60° .

Hetero-epitaxial growth on 4H substrate by standard chemistry

The substrates used here were n-type doped nominally on-axis 4H-SiC materials. In order to get lower net doping concentration, Si-face of the substrates was chosen for the growth. Standard chemistry (SiH_4 and C_3H_8), was used at a pressure of 200 mbar. Important growth parameters, such as temperature, C/Si ratio, starting-up condition, were varied to investigate their influence on the 3C formation.

The growth temperature is one of the most important parameters that influenced the obtained epilayers' morphology. After testing between 1200°C and 1500°C , 1350°C was found to be the most suitable temperature for

growing single domain 3C-SiC epilayer. When the temperature was lower than 1325 °C, the epilayer surface was carbonized and it appeared as dark brown. Polycrystalline surface was observed, when 1375 °C or even higher temperature was used.

C/Si ratio equals 1 seems to be the best condition at 1350 °C. Silicon droplets or even clusters appear at C/Si ratio higher than 1.1 and below 1400 °C. Polycrystalline material appears when C/Si is less than 0.9.

C-rich surface preparation was found to favor the growth of 3C layers. Two ways of starting-up conditions were shown to be useful to effectively reduce DPBs. One is to do an optimal time of in-situ etching right after reaching the growth temperature. The other method is to flow certain amount of C₃H₈ from room temperature to the growth temperature before introducing any Si precursors. The amount of C₃H₈ used during temperature ramp-up should be comparable with the flow used during growth. If the flow is not enough, the DPBs problem could not be solved. But too much of C₃H₈ flow will cause even higher density of DPBs and also apparition of other surface defects probably carbon related. This is similar to the first method, which will lead to bad morphology for both too short and too long etching time.

The growth rate varied from 2 to 6 μm/h, which was mainly governed by the SiH₄ flow. Layers with thicknesses from a few micrometers up to 50 μm were grown. The sample with the best obtained results (see fig. 8) was grown on a 2x2 cm² substrate at 1350 °C, 200 mbar with C/Si = 1 and 5 min in-situ etching with C ambient before growth and a small addition of nitrogen gas (N/C = 0.4 %). The stripes shown in this picture could be stacking faults [41].

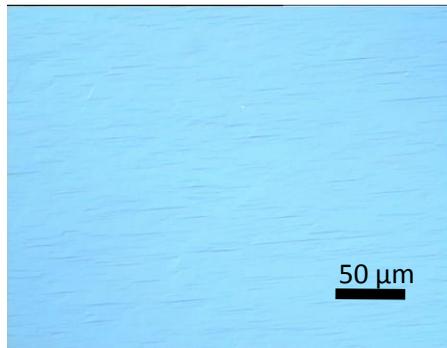


Figure 8. Optical microscopy images at 400x magnification of 3C-SiC epilayers deposited at 1350 °C on (0001) 4H-SiC substrates with C/Si = 1, N/C = 0.004, Si/H₂ = 0.015 % with 7 ml/min propane in-situ etching for 5 min. The epilayer thickness is 12 μm. The surface roughness is 0.94 nm in a 10x10 μm² area.

This feature becomes more pronounced when the epilayer is thicker. EBSD technique confirmed that the whole layer was single domain 3C-SiC. The net doping concentration measured by Hg probe CV was $5 \times 10^{16} \text{ cm}^{-3}$ at room temperature which was confirmed by LTPL. For most samples, the near-band gap emission was detected. No donor-acceptor pair recombination was observed, but weak D_1 related luminescence was detected [42]. The RMS roughness examined by AFM was 3 to 8 nm at $50 \times 50 \text{ } \mu\text{m}^2$ for most of the samples.

Device related issues

As the main goal of this work is to obtain high quality layers suitable for device fabrication, first tests have been conducted for both homo-epitaxial and hetero-epitaxial material.

Homo-epitaxy material as device material

A first complete device structure including a low doped n-type $30 \text{ } \mu\text{m}$ thick active layer and a heavy p-type layer was grown without interruptions, and simple PiN diodes were processed, which showed stable behavior without bipolar degradation and stacking fault formation [43]. However no reverse characteristics were presented and the forward voltage drop was relatively high. More recently 600V PiN diodes were fabricated using on-axis material, the active layer being only $10 \text{ } \mu\text{m}$ thick. [44]. Those diodes also showed stable forward characteristics without stacking fault generation and were compared with diodes done with the same device process but using off-axis material; stacking fault generation was rapidly observed as well as an important forward voltage drift [45]. However as the epitaxial growth mechanism on on-axis 4H SiC substrate includes both spiral growth and step growth mode, high roughness of the grown surface is observed on a very large scan with both the standard and the chloride based chemistry approaches. An example is given in Fig.9 where steps as high as almost $2 \text{ } \mu\text{m}$ are observed for a $17 \text{ } \mu\text{m}$ thick epilayers grown with the Cl based process. Similar results are obtained when using the standard chemistry process and on $100 \text{ } \mu\text{m}$ thick epilayers steps as high as $7 \text{ } \mu\text{m}$ have been measured. This will affect both the mesa thickness control and the PiN junction planarity during the processing of devices. This is the main reason why high mesas with a height of $8 \text{ } \mu\text{m}$ were needed. Higher surface state density is suggested to decrease the resulted break down voltage [44]. Additional steps for the realization of the epilayer structures are thus needed; planarization of the active layer prior to the re-growth of the p+/p++ layers. If the latter (regrowth)

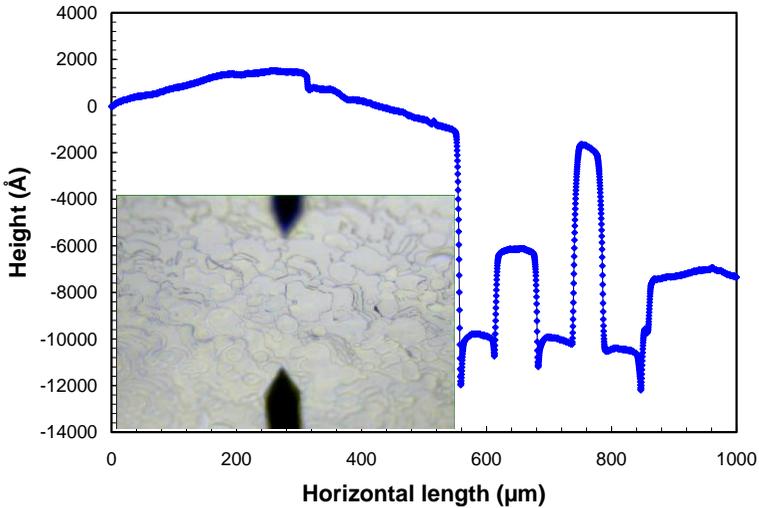


Figure 9. Roughness of a 20 μm thick epilayer grown on on-axis substrate and measured with a surface profiler, (Dektak 6M). The inset is a view obtained with this profiler.

can be easily demonstrated as it was for off-axis material [46] and the first step (planarization) involving polishing and surface preparation is still a drawback. To resolve this problem the spiral growth should be avoided and very low off angle substrate would be the more appropriate substrate where only step growth mode will dominate the growth mechanism, as recently demonstrated [47].

Hetero-epitaxy material as device material

Epilayers grown with the chloride based chemistry have been used for the fabrication of single Schottky diode. The epilayers were doped in the mid 10^{15} cm^{-3} range, very low leakage current of $1.5 \times 10^{-8} \text{ A/cm}^2$ at a reverse voltage of -2V was measured on such layers. Deep level transient spectroscopy (DLTS) analysis showed higher quality material compared to 3C layers grown on silicon substrates, which instead showed a number of peaks related to deep level defects [48]. It should be noted that the epilayer thickness should be high enough, typically more than $10 \mu\text{m}$, to reduce the DPB density. This could limit the interest of 3C as material for device application. High DPB density is equivalent to high probability to locate a device on grain boundary which leads to high leakage current and non-ideal”

Schottky behavior [41]. In addition the defect density, mainly the stacking fault density should be reduced. Comparative studies using 3C epilayers grown with different techniques have proved that the epilayers grown with the chloride based chemistry have an order of magnitude less defect density than material grown with other techniques [49].

Conclusions

Homo-epitaxy of 4H-SiC on nominally on-axis substrate is demonstrated using chemical vapor deposition with both the standard and the chloride based chemistry. The standard chemistry which was first applied, has rapidly shown the importance of the *in-situ* preparation and starting condition of the growth. This has been confirmed by the chloride based chemistry which in addition allowed higher growth rate. However due to high roughness of the grown layer, material with vicinal small angle ($0.3 - 1^\circ$) should be tested for bipolar application. Hetero-epitaxy of single domain 3C on 4H-SiC on-axis substrate is also possible; the growth parameters window is however smaller when using standard chemistry compared to chloride-based CVD. To obtain single domain without double-position-boundaries thick enough layer is required, however more efforts are needed to decrease the stacking fault density and demonstrate the use of this hetero material in device application.

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