Chemical Vapor Deposition of Si and SiGe Films for High-Speed Bipolar Transistors

Johan Pejnefors

KTH, Royal Institute of Technology
Department of Microelectronics and Information Technology
Device Technology Laboratory

Stockholm 2001
Chemical Vapor Deposition of Si and SiGe Films for High-Speed Bipolar Transistors

A dissertation submitted to Kungliga Tekniska Högskolan, Stockholm, Sweden, in partial fulfillment of the requirements for the degree of Teknisk Doktor.

© 2001 Johan Pejnefors
KTH, Royal Institute of Technology
Department of Microelectronics and Information Technology
Electrum 229
S-164 40 Kista
SWEDEN

ISRN KTH/EKT/FR-2001/6-SE
ISSN 0284-0545
TRITA – EKT
Forskningsrapport 2000:6

Abstract

This thesis deals with the main aspects in chemical vapor deposition (CVD) of silicon (Si) and silicon-germanium (Si$_{1-x}$Ge$_x$) films for high-speed bipolar transistors. In situ doping of polycrystalline silicon (poly-Si) using phosphine (PH$_3$) and disilane (Si$_2$H$_6$) in a low-pressure CVD reactor was investigated to establish a poly-Si emitter fabrication process. The growth kinetics and P incorporation was studied for amorphous Si film growth. Hydrogen (H) incorporated in the as-deposited films was related to growth kinetics and the energy for H$_2$ desorption was extracted. Film properties such as resistivity, mobility, carrier concentration and grain growth were studied after crystallization using either furnace annealing or rapid thermal annealing (RTA). In order to integrate an epitaxial base, non-selective epitaxial growth (NSEG) of Si and SiGe in a lamp-heated single-wafer reduced-pressure CVD reactor was examined. The growth kinetics for Si epitaxy and poly-Si deposition showed a different dependence on the deposition conditions i.e. temperature and pressure. The growth rate difference was mainly due to growth kinetics rather than wafer surface emissivity effects. However, it was observed that the growth rate for Si epitaxy and poly-Si deposition was varying during growth and the time-dependence was attributed to wafer surface emissivity variations. A model to describe the emissivity effects was established, taking into consideration kinetics and the reactor heating mechanisms such as heat absorption, emission and conduction. Growth rate variations in opening of different sizes (local loading) and for different oxide surface coverage (global loading) were investigated. No local loading effects were observed, while global loading effects were attributed to chemical as well as temperature effects. Finally, misfit dislocations formed in the SiGe epitaxy during NSEG were found to originate from the interface between the epitaxial and polycrystalline regions. The dislocations tended to propagate across the active area.

Keywords: chemical vapor deposition (CVD), bipolar junction transistor (BJT), heterojunction bipolar transistor (HBT), silicon-germanium (SiGe), epitaxy, poly-Si emitter, in situ doping, non-selective epitaxy (NSEG), loading effect, emissivity effect
Contents

Preface vii
   Appended papers ix
   Related papers not included in the thesis x

1 Introduction 1

2 Background 3
   2.1 Structure and realization of bipolar transistors 3
   2.2 Poly-Si emitter technology 7
   2.3 Epitaxial base integration 9

3 Deposition of poly-Si for emitter 13
   3.1 In situ P doping 13
   3.2 Emitter formation 16

4 Non-selective epitaxy for base 21
   4.1 ASM reactor 21
   4.2 Pre-epitaxy cleaning 23
   4.3 NSEG of Si and SiGe films 26

5 Temperature control 33
   5.1 Heat transfer model 34
   5.2 Instantaneous growth rate 37
   5.3 Influence of estimated parameters 37

6 Concluding remarks 43
   References 45
   Summary of the appended papers 51
Preface

It all began in the autumn of 1995, when I had an appointment with Prof. Mikael Östling for the purpose of discussing subjects for diploma work. It was the first time I met Mikael and soon he convinced me that research on silicon high-speed bipolar transistors, with possibilities of close co-operation with other universities in Sweden, was the right track. As a consequence, I began my diploma work two weeks later. Because of my background in material physics it was natural that the work considered processing of transistors in particular chemical vapor deposition. A half-year later, the decision to continue the research as a graduate student in the eminent ‘bipolar group’ was as simple. During 1996 the research co-operation broadened over Europe. My decision, in March 1997, of going to France Télécom-CNET was a lot more difficult to make since I had to leave my girlfriend Sara in Stockholm. Still, the time in Grenoble was very enriching and pleasant. When I came back to the department, the research activities on bipolar transistors had grown and quite soon came the first promising results. This thesis is a summing up of my research during all these years. On this journey, I have met many helpful people to whom I am very grateful.

First of all I would like to thank Mikael Östling for giving me the opportunity of being a graduate student. His optimism and many research contacts over the world have been a good basis for my work. I would like to express my deep appreciation to my supervisor Dr. Shi-Li Zhang for always showing his interest and for enabling an environment for fruitful discussions. It has been a pleasure working with you. I am grateful to Dr. Jan V. Grahn for supervision and for teaching me the basics of designing experiments. He has also been an excellent guide in the bipolar jungle. I also want to acknowledge Dr. Henry Radamson for many helpful hours spent in the clean room working with the epitaxy reactor. Dr. Wlodek
Kaplan is acknowledged for sharing some of his skills in the clean room. Many of my experiments would not have been possible without the help from Cyril Menon, Andreas Bentzen, Patrick Jönsson, Hans Fosshaug, Magnus Lindberg and many others working in the clean room, thank you all. Ingmar Höglund is acknowledged for being my mentor during these years. In Grenoble I met a lot of friendly and nice people at CNET to whom I am deeply thankful for many exiting events. In particular, I would like to acknowledge my supervisors Christine Morin, Dr. Jorge Luis Regolini and Dr. Alain Chantre.

A special thanks goes to the ‘bipolar group’ consisting of Dr. Martin Linder, Dr. Martin Sandén, Dr. Tord Karlin, Gunnar Malm and Erdal Suvar. Furthermore, I am grateful to all members of the departments of Device Technology Laboratory and Solid State Electronics for creating an inspiring and entertaining atmosphere. Specially, I thank my former neighbour Denny Åberg for every now and then showing up with another semla. Finally, I would like to thank my family, all of my friends and especially my wife Sara for her support and love.

Johan Pejnefors
Stockholm, August 2001
Appended papers

1. **Characterization of in situ phosphorus-doped polycrystalline silicon films grown by disilane-based low-pressure chemical vapor deposition**
   J. V. Grahn, J. Pejnefors, M. Sandén, S.-L. Zhang and M. Östling

2. **Epitaxial growth of SiGe layers for BiCMOS applications**

3. **Hydrogen in undoped and heavily in situ phosphorus doped silicon films deposited using disilane and phosphine**
   J. Pejnefors, S.-L. Zhang, J. V. Grahn, M. Östling, L. Persson and M. Hult

4. **Chemical vapor deposition of undoped and in-situ boron- and arsenic-doped epitaxial and polycrystalline silicon films grown using silane at reduced pressure**
   J. Pejnefors, S.-L. Zhang, H. H. Radamson, J. V. Grahn and M. Östling

5. **Loading effects during non-selective epitaxial growth of Si and SiGe**
   In *Proc. 15th Int. Conf. Chemical Vapor Deposition*, p. 403 (2000).

6. **Effects of growth kinetics and surface emissivity on chemical vapor deposition of silicon in a lamp-heated single-wafer reactor**
   J. Pejnefors, S.-L. Zhang, H. H. Radamson and M. Östling

7. **Chemical vapor deposition of silicon in a lamp-heated reactor: Effects of heat absorption, emission and conduction**
   J. Pejnefors, S.-L. Zhang, H. H. Radamson and M. Östling
   Submitted for publication in J. Electrochem. Soc.
Related papers not included in the thesis

8 A simplified high-speed bipolar process with Ti SALICIDE metallization: Implementation of in situ P-doped polysilicon emitter

9 A high speed SiGe HBT process using non-selective epitaxy and in situ phosphorus doped polysilicon emitter: Optimization of device design rules

10 A low-complexity 62-GHz $f_T$ SiGe HBT process using differential epitaxy and in situ phosphorus-doped poly-Si emitter at very low thermal budget

11 Scanning $\mu$-RBS characterisation of local loading effects of non-selectively grown SiGe thin films
T. Winzell, J. Pejnefors, M. Elfman, M. Östling and H. J. Whitlow
Chapter 1

Introduction

Very large scale integration (VLSI) makes it possible to design integrated circuits with more than hundred thousands silicon (Si) devices on a single chip. The transistor is the fundamental active building block in integrated circuits. The most frequently used transistor in VLSI technology is the metal-oxide-semiconductor field effect transistor (MOSFET), due to its low power consumption and high level of integration. However, for circuits where high switching speed and high transconductance are important, the bipolar junction transistor (BJT) is the preferable choice. As today’s communication circuits use frequency bands in the GHz range, the development of high-speed bipolar transistor technology has become very important.

The electrical performance of a transistor could be improved by scaling down the physical device dimensions, incorporating new materials or introducing new process concepts for device fabrication. State-of-the-art high-speed bipolar technology is built on two important innovations concerning the emitter and the base. The current gain for a transistor was greatly increased when a polycrystalline Si (poly-Si) layer was used to contact the intrinsic emitter of single crystalline Si. This is now widely termed as poly-Si emitter technology, which was first reported by Graul et al in 1976 [1]. A decade later when Meyerson et al. succeeded with low-temperature epitaxy of Si and silicon-germanium (Si$_{1-x}$Ge$_x$ hereafter SiGe) [2], it became possible to replace the ion-implanted base with an epitaxial one. As a result, remarkable improvements in transistor performance have occurred, in particular with respect to high-frequency behavior and power consumption. Therefore, Si-based bipolar transistor technology is today competitive to the traditionally dominating III-V devices for RF-applications.
The focus of this thesis is on process development and realization of the emitter and base fabrication for a high-speed bipolar transistor aimed for VLSI integration. Both processes are based on chemical vapor deposition (CVD) of Si. The emitter is prepared using in situ phosphorus (P) doping of poly-Si and the base is fabricated using non-selective epitaxial growth (NSEG) of Si and SiGe. The poly-Si emitter and epitaxial SiGe base studied in this thesis have directly contributed to successful development of an HBT with a cut-off frequency of 62 GHz presented in Papers 9 and 10. The thesis, however, will be devoted to the materials and process aspects of these two techniques.

In Chapter 2, a background of the transistor performance as well as integration issues for emitter and base are outlined. This is followed by detailed analysis of in situ doped poly-Si emitter technology in Chapter 3. The fabrication of the base using NSEG is presented in Chapter 4. In Chapter 5, temperature control in the epitaxy reactor is thoroughly investigated when Si films are grown. The thesis ends with a summary and a discussion of future integration issues for high-speed Si-based bipolar transistors.
Chapter 2

Background

In this chapter, an overview of the bipolar transistor is presented. For a more detailed description the reader is referred to textbooks [3,4]. The active parts in the transistor, i.e. the emitter, base and collector, are described with the emphasis on the transistor performance as a result of the design of each of them. Deposition and integration issues for poly-Si emitters are summarized. The benefits of using \textit{in situ} doping of poly-Si for emitter integration are then highlighted. The requirements of using low-temperature epitaxy for base integration are discussed. Finally, selective epitaxial growth (SEG) as well as NSEG for the implementation of an epitaxial base are presented.

2.1 Structure and realization of bipolar transistors

A typical state-of-the-art double poly-Si BJT is shown in Fig. 1. In a double poly-Si process, the external base contact is connected to the intrinsic base through the poly-Si base and the in-diffused dopants from the poly-Si base layer, see Fig. 1. These two regions are generally called the extrinsic base. The implementation of a base and emitter poly-Si makes the transistor a so-called double poly-Si. In these types of transistors the emitter and base are self-aligned. Finally, the extrinsic collector is composed of the implanted collector plug and the buried collector layer as shown in Fig. 1. The intrinsic collector includes the lightly doped region immediately beneath the intrinsic base as well as a pedestal region below that. The pedestal is formed using selective implantation of the collector (SIC) i.e. implantation of ions through the emitter window before poly-Si emitter deposition. As a consequence the intrinsic collector is also self-aligned with respect to the emitter window.
Figure 1. Schematic cross-section of a double poly-Si bipolar junction transistor.

Emitter

The poly-Si emitter layer serves as a low resistivity contact between the intrinsic emitter and the metallization. Normally, it is doped to a concentration on the order of $10^{20}$ cm$^{-3}$ and acts as a diffusion source to form the intrinsic emitter. The depth of the in-diffused intrinsic emitter could be as shallow as a few hundreds of Å. A highly doped intrinsic emitter is preferable in order to increase the current gain since it is directly proportional to the doping concentration. In addition, a shallow emitter junction reduces the parasitic emitter-base capacitance important for high switching speeds [5].

Poly-Si is advantageous to use for the extrinsic emitter because of a large increase in the current gain. The reduction in base current, which results from recombination of minority carriers, is proposed to mainly be due to two mechanisms. First, the transport of minority carriers in the poly-Si layer is retarded because of a lower mobility, originating from the presence of grain boundaries in poly-Si films. Second, the interface at the poly-Si and single crystal Si reduces the injection of minority carriers into the extrinsic poly-Si emitter [3,6]. The interface can be composed of (a) a thin oxide layer, resulting in tunneling of carriers and thus an improved current gain with the expense of an increased emitter resistance, (b) a pseudo-grain boundary, yielding an improved current gain for small density of interface states and reduced for large densities and/or (c)
segregation of dopants or an interfacial strain, causing potential barriers for hole injection. In practice, the current gain is not strongly dependent on the grain size or the poly-Si thickness, since the recombination of minority carriers in the poly-Si emitter is dominated by the recombination at the interface between the poly-Si and single crystal Si [3]. Hence, poly-Si films with large grains are desirable to benefit from the higher mobility for majority carriers and a well-controlled interface is necessary in order to minimize the emitter resistance and maximize the current gain.

**Base**

The doping profile for the ion implanted intrinsic base is controlled by the energy and dose used for the implantation as well as the subsequent annealing for dopant activation. The doping concentration is optimized between two conflicting demands of a low base resistance and a large current gain. Generally, the doping concentration is on the order of $10^{18}$ cm$^{-3}$. A narrow base results in increased current gain as well as reduced base transit time. As a consequence, the base width is minimized by reducing the ion implantation energy and by replacing boron (B) with the heavier boron difluoride (BF$_2$). The width of an implanted base is on the order of 1500 – 2000 Å [7]. When the base width shrinks it is important to keep the base resistance intact, i.e. increasing the base doping in order to avoid a decrease in power gain. Using epitaxy to form the base region makes it possible to perfectly control the doping profile within the vertical section. Hence base width as shallow as a few hundreds of Å can easily be obtained [8].

With epitaxy, a SiGe alloy layer can be used as the base. SiGe alloys doped with B are used in heterojunction bipolar transistors (HBTs) because of the smaller energy bandgap of Ge compared to that of Si. As a result, the energy bandgap of the SiGe alloy decreases with increasing Ge content. The introduced bandgap offset results in a lowered potential barrier for electron injection from the emitter to the base. Hence, the collector current is enhanced and a larger current gain is obtained compared to a transistor with a Si base. Usually, the enhanced current gain for SiGe HBTs is traded for an increase in the base doping in order to increase the power gain. The Ge profile could be designed in many different ways. In general, the profile is either constant (a box profile), graded or a combination of these [9,10]. For a graded profile, the Ge content is increasing towards the collector thus the bandgap is gradually reduced. This will cause a built–in drift
field in the base that accelerates the injected electrons. As a consequence the base transit time is further reduced and the switching speed increased. For such a Ge profile, it is favorable to have the emitter-base metallurgical junction at the Si-SiGe transition in order to take advantage of the drift field and the increased current gain [9]. Hence, a Si cap layer with thickness of the emitter in-diffusion depth must be deposited on the SiGe base layer. The electrical performance of the transistor is very sensitive to the positioning of the SiGe layer with respect to the emitter-base and base-collector metallurgical junctions. If B diffuses out of SiGe layer, the SiGe-Si transition is situated in the neutral base resulting in a potential barrier in the conduction band, which will degrade the performance [11]. This is avoided by growing undoped SiGe layers beneath and above the B doped SiGe base.

The extrinsic base is formed by a high dose of B implantation into the deposited poly-Si base followed by in-diffusion of B into the single crystal to contact the intrinsic base region. Since the extrinsic base is a parasitic component, it is important to minimize its resistivity and to reduce the parasitic base-collector capacitance by decreasing the area overlapping the collector.

**Collector**

The n⁺-region, between the intrinsic collector and the collector contact, is necessary in order to reduce the series resistance. The intrinsic collector is optimized between the ability of driving a high collector current density (high doping level) and the necessity of keeping a low base-collector capacitance as well as taking a high reverse potential bias (low doping level). Doping concentrations in the low $10^{17}$ cm⁻³ are frequently used. With the introduction of SIC, the doping concentration in the intrinsic collector could be increased without suffering of a large increase in the base-collector capacitance. Growing the pedestal collector by epitaxy has also been investigated in order to reduce the parasitic base-collector capacitance and simultaneously control the doping profile [12].
2.2 Poly-Si emitter technology

LPCVD for poly-Si deposition

The deposition of undoped or in situ doped poly-Si for the emitter is often performed in low-pressure CVD (LPCVD) reactors where the chamber pressure is lower than 1 Torr. Such reactors are often of the hot-wall diffusion furnace type in which the wafer substrates are heated by resistive coils surrounding the reactor tube. Poly-Si depositions are usually carried out with silane (SiH₄) as the Si source gas. Under low-pressure conditions, it is possible to load a large number of wafers for each deposition run due to the growth being surface-reaction controlled and the large mean free path of gas molecules. Lately, poly-Si has also been deposited at reduced-pressure CVD (RPCVD) and atmospheric pressure CVD (APCVD) in lamp-heated single-wafer reactors designed for epitaxy [13]. The depositions in RPCVD (deposition pressures from 10 to 100 Torr) or APCVD, giving rise to extremely clean poly-Si films containing low amounts of oxygen, are described in the following section. Poly-Si emitters are usually highly doped to the level of 3-5 x 10²⁰ cm⁻³, independent of the dopant being P or arsenic (As) [14,15]. In situ doping of poly-Si to such a high doping level results in significantly reduced deposition rate due to preferential adsorption of the dopant bearing species.

Emitter integration

Deposition of undoped poly-Si followed by ion implantation is the common approach to fabricate the poly-Si emitter. For such a process the energy and dose of the implantation are optimized to confine the doping atoms within the poly-Si layer from which the dopants are diffused into the underlying single crystal Si to form the intrinsic emitter. Thus, a high temperature anneal is necessary for the in-diffusion and activation of the dopants. Ion implantation could be performed using either P or As. However, As is the preferable doping element due to the lower diffusion coefficient compared to that for P. Hence the intrinsic emitter region could be shallow even after a high temperature anneal. Further on, the well-known and complex diffusion of P resulting in a kink in the diffusion profile as well as a push-out of the base dopants has limited the use of P for emitter diffusions [16]. For very shallow junctions, P may be suitable since the known drawbacks with P diffusion are much less pronounced.
Figure 2. Schematics of (a) the emitter perimeter depletion effect and (a and b) the Plug effect from Ref. [17].

For sub-micrometer emitters the depth of the implanted ions will vary along the emitter window since the effective poly-Si thickness is larger along the perimeter, see Fig. 2. After the in-diffusion step, the depth of the intrinsic emitter can be shallower close to the emitter window edge [17]. This effect is known as the emitter perimeter depletion and is shown in Fig. 2 (a) by comparing the profiles of Emitter 1 and Emitter 2. The effective poly-Si thickness over the emitter window can also be thicker for smaller emitter windows than for large ones. In such a structures, the junction can be shallower than expected over the entire emitter, as the implanted dopants need to diffuse a longer distance [17]. This effect, called the emitter plug-effect, is illustrated in Figs. 2 (a) and (b) by comparing Emitter 1 with Emitter 3.

Emitter perimeter depletion and plug-effect are avoided when the poly-Si is doped by in situ deposition, as the amount of dopants is constant throughout the whole poly-Si film independent of surface morphology or film thickness. In situ doping is also attractive for elimination of one processing step. The reduction in growth rate of poly-Si is more severe for in situ doping using arsine (AsH₃) compared to phosphine (PH₃) [18]. In addition, a lower resistivity is obtained using P doping than using As for the same doping concentration [18]. Phosphorus also becomes interesting to use as an emitter dopant instead of As due to the higher diffusivity and the easier activation of dopants as the thermal budget, i.e. temperature and time, are reduced. Emitter integration using in situ P doping of poly-Si was first reported by Nanba et al. showing transistors with a high current gain as well as a high switching speed [5].
2.3 Epitaxial base integration

Low-temperature epitaxy

Base integration into the transistor fabrication sequence using epitaxy is generally performed on partially processed wafers. Therefore, the epitaxy must be performed under low-temperature conditions in order not to alter the underlying doping profiles or to destroy the isolation. Using low-temperature epitaxy makes it possible to grow abrupt doping profiles due to the suppressed auto-doping [19]. Low-temperature epitaxy at 550-750 °C was first reported in the middle of the eighties [2,20,21]. Different growth methods can be used to make high quality epitaxy. They include molecular beam epitaxy (MBE), ultra-high vacuum CVD (UHV/CVD), RPCVD and APCVD. For commercial applications, it is generally realized that CVD is the realistic candidate [22], although well behaving transistors have been fabricated with all these processes [8-10,23,24]. The UHV/CVD technique is basically an ordinary LPCVD process, described in the section above, with a load lock and a base pressure of $10^{-9}$ Torr in order to reduce contamination from water vapor and oxygen [2]. The depositions are performed at chamber pressures of 1 mTorr. The RPCVD and APCVD reactors are usually cold-wall single-wafer reactors. They achieve the clean conditions necessary for epitaxy by load locks and hydrogen gas ($H_2$) purification. Using low-temperature epitaxy, the integration of the base can be realized using either selective or non-selective epitaxy.

Selective epitaxy for base

Selective epitaxial growth (SEG) yields epitaxial layers only on Si surfaces whereas no deposition occurs on the surrounding oxide and nitride. Normally, SEG is carried out using dichlorosilane ($SiH_2Cl_2$) as the Si source gas. In order to improve selectivity, hydrogen chloride ($HCl$) is added to the gas flow. A well-known difficulty with SEG is the formation of facets since the growth rate varies for different Si surface [25,26]. Thus the angle between the growing surface and the facet is dependent on the orientation of the Si substrate and the alignment of the pattern. Base integration using SEG has been investigated for double poly-Si as well as single poly-Si processes [27-29]. In the double poly-Si process, the epitaxy is grown selectively in the emitter window where it is simply replacing the implanted base [27,28]. In the single poly-Si process, shown in Fig. 3, the
epitaxy occurs in the entire active area defined with LOCOS isolation [29]. The former process results in a transistor similar to the one shown in Fig. 1 with features such as self-alignment and base poly-Si. However, it is difficult for SEG to occur in the small emitter windows due to the complex pre-epitaxial cleaning. In addition, facets are formed close to the base poly-Si yielding a defected region that may propagate laterally to the entire intrinsic base. The latter process avoids these problems by growing the epitaxy in larger windows, which requires a relatively less stringent cleaning. Besides, facets are kept outside the intrinsic transistor region. However, the emitter window is not self-aligned to the extrinsic base implantation. Furthermore, implanting the extrinsic base in the single crystal Si generates Si interstitials, which enhance the B out-diffusion from the intrinsic base. Finally, the single poly-Si transistors are in general characterized with a high collector-base capacitance since the active area has to be sufficiently large to accommodate the base contacts (see Fig. 3) resulting in a large base-collector junction area.

**Non-selective epitaxy for base**

Non-selective epitaxial growth (NSEG) results in simultaneous growth of epitaxy on the Si surfaces and poly-Si deposition on the surrounding isolation. In lamp-heated reactors, wafer temperature variation during growth may occur since the wafer surface emissivity varies with thickness of the deposited poly-Si. The variation of substrate temperature due to surface emissivity will be treated in Chapter 5. During NSEG, SiH$_4$ is usually used as the Si source gas, though
SiH$_2$Cl$_2$ can also be utilized provided a poly-Si seed layer is present on the isolation in order to facilitate the poly-Si deposition. The deposition conditions for NSEG are crucial in order to obtain a high quality epitaxy with the specified thickness and simultaneously a smooth poly-Si with a thickness suitable for base poly-Si. The interface formed between the epitaxial Si and poly-Si can be a source for defects to propagate into the epitaxial region. The integration of base epitaxy using NSEG is usually performed directly after the isolation process [23,24,30-32]. Figure 4 illustrates one example of a typical transistor fabricated using NSEG [8]. Many similarities between the transistors shown in Figs. 1 and 3 are observed. However, compared to the ion implanted double poly-Si transistor in Fig. 1 the main drawbacks are again the extrinsic base implantation into the epitaxial region as well as the absence of self-alignment between the emitter and base. The self-alignment issue can be solved using a different process flow. However, a similar cross-section as shown in Fig. 4 is obtained [30]. Compared to the single poly-Si process shown in Fig. 3, the base contacts in the transistor using NSEG in Fig. 4 are situated on top of the LOCOS isolation thereby reducing the area for the parasitic base-collector junction. Therefore, epitaxial base integration using NSEG provides a way of combine the strengths of single and double poly-Si processes.
Chapter 3

Deposition of poly-Si for emitter

The importance of a poly-Si emitter for the electrical performance of a transistor as well as the advantages of using *in situ* doping for the emitter formation were discussed earlier in Chapter 2. In order to obtain a proper growth rate as well as the desired film doping and large grains, *in situ* P doping of poly-Si was thoroughly studied. This process is not well studied in particular with respect to film growth using disilane (Si$_2$H$_6$). In this chapter some of those results are presented. In Section 3.1, the growth kinetics and the incorporation of P and H in the films are discussed. The emitter formation used for BJTs and HBTs is summarized in Section 3.2. This includes crystallization of the as-deposited amorphous films, formation of a shallow intrinsic emitter by rapid thermal annealing (RTA) and interfacial cleaning before the poly-Si emitter deposition.

3.1 *In situ* P doping

The depositions for poly-Si emitter were performed in a conventional LPCVD system (BTI Engineering Corporation), shown in Fig. 5. The wafers were placed in a boat that in turn was encapsulated in a wafer cage in order to improve the radial thickness uniformity [33]. The SiH$_4$ and Si$_2$H$_6$ source gases are injected from the load end. Phosphine, diluted to 1% in H$_2$, is introduced through a thin injector positioned under the cage. The gas flows were regulated by mass flow controllers (MFCs). The deposition temperature ranges from 415 to 560 °C. Depositions were made at a pressure of 270 mTorr. The majority of the films were deposited from the Si$_2$H$_6$-based gas chemistry since the reduction in poly-Si deposition rate during *in situ* doping using PH$_3$ is less pronounced compared to using SiH$_4$ [34]. The deposition rate is depicted vs. the molar ratio PH$_3$/Si$_2$H$_6$ in
Fig. 6, reproduced from Paper 1. Even though Si$_2$H$_6$ was used as the Si source gas, a clear reduction in deposition rate with increasing PH$_3$ is revealed. For comparison some depositions were also performed using SiH$_4$ and no essential differences were observed after annealing despite of a slightly higher resistivity and smaller grains for the SiH$_4$-based than for the Si$_2$H$_6$-based films. This was attributed to the higher deposition temperature being 560 °C for the SiH$_4$-based films compared to 480 °C for Si$_2$H$_6$-based films. The higher deposition rate when using Si$_2$H$_6$ made it possible to reduce the deposition temperature, improving film
uniformity and yielding amorphous Si films. Post-annealing of amorphous Si films to convert them to poly-Si has been shown to improve the surface morphology and to grow large grains [35,36].

The deposition rate of undoped and heavily doped Si$_2$H$_6$-based films was limited by surface-reaction at temperature below 480 °C and by mass-transport at higher temperature, as shown in Fig. 7 (a). In low-temperature LPCVD, the incorporated H during deposition is expected to be high due to incomplete dissociation of Si hydrides. Therefore, the H incorporation in these films was studied in relation with growth kinetics. The H concentration was investigated using nuclear resonant reaction analysis (NRRA). The H incorporation in the as-deposited films was in the order of $10^{20}$ cm$^{-3}$ and showed a clear correlation with the deposition kinetics for the undoped and the heavily doped films as shown in Fig. 7. The results

![Figure 7](image-url)

**Figure 7.** Arrhenius plots of the (a) deposition rate and (b) H concentration in undoped (□) and heavily P doped (■) films presented in Paper 3.
showed that a study of bulk H concentration was indicative of surface adsorption-desorption processes. The activation energy for H desorption from the Si surface during film growth could be estimated from the H concentration in the films. The results were comparable to those obtained in the literature by more direct measurement of H adsorption and desorption [37,38].

### 3.2 Emitter formation

**Crystallization**

Crystallization of the as-deposited amorphous Si films affects surface morphology, dopant activation and induces grain growth in the poly-Si films. The resulting grain size in the films is sensitive to post-anneal temperature, time and procedure. Further on, the number of active dopants in the grains as well as the number of dopants segregated to the grain boundaries has been found to be dependent on the annealing [39]. In this work, the crystallization was performed using a furnace anneal in a computer-controlled BTI furnace in oxygen (O₂) at atmospheric pressure. During annealing O₂ was used in order to produce a thin surface oxide layer to suppress potential out-diffusion of P atoms. The furnace annealing lasted for 60 minutes. In Fig. 8, it is observed that the resistivity decreases with increasing anneal temperature. This is due to the increase in the solid solubility at higher temperatures and was discussed in detail in Paper 1. In

![Figure 8](image.png)

**Figure 8.** Deposition rate vs. molar ratio PH₃/Si₂H₆ data from Paper 1.
addition, it is seen that the grain size increases with annealing temperature. However, for the fabrication of SiGe HBTs using a low temperature is preferred although high temperature anneals yield reductions in resistivity and growth of the grains. Therefore, the lowest anneal temperature (650 °C) resulting in poly-Si films was employed to crystallize the poly-Si emitter in the transistor fabrication process [32]. Furthermore, this temperature was also the growth temperature for the NSEG base, which is advantageous for minimization of the thermal budget. At such a low temperature minor diffusion of dopants occurs [16]. Hence, a high temperature dopant drive-in step using RTA was necessary.

**Dopant drive-in**

It was pointed out in Chapter 2 that the transistor performance is extremely sensitive to the positioning of the emitter-base junction and hence the intrinsic emitter depth. It is therefore important to optimize the RTA dopant drive-in. In addition, it has been reported that an RTA could break-up interfacial oxide present between the emitter poly-Si and the underlying single crystal Si [3], resulting in epitaxial regrowth of the poly-Si film [3]. When epitaxial regrowth of the poly-Si emitter occurs, not only the current gain is reduced but also the profile of the indiffused dopants will be altered [40]. The resistance of the emitter is on the other hand reduced due to the higher mobility of epitaxially grown Si. High performance transistors have indeed been reported with a fully epitaxially

![Channeling and random backscattering spectra of an RTA annealed (1050 °C) and a reference sample.](image)

**Figure 9.** Channeling and random backscattering spectra of an RTA annealed (1050 °C) and a reference sample.
realigned poly-Si emitter [15]. In this work, epitaxial regrowth was investigated for films exposed to different annealing conditions usually used in transistor processing. Figure 9 shows backscattering spectra for an un-annealed sample (reference) and a as-deposited sample heat treated in RTA (1050 °C for 10 seconds). However, no tendency of epitaxial realignment was observed according to the backscattering results independently of heat treatment. Further evidence for non-epitaxy was obtained from transmission electron microscopy (TEM) for fabricated transistors shown in Fig. 10. However, careful analysis of the TEM picture revealed epitaxial realignment under the nitride wings. The lack of epitaxial regrowth could be due to an unclean single crystal Si surface subsequent to the dry etching of the nitride wings, since the selectivity of the dry etch was found to be poor [41]. In addition, the large amount of oxygen (10^{20} cm^{-3}) incorporated during deposition may also hinder epitaxial regrowth.

Interface

The condition of the Si surface prior to deposition of the in situ doped film is important for the current gain of the transistor. Four different cleaning procedures resulting in different oxide thickness were investigated in this work. An 8 Å thick oxide was obtained by oxidizing the wafer in H_{2}O_{2}:H_{2}SO_{4} (2:5) at a temperature above 80 °C for 5 minutes. The oxide became 3 Å thick when an etch step in C_{3}H_{7}OH:HF(50%):H_{2}O (1:1:100) solution for 100 seconds was added. The
thickness of the interfacial oxide remained, according to ellipsometry measurements, when a further etch in HF(50%):H₂O (1:10) for 10 seconds was included. These interfacial cleanings were all ended with a deionized water rinse for 5 minutes and a spin-dry sequence. No detectable interfacial oxide was obtained when the wafer received no rinse after the HF:H₂O etch. The wafer was nitrogen (N₂) blow-dried instead. The P depth profiles measured by secondary ion mass spectrometry (SIMS) are shown in Fig. 11 as a function of depth for the different interface treatments. These films were all crystallized at 650 °C followed by a dopant drive-in using RTA at 900 °C for 10 seconds. It is observed that the in-diffusion depth at a concentration of 10¹⁸ cm⁻³ varies as much as 200 Å among the different cases, confirming that the depth of a shallow emitter is very sensitive to the surface cleaning prior to emitter poly-Si deposition. These results point to the great importance of a reproducible and uniform interface for uniform device performance. The presence of interfacial oxide is therefore considered to negatively influence uniformity of emitter depth and emitter resistance [5]. For transistor fabrication, an ordinary cleaning consisted of H₂O₂:H₂SO₄ and C₃H₇OH:HF(50%):H₂O followed by water rinse and spin-dry, which could give rise to a 3 Å thick interfacial oxide.

Figure 11. The emitter junction depth at various interfacial oxide thicknesses for films crystallized at 650 °C and RTA annealed in 900 °C for 10 seconds.
Chapter 4

Non-selective epitaxy for base

The deposition of *in situ* P doped amorphous Si films and the formation of poly-Si emitters were presented in the preceding Chapter 3. This chapter is devoted to base integration using NSEG performed in a single-wafer RPCVD reactor. The epitaxial growth and the poly-Si deposition were studied in detail in order to simultaneously obtain a high quality epitaxy and a smooth poly-Si with the desired thicknesses. In addition, since the actual NSEG process consisted of a consecutive deposition of several different layers from As-doped Si, intrinsic Si, intrinsic SiGe, B-doped SiGe to B-doped Si, all these growth conditions have to be investigated in order to produce a high performance HBT. The first two Si layers are referred to as buffer while the last Si layer cap. Epitaxy performed on patterned substrates is further complicated due to the so-called loading effects that causes growth rate to change with surface pattern. The reactor used for epitaxy is presented in Section 4.1. The pre-epitaxy cleaning procedure is summarized in Section 4.2. In Section 4.3, growth kinetics and dopant incorporation for Si epitaxy and poly-Si deposition, loading effects during NSEG as well as stability issues of SiGe films are discussed.

4.1 ASM reactor

The single-wafer ASM Epsilon-2000 reactor is divided into three main parts; the two load-locks, the wafer handling chamber and the process chamber, illustrated in Fig. 12. The system can be used for processing wafer of 100, 125, 150 or 200 mm in diameter. The wafers are placed in a cassette with 26 positions in one of the load-locks. A quartz wand positioned by a wafer transfer arm picks up the wafer from the cassette and transfers it into the process chamber. The wafer is put
onto a SiC coated graphite susceptor comprising two parts: an inner rotating part and an outer fixed part. After processing, the wafer is transferred into another load-lock. The wafer handling chamber and the load-locks are always purged with N₂. In order to avoid contamination from air, the load locks are purged with N₂ for 30 minutes when the load-lock access door has been opened before a wafer can be transferred into the wafer handling chamber.

The gas module handles H₂, N₂, HCl, two Si source gases, germane (GeH₄) and three dopant gases. The Si source gases are SiH₄ and SiH₂Cl₂. N-type doping can be realized with either PH₃ or AsH₃. P-type doping is obtained with diborane (B₂H₆). Pneumatic valves control on/off and mixing of the gas flows and MFCs regulate the respective gas flow rates. The dopant gases are mixed and diluted with H₂ before injection into the process chamber. HCl is used for cleaning the process chamber as well as etching away undesired Si on the wafer surface. Each gas can be let either into the process chamber or to vent. This is practical for growth of different layers with sharp interfaces since a gas flow generally requires three minutes to stabilize its flow rate before being introduced to the process chamber. The working pressure is either atmospheric or reduced in the range of 10-100 Torr.

**Figure 12.** Schematics of the reactor section [42].
Tungsten-halogen lamps placed below and above the susceptor radiantly heat the wafer and the susceptor. The temperature is measured by four thermocouples placed in the susceptor, one encapsulated in the center of the rotating part (center) and three placed in the fixed part (front, side and rear). The thermocouples provide controlling signals to the lamp-banks to obtain the set-point susceptor temperature. A schematic of the thermocouple controlling system for the lamps is depicted in Fig. 13. The front and rear thermocouples are each responsible for two lamps in the lower lamp-bank closest to the gas inlet (number 4 and 5) and the exhaust (number 10), respectively. The side thermocouple is assigned to the two lamps on each side in the upper lamp-bank (number 3). Finally, all the other lamps are controlled by the center thermocouple. The wafer is placed in the center of the rotating susceptor above the center thermocouple. The processing system can be used in a temperature range from 575 to 1200 °C.

4.2 Pre-epitaxy cleaning

In order to enable epitaxy on Si substrates, the initial growth surface must be perfect without any chemical impurities. For blanket wafers, impurities such as oxygen and carbon are desorbed during an in situ clean carried out in H₂ at temperatures around 1050 °C. However, this high-temperature in situ clean cannot...
be applied to partially processed wafers with dopants and/or with oxide patterns since redistribution of dopants and undercut of the oxide can occur. Figure 14 shows a cross-section scanning electron microscopy (SEM) picture of two LOCOS patterned wafers that have been in situ cleaned in H₂ at atmospheric pressure at (a) 950 °C for 20 minutes and (b) 1050 °C for 10 minutes. For the former case no undercut is observed whereas for the latter case an undercut of the bird’s beak is clearly revealed. In agreement with the literature, the rate of formation of the undercut is strongly dependent on temperature [22,43]. It is also dependent on the type of gas, since no undercut was observed in N₂ [22,43]. Since

**Figure 14.** Cross-sectional SEM picture of NSEG films grown on LOCOS patterned substrates after in situ pre-epitaxy clean at (a) 950 °C for 20 minutes and (b) 1050 °C for 10 minutes.
the temperature for the in situ clean has to decrease more stringent demands are placed on ex situ cleaning.

The ex situ wet chemical cleaning procedure should be able to remove contaminations such as particles, organics and native oxides leaving a clean Si surface. Several different kinds of ex situ cleaning procedures were utilized in this work until a high quality epitaxy could be obtained. Figure 15 shows the top-view micrograph of a NSEG sample with un-optimized cleaning conditions. Dislocations such as stacking faults and misfit dislocations are revealed using Secco etching [44]. A successful ex situ clean could consist of H₂O₂:H₂SO₄(2:5) to remove particles and organics followed by a bath in HF(5%) to etch the chemical oxide produced in the preceding cleaning step. Then the wafers were flushed in C₃H₇OH followed by a water rinse. Finally, the wafers were spin-dried. A thin native oxide could be present on the Si surface after the ex situ cleaning. This oxide was removed during the in situ cleaning at 950 °C for 20 minutes in H₂ without any formation of undercut. Further reduction of the temperature and time for the in situ clean, or in the best case removing it, is necessary for future devices in order to maintain the underlying doping profiles. Therefore it is of major importance to further improve the ex situ wet chemical cleaning procedure.

Figure 15. Micrograph of defects observed when un-optimized ex situ cleaning conditions were used.
4.3 NSEG of Si and SiGe films

The growth rates of epitaxial and polycrystalline Si on un-patterned wafers were extensively investigated in Paper 4. It was found that the growth rate was surface-reaction limited for epitaxy as well as for poly-Si deposition at temperatures in the range of 600 – 750 ºC. For epitaxy the apparent activation energy was 2.1 eV, which could be related to the growth being limited by H\textsubscript{2} desorption [45]. For poly-Si deposition, a lower apparent activation energy of 1.6 eV was extracted and the growth rate was suggested to be limited by the balance between SiH\textsubscript{4} adsorption and H\textsubscript{2} desorption [45].

Both for epitaxy and for poly-Si deposition the growth rate was linearly dependent on the SiH\textsubscript{4} partial pressure. However, the epitaxy showed a slightly stronger dependence on the H\textsubscript{2} partial pressure compared to the poly-Si deposition, which could explain the difference in their apparent activation energy. Since the poly-Si growth rate depicts a stronger increase with total pressure compared to epitaxial growth, as being revealed in Fig. 16, it is possible to adjust the individual thickness of the epitaxial and poly-Si layers by selection of the total pressure. This could be used as a means to achieve a thick poly-Si layer for the base contact and simultaneously a thin epitaxial layer for the intrinsic base.

![Figure 16](image-url)

Figure 16. Growth rates vs. deposition pressure for Si epitaxy and poly-Si deposition, graph from Paper 4.
The observed differences in growth kinetics between epitaxy and poly-Si deposition could also be due to wafer temperature variations caused by differences in the wafer surface emissivity. In Paper 6, the difference in growth rate is shown to mainly be related to growth kinetics. However, the wafer surface emissivity also influences the growth rate, though to a lesser extent, through altering the wafer temperature.

The dependence of dopant incorporation on total pressure was also studied in Paper 4. The incorporation of B atoms in the Si films showed a weak pressure dependence. For identical gas flow conditions, the incorporation of B was greater in polycrystalline films than in epitaxial layers. Moreover, an increased resistivity with increasing deposition pressure was observed for the B-doped poly-Si films. This was attributed to a reduction in grain size as a consequence of the increased deposition rate at higher pressures, as shown in Fig. 16. The greater B incorporation in poly-Si than in Si epitaxy is in fact favorable for base integration since a lower amount of B atoms need to be implanted for the extrinsic poly-Si base. For comparison, the incorporation of As atoms, to similar doping concentrations as for B, was studied. Arsenic was selected as the doping element due to the lower diffusion coefficient compared to P. Such films could be used as the buffer collector grown prior to the base. However, the actual doping concentration needed in today’s collector should be slightly lower than found in these films, reported in Paper 4. The incorporation of As atoms increases for both epitaxial and poly-Si films as a function of pressure, see Paper 4. Further, the As incorporation was much higher in the poly-Si films compared to the epitaxial ones.

**Growth on patterned wafers**

NSEG on patterned wafers can be performed directly after LOCOS formation. Alternatively, it can be done after a seed layer of amorphous Si is added on the isolation, see Fig. 17. The former approach has the advantage of avoiding a mask layer and was used in Papers 5, 9 and 10. It is then necessary to begin the growth sequence with a buffer/pedestal layer of Si since nucleation of polycrystalline SiGe films on top of oxide is difficult [46,47]. Usually the thickness of the Si buffer layer is between 200 and 1000 Å. The latter approach, with the amorphous Si film as a hard mask for the wet-etch of the barrier oxide, was used in Paper 2.
Figure 17. A schematic cross-section prior to barrier oxide etching and epitaxy for a (a) LOCOS wafer and (b) LOCOS wafer with a Si seed layer.

for several reasons. First, the wafer surface is hydrophobic when the pre-epitaxy ex situ clean is carried out, simplifying the cleaning process. Second, loading effects will be minimized since Si covers almost the whole wafer surface. Finally, the resulting extrinsic base poly-Si layer becomes thicker with the amorphous Si seed layer, yielding a lower base resistance. One complication with the amorphous Si seed layer is the crystallization that occurs during the high temperature pre-epitaxy in situ clean. This may give rise to an extremely rough polycrystalline film.

In SEG, the growth rate of Si and SiGe in the active areas of exposed Si has been found to depend on the pattern [48-52]. Differences in growth rate are observed by changing the absolute size of an exposed Si area, referred to as local loading effect. It is also dependent on the ratio of the total exposed Si surface area to the wafer surface area, referred to as global loading effect. The local loading effect has been attributed to a chemical effect that is related to variations in lateral transport of the reactive species in the gas phase as well as on the surface [48,49,51]. The local loading effect could therefore be minimized by decreasing chamber pressure in order to maximize the lateral gas phase diffusion [49] and/or by adding a sacrificial Si seed layer on top of the surrounding isolation in order to minimize the lateral surface diffusion [50]. However, little has been reported for loading effects during NSEG, which motivates the studies in Paper 5. At the reduced-pressure conditions used, the local loading effects were indeed found to be minor, which could be attributed to a long lateral gas phase diffusion and a short lateral surface diffusion on the surrounding poly-Si layer.

The global loading effect is caused by chemical as well as thermal effects [53]. The thermal effect is only present when the heating of the wafer substrate is
dependent on the wafer surface emissivity. The thermal effect is considered to arise from wafer temperature variations caused by different wafer patterning as well as by different film stacks. The precise contribution of each of the two effects (thermal and chemical) is difficult to quantify since the reactor power supply is regulated in such a manner that the differences in wafer emissivity are being compensated; at least it is attempted to do so. The regulation of the reactor power supply could be revealed by measurement of the susceptor temperature \[\Delta T\]. The time-dependent difference in measured susceptor temperature, as referenced to the susceptor temperature for deposition on a bare Si wafer, \((\Delta T)\), is shown in Fig. 18 for three wafers with different oxide coverage. As expected, \(\Delta T\) varies during deposition and increases with oxide thickness. Such a behavior is attributed to differences in surface emissivity as discussed in Papers 6 and 7. In addition, \(\Delta T\) is almost doubled for a wafer fully covered with oxide compared to a chess patterned wafer covered with 50% of oxide. Hence, the dependence of \(\Delta T\) on the total oxide surface coverage is the cause for the thermal effect.

In Paper 5, global loading effects were observed when the oxide surface coverage increased from 0 to 50%, at the same time the size of the exposed Si area also varied. According to Fig. 18, the thermal effects should be equally large when the oxide coverage is increased from 0 to 50% as from 50 to 100%. Therefore, the main contribution to the global loading is likely due to the change in the size of the exposed Si area i.e. chemical effect. That the chemical effect is the dominant
factor is also in accordance with the observation of pressure dependence. Finally, for NSEG of SiGe without any Si buffer or a Si seed layer, the lateral surface diffusion is increased due to the difficulty to nucleate polycrystalline SiGe on oxide. Consequently, the global loading effect is present for all oxide coverage.

Stability

The lattice constant of Ge is about 4 % larger than that of Si, hence epitaxial SiGe layers on Si free from misfit dislocations are strained [54]. The stored energy, leading to generation of misfit dislocations and relieve of the strain, is therefore increased with Ge content and thickness of the SiGe layer. For a specific Ge content, there exists a certain critical thickness of the layer above which it becomes energetically favorable to form misfit dislocations [54,55]. Thus, films with thickness smaller than the critical thickness are stable whereas those with larger thickness are metastable. Stable films could be exposed to high temperature heat treatments without relaxation. For metastable films relaxation can occur, however, it is necessary to overcome an initial energy for nucleation and propagation of dislocations. Therefore, relaxation in metastable films is a consequence of many factors such as thermal process during as well as after growth, defects, stress induced by the isolation process and the size of the active area [56-58]. The stability of a SiGe film could be improved by adding a Si cap layer on top of the SiGe layer [59]. For such SiGe films with a Si cap, a theoretical maximum effective strain, \( \varepsilon_{\text{eff}} \), could be calculated according to [56,60]

\[
\varepsilon_{\text{eff}} = \frac{f_{\text{SiGe}}}{h_{\text{eff}}} \times \int_0^{h_{\text{Ge}}} \text{Ge}(z)dz
\]

for evaluation of the theoretical stability of the film. Here \( f_{\text{SiGe}} \) is the lattice mismatch between Si and Ge, \( h_{\text{eff}} \) is the total thickness of the SiGe layer and the Si cap and \( \text{Ge}(z) \) is the Ge concentration at depth \( z \) from the surface. Using Eq. (1) together with the empirical maximum effective strain found in Fig. 4 from Paper 2, the theoretical Ge concentration for a 250 Å thick SiGe box profile covered by 400 Å Si cap-layer is calculated to be approximately 25%. This calculation points to the possibility of increasing the Ge concentration (12%) used for HBTs in Papers 2, 9 and 10 to almost the double.
In Paper 2 it was found that the generation of misfit dislocations was decreased when the deposition conditions changed from 700 °C and 20 Torr to 650 °C and 80 Torr. Further, it was found in that paper that the misfit dislocations usually propagate through the active area from one side to the other. It is therefore believed that the energy needed for propagation of a dislocation is lower than the energy for nucleation of the dislocation. In addition, it seems that the energy needed to nucleate a dislocation is low at the transition between epitaxy and polycrystalline regions. The density of misfit dislocations was also studied for two samples with different thickness of the Si buffer layer. A top-view micrograph of the active areas (diameter 150 µm) is shown in Fig. 19 after Secco etching. The samples have almost identical stacks but consisting of a (a) 100 Å or (b) 300 Å Si buffer with a 400 Å SiGe with 22 % Ge and then a 400 Å B-doped \(5 \times 10^{18} \text{ cm}^{-3}\) Si cap. From Eq. (1) it is apparent that the effective strain in those samples should be identical. However, it is clearly revealed in Fig. 19 that misfit dislocations have only been generated for the sample with a thicker buffer layer. This indicates that the stability is also sensitive to the thickness of the buffer layer for NSEG. The origin of this dependence is not understood but it could be due to the poly-Si extending into the epitaxy.

The stability of these two films was also investigated by implanting P through the NSEG film, in order to simulate an ordinary SIC process. These wafers were compared to wafers where the SIC implantation had been performed before the NSEG process. Utilizing the SIC implantation before or after the SiGe epitaxy does not introduce any visible defects in agreement with literature data [61]. However, an increase in the leakage current emitter-collector has been observed when the SIC implantation was performed after NSEG [61].

Figure 19. Top-view micrographs for two identical film stacks with different thickness of the Si buffer layer (a) 100 Å and (b) 300 Å.
Chapter 5

Temperature control

In the preceding chapter, variations in growth rates for epitaxy and polycrystalline deposition were discussed with reference to appended Papers 4 and 5. The distinct growth rates for epitaxy and poly-Si deposition can be caused by two concurrent effects. One is the difference in growth kinetics that governs how the growths depend on the various parameters for deposition (temperature, pressure, gas composition, etc.). The other is the deviation in wafer temperature from the expected values, which can arise from wafer surface emissivity changes. The influence of these two effects on the growth rate was investigated in Paper 6 from which the former was shown to be the dominant effect. However in Paper 7, the wafer heating mechanisms in a lamp-heated reactor was thoroughly investigated in order to reveal the effect of wafer surface emissivity and absorptivity. The emissivity and absorptivity are defined as the efficiency to emit and to absorb, respectively, energy via thermal radiation compared to the ideal case of a blackbody. Since the wavelengths of thermal radiation are comparable with the thickness of the oxide isolation and the poly-Si film deposited using NSEG, interference occurs resulting in variation of the wafer emissivity and absorptivity during deposition. As a consequence, the wafer temperature may change with deposition time. Since the deposition is done in the surface-reaction limited regime at relatively low temperatures, small temperature variations may cause large differences in growth rate. The purpose of this chapter is therefore to review the heating mechanisms, used in Paper 7, in a lamp-heated reactor with a heat conducting susceptor. In Section 5.1, the heat transfer model used in this work is described. Once the temperature variation is known, the instantaneous growth rate can be calculated, which is presented in Section 5.2. Finally in Section 5.3, a discussion of how the various parameters used in the model affect the calculation is presented.
5.1 Heat transfer model

In order to obtain a better understanding of the growth rate variation during deposition as observed in the appended Papers 6 and 7, it is necessary to calculate the wafer emissivity and absorptivity for each layer of deposited poly-Si on oxidized Si substrate wafers. When considering the normal incident heat radiation to the wafer surface only, the total normal emissivity ($E$) and absorptivity ($A$) of the wafer for a specific poly-Si and oxide thickness can be determined according to [62-64],

$$E = \int \varepsilon_w I_{b,w} d\lambda / \int I_{b,w} d\lambda$$

and

$$A = \int \alpha_w I_{b,l} d\lambda / \int I_{b,l} d\lambda$$

where $\varepsilon_w$ and $\alpha_w$ are respectively the wafer spectral emissivity and absorptivity. $I_{b,w}$ and $I_{b,l}$ are the wafer and lamp spectral intensity, respectively, at their respective temperature. The spectral emissivity and absorptivity are related by Kirchhoff’s law, stating that the emissivity is equal to the absorptivity under same conditions. When an incident beam hits a surface, one part of it is reflected and another part is transmitted. The part which is neither reflected nor transmitted is absorbed. Using Kirchhoff’s law, the emissivity of a surface could be extracted from the relation $1 = \varepsilon + R + T$, where $R$ is the total reflectivity and $T$ the total transmissivity. Calculations of $R$ and $T$ are described in textbooks using the theory of thin film coating [62]. $R$ and $T$ are consequences of multiple reflections and are strongly dependent on thickness and complex refractive index of the different films covering the sample surface. In the calculations presented in this thesis, literature data for the optical parameters of Si at 650 °C was used [62]. The optical parameters for single-crystal Si were employed for poly-Si, as the optical properties of them are comparable [62]. The refractive index of SiO$_2$ was assumed to be independent of wavelength in the region investigated and taken at a wavelength of 2 µm from Ref. [65].

A simple model of energy balance for the wafer is derived by considering the absorption on the wafer front surface due to the lamp radiation, the emission from the wafer front surface, the thermal conduction and convection on the front surface as well as the thermal conduction on the wafer back surface. The radiative
heat exchange between the wafer back surface and the susceptor is assumed to be minor, as the temperature and emissivity of these bodies are comparable. The heating rate of the wafer, for a specific poly-Si and oxide thickness, is then given by,

\[
\frac{dT_w}{dt} = \frac{a}{m C_p} \left[ \varepsilon_i \times \int_{\lambda} \alpha \lambda\lambda d\lambda - \left( \varepsilon_w I_{w} d\lambda - R_f \times (T_w - T_c) - R_b \times (T_w - T_s) \right) \right]
\]

where \( T \) denotes temperature, \( t \) time, \( a \) wafer area, \( m \) wafer mass, \( C_p \) specific heat, \( \varepsilon_i \) the effective lamp emissivity, \( R_f \) and \( R_b \) the heat transfer coefficients on the wafer front and back surface, respectively. The subscripts \( w, c \) and \( s \) stand for wafer, chamber and susceptor, respectively. The first term in the brackets on the right hand side correspond to the absorption of the incident tungsten-halogen lamp radiation to the wafer front surface. Usually the lamp radiation is modeled as a blackbody between 2000 and 3000 °C \([62-64,66-68]\). In this temperature range, the peak of the radiation spectrum is at the wavelength close to 1 \( \mu \)m. Since the incident lamp radiation is transmitted through the quartz process chamber, wavelengths greater than 4.5 \( \mu \)m are prohibited \([63,67]\). Thus, the integration of the first term covers wavelengths in the range of 0.5-4.5 \( \mu \)m. In this range, the normal spectral emissivity of the tungsten filament varies from 0.45 to 0.15, independently of the actual temperature range \([66]\). For simplicity, an average value of 0.3 is used for modeling the emissivity of the tungsten filament \([64,68]\).

The view factor, expressing the radiative heat exchange between the lamp bank and the wafer, is dependent on the physical dimensions of the lamps, the number of lamps and their individual spacing, and the perpendicular distance between the lamps and the wafer. Since the thickness of an non-rotating wafer was rather uniform, the energy supply from the lamp bank is considered to be uniform over the wafer. Hence, the view factors are assumed to be the same over the wafer. From the literature, a view factor of 0.1 is used \([64]\). The effect of the view factor and the tungsten emissivity were combined in Eq. (4) as part of the effective lamp emissivity in our model.

The second term in the brackets, corresponds to the thermal emission from the wafer front surface. The integration was performed from 0.5 to 33 \( \mu \)m wavelengths, covering 99.5 % of the energy radiated from a blackbody at the temperature considered, 650 °C.
The third term in Eq. (4) is an estimate of the heat loss from the wafer front surface due to thermal conduction and convection to the process chamber. The heat transfer coefficient $R_f$ is calculated according to [69],

$$R_f = \left( \frac{h_{\text{quartz}}}{k_{\text{quartz}}} + \frac{h_{\text{chamber}}}{k_{\text{H}_2}} \right)^{-1} + \frac{0.664 \times k_{\text{H}_2} \times Pr^{1/3} \times Re^{1/2}}{l_s}$$

(5)

where the first term represents the thermal conduction and the second term the thermal convection. $h_{\text{quartz}}$ is the thickness of the quartz process chamber wall and $h_{\text{chamber}}$ is the perpendicular distance from the susceptor to process chamber wall. $k_{\text{quartz}}$ and $k_{\text{H}_2}$ are the thermal conductivity of quartz at 200 °C [70] and H$_2$ gas at 700 °C, respectively [71]. From the calculations, it was concluded that the thermal resistance in the H$_2$ gas dominates the thermal conduction. The contribution from the thermal convection is calculated using a simple approximation of H$_2$ gas flow over a hot plate [69,70]. Here, $l_s$ is the length of the susceptor, $Pr$ the Prandtl number and $Re$ the Reynold number. They are given by [69],

$$Pr = \frac{\eta \times C_p}{k_{\text{H}_2}}$$

(6)

$$Re = \frac{\rho \times l_s}{\nu \times \eta}$$

(7)

where $\eta$ is viscosity, $\rho$ density of H$_2$ gas at 700 °C [71], and $\nu$ the H$_2$ gas flow velocity. When $Re$ is smaller than 1200, the flow is laminar. For higher numbers of $Re$, the gas flow becomes turbulent. For the conditions used here $Re$ on the order of 700 was calculated. The contributions of the conduction and convection to $R_f$ in Eq. (5) were rather evenly divided. The estimations showed that the emission from the wafer front surface contributed to approximately 75 % of the total heat loss from the wafer front surface.

The contact and thermal resistance between the wafer and susceptor was accounted for by the heat transfer coefficient on the wafer back surface $R_b$ in Eq. (4). Because of the difficulty to estimate its value, the wafer and susceptor were simply assumed to be separated by a 0.5-mm thick H$_2$ gas film similarly as in the calculations presented in Papers 5 and 7.
5.2 Instantaneous growth rate

Once the heating rate of the wafer was known from Eq. (4), the instantaneous wafer temperature could be calculated. Since the wafer is not in direct contact with the susceptor, its temperature can differ from the set-point read at the thermocouple in the susceptor. This can be the case even prior to deposition. The initial wafer temperature is in our case determined by adjusting the energy supply from the lamps in order to yield a wafer as well as susceptor temperature close to the set-point value. The instantaneous wafer temperature is then given by,

\[ T_{w,i} = T_{w,i-1} + \frac{dT_{w,i}}{dt} \Delta t \]  

(8)

where \( T_{w,i-1} \) is the wafer temperature at the preceding time-interval and \( \Delta t \) an infinitesimal time-interval over which the wafer temperature is taken as constant. At the beginning of the growth, \( T_{w,i-1} \) is identical to the initial wafer temperature. Thus, the wafer temperature at any deposition time was obtained. The instantaneous growth rate of poly-Si could then be modeled according to,

\[ GR_i = A_0 \times e^{-E_a/kT_{w,i}} \]  

(9)

using the growth rate kinetic parameters from Paper 4. Here, \( GR_i \) is a time dependent growth rate, \( A_0 \) the pre-exponential factor, \( E_a \) the apparent activation energy and \( k \) the Boltzmann constant.

5.3 Influence of estimated parameters

In this section, some of the parameters estimated for Eq. (4) are varied in order to quantify influence on the growth rate calculations. The results are compared to the model conditions used in the calculations in Paper 7 and described in Section 5.1. In Figs. 20, 21 and 22 calculations results are shown for poly-Si deposition on a Si wafer covered with a 4000 Å thick oxide.

As pointed out in Paper 7, a precise knowledge of the algorithm for controlling the power supply to the lamp bank in the reactor is lacking. However, it is only
the first term in the heat transfer model, Eq. (4), that is affected by the lamp regulation. Therefore, the two extreme temperature regulation cases were evaluated; (a) constant radiation in which the lamp temperature was kept constant during deposition and (b) constant absorption in which the lamp temperature was regulated following the variations of the wafer absorptivity in order to maintain a constant energy supply to the wafer. In Paper 7, it was shown that the constant absorption approach agreed better with susceptor temperature measurements as well as observed growth rate behavior than the constant radiation approach. Nonetheless, both approaches were studied and the calculated growth rate is shown in Fig. 20 for two different effective lamp emissivities 0.03 (model conditions used in Paper 7) and 0.21. The latter value was calculated from the product of the tungsten filament emissivity (0.3) and the view factor for two parallel plates (0.7) extracted according to a textbook [70]. For the constant absorption approach, a minor difference is observed, however, a difference is noticed for the constant radiation approach. This difference is due to the lower lamp temperature required when the effective lamp emissivity is increased. As a result, the peak wavelength in the blackbody spectrum is shifted towards longer wavelength and the minimum growth rate occurs at a thinner poly-Si thickness.

Figure 20. Growth rate as a function of thickness of deposited poly-Si for constant absorption and constant radiation.
The influence of heat transfer coefficient due to conduction and convection on the wafer front surface is shown in Fig. 21. The growth rate is plotted as a function of thickness of the deposited poly-Si for \( R_f \) values varied from one fifth of the extracted value using Eq. (5) in Section 5.1 to five times that value. As expected, only a minor difference in growth rate is observed since the main contribution for the thermal heat loss on the wafer front side is due to heat emission. The increase in growth rate when decreasing \( R_f \) is due to the reduced heat transferred away from the wafer. From these calculations, it is concluded that the calculated growth rate is only slightly influenced by the thermal conduction and convection on the wafer front surface. Furthermore, the shape of the curve is almost independent of this parameter.

The heat transfer coefficient, \( R_b \), due to the thermal resistance between the wafer and susceptor is varied from half the estimated value to twice that value, for the calculations presented in Fig. 22. This is equivalent to changing the thickness of the \( \text{H}_2 \) gas film between the wafer and susceptor, as in Paper 5. For poly-Si films with thickness smaller than 1000 Å, the growth rate is quite independent of \( R_b \). For thicker films, the growth rate increases with decreasing \( R_b \). Consequently, the wafer temperature increases with increasing thermal resistance between the wafer.
and susceptor. According to the total normal emissivity of the wafer calculated in Paper 6, the growth rate begins to increase and becomes dependent on $R_b$ (see Fig. 22) when the wafer emissivity starts to drop at a poly-Si thickness of approximately 1000 Å. However, the overall shape of the growth rate curves seems to be independent of $R_b$, although the difference between the minimum and maximum growth rate is a strong function of this parameter. As observed in Fig. 22, it is of major importance to minimize the thermal resistance in order to yield a growth rate that is less sensitive to the surface absorptivity/emissivity. Hence, a better thermal contact for the wafer substrate to the susceptor is crucial.

Finally, Fig. 23 shows how the growth rate varies for oxide thickness of 15, 1000, 4000 and 5300 Å. The results with 15 Å thick oxide indicates a negligible influence of such thin oxides on wafer surface emissivity as expected. Furthermore, a large variation in the growth rate behavior is seen for the different oxide thickness since the wafer emissivity is a strong function of the thickness of each individual film. Comparing these results of the growth rate variations in Fig. 23 with wafer temperature calculations in Paper 5, a different behavior of the temperature change with the thickness of deposited poly-Si is noticed. This difference is primarily due to the assumption of a constant lamp radiation in Paper 5 in combination with the simulation of the lamp bank as a blackbody at a much

Figure 22. Growth rate as a function of deposited poly-Si for different values of the back surface heat transfer coefficient ($R_b$).
lower temperature. Moreover, the shape of the growth rate in Fig. 23 looks very similar to the experimentally determined results in Ref. [53]. However in those experiments, the growth rate on a bare Si wafer was always higher than on a wafer with a film stack containing oxide [53], opposite to what is anticipated in Fig. 23. This might be due to different reactor design and/or different algorithm for controlling the power supply to the lamp bank.

From the calculations above, it is clear that the thermal contact between the wafer and the thermocouple becomes crucial when the wafer temperature deviates from the susceptor temperature. On the other hand, direct wafer temperature measurements relying on pyrometers suffer from variations of wafer surface emissivity. Therefore, methods for direct measurement of wafer temperature, such as monitoring the propagation of acoustic waves in Si, are needed [72].
Chapter 6

Concluding remarks

The vertical dimensions of the bipolar transistor have been scaled down by the implementation of an in situ P doped poly-Si emitter and the growth of a non-selective epitaxial base. The use of epitaxy for base fabrication permits the incorporation of SiGe. This addition has, due to the possibility of bandgap engineering, greatly promoted Si-based high-speed HBTs. Using these two techniques, high-speed bipolar transistors with cut-off frequency of 62 GHz have been fabricated at KTH.

In this thesis, several aspects of the deposition of in situ P doped poly-Si emitter have been investigated, starting from growth kinetics, use of Si source gas and dopant incorporation, through crystallization, dopant segregation and grain growth, to implementation of the poly-Si emitter with interface treatments and dopant drive-in. Furthermore, NSEG for base fabrication has been thoroughly investigated with a focus on pre-epitaxy cleaning, growth kinetics for epitaxy as well as for poly-Si deposition, dopant incorporation, generation of misfit dislocations and loading effects. In addition, temperature control of a lamp-heated single-wafer reactor has been examined in depth since the wafer surface emissivity varies during growth causing the wafer temperature to change. A small change in wafer temperature can result in a drastic variation in growth rate since the growth is performed in the surface-reaction controlled regime.

As the lateral dimensions of the devices will shrink even further, the control of the vertical profiles will be even more critical in order to attain desired device performance. Hence, the diffusion of dopants must be further minimized by lowering the various processing temperature after base epitaxy, e.g. oxide and nitride depositions as well as silicide formation. The integrity of SiGe films will
also benefit from a lowered thermal budget permitting an increased Ge concentration. Another method to maintain the sharp doping profiles after epitaxy is the incorporation of carbon in the SiGe base layer to suppress B diffusion [73]. The addition of carbon to the SiGe layer can also reduce the strain induced by the mismatch between Si and Ge, since the atomic size of carbon is smaller than that of Si and Ge. As a result, CVD of SiGeC has to be investigated with respect to growth and materials properties such as quality of epitaxy, dopant incorporation and diffusion and loading effects. In addition, bipolar transistor architectures designed to implement the collector using low-temperature epitaxy are also likely to appear. The performance of high-speed bipolar transistors could be further improved by replacing the Si wafer substrate with silicon-on-insulator (SOI) or silicon-on-sapphire (SOS) wafers. Thus, epitaxy on SOI and SOS wafers should be studied with emphasis on issues such as quality of epitaxy and temperature control. Nevertheless with today’s process techniques, researchers at IBM have demonstrated SiGe HBTs working at 210 GHz [74]. This latest achievement shows once again the bright prospect as well as the robustness of Si technology.
References


Summary of the appended papers

**Paper 1  Characterization of in situ phosphorus-doped polycrystalline silicon films grown by disilane-based low-pressure chemical vapor deposition**

LPCVD of *in situ* P doped poly-Si films was investigated in the temperature range of 415 to 560 ºC. No difference in activation energy was observed between undoped and doped films. The electrical and structural properties were studied as a function of doping as well as heat treatments for films deposited at 480 ºC. Differences such as grain size, film texture and resistivity for films grown using Si$_2$H$_6$ or SiH$_4$ were attributed to the difference in growth temperature. The author made all the samples, did most of the measurements and participated in writing the manuscript.

**Paper 2  Epitaxial growth of SiGe layers for BiCMOS applications**

Generation of misfit dislocations, the thermal stability and the correlation of leakage current with the presence of defects were investigated for NSEG of SiGe films for HBTs. The films were grown at 650 and 700 ºC under reduced-pressure conditions. The misfit dislocations originated from the transition poly-Si/epitaxy and could be correlated to leakage in the devices. Growing the films at 650 ºC resulted in defect free films. The author performed most of the sample preparation and measurements and participated in writing the manuscript.

**Paper 3  Hydrogen in undoped and heavily in situ phosphorus doped silicon films deposited using disilane and phosphine**

The kinetics of hydrogen incorporation in amorphous silicon films was studied. The hydrogen concentration, determined by NRRA, decreased with increasing deposition temperature. The addition of phosphine also reduced the hydrogen incorporation. The activation energy for H$_2$ desorption from undoped silicon was
estimated to be $1.8 \pm 0.2$ eV. This energy increased with the addition of phosphine. The author made all the samples, did some of the measurements, conducted the analysis and wrote the manuscript.

**Paper 4**  
*Chemical vapor deposition of undoped and in-situ boron- and arsenic-doped epitaxial and polycrystalline silicon films grown using silane at reduced pressure*

The growth kinetics were studied for epitaxy and poly-Si depositions at similar conditions. A growth mechanism assuming dissociative adsorption of SiH$_4$ together with first-order H$_2$ desorption kinetics could explain the observed differences in activation energy and partial pressure of H$_2$. The difference in dopant incorporation in epitaxy and poly-Si films was investigated for B and As. The incorporation was larger in poly-Si with a factor of 5 and 20 for B and As, respectively. The author proposed and organized the work, made all samples, did most of the measurements and wrote the manuscript.

**Paper 5**  
*Loading effects during non-selective epitaxial growth of Si and SiGe*

Growth rate variations due to different pattern on the oxide as well as different sizes of the openings are presented. Doping incorporation of B and As on blanket wafer and on patterned wafers were compared. A simple model for estimating the wafer temperature was developed. The author came up with the idea, organized the work, made all samples, did most of the measurements and wrote the manuscript.

**Paper 6**  
*Effects of growth kinetics and surface emissivity on chemical vapor deposition of silicon in a lamp-heated single-wafer reactor*

An investigation on the contribution from growth kinetic and surface emissivity for the different growth rate observed for epitaxy and poly-Si deposition was performed. Deposition were done on bare silicon, oxidized silicon wafers and SOI substrates. The difference in kinetics was found to play a more dominant role than the surface emissivity. The author proposed and organized the work, performed sample preparation, made all calculations and wrote the manuscript.

**Paper 7**  
*Chemical vapor deposition of silicon in a lamp-heated reactor: Effects of heat absorption, emission and conduction*

Poly-Si depositions were performed on 100 mm in diameter silicon-on-sapphire (SOI) wafers and on 100 and 200 mm silicon wafers in order to study the
temperature control in the lamp-heated ASM reactor. Similar deposition rates on silicon and SOS substrates confirmed that heating by conduction was the main mechanism for heating the wafers. Calculations of emissivity and absorptivity in combination with susceptor temperature measurement indicated that the lamp radiation was regulated in response to wafer emissivity and absorptivity variations. A model to describe the growth rate and temperature regulation was developed. The author suggested and organized the work, performed sample preparation, did all theoretical analysis and wrote the manuscript.