Process optimization for the 4H-SiC/SiO2 interface.

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Finally this thesis is dedicated to all the oppressed of this world, with the expression of the desire and hope that any kind of exploitation in this society will be extinct one day.
Abstract

This thesis aims to optimize the process for the 4H-SiC/SiO₂ interface formations. The experiments are made on metal-oxide-semiconductor (MOS) structures, where the semiconductor is an n-type epitaxially grown 4H-SiC thin film. The oxide is fabricated either with thermal oxidation, or by using plasma-enhanced chemical vapour deposition (PeCVD), utilising two different tools, Precision 5000 Mark II (P5000) and Plasmalab 80Plus system (Pekka). The deposition temperature is varied for the thermally grown oxide, while power, pressure and gas ratio of N₂O/SiH₄ is investigated for the PeCVD method. Also the post deposition annealing (PDA) temperature is studied for both techniques. The oxide formation and PDA is done in N₂O ambient in order to study the effect of nitrogen passivation of the traps that exist at the interface of 4H-SiC/SiO₂. After the dielectric formation the structures are electrically and structurally characterized. The electrical characterization is done by capacitance-voltage (CV) and current-voltage (IV) measurements while the structural characterization is done with atomic force microscopy (AFM). The density of interface traps (D𝑖𝑡) is extracted using the Terman method from CV data. It is observed that the flatband voltage drops almost to zero when the samples are annealed in nitrogen rich ambient, resulting in a more electrically uniform oxide. Also, D𝑖𝑡 can also be reduced by nitrogen treatment when the oxide is deposited by the PeCVD technique. However, it appears that the Terman method cannot determine the amount of traps along the entire bandgap and it is clear that a large amount of D𝑖𝑡 are still present closer to the conduction band. Finally, it is found that there is a larger spread in the data extracted from the samples deposited by P5000 in comparison to Pekka, indicating that Pekka is a more reliable tool for oxide deposition in SiC substrate.
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Chapter 1. Introduction

By considering the main criteria for high power electronic systems, such as power density, efficiency, and reliability, one can see the limitation of silicon based devices. For example, the maximum temperature for operation of Si based devices is 150-175 °C, which make them unsuitable for harsh environmental conditions and high power densities [1]. Due to this fact, researchers head for new alternative material systems for high power and high temperature applications. Silicon carbide of the 4H polytype (4H-SiC), which is one of the three SiC polytypes that are used in power electronics, has very suitable properties for these applications, such as wide band gap (3.2 eV), high thermal conductivity (4.9 W/cmK), high saturated carrier velocity ($2\times10^7$ cm/s) and high breakdown electric field (2.2 MV/cm) [1,2]. With these excellent material properties, 4H-SiC has become a leading material for future electronic power devices. Another advantage is that the dielectric material silicon dioxide (SiO$_2$) is the native oxide of SiC and this can be thermally grown [2,3]. Dielectric materials are needed to passivate the semiconductor surface and also to form gate oxide in field effect devices. Although promising properties of SiC have been extensively studied and verified, there are still many challenges waiting to be overcome in order to manufacture reliable devices based on SiC. One of these challenges is the high density of interface traps between SiC and SiO$_2$ [4]. Such traps can capture electrons or holes and are very difficult to control in the process. They cause degradation and problems with long term stability of devices and also lower the mobility of charge carriers underneath the gate in MOS devices.

The main method today to reduce the negative effect of such traps is to passivate them by introducing nitrogen at the interface. The nitrogen atoms form chemical bonds with defects, thus passivating the electrical activity at these bonds so they no longer can trap and de-trap charges. During the past two decades different techniques have developed for adding nitrogen, for instance oxide deposition, or thermal oxidation in N$_2$O ambient and/or post deposition/growth annealing in N$_2$O ambient [4,5,6].

In this thesis two different ways of oxide fabrication and the effect of annealing in N$_2$O ambient will be studied. The first of them is plasma-enhanced chemical vapour deposition (PECVD) by using two different instruments, Precision 5000 Mark II (P5000) and Plasmalab 80Plus system (Pekka). The other way to fabricate the oxide layer is by thermal growth. By varying the different parameters of the fabrication, such as power, pressure and the gas ratio of N$_2$O/SiH$_4$ for PeCVD, and also the post-deposition/growth annealing temperature for both methods, we hope to optimize the oxide formation process for 4H-SiC device fabrication. The samples used for the study are MOS capacitors with n-type 4H-SiC as semiconductor, SiO$_2$ is the dielectric and a circular aluminium gate forms the metal contact. The characterization techniques that are used are capacitance-voltage (CV) and current-voltage (IV) for electrical characterization, atomic force microscopy (AFM) for the structural characterization.

The study shows that it is possible to reduce the interface traps by forming the SiO$_2$ in nitrogen containing ambient. Post deposition annealing in nitrogen ambient results in a more homogeneous oxide in terms of electrical behaviour. Finally, when comparing the two setups for SiO$_2$ deposition, Pekka appeared to be more reliable.
Chapter 2. Material properties and MOS theory

In this chapter the properties of SiC and SiO$_2$ will be discussed and also the SiC/SiO$_2$ interface will be examined. Finally, there will be a short review of MOS theory to define the parameters used for analysis.

2.1 Material properties

2.1.1 Silicon Carbide properties

Silicon carbide (SiC) is composed of stacked layers of closed-packed planes of silicon and carbon atoms. SiC exists in 300 different crystal structures, which are called polytypes [7], depending on the stacking sequence of the layers. Among them only three polytypes are presently of interest for the semiconductors industry due to their remarkable electric properties. The first is 3C-SiC, where C stands for cubic, which is also called β-SiC. The other two are 4H-SiC and 6H-SiC, where H stands for hexagonal lattice. The hexagonal lattice polytypes are referred to as α-SiC. The stacking sequence of Si-C bi-planes of these different polytypes is illustrated in Figure 2.1.

![Figure 2.1 The three different types that are used in the electronics industry [7]](image)

A comparison of the various material properties of the three different polytypes is given in Table 2.1. In this investigation the 4H-SiC polytype is used.

<table>
<thead>
<tr>
<th>Property</th>
<th>3C-SiC</th>
<th>4H-SiC</th>
<th>6H-SiC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Band Gap (eV)</td>
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<td>3.2</td>
<td>3</td>
</tr>
<tr>
<td>Critical Electric Field (MV/cm)</td>
<td>2</td>
<td>2.2</td>
<td>2.5</td>
</tr>
<tr>
<td>$\varepsilon_r$</td>
<td>9.7</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>$\lambda$ (W/cmK)</td>
<td>5</td>
<td>4.9</td>
<td>5</td>
</tr>
<tr>
<td>$\mu_n$ (cm$^2$/Vs)</td>
<td>750-1000</td>
<td>800-1000</td>
<td>370-500</td>
</tr>
<tr>
<td>$\mu_p$ (cm$^2$/Vs)</td>
<td>40</td>
<td>115</td>
<td>90</td>
</tr>
</tbody>
</table>
2.1.2 Silicon Dioxide properties

Silicon dioxide (SiO$_2$) is the natural oxide of Si and SiC, which makes it a preferable candidate for gate dielectric and passivation. Silicon dioxide has a relative dielectric constant of 3.9, a band gap of 9 eV, and an offset of 2.7 eV in comparison to the conduction band of 4H-SiC. The critical electric field and thermal conductivity of SiO$_2$ are 10 MV/cm and 0.015 W/cmK, respectively [9]. There are different techniques to fabricate the SiO$_2$ dielectric, either with thermal growth or by deposition. Deposition can be done in different ways, such as chemical vapour deposition (CVD), plasma enhanced chemical vapour deposition (PeCVD) and atomic layer deposition (ALD) [9].

2.1.3 Traps in SiC/SiO$_2$ interface

The channel mobility for 4H-SiC is found to be lower by two to three orders of magnitude than the bulk mobility because of the existence of traps along the interface between SiC and SiO$_2$ [6,10]. There are two main reasons for these traps to be formed, a) interfacial carbon clusters and b) near interfacial oxide defects [11,12]. The behaviour of the interfacial carbon clusters vary depending on the size of the cluster. The energy spectrum for electrons of small sized clusters is similar to the electronic energies of wide band gap amorphous hydrogenated carbon (a-C:H). Figure 2.2a shows the electronic energies around the bandgap of a-C:H. The filled states to the right in Fig. 2.2a, which are $\pi$-bonds of $sp^2$-hybridised carbon atom, are distributed up to 1.4 eV above the valence band of 4H-SiC. As long as those states are filled, they are neutral. Though it is possible that electrons transit from these states to the Fermi level of the semiconductor, resulting in a positive charge and, in the case of a p-type semiconductor, this phenomenon will affect its mobility. On the other hand, the empty states of the antibonding $\pi^*$ levels appear to be more than 1 eV higher than the upper conduction band of 4H-SiC, which has the broadest band gap of all the SiC polytypes, so they do not seem to affect the performance of the device [11,12].

Figure 2.2.b shows the energy spectrum of graphite. As the size of the cluster increases, it starts to behave more like graphite with a continuous electronic spectrum, which can be charged positively if it traps a hole, or negatively if it traps an electron in p-type and n-type SiC, respectively. In other words, depending on the relative position of the Fermi level of SiC and the neutrality level of graphite, which coincide with the Fermi level of the cluster, found at 2.5 eV above the valence band of SiC, electrons may be emitted or be trapped[11,12].

Figure 2.2.c illustrates the energy spectrum of the oxide defects, who will affect the performance of the n-type MOS of 4H-SiC [12]. The near interfacial oxide defects, which may be oxygen vacancies or carbon interstitial, have an energy level are around 2.8 eV below the conduction band of SiO$_2$ as can be seen from the figure.
2.1.4 Passivation of the interface traps

Afanasev et al. found in the early 90’s that the density of interface traps ($D_{it}$) in SiC/SiO$_2$ is in the order of $10^{13}$ eV$^{-1}$ cm$^{-2}$ close to the conduction band [10], which is several orders of magnitude higher than at a well-passivated Si/SiO$_2$ interface. One of the common methods to passivate the interface traps is to introduce nitrogen (N) [10,13,14]. The most probable explanation of why N can actually passivate the traps at the SiC/SiO$_2$ interface is that N can replace the interstitial carbon, or can be placed in a vacancy. Also N can react with the carbon clusters and form CN molecules, which later diffuse into the oxide away from the interface [13].

There are different ways of inserting N into a MOS structure. Firstly, the oxide can be thermally grown in nitric oxide (NO) or nitrous oxide (N$_2$O) ambient [10,13,14]. It has been reported that $D_{it}$ decreased to 2$\times$10$^{11}$ eV$^{-1}$ cm$^{-2}$ for NO oxidation at 1175 °C and to 4$\times$10$^{11}$ and 1$\times$10$^{12}$ eV$^{-1}$ cm$^{-2}$ for N$_2$O oxidation at 1300 °C and 1410 °C, respectively [6]. Another way is, after the fabrication of the dielectric, to anneal the samples in NO, N$_2$O and N$_2$ ambient [10,13,14]. For NO post oxidation annealing (POA) it has been reported that the $D_{it}$ value dropped to 1-2$\times$10$^{12}$ eV$^{-1}$ cm$^{-2}$ and 3-5$\times$10$^{11}$ eV$^{-1}$ cm$^{-2}$ for annealing temperatures 1175 °C and 1410 °C, respectively, while the channel mobility increase to 30-40 cm$^2$ V$^{-1}$ s$^{-1}$. For N$_2$O POA at 1175 °C the $D_{it}$ reduced to 3$\times$10$^{11}$ eV$^{-1}$ cm$^{-2}$ and the mobility rose at 49 cm$^2$ V$^{-1}$ s$^{-1}$. On the other hand, when oxide was deposited and annealed in N$_2$O ambient at 1150 °C there are references that measured the $D_{it}$ at 4-8$\times$10$^{11}$ eV$^{-1}$ cm$^{-2}$ and the channel mobility at 24-40 cm$^2$ V$^{-1}$ s$^{-1}$. Finally, for N$_2$ POA the $D_{it}$ was found 4$\times$10$^{11}$ eV$^{-1}$ cm$^{-2}$ [6]. All the above $D_{it}$s were measured at 0.2 eV below the conduction band of 4H-SiC.
2.2 MOS theory

One of the most important electronic components, which are used in integrated circuits, is the metal-oxide-semiconductor (MOS). The MOS structure consists of the following: a semiconductor as the substrate (or body), doped p- or n-type. On top of the substrate is an oxide deposited, or grown, depending on the oxidation method and on top of this oxide a metal is placed which function as the gate contact. An ideal MOS capacitor is at flatband condition when there is no applied voltage at the gate. The energy band diagram is the following.

Figure 2.3. Energy band diagram of the flatband condition ($V_G=0$) for an Ideal MOS capacitor for a) nMOS b) pMOS [15]

In Figure 2.3 $E_V$, $E_C$, $E_F$, $E_g$ and $E_i$ are the valence band edge, conduction band edge, Fermi level, energy band gap and the intrinsic level ($E_i=E_g/2$) of the semiconductor, respectively. Using the elementary charge $q$, the electron affinity expressed in electron volts is $q\chi$ of the semiconductor and $q\chi_i$ is the electron affinity of the oxide. The energy differences $\Psi_{Bn}$, $\Psi_{Bp}$, $\Phi_n$, $\Phi_p$ are the fermi potentials with respect to midgap and the band edges [16]. The quantities $\Phi_m$ are the metal work function and $\Phi_B$ the potential difference between the metal fermi level and the conduction band of the dielectric. The top level is the vacuum level used as a reference level for free electrons.

As can be seen from the figure, under the conditions of flat bands the difference between the metal work function and the semiconductor work function ($\Phi_{ms}$) is zero:

$$\Phi_{ms} = \Phi_m - \left(x + \frac{E_g}{2q} + \Psi_{Bp}\right) = \Phi_m - \left(x + \frac{E_g}{q} - \Phi_p\right) = 0 \text{ for } p\text{-type} \quad (2.1a)$$

$$\Phi_{ms} = \Phi_m - \left(x + \frac{E_g}{2q} - \Psi_{Bn}\right) = \Phi_m - (\chi + \Phi_n) = 0 \text{ for } n\text{-type} \quad (2.1b)$$
In real cases, however, $\Phi_{ms}$ is seldom negligible and must be taken into account. In addition, there are always in the real case extra charges in the oxide and at the interface that needs to be taken into account, and will result in band bending of the structure.

In case the gate voltage is not zero, three different situations are distinguished: accumulation, depletion and inversion. Figure 2.4 illustrates the cross section of the MOS capacitor and the band diagrams for these states for a p-type semiconductor.

![Figure 2.4](image)

*Figure 2.4. The charge distribution in the top figure and band diagram for a p-type MOS capacitor at the bottom figure, for a) accumulation b) depletion and c) inversion is shown. The Fermi level in the semiconductor is denoted by a dashed line [15, 17]*

a) **Accumulation**

When negative voltage is applied at the gate for p-type substrate, the band edges of the semiconductor are bent upwards which results in the accumulation of holes at the interface of the semiconductor and the oxide.

b) **Depletion**

When a positive voltage is applied, lower than the threshold voltage which will be defined below, the bands are bending downwards, while the intrinsic level is still above the Fermi level. This results in the appearance of depletion region with width $W_{dep}$ which is given by:

$$W_{dep} = \sqrt{\frac{2 \varepsilon_s \Phi_s}{qN_A}}$$  \hspace{1cm} (2.2)

where $\varepsilon_s$ is the electrical permittivity of the semiconductor, $q\Phi_s$ is the band bending ($\Phi_s$ is called surface potential) and $N_A$ is the doping concentration. The charge in the depletion region is equal to $-qN_A W_{dep}$.
c) Inversion

The voltage at which the inversion begins is called threshold voltage and is given by:

$$V_t = V_{fb} + \Phi_{st} + \frac{\sqrt{q N_A^2 \varepsilon_s \Phi_{st}}}{C_{ox}}$$  \hspace{1cm} (2.3)

As seen for an ideal MOS capacitor (Fig. 2.3), the flatband voltage $V_{fb}=0$, but in a real case some voltage needs to be applied to reach flat band conditions. When the voltage, which is applied, is higher than threshold, the bands are bending more until the intrinsic level goes below the Fermi level, which results in that the p-type substrate is inverted to n-type, i.e. there will be a higher concentration of electrons than holes at the interface. A practical criterion for when the semiconductor surface is sufficiently n-type to allow an electron channel to appear is given by the strong inversion. The condition for strong inversion is when the surface potential is as high above the Fermi level as it was below in the unbiased case, i.e. for

$$\Phi_{st} = 2\Phi_B = 2 \left( \frac{kT}{q} \right) \ln \left( \frac{N_A}{n_i} \right)$$  \hspace{1cm} (2.4)

Here, $C_{ox}$ is the oxide capacitance, $k$ is the Boltzmann constant, $T$ the temperature and $n_i$ the intrinsic carrier concentration [16,18]. The n-type substrate behaves the opposite way.
Chapter 3. Fabrication Process

This chapter describes the fabrication of the MOS structures step by step. In particular, the different techniques and equipment used for dielectric deposition, or growth, are explained. The chapter also includes a table of the sample names and their preparation schemes.

3.1 Pre-deposition Surface Cleaning process

The wafer that has been used is n-type epitaxial 4H-SiC grown on 4° off-axis purchased from SiC Crystal AG with $3 \times 10^{15} \text{cm}^{-3}$ nitrogen doping. The wafer has been diced into square pieces with area of 1 cm$^2$. The first step of the fabrication is the surface cleaning, which has been done in two stages, in order to remove the impurities like organic and metal particles [19]. The first stage of the cleaning is a standard 7up/IMEC process:

- 5 minutes in 3 l HSO$_4$: 1 l H$_2$O$_2$ solution
- 5 minutes in de-ionised water (DI)
- 100 seconds IMEC clean in 6 l DI H$_2$O: 60 ml isopropanol : 60 ml HF (50%) solution
- rinse again in DI water

Afterwards 150 nm of Nickel (Ni) has been deposited at the wafer back side using metal evaporation followed by rapid thermal annealing (RTA) at 950 °C (for the samples where either the oxide has been thermally grown, or they have been annealed in the furnace, the nickel deposition has been done after the oxidation/annealing). Then a weak RCA1 cleaning process consisting of:

- 100 ml NH$_4$: 2 l DI H$_2$O: 400 ml H$_2$O$_2$ solution at 60 °C for 10 minutes was used
- rinse in DI water for 5 minutes
- kept 30 seconds in HF (1:50)
- rinse in DI water for 60 seconds

3.2 Oxide Deposition

The cleaning procedure has been followed by the formation of the dielectric. The samples have been divided in three batches of 10, 13 and 3 samples. In the first two batches the oxide has been deposited by two versions of the plasma enhanced chemical vapour deposition (PeCVD) method, the first by using the Applied Materials P5000 processing tool (10 samples) and the second batch by using Plasmalab 80Plus (Pekka) processing tool (13 samples). The oxide of the third batch has been thermally grown (3 samples).

3.2.1 PeCVD

As mentioned before, one of the oxide formation method is plasma enhanced chemical vapour deposition (PeCVD). Plasma is the fourth state of matter and it can be described as a gas containing positive ions and negative electrons. The main advantage of this method is that the energy required for initiating the oxide formation, is provided by an RF source, which accelerates the positive ions towards the surface where they deposit their kinetic energy and facilitate the chemical processes leading to oxidation [19,20,21]. Thus the deposition can take place at lower temperatures than plain chemical vapour deposition (CVD). Silane
(SiH₄) and nitrous oxide (N₂O) are the precursors that have been used for the formation of the oxide and the reaction is the following [21].

\[ \text{SiH}_4 \text{ (gas)} + 4 \text{N}_2\text{O (gas)} \rightarrow \text{SiO}_2 \text{ (solid)} + 2 \text{H}_2\text{O (gas)} + 4 \text{N}_2 \text{ (gas)} \]

The configuration of PeCVD process is illustrated in Figure 3.1.

![Figure 3.1. PeCVD process for the formation of SiO₂ [21]](image)

As it can be seen from Figure 3.1, the wafer is positioned at the bottom electrode, where heat can be provided. SiH₄ and N₂O are inserted into the chamber through the inlets at the top. Between the two electrodes a high voltage is applied, typically a few hundred volts, thus plasma is created. The plasma particles collide with the reactant gases and produce ions and radical reactive species. These products are adsorbed and they react with the surface of the wafer, building up a SiO₂ layer. The byproducts are desorbed from the surface and driven away through the outlets [19,20,21]. The typical parameters that one can use to control the process are the RF power applied to maintain the plasma, wafer heating, gas ratios, and gas inlet pressure. In this experiment the wafer temperature is kept constant at 400 and 300 °C for P5000 and Pekka, respectively.

### 3.2.1.1 P5000

Precision 5000 Mark II (P5000) is a dry etching and PeCVD system with four process chambers. It is manufactured by Applied Materials Inc. [22,23]. Chamber A is used for SiO₂ and SiN etching, chamber B is for Al, TiW, TiN and Al (500nm)/TiW (100nm) etching, chamber C is for poly-Si and c-Si etching and chamber D is for SiO₂ and SiN deposition. For this experiment the deposition was done in chamber D at 400 °C while the pressure and the RF power varied from 1.5 Torr to 6 Torr and from 50 W to 300 W, respectively. Lastly, the gas ratios of N₂O/SiH₄ that were used are 600/30 sccm, 800/60 sccm, 600/60 sccm and 1200/60 sccm. The unit “sccm” means standard cubic centimeters per minute.
3.2.1.2 Pekka

The 80Plus is PeCVD system, used for deposition of dielectric thin films, is manufactured by Plasmalab [24]. The deposition temperature was 300 °C, the pressure ranged from 0.2 Torr to 0.8 Torr, the power from 10 W to 20 W and the different gas ratios of N₂O/SiH₄ were 425/710 sccm, 500/53 sccm, 700/75 sccm and 650/142 sccm.

3.2.2 Thermal Growth

Thermal growth is used for the third batch and it was done in N₂O ambient. The process proceeds in several steps. First the N₂O dissociates according to the following two reactions [25].

\[
2N₂O \rightarrow 2NO + N₂
\]
\[
2N₂O \rightarrow 2N₂ + O₂
\]

The main contribution to the oxidation is from O₂, which follows the Deal-Grove model [26].

\[
SiC + O \rightarrow CO + Si
\]
\[
CO + O \rightarrow CO₂
\]
\[
Si + 2O \rightarrow SiO₂
\]

On the other hand, NO is either removing excess carbons [13], or form SiOₓNᵧ (x<2, 0<y<2) as it can be seen from the reaction below:

\[
Si + xNO \rightarrow SiOₓNᵧ + \frac{x - y}{2} N₂
\]

N₂ is inert and it diffuses out of the dielectric [25].

The oxide of two of the three samples in batch 3 has been grown at 1250 °C for 15 hours and, as for the third sample, it has been grown at 1150 °C for 12 hours. The oxidation of the samples took place in the furnace which is shown in Figure 3.2.
3.3 Post oxidation/deposition annealing

After the oxide fabrication, several samples have been annealed, either with rapid thermal annealing by using Mattson 100 RTP System for 300 sec at temperatures of 850, 1000 and 1150 °C, or in the furnace for 3 hours at 1150 °C.

3.4 Gate metallization

3.4.1 Lithography

For the formation of the gate contact, a layer of 150 nm thick Aluminium is deposited on the dielectric by metal evaporation. Then the samples are coated with positive photoresist spun at 4000 rpm for 60 sec to form a 1.4 μm thick resist (see Fig. 3.4). They are soft baked at 90 °C for 90 sec. to harden the resist and then aligned with a mask, defining the areas of the top circular gate contacts with different diameters of 50-500 μm.
and then expose to UV-light for 7 seconds. In order to remove the exposed photoresist, the samples are developed in CD26 solvent for 40 seconds. Finally, the samples are hard baked at 110 °C for 20 min in an oven to harden the photoresist that is still on the samples, covering the areas where the Al should be preserved.

3.4.2 Aluminium etching

The top aluminium contact is dry etched in Applied Material P500 processing tool. It is done by using the gases BCl₃ and Cl₂ with ratio 40/30 sccm for 40 sec. Finally, the remaining photoresist is stripped by dipping the samples in acetone. The gate formation process is schematically illustrated in Figure 3.3.

Figure 3. 4. Schematic diagram of the gate formation

3.5 Fabrication Parameters of the samples

In Tables 3.1-3 all the parameters, including the thickness of the oxides for the different fabrication processes, are tabulated.
### Table 3.1 P5000 samples

<table>
<thead>
<tr>
<th>Sample number</th>
<th>Deposition Temperature (°C)</th>
<th>Pressure (Torr)</th>
<th>Power (W)</th>
<th>Spacing (mils)</th>
<th>SiH₄ (sccm)</th>
<th>N₂O (sccm)</th>
<th>PDA (C)</th>
<th>Annealing Time (sec)</th>
<th>Thickness (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
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<td>100</td>
<td>450</td>
<td>60</td>
<td>1200</td>
<td>1150</td>
<td>300</td>
<td>47</td>
</tr>
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### Table 3.2 Pekka samples

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### Table 3.3 Thermally Grown samples

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</table>
Chapter 4. Characterization

In this chapter the experimental setup and the different types of measurements for the characterization and analysis of the samples will be discussed.

4.1 Electrical Measurements

4.1.1 Probestation 3 semi-automatic

The electrical measurements are accomplished by using Probe Station 3 semi-automatic in KTH electrum manufactured by Cascade Microtech. The tool is shown in Figure 4.1.

Figure 4. 1. Probestation Semi-automatic for CV and IV measurements.

The samples are placed on the chuck and are fixed by turning on the vacuum pump. The microscope is connected to the computer on the left and, by rotating the handles of one of the four probes, which are used for the electrical contact, the probe is placed onto the gate of the MOS structure. During the measurements, the light is turned off. From the control unit to the right we choose either the CV or the IV configuration for our measurements.

4.1.2 CV

The configuration for the CV measurements is the following. Two different voltage sources were superimposed on the device terminals, one AC voltage measurement signal, whose magnitude (50 mV) and frequency (200 kHz) are kept constant, and one DC bias voltage whose magnitude is changed in steps with time. By integrating the current from the AC signal over time, the gate charge \( Q_g \) is derived. Then the
capacitance is calculated from $Q_g$ and the DC voltage [27]. The voltage is applied at the bottom of the MOS structure (Nickel side), so the whole back side will be at the same potential. With a probe tip on the upper side individual MOS structures can be measured. The voltage interval is mostly from -5 V to 5 V, although for several samples who’s $V_{fb}$ are close to ± 5 V, other start and stop voltages is used. The full interval is still 10 V each time. The voltage is swept from low to high bias in steps of 0.1 V/s. In this experiment, a high frequency (200 kHz) is used for measuring the CV curves. In this case, the minority carries and the interface traps do not have time to response to the AC signal [28]. A typical CV curve, where the three different states of the MOS structure are shown, is illustrated in Figure 4.2.

![Figure 4.2](image)

*Figure 4.2. High frequency capacitance vs voltage curve, where the inversion, depletion and accumulation region are shown for Sample 3.*

A MOS structure with an n-type substrate under voltage bias can be seen as a system of two capacitors in series connection - the oxide capacitor and the depleted semiconductor capacitor. With a positive bias the majority carriers, electrons, are accumulated in the channel at the semiconductor-dielectric interface, and the total capacitance is equal to the oxide capacitance. When the gate voltage is smaller than the flatband voltage, a depletion region is formed, which acts like a capacitor connected in series with the oxide capacitor, thus the total capacitance is decreased. Depending on the frequency there are two different responses from the MOS structure on negative bias. At low frequency (typically less 100 Hz) the minority carriers have time to respond to the AC signal and they form a capacitor in parallel with the depletion region capacitor, which results in increasing the total capacitance until the total capacitance again reaches the oxide capacitance value. At high frequency, the minority carriers are not generated and transported fast enough to give a response to the AC signal and the total capacitance reaches its minimum value when the inversion is achieved and the depletion region has its maximum width [28,29].

In this experiment two parameters will be extracted from the measurements. Firstly, the flatband voltage $V_{fb}$, which can be found from the horizontal shift of the CV curve in respect to the theoretical one, as illustrated in Figure 4.3. Secondly, the density of interface traps, $D_{it}$, which will be extracted with the Terman method from the measured CV curves. The Terman method will be discussed in Section 4.1.2.2.
Figure 4.3. The shift of the CV curve for sample 21 according to the theoretical curve shows the \( V_{fb} \). The theoretical curve has no extra charges at the interface or in the oxide, in addition to equal work functions for the semiconductor and contact metal, resulting in \( V_{fb}=0 \) V.

4.1.2.1 Defects in the oxide

In reality there are always charges in the oxide and at the interface. These charges are often classified in four different types and this makes the MOS structure deviate from the ideal behaviour, as described in Section 2.2. A committee, which was set up by the *Electronics Division of the Electrochemical Society* and the IEEE in January 1978, decided on a terminology for the different oxide charges [30], which are displayed in Figure 4.4.

Figure 4.4. A cross section of a MOS structure, which shows the different types and location of the charges inside the dielectric.

1) Mobile ionic charges \( (Q_m) \) are the result of ionic impurities, such as \( \text{Na}^+ \), \( \text{Li}^+ \) and \( \text{K}^+ \). Negative ions and heavy metals are also added to this type of charge for oxidation at temperature over 500 \(^\circ\text{C}\).
2) Oxide trapped charge ($Q_{ot}$): Holes or electrons can be trapped due to ionizing radiation, avalanche injection in the bulk of the oxide, or similar processes. Depending on the sign of these charges there is the analogous shift in the positive or negative direction of the CV curve with respect to the ideal curve.

3) Fixed oxide charge ($Q_{f}$): These charges are structural defects created during the oxidation process. The presence of these defects can be observed in the CV curves as a hysteresis loop when the CV measurement is swept from accumulation to inversion and vice versa.

4) Interface trapped charge ($Q_{it}$): These can be positive, or negative charges and they are caused by broken bonds, structural or oxidation-induced defects and metal impurities at the interface, or near interface. They can be identified by evaluating the slope of the CV curve in the depletion region. [28,30,31]

4.1.2.2 Terman Method

One of the methods to determine the $D_{it}$ is the Terman method using high frequency CV measurements. Even though the interface traps do not respond to a higher frequency AC signal, they respond to slow change of the DC voltage by filling, or emptying the traps that are below the conduction band, according to the relative bending of the Fermi level. This results in stretching of the CV curve with respect to the ideal, theoretical curve at the depletion, as can be seen in Figure 4.5a [28]. From the comparison of the two curves, the surface potential, $\Psi_s$, versus the gate voltage is extracted and plotted, as in Figure 4.5b. From the slope of this curve, the $D_{it}$ can be calculated according to Equation 4.1 [28].

\[
D_{it} = \left( \frac{C_{ox}}{q^2} \right) \left( \frac{dV_g}{d\Psi_s} - 1 \right) - \left( \frac{C_{dep}}{q^2} \right)
\]  

(4.1)

![Image](https://example.com/image.png)

*Figure 4.5. a) Experimental and theoretical (ideal) high frequency capacitance-voltage curve, showing the non-parallel shift of the experimental curve. b) Surface potential versus experimental voltage for the extraction of $D_{it}$ for Sample 6*
4.1.3 IV

The configuration for current-voltage measurements is almost the same as the capacitance-voltage, but now only a DC bias is applied, which is increased in steps of 0.2 V/sec. The maximum voltage is estimated for each sample as the voltage where the electric field of 10 MV/cm is reached, which depends also on the oxide thickness. A typical IV curve is shown in Figure 4.6. While the voltage increases, so called Fowler-Nordheim tunnelling current may appear. Then electrons trapped at the defects in the oxide gain enough energy to jump into the conduction band which results in the Frenkel-Poole emission of electrons and, finally, when the critical field is reached, a chain of defects creates a conduction path and the breakdown of the oxide occurs [32].

![IV curve](image)

*Figure 4.6. Current-Voltage curve, in which the different types of currents and the breakdown is indicated for Sample 14*

4.2 AFM

4.2.1 AFM system

The surface roughness of the samples is measured using a commercial setup *Dimension 3000*, which was manufactured by Veeco/Digital Instruments. The principle of the Atomic Force Microscopy (AFM) is to drag/push a small needle across a surface and monitor the vertical motion of this needle. To do this, a sharp tip, which is connected to a cantilever placed in a holder, scans the surface of the sample. A laser beam is aligned with the backside of the tip and is reflected to a segmented photodiode. The photodiode can then detect any kind of deformation of the cantilever. Another piezoelectric element is located at the base of the cantilever, which can translate any deformation into an electrical signal. The atoms of the tip interact with the atoms of the surface via Van der Waals forces [33]. A schematic view of the AFM is shown in Figure 4.7.
4.2.2 Tapping Mode

There are three different operation modes for AFM, contact, non-contact and tapping mode. For this experiment the latter is used. The principle of tapping mode is that the piezoelectric element makes the cantilever oscillate close to its resonant frequency and keeps the oscillating amplitude constant. When the tip reaches a step on the investigated surface the amplitude decreases, but when it reaches a void the amplitude increases. In the detector a sinusoidal signal arrives, which tracks the changes in the amplitude and translates them to an image [33].

The purpose of the AFM measurements for this thesis is to measure the surface roughness from the images that have been recorded by Nanoscope IIIa software and to check if there is any correlation between the $V_{fb}$s or $D_{it}$s with the roughness root mean square (rms).

The configuration set-up for the measurement is the following: first the laser is aligned from the knobs at the top of the SPM (scanning probe microscopy) head until the spot is visible in the Dimension Head Filter Screen and the detected signal is between 4-6 V. Then the photodetector is adjusted from the knobs at the left side of the SPM head, until the spot goes to the center of the screen. In Figure 4.8 a picture of the tool and of the SPM head is shown.

Figure 4. 7 A schematic illustration of the AFM system and the image of Sample 20 [34].
Figure 4.8. Commercial AFM system tool a) Computer b) SPM Head.
Chapter 5. Results

In the following sections, the influence of the different oxide fabrication parameters, such as pressure of the gases, power, gas ratio and post deposition annealing (PDA) for the PECVD method and growth temperature and post oxidation annealing (POA) for the thermally grown oxides, on the electrical characteristics will be investigated. The error bars presented in this report is a standard deviation taken on 8-12 different MOS devices on each sample. A summary of all the electrical characteristics for various samples can be found in Appendix 1.

5.1 P5000

This section elucidates the electrical measurement and surface analysis results obtained for the metal oxide semiconductor (MOS) structures with oxide deposited using plasma enhanced chemical vapour deposition (PECVD) in an Applied Mechanic P5000 processing tool. Figure 5.1 a and b shows the capacitance voltage (CV) and current voltage (IV) curves of three samples (P1, P2 and P9 for the CV and P6, P7 and P10 for the IV) with different deposition parameters, respectively. From now on the samples grown by P5000 tool will be named as Px, where x is the sample number. The CV plots are chosen in order to show the spread of the results, while the IVs show samples that break at low, medium and high electrical field. As it can be seen from the Figure 5.1, this method is quite unstable since the values of the CV curves spread. In general, the flatband voltage (Vfb) varies from -10 V to 3.5 V and the density of interface traps (Dit) from $2 \times 10^{11}$ eV$^{-1}$cm$^{-2}$ to $1 \times 10^{12}$ eV$^{-1}$cm$^{-2}$. A similar trend is observed for IV curves and an average critical field is found to be 3.5 MV/cm.

![Figure 5.1](image)

**Figure 5.1.** a) An example of high frequency capacitance-voltage curves for samples whose oxide has been deposited with P5000 b) a sample of current density versus electric field curves.

5.1.1 Influence of Pressure

For these investigation two samples P1 and P6 have been utilized. Sample P1 and P6 are deposited at a pressure of 2 and 6 Torr respectively while the other oxide parameters power and gas ratio (N$_2$O/SiH$_4$) have been fixed at 100 W and 1200/60 respectively. After oxide depositions both the samples have been annealed at 1150 °C for 300 seconds. Figure 5.2 a and b show the flatband voltage and density of interface traps results for fabricated samples, respectively.
Increasing the deposition pressure results in a reduction of the concentration of negative oxide charges indicated by shift of $V_{fb}$ from 3.55 V for sample $P_1$ towards to zero (0.8 V) for sample $P_6$ as shown in Figure 5.2.a. Also, the standard deviation of different devices for a process varies from 1.4 V for 2.8 Torr to 0.4 V for 6 Torr, showing that deposition at higher pressure i.e. 6 Torr is more stable. On the other hand, change in $D_{it}$ is meagre as a function of deposition pressure as can be seen in Figure 5.2.b. Thus the deposition pressure does not seem to affect the $D_{it}$, which is around $2.7 \times 10^{11}$ eV$^{-1}$ cm$^2$; although in this case the stability decreases significantly at higher pressure ($2 \times 10^{11}$ eV$^{-1}$ cm$^2$) compared to the lower pressure ($0.4 \times 10^{11}$ eV$^{-1}$ cm$^2$). Finally, by increasing the pressure, the critical electric field of oxide was found to increase from 3 MV/cm to 5.5 MV/cm.

While the pressure is increased, the surface roughness increases dramatically and the rms values are 0.7 nm and 6.7 nm for $P_1$ and $P_6$, respectively.

5.1.2 Influence of Power

In this section the influence of deposition power is discussed. The deposition power is varied from 50 W for sample $P_7$ and 300 W for sample $P_8$ while the other oxide deposition parameters have been fixed as following: Pressure of 1.5 Torr, the gas ratio of (N$_2$O/SiH$_4$) was 1200/60 and the PDA temperature was 1150 °C for 300 seconds. Figure 5.3 a and b shows the $V_{fb}$ and $D_{it}$ results obtained for CV curves for the samples in this study.
It can be observed from Figure 5.3.a that the sample with the lowest deposition power has a $V_{fb}$ of 0.1±0.4 V and $D_{it}$ of $4\times10^{11}$ eV$^{-1}$ cm$^{-2}$. While, higher power has a $V_{fb}$ of -4±0.8 V, indicating an increase in positive charges. Also, $D_{it}$s increase by 4 times to $1.5\times10^{12}$ eV$^{-1}$ cm$^{-2}$ and they have larger spread in comparison to the sample with low deposition power. The critical electric field is found to be 3.5 MV/cm and 4 MV/cm for low and high deposition power, respectively. Thus it can inferred that change in power have a minimal effect on the dielectric breakdown field.

As a result of increased power, surface roughness varies from 0.9 nm for sample P7 to 1.2 nm for sample P8.

5.1.3 Influence of Gas ratio

For this investigations gas ratio of N$_2$O/SiH$_4$ have been varied from 20 to 10 while other parameters have been fixed as follows: pressure of 2.8 Torr, power of 100 W and a PDA at 1150 °C for 300 seconds. Figure 5.4 a and b show influence of gas ratios on the flatband voltage and density interface states, respectively. It can be observed that the gas ratio of 20, sample P1, have a $V_{fb}$ of 3.5 V and $D_{it}$s of $2.7\times10^{11}$ eV$^{-1}$ cm$^{-2}$. While, in case of 13.33 (sample P9) and 10 (sample P10) the $V_{fb}$s are -10.6 V and -0.2 V and the density of traps $2\times10^{12}$ eV$^{-1}$cm$^{-2}$ and $5.5\times10^{11}$ eV$^{-1}$cm$^{-2}$ respectively. Also, it can be seen that higher the gas ratio, less stable is the $V_{fb}$, but the stability dramatically increases for the $D_{it}$s.

As for the maximum electric field that the oxide is able to withstand, the general trend shows that the critical electric field decreases as the gas ratio increases. For gas ratios of 20, 13.33 and 10 the measured fields are 3 MV/cm, 2 MV/cm and 1.5 MV/cm, respectively.
Gas ratio does not seem to affect the surface roughness as the rms values are very low, 0.7, 0.6 and 0.8 nm for sample P1, P9 and P10, respectively.

5.1.4 Influence of Annealing Temperature

Two different groups of samples were used to investigate the effects of annealing temperature on $V_{fb}$ and $D_{it}$. The first group consists of two samples P4 and P5 deposited under the following conditions: 4.5 Torr pressure, 300 W power and (N$_2$O/SiH$_4$) 20 gas ratio. P4 is not annealed whereas P5 is annealed at 1150 °C for 300 s. The second group consists of three samples P1, P2 and P3. P3 and P1 are annealed at 1000 °C and 1150 °C, respectively and P2 is unannealed reference sample. These samples are deposited with a pressure of 2.8 Torr, power of 100 W and gas ratio (N$_2$O/SiH$_4$) 20.

Figure 5.5.a shows the effect of annealing temperature on $V_{fb}$. It can be seen that in the first group annealing causes reduction in the concentration of the negative oxide charges but it leads to slightly lower stability. On the contrary, in the second group, unannealed reference have a negative $V_{fb}$ of -3.97 V and annealing at temperature of 1000 °C shifts $V_{fb}$ closer to zero. Further increasing the PDA temperature to 1150 °C shifts $V_{fb}$ to a positive voltage of 3.55 V.
Table 5.1. $V_{fb}$s and the standard deviation for group of samples $P_4$ and $P_5$ (4.5 Torr, 300 W, 20 N2O/SiH4) and group of samples $P_1$, $P_2$ and $P_3$ (2.8 Torr, 100 W, 20 N2O/SiH4)

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<td>3.55</td>
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<td>1000</td>
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Figure 5.5.b shows the effect of PDA temperatures on $D_i$s extracted from the CV curves. For samples $P_4$ and $P_5$, annealed at 1150 °C, the annealing process caused $D_i$s to slightly decrease, but made them more unstable. In the second set of samples, $D_i$s dropped more than one third of the value of the not annealed sample and made it 4 times more reliable, but between $P_3$, annealed at 1000 °C and $P_1$, annealed at 1150 °C there is no significant difference.

Table 5.2. $D_i$s and the standard deviation for group of samples $P_4$ and $P_5$ (4.5 Torr, 300 W, 20 N2O/SiH4) and group of samples $P_1$, $P_2$ and $P_3$ (2.8 Torr, 100 W, 20 N2O/SiH4)

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<td>$D_i$ ($10^{11}$ eV$^{-1}$cm$^{-2}$)</td>
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<td>4.37</td>
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For both of the groups annealing leads to an increase of the critical field. Especially for the $1^{st}$ group ($P_4$ and $P_5$) there is a considerable change from 1.5 MV/cm for the unannealed sample to 6 MV/cm for the sample annealed at 1150 °C. For $2^{nd}$ group ($P_1$, $P_2$ and $P_3$) the effect is less pertinent and varies from 3 MV/cm, 3.5 MV/cm and 4 MV/cm for the unannealed, 1000 °C and 1150 °C PDA temperatures, respectively.

The next table shows the rms values of roughness of the above groups. Except sample $P_4$, which is not annealed and the roughness is 5.7 nm, all the others are around 0.7 nm.

Table 5.3. Roughness rms for group of samples $P_4$ and $P_5$ (4.5 Torr, 300 W, 20 N2O/SiH4) and group of samples $P_1$, $P_2$ and $P_3$ (2.8 Torr, 100 W, 20 N2O/SiH4)

<table>
<thead>
<tr>
<th></th>
<th>$P_4$</th>
<th>$P_5$</th>
<th>$P_2$</th>
<th>$P_3$</th>
<th>$P_1$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Roughness (nm)</td>
<td>5.7</td>
<td>0.7</td>
<td>0.6</td>
<td>0.8</td>
<td>0.7</td>
</tr>
</tbody>
</table>

5.2 Pekka

In this section, electrical characterization and surface analysis results of samples with the gate oxides deposited using Plasmalab 80Plus (Pekka) plasma enhanced chemical vapour deposition (PECVD) system are presented. Different set of samples are fabricated by varying chamber conditions, pressure, gas ratio and annealing temperature in order to study the effect on device performance. A summary of all the samples is tabulated in Appendix 1. From now on the samples fabricated by Pekka tool will be named as $P_{ex}$, where $x$ is the number of the sample.
Figure 5.6.a shows the spreading of the CV curves of three different samples Pe14, Pe16 and Pe22, deposited using this tool. The Vfb varies from 3 V to 0.5 V and the Dit from $10^{11}$ eV$^{-1}$ cm$^{-2}$ to $5 \times 10^{11}$ eV$^{-1}$ cm$^{-2}$. Despite the positive results in CV measurements, IV curves, from samples Pe13, Pe15 and Pe20, show unstable behaviour. Figure 5.6.b show a wide distribution of IV curves with an average critical field around 5 MV/cm.

5.2.1 Influence of Pressure

In order to study the influence of pressure, three groups of samples are organized. In each group, there are two samples. For the first group the pressure vary from 0.2 Torr (Pe12) to 0.4 Torr (Pe13). For the other two groups it is varied from 0.5 Torr (Pe17, Pe23) to 0.8 Torr (Pe11, Pe19). The samples in the first group are deposited under the condition of 10 W power and gas ratio of (N2O/SiH4) of 10. They are annealed at 1150 °C for 300 sec. The samples in the other two groups are fabricated under the condition of 20 W power and (N2O/SiH4) 425/710 gas ratio. Samples Pe17 and Pe11 are annealed at 1150 °C for 3 hours, whereas samples Pe23 and Pe19 are unannealed.

Figure 5.7.a shows, as the pressure is increased, the VfbS of all samples approach zero, meaning that defects inside the oxide decrease as well as the stability of the samples. However, the trend shows an
alteration depending on the set of samples. The first two groups, which are annealed, start from a $V_{fb}$ of 1.34 V for $P_{e12}$ and drops to 0.5 V for the rest of the samples. For the last set of samples, which are not annealed, as pressure increases the $V_{fb}$ decreases 4 times.

Table 5.4. $V_{fb}$s and the standard deviation for group of samples $P_{e13}$ and $P_{e12}$ (10W, 10 $N_2O$/$SiH_4$ annealed at 1150 °C for 300 seconds), $P_{e17}$ and $P_{e11}$ (20W, 425/710 $N_2O$/$SiH_4$ annealed at 1150 °C for 3 hours) and $P_{e23}$ and $P_{e19}$ (20W, 425/710 $N_2O$/$SiH_4$ and not annealed)

<table>
<thead>
<tr>
<th></th>
<th>$P_{e12}$</th>
<th>$P_{e13}$</th>
<th>$P_{e17}$</th>
<th>$P_{e11}$</th>
<th>$P_{e23}$</th>
<th>$P_{e19}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{fb}$ (V)</td>
<td>1.34</td>
<td>0.55</td>
<td>0.61</td>
<td>0.45</td>
<td>4.78</td>
<td>1.46</td>
</tr>
<tr>
<td>Standard Deviation (V)</td>
<td>0.68</td>
<td>0.39</td>
<td>0.96</td>
<td>0.36</td>
<td>1.36</td>
<td>0.88</td>
</tr>
<tr>
<td>Pressure (Torr)</td>
<td>0.20</td>
<td>0.40</td>
<td>0.50</td>
<td>0.80</td>
<td>0.50</td>
<td>0.80</td>
</tr>
</tbody>
</table>

Figure 5.7.b illustrates change in $D_{it}$s for the same set of samples. As it can be seen, for the first group of samples, $P_{e12}$ and $P_{e113}$, changing the pressure does not have any effect on value of $D_{it}$s, but only on the stability, which increase. For the rest of two groups, increasing the pressure results in decreasing $D_{it}$ values as can be seen in the second group, where there is an 80% reduction for 0.5 to 0.8 Torr.

Table 5.5. $D_{it}$s and the standard deviation for group of samples $P_{e13}$ and $P_{e12}$ (10W, 10 $N_2O$/$SiH_4$ annealed at 1150 °C for 300 seconds), $P_{e17}$ and $P_{e11}$ (20W, 425/710 $N_2O$/$SiH_4$ annealed at 1150 °C for 3 hours) and $P_{e23}$ and $P_{e19}$ (20W, 425/710 $N_2O$/$SiH_4$ and not annealed)

<table>
<thead>
<tr>
<th></th>
<th>$P_{e12}$</th>
<th>$P_{e13}$</th>
<th>$P_{e17}$</th>
<th>$P_{e11}$</th>
<th>$P_{e23}$</th>
<th>$P_{e19}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$D_{it}(10^{11} \text{ eV}^{-1} \text{ cm}^{-2})$</td>
<td>2.99</td>
<td>3.40</td>
<td>7.54</td>
<td>1.61</td>
<td>6.37</td>
<td>5.25</td>
</tr>
<tr>
<td>Standard Deviation ($10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$)</td>
<td>2.17</td>
<td>0.86</td>
<td>4.63</td>
<td>0.89</td>
<td>4.29</td>
<td>4.52</td>
</tr>
<tr>
<td>Pressure (Torr)</td>
<td>0.20</td>
<td>0.40</td>
<td>0.50</td>
<td>0.80</td>
<td>0.50</td>
<td>0.80</td>
</tr>
</tbody>
</table>

The critical field decreases from 5 MV/cm for sample $P_{e12}$ to 2 MV/cm for sample $P_{e13}$, while for sample $P_{e11}$ is 7 MV/cm and it slightly decreases to 6 MV/cm for sample $P_{e17}$.

In the next table (Table 5.6) the roughness of the previous sample groups are shown.

Table 5.6. Roughness rms for group of samples $P_{e13}$ and $P_{e12}$ (10W, 10 $N_2O$/$SiH_4$ annealed at 1150 °C for 300 seconds), $P_{e17}$ and $P_{e11}$ (20W, 425/710 $N_2O$/$SiH_4$ annealed at 1150 °C for 3 hours) and $P_{e23}$ and $P_{e19}$ (20W, 425/710 $N_2O$/$SiH_4$ and not annealed)

<table>
<thead>
<tr>
<th></th>
<th>$P_{e12}$</th>
<th>$P_{e13}$</th>
<th>$P_{e17}$</th>
<th>$P_{e11}$</th>
<th>$P_{e23}$</th>
<th>$P_{e19}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Roughness (nm)</td>
<td>2.9</td>
<td>1.2</td>
<td>0.9</td>
<td>0.8</td>
<td>1.1</td>
<td>2.7</td>
</tr>
</tbody>
</table>

5.2.2 Influence of Gas ratio

In order to study the influence of gas ratio, two samples are deposited, $P_{e12}$ and $P_{e15}$. The samples are deposited under the condition of 10 W of power, pressure of 0.2 Torr and a PDA of 1150 °C for 300 s. The gas ratios of $N_2O$/$SiH_4$ are varied from 500/53 to 650/142 for this study.
Figure 5.8 a) Effect of gas ratio on $V_{fb}$; b) effect of pressure of $D_{it}$. Samples fabricated at 20W deposition power, 0.2 Torr pressure and annealed at 1150 °C for 300 seconds.

Figure 5.8 a shows the change in $V_{fb}$ for two different gas ratios. The $V_{fb}$ and their standard deviation are basically unchanged while the gas ratio decreases (500/53 to 650/142) as the values are 1.40 V and 1.34 V for $V_{fb}$ and 0.65 V to 0.68 V for the standard deviation. Also the $D_{it}$ (Figure 5.8.b) do not change, since for the gas ratio of 500/53 is $2.99 \times 10^{11}$ eV$^{-1}$cm$^{-2}$ and $2.26 \times 10^{11}$ eV$^{-1}$cm$^{-2}$ for gas ratio of 650/142. But the standard deviation decreases from $2.17 \times 10^{11}$ eV$^{-1}$cm$^{-2}$ to $6.68 \times 10^{10}$ eV$^{-1}$cm$^{-2}$, respectively.

The maximum electric field the oxide can tolerate increases for lower gas ratio from 5 to 7.5 MV/cm.

As in P5000, the gas ratio does not change the roughness of the surface. The rms values are 2.9 for sample P$e_{12}$ and 2.4 for sample P$e_{15}$.

5.2.3 Influence of Annealing Temperature

In order to study influence of annealing temperature, two groups of samples, are selected. In the first group there are four samples, P$e_{22}$, P$e_{21}$, P$e_{20}$ and P$e_{18}$. The oxide is deposited under the condition of 20 W power, 0.8 Torr pressure and (N$_2$O/SiH$_4$) 425/710 gas ratio and the annealing temperatures are 850 °C, 1000 °C and 1150 °C, for sample P$e_{22}$, P$e_{21}$ and P$e_{20}$, respectively. The same parameters of power, pressure and gas ratio are used for sample P$e_{18}$, but the PDA is performed in two steps. First, one third of the required oxide is deposited, in this case 15 nm and PDA at 1150 °C for 300 s. Second, the remaining oxide is deposited, in this case 35 nm followed by PDA at 1150 °C for 60 s. The second group of samples, P$e_{14}$ and P$e_{15}$, are fabricated under the condition of 10 W power, (N$_2$O/SiH$_4$) 650/142 gas ratio and 0.2 Torr. Sample P$e_{14}$ is un-annealed, whereas P$e_{15}$ is annealed at 1150 °C.
Figure 5.9.a shows the change in $V_{fb}$ versus PDA temperature. Sample $P_{e22}$ (annealed at 850 °C) and sample $P_{e21}$ (annealed at 1000 °C) exhibit similar behaviour in terms of $V_{fb}$, which is around 0.5 V and also standard deviation which is 0.4 V. As the annealing temperature goes to 1150 °C, as in the case of sample $P_{e20}$, there is an increase in the amount of the positive oxide charges which leads $V_{fb}$ to drop to -4.53 V and a decreased stability by 2 times. On the other hand, in sample $P_{e18}$, it has been observed that the positive oxide charges are reduced. Flatband voltage for this sample is -1.15 V and the standard deviation is reduced by half and reach the value of 0.5 V. Flatband voltage shows a slight decrease as the sample is annealed from $P_{e14}$, which is not annealed and having a $V_{fb}$ of 1.48 V, to $P_{e15}$ which is annealed at 1150 °C and having the $V_{fb}$ of 1.40 V. In terms of stability, the standard deviation change is also very small, 0.62 V for $P_{e14}$ and 0.65 V for $P_{e15}$.

Figure 5.9.b shows the change in $D_{it}$ versus annealing temperature. The measured $D_{it}$ for sample $P_{e22}$ is $7.94 \times 10^{10}$ eV$^{-1}$cm$^{-2}$ and its standard deviation is $6.71 \times 10^{10}$ eV$^{-1}$cm$^{-2}$, while for sample $P_{e21}$, the $D_{it}$ is $2.04 \times 10^{11}$ eV$^{-1}$cm$^{-2}$ and the standard deviation is $1.53 \times 10^{11}$ eV$^{-1}$cm$^{-2}$. Sample $P_{e20}$ has $D_{it}$ of $1.16 \times 10^{12}$ eV$^{-1}$cm$^{-2}$ with standard deviation of $5.32 \times 10^{11}$ eV$^{-1}$cm$^{-2}$ and $D_{it}$ of sample $P_{e18}$ is $3.87 \times 10^{11}$ eV$^{-1}$cm$^{-2}$ with the standard deviation of $1.66 \times 10^{11}$ eV$^{-1}$cm$^{-2}$. Therefore, as seen by these results, $D_{it}$ is directly proportional to the PDA temperature, but for the last sample, $P_{e18}$, which was exposed to a different annealing procedure, the value is decreased. The same trend also applies to the standard deviation, which means that the stability of the samples decreases for an increase in the annealing temperature while for sample $P_{e18}$, it becomes more stable than sample $P_{e20}$. Sample $P_{e14}$ and $P_{e15}$ have $D_{it}$ of $4.20 \pm 1.50 \times 10^{11}$ eV$^{-1}$cm$^{-2}$ and $2.26 \pm 0.67 \times 10^{11}$ eV$^{-1}$cm$^{-2}$, respectively. The results show that annealing the sample causes a decrease in $D_{it}$, but the stability increases.

For the first set of samples, increase in PDA temperature leads to a drop in the critical electric fields, since the values are 7 MV/cm for $P_{e20}$ and $P_{e18}$, 2.5 MV/cm for $P_{e21}$ and 1.5 MV/cm for $P_{e22}$. For the second set of samples, annealing the sample decreases dramatically the critical electric field from 7.5 MV/cm to 2 MV/cm for $P_{e15}$ and $P_{e14}$, respectively.

Annealing appears to increase the roughness of the samples. For the first group the rms value goes from 0.5 nm for the unannealed sample, $P_{e14}$, to 2.5 nm for sample $P_{e15}$, which was annealed at 1150 °C. The same trend is followed by the second group too. The values are 0.7 nm, 1.2 nm, 1.4 nm and 2.4 nm for the sample $P_{e22}$, $P_{e21}$, $P_{e20}$ and $P_{e18}$, respectively.
5.3 Thermal Growth

The last process that has been examined is thermal growth process. There are only three samples, T_{24}, T_{25} and T_{26}, which have thermally grown oxide. In general these oxides are more stable with $V_{fb}$ around 1 V and $D_{it}$ around $1.5 \times 10^{11} \text{eV}^{-1} \text{cm}^{-2}$. The oxide breakdown occurred around 3 MV/cm. Figure 5.10 a and b shows CV and the IV curves for the three different samples.

The rms values of the roughness are 0.8 nm, 1.2 nm and 3.2 nm for the samples T_{24}, T_{25} and T_{26}. Sample T_{26} is the not annealed sample of the thermally grown ones.

![Figure 5.10](image1)

**Figure 5.10.** a) A sample of high frequency capacitance-voltage curves for samples whose oxide has been grown thermally b) a sample of current density versus electric field curves

5.3.1 Influence of Growth Temperature

![Figure 5.11](image2)

**Figure 5.11.** a) Effect of grown temperature on $V_{fb}$; b) effect of grown temperature on $D_{it}$.

In this section the effect of growth temperature on the thermally grown oxide samples is shown. Two temperatures, 1150 °C and 1250 °C, are defined, for sample T_{24} and T_{26}, respectively. Figure 5.12 a shows that $V_{fb}$ decreases from 1.19 V for sample deposited at 1150 °C to 0.81 V for 1250 °C grown sample, as well as the decrease in the standard deviation from 0.51 V to 0.47 V. Figure 5.12 b shows the change in $D_{it}$ with respect to the growth temperature. The $D_{it}$ for the sample grown at 1150 °C is $1.99 \times 10^{11} \text{eV}^{-1} \text{cm}^{-2}$ and it increases
slightly to $2.1 \times 10^{11} \text{ eV}^{-1} \text{cm}^{-2}$ for the sample grown at 1250 °C. Standard deviation also decreases from $1.92 \times 10^{11} \text{ eV}^{-1} \text{cm}^{-2}$ to $1.28 \times 10^{11} \text{ eV}^{-1} \text{cm}^{-2}$, respectively, showing that the stability of the samples improved by increasing growth temperature.

5.3.2 Influence of Annealing

![Graphs](image)

*Figure 5. 12. a) Effect of annealing temperature on $V_{fb}$; b) effect of annealing temperature on $D_{it}$*

This section investigates the influence of PDA temperature for two samples; T$_{25}$ with no annealing (N/A) and T$_{26}$ annealed at 1150°C. Figure 5.11 a, shows that $V_{fb}$ decreases after annealing as well as the stability of the sample. In case of unannealed sample (T$_{25}$), the measured $V_{fb}$ is 2.00 V with a standard deviation of 0.35 V. In the case of the annealed sample (T$_{26}$), $V_{fb}$ is 0.81 V and the standard deviation is 0.47 V. The trend is opposite for $D_{it}$ (Figure 5.11 b). For the unannealed sample (T$_{25}$), the measured $D_{it}$ and standard deviation are $1.23 \times 10^{11} \text{ eV}^{-1} \text{cm}^{-2}$ and $4.53 \times 10^{10} \text{ eV}^{-1} \text{cm}^{-2}$, respectively and for the annealed sample (T$_{26}$) $D_{it}$ is $2.1 \times 10^{11} \text{ eV}^{-1} \text{cm}^{-2}$ and standard deviation is $1.28 \times 10^{11} \text{ eV}^{-1} \text{cm}^{-2}$.
Chapter 6. Discussion

In this chapter a summary of the important results from the experiments will be given and some general trends will be discussed. However, first it should be stated that there is often a considerable spread in the values measured on each sample, as seen by the relatively large error bars (standard deviation). Several samples also deviate from any trends, which makes the analysis difficult. These inconsistencies may be related to the small size of the samples and that each sample is cleaned and handled separately, which could lead to a spread in data.

It is, nevertheless, observed that for all methods, annealing the samples generally results in a $V_{fb}$ closer to zero. Tables 6.1-3 show all the $V_{fb}$ values and the corresponding annealing temperatures for the two PeCVD tools and the thermal growth.

<table>
<thead>
<tr>
<th>Table 6.1. Annealing temperatures versus $V_{fb}$ for P5000 samples.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Annealing Temperature ($^\circ$C)</td>
</tr>
<tr>
<td>----------------------------------</td>
</tr>
<tr>
<td>1150</td>
</tr>
<tr>
<td>1150</td>
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<tr>
<td>1000</td>
</tr>
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<td>N/A</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Table 6.2. Annealing temperatures versus $V_{fb}$ for Pekka samples.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Annealing Temperature ($^\circ$C)</td>
</tr>
<tr>
<td>----------------------------------</td>
</tr>
<tr>
<td>Pekka</td>
</tr>
<tr>
<td>1150</td>
</tr>
<tr>
<td>1000</td>
</tr>
<tr>
<td>850</td>
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<tr>
<td>N/A</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Table 6.3. Annealing temperature versus $V_{fb}$ for thermally grown oxide samples.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Annealing Temperature ($^\circ$C)</td>
</tr>
<tr>
<td>----------------------------------</td>
</tr>
<tr>
<td>Thermally grown oxide</td>
</tr>
<tr>
<td>1150</td>
</tr>
<tr>
<td>N/A</td>
</tr>
</tbody>
</table>

As shown by the tables 6.1-3, annealing leads to a reduction of oxide defects. This effect is perhaps more clearly seen for samples processed in Pekka, since in P5000 several samples, like P1, P7 and P9, still have high absolute value of $V_{fb}$ even though they are annealed. This difference between Pekka and P5000 could possibly be explained by that the power of P500 is one order of magnitude higher than Pekka. Even if it
is not possible to directly compare this parameter between the two setups due to different geometries and designs, it could imply that the ions arrive at the sample surface with higher energy in P5000, which causes more defects in the oxide structure.

For the PeCVD tools, it is also found that the samples with low $D_{it}$ are nearly always combined with a low absolute value of $V_{fb}$. Figure 6.1 shows the results for both tools.

![Figure 6.1](image)

Figure 6.1 $D_{it}$s versus $V_{fb}$s for all a) P5000 and b) Pekka samples.

P5000 sample values are plotted in Figure 6.1a. As it can be seen it starts from a high $D_{it}$ in the order of $10^{12}$ eV$^{-1}$ cm$^{-2}$ and $V_{fb}$ less than -10 V and it drops linearly to $2\times10^{11}$ eV$^{-1}$ cm$^{-2}$ with $V_{fb}$ almost zero, or slightly positive values for a majority of the samples. Figure 6.1b shows values from Pekka samples. Again it begins from a $D_{it}$ of the order of $10^{12}$ eV$^{-1}$ cm$^{-2}$ with $V_{fb}$ -5 V, it drops to a minimum with $D_{it}$ of $2\times10^{11}$ eV$^{-1}$ cm$^{-2}$ with $V_{fb}$ close to zero V, but then $D_{it}$ values saturates or even increases again at $6\times10^{11}$ eV$^{-1}$ cm$^{-2}$ while $V_{fb}$ rises to 5 V. The two graphs in Fig. 6.1 shows that for both tools there is a cluster of samples with $D_{it}$s less than $5\times10^{11}$ eV$^{-1}$ cm$^{-2}$ while at the same time the $V_{fb}$ is less than 1 V. This behaviour indicates that there exist a rather wide range of process parameters for the PeCVD techniques that gives low $D_{it}$ values and flatband voltage around 0 V. A possible explanation is that the nitrogen treatment in PeCVD is an effective method to passivate the oxide defects since both properties, $D_{it}$ and $V_{fb}$, are minimized.

For the Pekka tool it is, furthermore, found that there is a correlation with $V_{fb}$s and $D_{it}$s with the surface roughness of the samples. By comparing all the samples that have been annealed at 1150 °C, this trend is illustrated in Figure 6.2.
Figure 6.2 a) Roughness (RMS) versus $V_{fb}$ and b) $D_{it}$ versus the product of roughness x Gas ratio for samples which oxide deposited with Pekka tool and have been annealed at 1150 °C

As can be seen from Figure 6.2a, a lower roughness is combined with $V_{fb}$ closer to zero. A small value of the roughness could mean that the oxide is more homogeneous, leading to fewer oxide defects, which leads to low $V_{fb}$. For larger roughness values, the flatband voltage will increase to either more positive or more negative values.

No clear trend could be seen for the relation between the surface roughness and the density of interface traps. However, in Figure 6.2b the product of roughness and gas ratio is shown with respect to $D_{it}$ and here the trend is clear. The $D_{it}$ values decrease and saturate at low values for large values of the roughness together with high levels of nitrogen. The relation in Fig. 6.2b is not easy to understand, but it seems that if the roughness is large at the same time as the nitrogen gas is enhanced, this will lead to a better uptake of the nitrogen and lower $D_{it}$. Of course, a high uptake of nitrogen could also lead to an increased roughness.

Furthermore, it is observed that by simultaneously increasing the power, pressure and the gas ratio during the deposition process, the $D_{it}$s tend to decrease. In Figure 6.3 the density of interface traps of the samples that are annealed at 1150 °C are compared to the product of power, pressure and gas ratio. The $D_{it}$ reduction is strong in the beginning and then tends to level out. Power, pressure and gas ratio can all be correlated with the energy and amount of nitrogen that is deposited and reach the interface. The more nitrogen at the interface, the lower value of $D_{it}$s.
From P5000 the sample that combines lowest $D_{it}$ ($2.82\pm2.19\times10^{11}$ eV$^{-1}$ cm$^2$) and low $V_{fb}$ ($0.79\pm0.42$ V) is $P_6$. It is fabricated with the highest pressure (6 Torr), medium power (100 W), high gas ratio ($N_2O/SiH_4=20$) and it is annealed at 1150 °C. As for Pekka, sample $Pe_{22}$ is the best with three times lower $D_{it}$ ($7.94\pm6.71\times10^{10}$ eV$^{-1}$ cm$^2$) compared to $P_6$ and about half the $V_{fb}$ ($0.48\pm0.29$ V) of the $P_6$. The fabrication parameters for $Pe_{22}$ are: pressure 0.8 Torr, power 20 W, which are the highest for this tool, gas ratio of 0.6, but it is annealed at only 850 °C. On the other hand the samples that have highest $D_{it}$ and $V_{fb}$ are $P_2$ and $P_{e23}$ from P5000 and Pekka, ($8.33\pm4.15\times10^{11}$ eV$^{-1}$ and $-3.96\pm0.88$ V, and $6.37\pm4.29\times10^{11}$ eV$^{-1}$ cm$^2$, $4.78\pm1.36$ V, respectively), respectively. $P_2$ is fabricated with power and pressure of 100 W and 2.8 Torr, while the gas ratio is ($N_2O/SiH_4$) 20 and it is not annealed. The parameters for $P_{e23}$ are: power 20 W and pressure 0.5 Torr, with gas ratio ($N_2O/SiH_4$) of 0.6, and it is also not annealed.

Finally, as for the samples with thermally grown oxide, they all appear to have low $D_{it}$, in the order of $1-2\times10^{11}$ eV$^{-1}$ cm$^2$ and low $V_{fb}$ of 1-2 V. Growth temperature appear to have no significant effect to $V_{fb}$ and $D_{it}$, whereas annealing results in a more uniform oxide, reducing the flatband voltage.
Chapter 7. Conclusions

In this thesis, the process for oxide fabrication in order to optimize the interface between 4H-SiC and SiO$_2$ is presented. Plasma-enhanced chemical vapour deposition (PeCVD), which is done in the Electrum cleanroom with two different tools, P5000 and Pekka, and thermal oxidation are the two methods that are investigated. Capacitance-voltage (CV) and current-voltage (IV) are utilised for the electrical characterization, whereas the structural characterization is done by using atomic force microscopy (AFM).

From our experiments a few main conclusions can be extracted, even if a large spread in the data makes it difficult to find very clear trends. The main results are the following:

- Annealing in N$_2$O ambient is very efficient to reduce the flatband voltage to nearly zero.
- Nitrogen treatment can also reduce the density of interface traps, D$_{it}$, introduced by the PeCVD technique.
- Terman method is used for extracting the interface trap density (D$_{it}$) from CV data. This method underestimates the real number of traps and it is clear that a large number of D$_{it}$s are still present.
- P5000 seems to be a more unreliable tool than Pekka for oxide deposition, since there is a larger spread in the data for samples processed in P5000.
- It should also be of interest to complement these electrical measurements with more extensive structural characterization of the samples, to see if the cause for the large variation in measured data could be, for instance, pinholes.

From the investigation, it is clear that nitrogen annealing has a positive effect on the flatband voltage and the interface trap densities, although it is not possible to reduce the D$_{it}$ values to levels that are acceptable for devices. For future work alternative dielectric deposition techniques, as well as other dielectric systems, should be investigated.
**Appendix**

In the next tables the results from the electrical and structural characterization are summarised for all samples.

### P5000 samples

<table>
<thead>
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<th>Sample number</th>
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### Pekka samples

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