Bachelor’s Thesis:
Designing a BPM board for use in a modular evaluation kit

Jonas Tallhage

31st May 2011
Bachelor’s Thesis:
Designing a BPM board for use
in a modular evaluation kit

Jonas Tallhage
Abstract

Ericsson Power Modules – a subdivision within the Ericsson Corporate Group that develops DC/DC converters – is currently developing an evaluation kit for its main product. In this bachelor’s thesis project an initial prototype for a part of this evaluation kit has been designed. The design work has focused on the electrical and to some degree mechanical construction and has largely consisted of adapting an already existing design to the requirements of the evaluation kit.
Acknowledgments

- I am greatly indebted to and wish to thank Torbjörn Holmberg – who has been my thesis supervisor at Ericsson – for his invaluable support, advice and assistance during this project.

- I would like to thank Henrik Isaksson who created the design upon which many parts of the design presented here is based and who have provided with valuable assistance during this project.

- I would like to thank Hans Lundström for the feedback he has provided me with during his work with designing a PCB layout from the schematics described in this report.

- I would like to thank Jan Carlsson – who has been my supervisor at BTH – for his advice during the project.
Bachelor’s Thesis:  
Designing a BPM board for use  
in a modular evaluation kit  
Jonas Tallhage

Contents

Abstract 3

Acknowledgments 4

Notation 8

Terminology 8

Typographical conventions 8

Notes on citations 9

1 Introduction 10

1.1 Background and problem motivation 10

1.2 Purpose 10

1.3 Scope 10

1.4 Problem statement 11

1.5 Outline 11

2 Background and theory 12

2.1 Voltage regulators 12

2.1.1 Linear regulators 12

2.1.2 Switching regulators 12

2.2 Hold-up capacitors 15

2.3 Communication protocols 16

2.3.1 SPI 16

2.3.2 JTAG 16

2.3.3 PMBus, SMBus and I²C 16

2.3.4 RS232 17

2.4 ADCs 17

2.5 Bypass/decoupling capacitors 17

3 Method 18

3.1 Analysis of the reference design 18

3.2 Writing a requirement specification 18

3.3 Partitioning of the schematic 18

3.4 Design of the power supply 19

3.4.1 Polarity protection and mains supply filtering 19

3.4.2 Conversion from -48V to 5V 19

3.4.3 Conversion from 5V to 3.3V 20

3.4.4 Generation of a 3V reference voltage 20

3.4.5 Generation of mains supply sense voltages 20

3.5 Design of the main circuit 21

3.5.1 Choice of a microcontroller 21

3.5.2 EEPROM 21

3.5.3 SPI 21

3.5.4 JTAG 22

3.5.5 Converter enable outputs 22

3.5.6 PMBus 22

3.5.7 Converter sync clocks 23

3.5.8 AVS (Automatic Voltage Scaling) 23

3.5.9 RS232 23
Bachelor’s Thesis:  
Designing a BPM board for use in a modular evaluation kit  
Jonas Tallhage

3.5.10 UART ......................................... 23
3.5.11 Sense inputs .................................. 24
3.5.12 General purpose I/O (GPIO) ................. 24
3.5.13 Reset button .................................. 24
3.5.14 Bootloader select jumpers ..................... 24
3.6 Design of the test logic .......................... 24
3.7 Considerations for a physical realisation ............. 25
3.8 Physical design .................................. 25

4 Results ............................................. 26
4.1 Power supply .................................... 26
4.1.1 Polarity protection .............................. 26
4.1.2 Conversion from -48V to 5V .................... 26
4.1.3 Conversion from 5V to 3.3V .................... 28
4.1.4 Generation of a 3V reference voltage .......... 29
4.1.5 Generation of sense voltages .................. 30
4.2 Main circuit .................................... 30
4.2.1 Microcontroller ................................ 30
4.2.2 EEPROM ..................................... 32
4.2.3 SPI ........................................... 33
4.2.4 JTAG .......................................... 34
4.2.5 Converter enable outputs ....................... 35
4.2.6 PMBus & PWM clocks .......................... 35
4.2.7 AVS (Automatic Voltage Scaling) ............... 36
4.2.8 RS232 .......................................... 36
4.2.9 UART ......................................... 38
4.2.10 Sense inputs ................................ 38
4.2.11 General purpose I/O (GPIO) .................. 39
4.2.12 Reset button ................................ 39
4.2.13 Bootloader select jumpers .................... 40
4.3 Test logic ...................................... 40
4.4 Considerations for the physical design ............. 41

5 Discussion ........................................ 42

References .......................................... 43

Appendices .......................................... 45

A Pin numbers ....................................... 45
A.1 SPI .............................................. 45
A.2 JTAG ............................................ 45
A.3 PMBus .......................................... 46
A.4 AVS .............................................. 46
A.5 RS232 ............................................ 47
A.6 UART ............................................ 47

B Numbering of schematic pages ....................... 47
# List of Figures

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Buck-boost converter concepts</td>
<td>13</td>
</tr>
<tr>
<td>2</td>
<td>Flyback converter concepts</td>
<td>14</td>
</tr>
<tr>
<td>3</td>
<td>Flyback power supply filtering-frequency model</td>
<td>14</td>
</tr>
<tr>
<td>4</td>
<td>Schematic of the -48V to 5V-conversion circuitry</td>
<td>26</td>
</tr>
<tr>
<td>5</td>
<td>Schematic of the 5V to 3.3V-conversion circuitry. The design shown here has been adapted from the reference design (Ericsson, 2009a) and the application notes for the LP2985 (National Semiconductor, 2007).</td>
<td>28</td>
</tr>
<tr>
<td>6</td>
<td>Schematic of the 3V reference voltage circuitry. The design shown here has been adapted from the reference design (Ericsson, 2009a) and the application notes for the MAX6126 (Maxim, 2003).</td>
<td>29</td>
</tr>
<tr>
<td>7</td>
<td>Conceptual overview of the sense voltage-generating circuitry. The design shown here has been adapted from the reference design (Ericsson, 2009a).</td>
<td>30</td>
</tr>
<tr>
<td>8</td>
<td>Conceptual overview of the MCU connections</td>
<td>31</td>
</tr>
<tr>
<td>9</td>
<td>Schematic of the EEPROM connections. The design shown here has been adapted from the reference design (Ericsson, 2009a) and the application notes for the Atmel EEPROM (Atmel, 2007).</td>
<td>32</td>
</tr>
<tr>
<td>10</td>
<td>Schematic of the SPI connector arrangement</td>
<td>33</td>
</tr>
<tr>
<td>11</td>
<td>Schematic of the JTAG connector arrangement. The design shown here has been adapted from the reference design (Ericsson, 2009a).</td>
<td>34</td>
</tr>
<tr>
<td>12</td>
<td>Schematic of the PMBus and PWM clock connector arrangement. The design shown here has been adapted from the reference design (Ericsson, 2009a).</td>
<td>35</td>
</tr>
<tr>
<td>13</td>
<td>Schematic of the AVS connector arrangement.</td>
<td>36</td>
</tr>
<tr>
<td>14</td>
<td>Schematic of the RS232 connector arrangement. The design shown here has been adapted from the reference design (Ericsson, 2009a) and the application notes for the transceiver IC (Maxim, 2011).</td>
<td>36</td>
</tr>
<tr>
<td>15</td>
<td>Schematic of the UART connectors arrangement</td>
<td>38</td>
</tr>
<tr>
<td>16</td>
<td>Schematic of the sense inputs filtering circuitry</td>
<td>38</td>
</tr>
<tr>
<td>17</td>
<td>Schematic of the bootloader select jumpers connections. The design shown here has been adapted from the reference design (Ericsson, 2009a).</td>
<td>40</td>
</tr>
<tr>
<td>18</td>
<td>Schematic of the test logic connections.</td>
<td>40</td>
</tr>
<tr>
<td>19</td>
<td>Pinout for the SPI connector.</td>
<td>45</td>
</tr>
<tr>
<td>20</td>
<td>Pinout for the JTAG connector.</td>
<td>45</td>
</tr>
<tr>
<td>21</td>
<td>Pinout for the PMBus connector.</td>
<td>46</td>
</tr>
<tr>
<td>22</td>
<td>Pinout for the AVS connector.</td>
<td>46</td>
</tr>
<tr>
<td>23</td>
<td>Pinout for the RS232 connector.</td>
<td>47</td>
</tr>
<tr>
<td>24</td>
<td>Pinout for the UART connector.</td>
<td>47</td>
</tr>
</tbody>
</table>
Notation

Terminology

- **ADC**: Analog-to-Digital Converter, an electronic device used to convert analog signals to digital data.
- **AVS**: Automatic Voltage Scaling, a general term for techniques used to provide automatic fine-tuning of a voltage.
- **JTAG**: Joint Test Action Group, a standard (officially standardised in IEEE 1149.1) used for testing, debugging and programming of integrated circuits mounted on PCB:s.
- **LQFPx**: Low-profile Quad Flat Package. A type of packaging used for integrated circuits, the number (represented by x here) shows the number of pins included in the package.
- **MCU**: Micro-Controller Unit, a computing processor including programmable memory and various peripherals.
- **MUX**: Multiplex, refers to various techniques for combining several signals into one in such a way that the original signals can be restored at a later point.
- **PMBus**: Power Management Bus, an SMBus-based protocol used for communicating with power converters.
- **RS232**: Recommended Standard 232, the standard used for the serial ports (still) found on many PC:s.
- **SM**: Surface Mount, a type of packaging used for electronic components.
- **SMBus**: System Management Bus, a protocol used for communication on computer motherboards.
- **SPI**: Serial Peripheral Interface bus, a communication protocol used in many integrated circuits.
- **UART**: Universal Asynchronous Receiver/Transmitter. A piece of hardware which adapts parallell data for serial communication, commonly included in microcontrollers.

Typographical conventions

- Pin names have been typeset in **sans serif** to distinguish them from the surrounding text, **overlines** have been used to denote inverting pins.
- In mathematic expression the usual italic letters have been used for variables (e.g. $U$ for voltages, see below) while unit abbreviations (e.g. V for Volts) have been typeset using upright letters.
- In spite of the language used in the report it is primarily expected to be read by swedes, for this reason $U$ rather than $V$ has been used to denote voltages since this should be more familiar to swedish readers.
Notes on citations

Overall the Harvard style has been used for citations. An exception has been made by using *ibid* for consecutive citations referring to the same source despite the use of *ibid* not normally being considered part of the Harvard style. In quite a few places in this report there has been a need to include a large number of such consecutive citations. The usual Harvard style of including these citations was found to come across as rather heave-handed, hence the use of *ibid* instead.
# 1 Introduction

Ericsson Power Modules is a part of the Ericsson corporate group that develops and markets DC/DC converters for use in tele- and data-communication systems. For retailers of electronic products and systems it is often desirable to make an evaluation kit available in order to provide customers with a quick and convenient way of evaluating the main product and to aid in developing systems involving it. Ericsson Power Modules are presently developing such an evaluation kit. The kit is envisioned to be modular in nature and to consist of several separate boards (Ericsson, 2010), thus making it possible for customers to tailor their evaluation setups to their specific needs. In this bachelor’s thesis project the electrical – and to some degree mechanical – design of a first prototype for a Board Power Management (BPM) board have been worked out. This board will provide functions for monitoring, controlling, configuring and supervising test setups constructed using other boards in the evaluation kit and for allowing the setups to communicate with a host processor or a PC.

## 1.1 Background and problem motivation

Within a board power test setup used for evaluating DC/DC converters of the type developed by Ericsson Power Modules, there is need for a central device which can be used for monitoring, control, configuration and supervison of the setup. This device needs to be able to communicate with external devices to allow various control and configuration data to be transferred to the test setup from a device where such data can be entered by a user (e.g. a host processor or a PC). In turn, the device needs to enable communicating data concerning the state of the setup to a device which can display it to a user (e.g. a host processor or a PC). In the evaluation kit currently under development at Ericsson Power Modules the BPM board is expected to provide this functionality.

## 1.2 Purpose

The purpose of this thesis project has been to design a first prototype for a BPM board which is to be part of the evaluation kit. The intent has not been to produce a finished product but rather to create an initial design which can be evaluated and tested in order to weed out problems and refine the design before final release. Additionally, it is intended to serve as a development tool for use in further developing the Board Power Management software and firmware.

## 1.3 Scope

Due to the nature of the functionality expected to be provided by the BPM board both hardware and software need to be designed. The scope of the present project has been limited to only include the hardware parts of the design and concerns regarding the software parts have only been taken into account when these have had an impact on the way in which the hardware should be designed (software development is ongoing at another site within Ericsson). Furthermore, although some mechanical details of the design have been taken into account the main focus has been on the abstract (i.e. shematic-level) electrical considerations. The creation of a physical layout of the board has been carried out by
another person within the company who specialises in this kind of task and the author has only had a supporting function during the work with this.

The design work has not been carried out from scratch but has rather been based on an already existing design (Ericsson, 2009a; this older design will from this point on be referred to as “the reference design”) which has been adapted to the needs of the evaluation kit. A significant part of the work has therefore focused on understanding the older design in order to make it possible to identify and isolate the parts needed.

1.4 Problem statement

The problem to be solved has been to carry out the electrical – and to some degree mechanical – construction of the BPM board through adaption of the reference design. This task has been possible to break down into a number of subtasks:

1. Analysis of the reference design.
2. Writing a requirement specification.
3. Designing a schematic for the BPM.
4. Assisting in creating a layout based on the previously created schematic.
5. Ordering components and PCB.
6. Assembling the board.

It should be noted that the main task was to be the abstract electrical design of the board performed in steps 1 to 3 above. The last three steps were considered as desirable outcomes and were to be carried out if time and resources permitted.

1.5 Outline

- A brief outline of concepts which are of importance to the report is given in the Theory section.
- The general workflow and the considerations leading up to the design are described in the Method section.
- The design itself is presented in the Results section.
- A brief discussion of insights gained and ideas gathered during the design work is given in the Discussion section.
2 Background and theory

2.1 Voltage regulators

Voltage regulators are used to provide stable, low-noise voltages for use in e.g. power supplies. As the name implies a voltage regulator will involve regulation of the output voltage in order to ensure that it remains within certain limits even in the face of varying input voltage (line regulation) and load (load regulation).

2.1.1 Linear regulators

A linear regulator regulates voltage by employing an active element – e.g. a transistor – to directly control the output voltage. Regulation is achieved through varying the effective resistance of the active element so that the output voltage is kept constant (Floyd, 1999). While fairly simple, this has the disadvantage that current flowing through the active element will cause power dissipation since \( P = VI \). For this reason, the use of linear regulators is limited to low-power applications since the power dissipated would not only make such regulators highly inefficient in high-power applications but could also cause enough heating to destroy the device (Floyd, 1999).

2.1.2 Switching regulators

In a switching regulator the active element is employed as a switch which is used to rapidly turn the input voltage on and off, producing a square wave from which the DC value is extracted through filtering to generate the output voltage (Floyd, 1999). The magnitude of the output voltage is proportional to the duty cycle of the switching (Erickson & Maksimović, 2001) and regulation can therefore be achieved by varying the duty cycle. Ideally, the active element would have a zero resistance in its on mode and an infinite resistance in its off mode, thus theoretically allowing the output voltage to be varied with no power dissipated in the switch (ibid). While such ideal active elements do not exist switching regulators are still superior to linear regulators in terms of efficiency which allows them to be used in situations where the amount of power lost in a linear regulator would have been unacceptably high, leading to intractable problems with heat management.
Switching converters come in a wide variety of configurations, for the purposes of this report the flyback variety will be of particular interest. This regulator type is derived from the somewhat simpler buck-boost converter type (Erickson & Maksimović, 2001), a conceptual outline of which is shown in Figure 1a. The principle of operation is that setting the switch to the on position will cause current to flow through the inductor which is used to store energy, when the switch is then thrown to its off position the resulting reverse voltage (due to the sudden change in current through the inductor) will cause the inductor to transfer energy to the capacitor (ibid). The capacitor acts as another energy storage element which supplies power to the load when the switch is in its off position, allowing it to be powered continuously (ibid). Since the voltage across an inductor is proportional to the derivative of the current through it (Irwin & Nelms, 2008) the suddenness of the change in current as the switch is thrown can cause the reverse voltage to become very high – theoretically infinite – and the output voltage of the buck-boost converter can therefore be made higher than the input voltage (Erickson & Maksimović, 2001). Theoretically any magnitude can be produced, however the polarity of the output voltage will be reversed with respect to the input voltage since the voltage seen by the capacitor is the reverse voltage developed across the inductor when the switch is thrown (ibid).

A more practical model is shown in Figure 1b, here the double-throw switch is implemented by a transistor used as single-throw switch controlled by \( v_c \) and a diode. When the transistor switch turns on the supply voltage will cause the diode to become reverse biased which will clearly cause the circuit to behave like the one in Figure 1a with the switch in the on position. When the transistor switch turns off the reverse voltage caused across the inductor will cause the diode to become forward biased and conduct, making the circuit behave (except for the voltage drop over the diode) like the one in Figure 1a with the switch in

---

**Figure 1:** Illustrations of the basic concepts of buck-boost converters, adapted from Erickson & Maksimović (2001).
the off position. (Erickson & Maksimović, 2001)

\[ \begin{align*} 
V_{in} & \quad C \quad V_{out} \\
+ & \quad - \quad + \\
\text{Vin} & \quad \text{vc} & \quad \text{Vout} \\
\end{align*} \]

(a) Flyback converter formed by replacing the inductor in Figure 1b with a transformer.

\[ \begin{align*} 
V_{in} & \quad C \quad V_{out} \\
+ & \quad - \quad + \\
\text{Vin} & \quad \text{vc} & \quad \text{Vout} \\
\end{align*} \]

(b) Flyback converter with positive (with respect to the input) output polarity and with the source of the transistor connected to ground to simplify voltage control.

Figure 2: Illustrations of the development of the flyback converter from the buck-boost converter, adapted from Erickson & Maksimović (2001).

An outline of the flyback converter is shown in Figure 2. The flyback converter is derived from the buck-boost converter by inserting a transformer in place of the inductor, since a transformer is made up out of two coupled inductors it will serve the same purpose as the inductor in the original circuit in terms of storing and releasing energy. Using a transformer in place of the inductor causes the input and output to be galvanically isolated from each other and also permits the output voltage to be of any polarity desired since one can simply reverse the polarity of the secondary side of the transformer – as shown in Figure 2b – to make the output voltage have the same polarity as the input voltage. (Erickson & Maksimović, 2001)

\[ \begin{align*} 
L & \quad C \quad R \\
V_{in} & \quad v_{out} \\
\end{align*} \]

Figure 3: Model used for calculating the filtering frequency of the low-pass filter present at the output a flyback converter.

Since the voltage at the outputs of the the secondary winding of a flyback
converter will be alternating in nature while DC voltages are desired, a low-pass filtering (or reservoir, from another point of view) capacitor is included at the output. The filtering frequency of the circuitry present at the output is of concern since too high a corner frequency here could allow unacceptable amounts of switching noise to leak into the circuit being powered and interfere with various functions there. The simplified model presented in Figure 3 – with $L$ representing the inductance of the secondary transformer winding and $R$ the load – can be used to get a rough idea about the break frequency of the filter. Using ordinary circuit analysis techniques this model yields the transfer function

$$H(s) = \frac{1/(LC)}{s^2 + s/(RC) + 1/(LC)} = \frac{\omega_c^2}{s^2 + 2\zeta\omega_cs + \omega_c^2}$$

from which it is seen that the corner frequency $\omega_c$ (in rad/s) and the damping coefficient $\zeta$ (dimensionless) are

$$\omega_c = \frac{1}{\sqrt{LC}} \quad \text{and} \quad \zeta = \frac{\sqrt{L}}{2\sqrt{CR}}.$$

As can be seen the filtering frequency is independent of $R$ and should therefore stay the same even in the face of load variations.

It should be noted that this model is in all likelihood too simple to yield very accurate results since it simply represents the transformer using a voltage source and an inductor despite the inductance of the transformer playing a central part in determining the output voltage in the first place. It should, however, be sufficient for obtaining a rough estimate of the filtering frequency.

### 2.2 Hold-up capacitors

In many situations it is desirable that an electronic device is able to operate normally for some time even in the presence of brown- or black-outs on the supply rail, for example to initiate a shut-down sequence. This calls for including some means of storing power within the system. Many such means can be imagined but in the case of an electronic system the most obvious is arguably to use the charge-storing property of capacitors to this end. When using such a solution it is of course important to be able to calculate the minimum capacitance needed in order to keep the system going for a specified amount of time.

Systems usually need a certain minimum voltage and current to operate properly, hence the hold-up capacitors need to be able to supply this amount of current for the specified time while still maintaining a voltage that is at least as high as the minimum voltage needed by the system. Current is defined as the change in charge (measured in Coulombs) per unit time – or

$$I(t)\,[A] = \frac{dQ(t)}{dt} \left[ \frac{C}{s} \right]$$

in mathematical terms (Irwin & Nelms, 2008) – while capacitance is measured in Farads which is the same thing as Coulombs per Volt, i.e.

$$C\,[F] = \frac{Q}{V} \left[ \frac{C}{V} \right]$$
(Tipler & Mosca, 2004). Assuming a constant current, the amount of charge required to supply the specified operating current for the specified amount of time can be calculated by multiplying the amount of current with the period of time, yielding \( q = i \times t \). The required value for the hold-up capacitors can then be calculated by substituting the total amount of charge needed \( q \) and the amount \( \Delta u \) by which the voltage across the hold-up capacitors can be allowed to drop into equation (2).

### 2.3 Communication protocols

#### 2.3.1 SPI

SPI (Serial Peripheral Interface) is a standard for communication over a synchronous serial bus, it originated at Motorola but has since become an industry standard (Huang, 2005). In an SPI setup one device will take the role of master and all other devices will be slaves (ibid). The master can select a slave by pulling its slave select (SS) pin low, a separate slave select line needs to be used for each slave but ordinary in/out pins can be used to implement the slave select function on the master (Kalinsky & Kalinsky, 2002). The master also provides a common clock signal (SCK) that is received by all slave devices (ibid).

Communication takes place through two lines: MOSI (Master Out Slave In) for messages from the master to a slave and MISO (Master In Slave Out) for messages in the opposite direction (ibid). Since SPI is a bus protocol several slaves may be connected to these lines simultaneously (ibid) with the master using the slave select function to ensure that only one slave at a time is active. As usual with bus interfaces, all devices which are not currently active must be placed in high-Z (high impedance) state in order not to load the communication line (Hemert, 2001). SPI devices may use different signaling voltages, creating a potential problem with interfacing two such devices (Maxim, 2002).

#### 2.3.2 JTAG

The JTAG (Joint Test Action Group) protocol is formally standardised in IEEE 1149.1. It was originally intended for production-testing of PCB:s using boundary scan techniques but is also commonly used for programming and debugging of embedded devices, for example microcontrollers. Five pins are used: TDI (Test Data In), TDO (Test Data Out), TCK (Test Clock), TMS (Test Mode Select) and TRST (Test Reset). (Corelis 2011)

#### 2.3.3 PMBus, SMBus and I²C

PMBus (Power Management Bus), details about this standard can be found at [http://pmbus.org](http://pmbus.org) is an open standard protocol used for communicating with power converters (SMIF, 2005). It is a layered protocol which is built on top of an earlier protocol called SMBus (System Management Bus) which it uses for physical layer communication, SMBus is in turn based on the I²C (Inter-Integrated Circuit) protocol which was originally created by Philips in 1982 (SMIF, 2010).

For the purposes of the present text the main concern is the electrical characteristics of the PMBus standard, since PMBus uses SMBus for its physical layer communication the specifications for these characteristics are to be found in
the SMBus specification documents. The electrical specifications mandate that pull-up resistors be placed on all bus lines and recommend constant-current sources as an alternative in case of high bus capacitance. Some requirements are also laid out for the design of the output stages of devices connected to the bus. (SBS Implementers Forum, 2000)

2.3.4 RS232

RS232 is a standard for serial communications. The standard is quite old – having first been introduced in 1962 – but is even so still used for a variety of applications (ARC Electronics, N.D.). It permits a range of different voltage magnitudes – from ±0.3V up to ±12V – to be used for signaling (ibid). This can cause some trouble in modern systems which will often operate from a single, low-voltage supply meaning that special methods have to be used to generate the voltages needed for true RS232 communication.

2.4 ADC:s

An ADC (Analog to Digital Converter) converts analog signals to digital ones and is a common feature included in microcontrollers. The various ways in which this can be done are described in detail in several places, for example Franco (2002). One method which is commonly used involves sampling the analog signal using sample-and-hold circuitry and then performing a successive approximation algorithm on the sampled value to produce a quantised binary number which approximates the magnitude of the signal, making the resulting data amplitude-as well as time-discrete (ibid). In using this method only voltages within a certain range are acceptable, voltages outside of it will often simply be clipped to the nearest (i.e. the highest or lowest) value (ibid). Due to the quantisation, it is important that the allowable range is as small as possible while still including all expected input values in order to use the available bits used for representing the input values as effectively as possible. To facilitate this the ADC:s included in MCU:s often allow the user to set the upper limit by applying a reference voltage of suitable magnitude to some pin on the MCU. The voltage thus supplied will generally be used for comparison in the conversion process and it is therefore important that this voltage be as accurate as possible in order to obtain good performance from the ADC.

2.5 Bypass/decoupling capacitors

Bypass capacitors – also known as decoupling capacitors – are common in electronic circuits, they employ the DC-blocking/AC-passing properties of capacitors to create a direct path to ground for AC signals while blocking DC-signals. This can be done for a variety of purposes, a common one is to provide a path to ground for interference on a line. Such interference will often be of high-frequency and a capacitor will therefore appear as a short-circuit to them, hence the inclusion of a bypass capacitor can suppress such disturbances by leading them to ground. (Glisson, 2011)
3 Method

3.1 Analysis of the reference design
The initial step of the project consisted of analysing the reference design (INX 106 781/10; Ericsson, 2009a) and determining what parts of it should be carried over to the new design, this analysis principally revolved around the circuitry including and surrounding the MCU and the power supply. In order to make the analysis manageable the initial work concentrated on identifying functional blocks and identifying which components were associated with each function. The circuitry performing each function was then examined in greater detail.

During the analysis work the designer of the reference design was contacted at various points and provided valuable insight into certain details of this design, especially regarding the reasons for why these details were included.

3.2 Writing a requirement specification
After having analysed the reference design (Ericsson, 2009a) a requirement specification (Ericsson, 2011a) was written, based in part on the analysis of the reference design, in part on an ongoing dialogue with the thesis supervisor and in part on an already existing requirement specification (Ericsson, 2010) which details the overall requirements for boards belonging to the evaluation kit. Details were included on a number of general aspects of the design such as physical dimensions, climate conditions and choice of components. Details were also included regarding the particular functions needed in the board, more information on these can be found in the relevant sections below.

3.3 Partitioning of the schematic
As a project grows in size and complexity the importance of dividing it into distinct subparts rapidly increases. Before the work with the details of the design was started some time was therefore spent on determining how the design should be partitioned into appropriate subcircuits. The schematic was drawn using Cadence OrCAD, this software provides features for dividing a projects into a hierarchical structure of subschematics and also provides functions for further dividing these schematics into separate pages. It was decided to divide the design into three different schematics corresponding to the primary functions required in the board: power supply, main circuitry and test logic. A further master schematic was added where the three sub-schematics were connected together, thereby enabling a viewer to quickly get a rough outline of the design’s general structure. Each sub-schematic was in turn divided into separate pages corresponding to the various functions needed within the particular schematic, for instance the schematic for the power supply was divided according to the steps used in the conversion. A numbering system was also created for the various schematic pages in which the first digit corresponded to the schematic (e.g. a number of the form 1x would mean that it referred to a page in the power supply schematic) while the second corresponded to a particular page within the schematic (e.g. the number 11 was used to refer to the particular page in the power supply schematic where -48V to 5V-conversion was detailed). This numbering scheme was also used for components which were numbered
in such a way that the first two digits were used to indicate on which page a particular component were to be found. For example, a component with the number R1101 would be a resistor and would be found on page 11. See section B in the appendices for a list of the numbers used.

It was briefly considered whether to place all connectors on the master schematic to provide a quick way for a viewer to see which connectors are included in the design. However, this idea was discarded as it was decided that the connectors should be regarded as parts of the circuitry for which they provide connectivity.

3.4 Design of the power supply

It was decided early on that the board needed to provide its own power supply as it is expected to be among the first parts of a test setup to be started. It was also decided that the power supply circuitry should contain hold-up capacitors and that these should enable the system to function properly for at least 10ms in case of a total blackout on the mains supply rail.

3.4.1 Polarity protection and mains supply filtering

During dialogue with the thesis supervisor it was decided that the design should incorporate simple polarity protection and filtering schemes which were not to be adapted from the reference design but from another previously existing design detailed in Ericsson (2011c). The polarity protection and filtering schemes used in the reference design were considerably more complex than the ones eventually employed and since such intricate schemes were not considered to be needed they would only have served to unnecessarily increase the component count and complexity of the design.

3.4.2 Conversion from -48V to 5V

The board was to be powered from a -48V supply voltage as commonly used in cellular phone base stations (Hermann, 2011), therefore simply using a linear regulator was precluded. Such a regulator would not be able to convert the negative voltage to a positive one as required by most off-the-shelf components and would furthermore be too inefficient by far which aside from wasting energy would lead to major problems with heat management. For these reasons a switching regulator was used to provide an initial conversion from -48V to +5V. The design implementing this conversion was based around an off-the-shelf PWM controller for switching regulators – the ON Semiconductor NCP1030 which is designed for use in -48V telecom systems (ON Semiconductor, 2010) – in conjunction with a transformer and was adapted with very few changes from the reference design (which in turn appears to have adapted from a design outlined in the controller datasheet [ibid]). The particular voltage level at the output of this stage of the conversion was chosen mainly because it was used in the reference design. Since time and resources did not permit any testing of the converter design ahead of construction it was considered prudent to stick with a tried and tested design rather than to make modifications which could potentially cause problems. Since a 5V supply was not needed anywhere within the circuit it might have been possible to increase efficiency somewhat by initial
conversion to a voltage closer to the one provided by the linear regulators but this potential increase in efficiency was considered unimportant when compared to the potential problems.

3.4.3 Conversion from 5V to 3.3V
Conversion from the 5V output of the switching regulator to the 3.3V needed by the main circuitry was performed using a linear regulator. This was feasible in this case since the output transistor of the linear regulator would only have to handle a relatively modest voltage drop, resulting in acceptable power dissipation. The basic configuration was taken from the reference design which had included hold-up capacitors at this stage of the conversion, placed just before the regulator. The values of these were tweaked somewhat in order to achieve the desired hold-up time. The regulator circuitry was based around the National Semiconductor LP2985 linear regulator which is guaranteed to deliver an output current of up to 150mA (National Semiconductor, 2007).

3.4.4 Generation of a 3V reference voltage
The ADC included in the family of microcontrollers to be used can use the supply voltage as a reference voltage for determining the input voltage range over which the ADC will operate normally, alternatively a lower reference voltage can be provided on a pin dedicated for this purpose. In the reference design the latter option was used, employing a precision voltage reference IC – the Maxim MAX6126 – for generating the voltage presented to the MCU. This voltage reference IC produces a reference voltage with of ±0.02%, it also has a low temperature coefficient and provides good regulation of line as well as load (Maxim, 2003). This solution was considered prudent since the quality of the reference voltage presented to an ADC will be a major factor in determining the accuracy of the conversion and it was therefore kept.

3.4.5 Generation of mains supply sense voltages
As mentioned earlier the board was required to be able to shut down gracefully in case of brown- or black-outs on the mains supply voltage. For this to be possible two conditions needed to be fulfilled: there was need for some form of storage element for storing power and it had to be possible for the device to detect disturbances on the supply rail so that a proper shutdown sequence could be initialised. The required storage element has already been mentioned in section 3.4.3. The detection could be performed by the ADC of the MCU but obviously the mains supply voltage could not be fed directly to the ADC inputs since it would be high enough to potentially being able to damage the MCU (apart from the problem that the signal level would be far outside of the allowable input range). For this reason some kind of conditioning of the supply voltages was needed so that a suitable signal could be presented to the detecting element. The circuitry for this conditioning was taken from the reference design, it uses the 3V reference voltage as input to an opamp to create a buffered 4.5V reference voltage which is mixed with the supply voltage through the use of resistive voltage dividers. The resulting voltages are buffered through the use of voltage follower-connected OP-amps and is then presented to the detection circuitry.
The reference design used two mains supply sense voltages: one taken right at the input of the mains supply rail and one taken at the output, i.e. after the polarity protection and filtering circuitry. This scheme was kept in the new design but considering the much simpler circuitry used for these functions it might not be necessary to include both and it might therefore be considered to exclude one of them in a further iteration of the design.

### 3.5 Design of the main circuit

#### 3.5.1 Choice of a microcontroller

The general microcontroller family was already decided on because of the requirement to follow the reference design but a particular controller or within the family still had to be decided on. Three main factors affected this choice: processing power, onboard memory and available pins. It was eventually decided that the controller should be available in an LQFP100 package in order to ensure that a large enough amount of pins were available. Concerning memory and processing power flexibility was desired and it was therefore decided that it should be possible to replace the particular MCU used for a related one with a different clock speed and amount of memory.

#### 3.5.2 EEPROM

EEPROM was to be included to enable the use of a bootloader residing on external (to the MCU) memory and for enabling storage of various data. Since the board being designed was primarily intended to be an early prototype a certain degree of flexibility was desired regarding the memory and it was therefore considered preferable that the memory be taken from a family of pin-compatible devices offering a range of different memory sizes. It was decided that communication with the MCU was to be done using the SPI protocol.

#### 3.5.3 SPI

An SPI interface was needed internally to allow the MCU to communicate with the EEPROM. In addition, it was desired that an SPI connection be available to allow an external unit to communicate with the MCU over this protocol. These two demands were quickly found to be somewhat conflicting as only one SPI port could be made available on the MCU due to the pins associated with the others being needed for other purposes.

It was briefly considered whether some form of MUXing circuitry should be added to allow the MCU to switch between communicating with the onboard EEPROM and an external unit. However, this idea was quickly discarded since SPI is a bus protocol and therefore essentially already contains the functionality that would have been implemented using the MUXing circuitry, albeit implemented in a slightly different fashion.

A further consideration was whether the connection to the external unit should be isolated in some fashion. It was considered unlikely that either the board or the external SPI unit would malfunction in such a way as to damage the device on the other end of the connection but since the SPI protocol allows communication using different voltages such isolation could still be useful as it could be used to allow the external unit to use a different voltage level than the
Due to the bus nature of the SPI interface such isolation would pose a problem since the isolator used on the connection between the output of the external unit and the input of the MCU would need to replicate the high-Z function in order not load the bus and therefore interfere with messages from the EEPROM.

Yet another problem was posed by the difficulties with actually testing the design before construction. Since the software parts of the construction was outside the scope of the project at hand there was no programming framework in place for testing such functions. In addition certain problems are posed with prototyping any design involving devices only available in SM packages. Furthermore the high frequencies involved in many digital communications can cause problems with prototyping since attempting to do so using breadboard might not work due to the non-zero capacitance between the contact strips of the breadboard. Because of the problems with testing the design ahead of construction it was considered prudent to include a “plan B” in the form of jumpers enabling the isolators to be bypassed in case the design were to turn out not to work as expected. In such a case the isolators would need to be removed in the next iteration of the design.

3.5.4 JTAG

A JTAG interface was to be included for programming and debugging of the board. Since the MCU family choosen supported JTAG communication inclusion of such an interface was fairly straightforward and involved few considerations. One thing that did need to be considered was powering the board during programming. In and of itself doing so is as simple as connecting the power supply pin of the JTAG interface to the supply rail used to power the MCU but doing so could potentially cause problems with the board’s internal power supply circuitry. Examination of the reference design and the datasheets for the linear regulators used in the internal power supply circuitry revealed that this was indeed the case since the regulators can be damaged if their outputs are pulled more than 0.3V above the inputs (National Semiconductor, 2007). The datasheet recommends using a Schottky diode to clamp the possible voltage between the ports, such protective diodes had been included in the reference design and the same solution was therefore carried over to the new design.

3.5.5 Converter enable outputs

Outputs were to be included for enabling/disabling individual DC/DC converters included in the system. These connections were straightforward to add since all that was needed was to make suitable output pins of the MCU available on some kind of physical connector. No particular protocol was needed for this function, hence general purpose in/out pins could be used.

3.5.6 PMBus

The board was to include PMBus connections to be used for communicating with the DC/DC converters included in the test setup. The overall requirement

\[1\] It was discovered during the writing of this report that off-the-shelf level translators specifically intended for this task are available, in future iterations of the product it could be considered to use such a device instead.
specification for the 3E GOLD kit demands that boards which are a part of the evaluation kit should be possible to jack together in a daisy chain as illustrated in Figures 1 and 2 of Ericsson (2010). Ideally, a separate PMBus would be used for each connector but practical concerns regarding other communication ports to be included and the number of I²C ports available on the MCU demanded that all such communications be handled by a single PMBus. Due to the bus nature of the PMBus protocol this was considered unproblematic and the main considerations regarding this part therefore ended up being the characteristics of the physical connectors and the pull-up resistors required by the PMBus specification.

3.5.7 Converter sync clocks

The board was to make two synchronisation signals – a high-speed one and a low-speed one created from the high-speed one by clock division – available to the DC/DC converters on the PMBus connector. It ought to be noted that these signals are not part of the PMBus standard but have been put on the PMBus connector for practical reasons. Each signal output could be expected to feed multiple inputs which could potentially present a large load to the output, the signals were therefore to be buffered. A suitable buffer was included in the reference design and the solution used there was carried over to the new design.

3.5.8 AVS (Automatic Voltage Scaling)

The board was to include AVS connectivity to be used for fine-tuning the output voltages of the DC/DC converters in the test setup, the communication to take place for this purpose was to be done through an SMBus connection. The precise details of these communications were considered outside the scope of the project and therefore only such features as required by the SMBus protocol were added in addition to a physical connector.

3.5.9 RS232

The board was required to include RS232 connectivity for communication with an external device. This presented a problem since the functional parts of the board were to powered from a 3.3V supply while the RS232 specification requires that dual voltages be used. In the reference design this had been solved through the use of an off-the-shelf RS232 transceiver – the Maxim MAX3226 – containing a charge pump enabling it to use 12V signaling despite being powered by a lower supply voltage, this solution was carried over to the new design.

3.5.10 UART

The board was to include two UART ports of which one should be isolated. Providing connectivity for the non-isolated UART was straightforward as it only involved connecting the relevant MCU pins to a suitable connector, making the type of connector and the pinout to be used the only concerns. Providing isolated connectivity was a bit more complicated as a suitable isolator had to be chosen. Inspection of the reference design revealed that a suitable solution – based around the Texas Instruments ISO7221 digital isolator – already existed there, this solution was therefore carried over to the new design.
3.5.11 Sense inputs

An important part of the functionality required in the board was the capability of monitoring the output voltages of the DC/DC converters included in the test setup. For this reason a number of sense inputs connected to ADC inputs on the MCU were to be included. Each input was to be equipped with a resistive voltage divider to scale the input voltage to a level suitable for the ADC, inputs for a number of different voltage ranges were to be provided to allow for measuring large signals without overflows while still being able to measure smaller signals with reasonable accuracy. A total of 12 inputs were to be provided with 8 of these having an allowable voltage range of 0V-3.6V, two having an allowable range of 0V-6V and two having an allowable range of 0V-17V. Furthermore, each input was to be equipped with a filter in order to reduce problems with noise on the input signals. The reference design contained suitable input conditioning circuitry which was carried over to the new design.

3.5.12 General purpose I/O (GPIO)

A number of general purpose in/out pins were to be included, these were to use any pins left over on the MCU and connectivity were to be provided by simply connecting the pins to headers.

3.5.13 Reset button

A manual reset button was to be included. A suitable scheme for including such a button already existed in the reference design and was therefore carried over to the new design.

3.5.14 Bootloader select jumpers

Jumper pins were to be included for selecting between different bootloaders. A suitable solution for this functionality already existed in the reference design and was therefore carried over to the new design.

3.6 Design of the test logic

The board was to include a number of diodes with one pin made available through a suitable connector to enable a user to quickly and easily set up various tests. It was decided that each diode should be buffered in order to minimise the load on the connected points, a suitable IC array of darlington-coupled transistors was found which was used for the buffering. Additional resistors were used at the base and the collectors of each darlington pair to set the characteristics of the buffers. Since the brightness levels corresponding to turn-on and turn-off of an LED can be rather subjective suitable values for the resistors are planned to be determined by experiment\(^2\) rather than through calculation. Because components have not yet been ordered at the time of writing this experiment has yet to be performed.

\(^2\)The planned experiment is rather straightforward and would simply involve assembling one stage of the test logic design on a breadboard and using trimpots to determine appropriate values for the resistors needed. Since surface mount diodes are to be used in the final design wires will have to be soldered to one of these in order to make it possible to connect it to the breadboard.
3.7 Considerations for a physical realisation

Carrying a design over to a physical realisation always presents certain difficulties as there are many considerations affecting the choice and placement of components. In the present case it was desirable to – wherever at all possible – restrict the choice of components to ones already present in Ericsson’s database systems in order to ensure that supplier deals existed for the components used. A further general design goal was to keep the number of component types as small as possible to simplify the logistics of keeping components in stock. As the board was intended to be soldered by hand, it was decided that 0603-sized components should be used to keep the involved components reasonably small while still keeping manual assembly feasible. Some considerations regarding the tolerances of certain components were also necessary since the values of these were critical and could not be allowed to vary too much from their nominal ones. Other components could be expected to be subjected to voltages and currents large enough that some attention needed be paid to their ratings when choosing them.

In some parts of the circuitry there were doubts whether a certain component should be included or not. In the case of some such components “dummy components” were included – i.e. components with somewhat unusual values (e.g. 0Ω for a resistor) were placed in the schematic – to ensure that paths for mounting these components were included in the PCB.

3.8 Physical design

In accordance with Ericsson practices the physical layout of the PCB was not carried out by the author but rather by an employee specialising in this type of design. Even so the author had some involvement in the process since the PCB designer needed to be provided with information about such as things as desired footprints and the intended placement of certain components (e.g. decoupling capacitors). Many of the problems in carrying over the abstract electrical design to a physical one were encountered at this stage, necessitating an ongoing dialogue between the author and the PCB designer.
4 Results

What is given below is an overview of the circuits resulting from the design process. It should be noted that the presentation has been kept conceptual in nature wherever possible to make it easier to follow by avoiding cluttering it with unnecessary details. For the precise details of the implementation see Ericsson (2011b). No information on pin numbers have been given for connectors in the schematics below and in addition, unused pins have generally not been shown. Details regarding pin numbers and the amount of pins actually included on each connector can be found in appendix A.

4.1 Power supply

4.1.1 Polarity protection

Polarity protection has been implemented by simply including a diode at the input for the mains supply voltage, this solution was adapted from one used in Ericsson (2011c).

4.1.2 Conversion from -48V to 5V

Figure 4: Schematic of the -48V to 5V-conversion circuitry, the design shown here has been adapted from the reference design (Ericsson, 2009a) and the application notes for the NCP1030 (ON Semiconductor, 2010). Note that the two different ground symbols used denotes different grounds. Due to the negative input voltage the conversion circuitry treats the $-48V$ rail as ground and this ground has been drawn using the triangular ground symbol otherwise often used to represent signal ground. The actual ground – i.e. the 0V line – used both externally and by the rest of the circuitry has been drawn using the usual three-lines ground symbol.

A general outline of the circuitry performing the -48V to 5V conversion is shown in Figure 4, it closely follows the application notes for the NCP1030 (ON Semiconductor, 2010). The circuit implements a switching power supply of the...
flyback type with the IC providing most of the functions needed for the implementation.

The NCP1030 contains an internal MOSFET – connected between the drain (\(V_{\text{DRAIN}}\)) pin and the ground (\(GND\)) pin – which performs the switching. This enables the pulse wave thus produced to drive a transformer by connecting the transformer’s primary winding between the positive input of the main supply voltage and the drain pin (of the controller IC) while connecting the ground pin to the ground input (ON Semiconductor, 2010). It should be noted that in the present design the ground pin has been connected to the \(-48\) V input while the drain pin has been connected to the input ground, this has been done because the mains supply voltage is a negative rather than a positive one.

The switching speed is set by the user by connecting a capacitor of a suitable value between the oscillator frequency selection (\(C_T\)) pin and ground, referring to Figure 18 in ON Semiconductor (2010) for choosing the value. In the present design the timing capacitor has been chosen to provide a switching speed of about 700 kHz since the transformer used is intended to be used at this frequency (Ericsson, 2009b).

Regulation of the duty cycle is performed by an internal error amplifier which compares the voltage on the feedback (\(V_{\text{FB}}\)) pin to an internally generated 2.5V reference. This enables the output voltage to be set using a simple resistor divider configured so that it provides an output of 2.5V at the desired output voltage (ON Semiconductor, 2010). The IC provides a compensation (\(\text{COMP}\)) pin which is connected to the output of the error amplifier, thus enabling the user to set the desired frequency compensation by connecting a suitable low-pass filter network between the \(BP\) pin and the \(V_{\text{FB}}\) pin (ibid). According to the datasheet the frequency response of the error amplifier should cross 0 dB below 80 kHz to ensure normal operation (ibid).

The IC also includes over- and undervoltage protection which can be used to shut down switching if an over- or undervoltage should be present on the supply rail. These are implemented through comparators with hysteresis which compare the voltage on the input pins (\(OV\) and \(UV\)) to an internally generated 2.5V reference, allowing the user to set the threshold values by employing suitably designed resistor divider networks. The datasheet recommends that the inputs be bypassed with capacitors to prevent accidental triggering caused by the switching. (ibid)

Powering an IC like the NCP1030 presents a chicken-and-egg-like problem since a suitable voltage for powering the IC might not be available until the IC itself has created one. The NCP1030 solves this problem by providing a boot-strap mechanism which draws a current from the the mains supply rail and sinks it into an external capacitor which must be supplied by the user and which should be connected to the \(V_{\text{CC}}\) pin. Once the voltage over this capacitor has become high enough the IC can use it to start switching. Once switching has started power should be provided by an auxiliary transformer winding in order to avoid connecting the load in parallel with the startup capacitor which could potentially interfere with the startup circuitry by causing the voltage over the capacitor to go low enough to drive the IC into startup mode. (ibid)

In the present design the auxiliary winding is also used for regulation which has the advantage of providing galvanic isolation between the input and the output of the power supply while on the other hand having the disadvantage of potentially making regulation less precise since regulation in this case must
be done assuming that the voltages in the main secondary and the auxiliary windings are proportional. It ought to be mentioned that the isolation achieved in this manner is ruined later on in the circuit as indicated below in section 4.2.10. It should also be emphasised that the present arrangement causes all voltages in the circuit to be referenced to the ground of the mains supply rails rather than allowing them to float freely, meaning that the isolation is not quite complete in the first place.

Due to the inductive nature of the transformer windings large reverse-voltages can be caused across the transformer primary winding when the switch transitions from the on- to the off-state. In order to protect the circuit a snubber network can be included as is suggested in the datasheet (ibid), this network – if present – will provide a path for a reverse voltage to dissipate. In the present design dummy components have been included for the snubber network to ensure that paths for including one is present in the PCB design but with the plan being to initially not mount any of the components. This will effectively exclude the snubber network while still allowing it to be added later on should the need arise.

A rough estimate of the output filtering frequency was calculated using the simple model described in section 2.1.2. The datasheet for the transformer (Ericsson, 2009b) gives no value for the inductance of the secondary windings but states a nominal value of $57\mu\text{H}$ for the primary winding. Assuming that winding inductances are proportional to the number of turns, the turns ratios of the transformer gives a value of about $12\mu\text{H}$ for the main secondary winding. The capacitor value is determined by a component and can therefore be chosen at will (subject to the usual constraints regarding such things as physical size). The capacitance was chosen to be the same value as the one used in the reference design, this value should give an $\omega_c$ of about 112 kHz.

### 4.1.3 Conversion from 5V to 3.3V

**Figure 5:** Schematic of the 5V to 3.3V-conversion circuitry. The design shown here has been adapted from the reference design (Ericsson, 2009a) and the application notes for the LP2985 (National Semiconductor, 2007).

The circuitry used for conversion from the 5V intermediate supply voltage to the 3.3V supply used by the main circuitry is outlined in Figure 5. It should be noted that while only one stage is shown two were actually included as mentioned below in section 4.2.1, since the two stages are identical there would be
little point in showing both. The circuitry employs the National Semiconductor LP2985 linear regulator connected in the manner recommended by its data sheet (National Semiconductor, 2007). The LP2985 provides an enable (ON/OFF) pin which should be set high by connecting it to the input voltage rail if the function is not to be used (ibid), this has been done in the present design. In order to ensure stability bypass capacitors of certain minimum values must be connected between the input (VIN) pin and ground, the output (VOUT) pin and ground and the bypass (BPIN) pin and ground (ibid).

4.1.4 Generation of a 3V reference voltage

The circuitry used for generating the 3V reference voltage is outlined in Figure 6, it is made fairly straightforward by the use of an off-the-shelf voltage reference. The datasheet for the IC (Maxim, 2003) provides an application note in which the two output pins (OUTF and OUTS) are tied together and mandates that a capacitor with a value between 0.1 µF and 10 µF be added between these two pins and ground It also recommends that capacitors be added between the supply rail and ground. The IC provides a noise reduction (NR) pin, bypassing this pin to ground with a capacitor of 0.1 µF reduces output noise (ibid).
4.1.5 Generation of sense voltages

![Diagram of sense voltage-generating circuitry](image)

**Figure 7:** Conceptual overview of the sense voltage-generating circuitry. The design shown here has been adapted from the reference design (Ericsson, 2009a).

A conceptual overview of the circuitry responsible for generating the sense voltages is presented in Figure 7, for more details see Ericsson (2011b). The basic principle is that the resistor divider between the input voltage and the 4.5V reference voltage is used to create a signal voltage that has been scaled to a suitable level. This signal voltage is then buffered before being fed to other parts of the circuit. In the physical circuit the 4.5V reference voltage is generated by connecting the 3V reference voltage to the input of a non-inverting op-amp stage using a 1:2 ratio between the feedback and ground resistors, thus yielding a gain of 1.5 which produces an output of 4.5V. Precision resistors with 0.1% tolerance are used to ensure that the generated voltage is very close to the nominal value. The two buffers are implemented using voltage follower-connected op-amps with clamping diodes at the input nodes to ensure that the differential amplifiers at the op-amp inputs are not exposed to high differential voltages in case of spikes on the mains supply voltage rails.

It ought to be noted that this arrangement ruins the galvanic isolation between the mains power supply rail and the rest of circuit that was achieved by using a transformer in the -48V to 5V conversion.

4.2 Main circuit

4.2.1 Microcontroller

In the reference design an MCU from the ST Microelectronics STM32F105xx family was used. It was eventually decided that a somewhat broader part of the family – corresponding to numbers of the form STM32F10xxx – could be used. It was further decided that an LQFP100 package should be used for the microcontroller in order to ensure that an adequate amount of pins is available, this restricts the choice of a particular device to the STM32F10xVx part of the family.
A conceptual overview of the MCU connections is given in Figure 8. $D_3$ and $D_4$ were included for general purposes, the idea being that their inclusion should make it simpler for a user to perform basic tests regarding such things as whether programming of the device works as intended. $D_1$ and $D_2$ are intended to be used for indicating problems on the -48V mains rail and the 3.3V internal (to the board) supply rail.

The datasheet (ST Microelectronics, 2010) for the STM32 family mandates that certain pins be bypassed to ground, these capacitors used for this have been included in the figure above (note that there are five 100nF capacitors in the actual circuit). Generally, these capacitors should be placed physically close to the pins between which they are connected. The capacitors connected between the VDD-ins and the VSS-pins should be evenly distributed between the pin pairs, i.e. there should be one capacitor between VDD1 and VSS1, one between VDD2 and VSS2 and so on (ibid). A special case is the 4.7µF capacitor which should be placed between VDD3 and VSS3 (ibid). To ensure that all analog voltages used by the MCU are reasonably noise-free, the total capacitance
used for bypassing the analog supply voltage pin (VDDA) is larger than what is recommended by the datasheet (ibid) and furthermore an EMI filter (represented by $L_1$ in the schematic above) has been added. A decoupling capacitor is also present between $V_{REF+}$ and $V_{REF-}$ which are the pins used for providing the ADC with a reference voltage (ibid).

The datasheet for the MCU family specifies a maximum current draw of 150mA (ibid) which is precisely what the linear regulators used will deliver at most (National Semiconductor, 2007). For this reason, two linear regulators have been included in the design: a main one dedicated to the MCU and an auxiliary one used for the rest of the circuitry.

All other connections are described below.

4.2.2 EEPROM

![Schematic of the EEPROM connections](image)

Figure 9: Schematic of the EEPROM connections. The design shown here has been adapted from the reference design (Ericsson, 2009a) and the application notes for the Atmel EEPROM (Atmel, 2007).

It was eventually decided that the EEPROM should be taken from either the Atmel AT25xxxx family, the ISSI IS25Cxxx family or the ST Microelectronics M95xxx family. All these families are compatible regarding pins as well as functionality and between them they offer a wide range of available memory sizes (ISSI, 2003; Atmel, 2007 and ST Microelectronics 2008), they are also preferred Ericsson components listed under product number 1301 - RYT 118 6058.

Memory connections are shown in Figure 9. The memory IC:s in the aforementioned families provide write protect (WP) and hold (HOLD) pins which can which can be used to disable writing to the memory and to suspend serial communications, respectively. Both of these pins are inverting and therefore need to pulled high in order to make it possible to communicate with and write to the memory. In the present design the functions will not be used and these pins have therefore been permanently connected to the 3.3V supply rail through a series resistor which effectively disables the associated functions. (Atmel, 2007)

The SPI bus and power supply connections are fairly self-evident and should require little explanation except to mention that the slave select pin was connected to a general in/out pin on the MCU rather than to a pin specifically as-
associated with SPI communication. The slave select function simply needs to pulled low before any communication takes place (ibid), hence no special pin is needed.

It should also be mentioned that the memory chip takes its power supply from the auxiliary rail with the result that it and the MCU are connected to two different voltage sources. Both of these sources deliver the same nominal voltage but in practice it is likely that their output voltages will differ somewhat, something which could potentially cause problems with currents going between the pins on the MCU and the associated pins on the memory IC. This is unlikely to happen as digital in/out pins will generally present a high resistance to connected elements but even so series dummy resistors have been added to the design to make sure that the PCB includes paths for current-limiting resistors in case they turn out to be needed.

A pull-up resistor has been placed between the slave select (SS) pin and the auxiliary 3.3V rail, this is not required by the SPI protocol but was done in the reference design and was considered good practice.

4.2.3 SPI

![Schematic of the SPI connector arrangement](image-url)

Figure 10: Schematic of the SPI connector arrangement, the parts illustrating the internal configurations of the isolators have been adapted from Avago (2010). Note that the rather low isolation voltage of 150V RMS presented here is the (sustained) working isolation voltage, the isolator family used provides isolation of transients voltages of up to 2500V (ibid). The actual design includes decoupling capacitors connected between each pair of supply pins (i.e. there are a total of four decoupling capacitors: one for each side of each of the isolators) but are not shown here to avoid cluttering the figure. Parts of the design have been adapted from the datasheet for the isolators (Avago, 2010).
The design for the external SPI connectivity is outlined in Figure 10. It was eventually decided that isolators for the SPI bus should be included to allow the external device to use a different signaling voltage compared to the one used by the MCU. The isolators used for this purpose were taken from the Avago Technologies HCPL-0xxx family. The isolator used for the MISO line provides the possibility to set its output in high-Z mode via the output enable (OE) pin (Avago, 2010), in order not to break the isolation barrier this function is controlled from the MCU via the slave selection line in such a way that the isolator output is in high-Z mode whenever the external unit has not been selected. It ought to be noted that this setup requires that the MCU is the master in any communication with an external SPI unit.

As mentioned in section 3.5.3 it was not practical to test the design ahead of construction and jumpers were therefore included to allow for bypassing the isolators in case this part of the design turns out not to work as intended.

### 4.2.4 JTAG

An outline of the connections used for the JTAG interface is shown in Figure 11. Small resistors have been included on the communication lines in order to alleviate possible problems with noise. A buffer – the Fairchild Semiconductor™ NC7SV34P5X which was also used in the reference design – has been included on the clock wire to ensure that a good-quality clock signal is received by the MCU even if the JTAG connector is connected to several places.

---

3Early on in the process it was thought that the chosen isolator would provide a high enough isolation voltage to be useful for providing meaningful galvanical isolation as well. More careful inspection of the datasheet has revealed that it’s not quite clear whether this is the case since an isolation value of 2500V RMS is given for transient voltages but no value seems to be given for the time during which such a high voltage would be acceptable.
4.2.5 Converter enable outputs

The converter enable outputs are simply connected to headers to make them available to external devices.

4.2.6 PMBus & PWM clocks

![Schematic of the PMBus and PWM clock connector arrangement. The design shown here has been adapted from the reference design (Ericsson, 2009a).](image)

Most of the PMBus connections are fairly straightforward and simply makes the relevant MCU pins available to external devices by connecting them to header pins while including the pull-up resistors required by the protocol. Two clock-sources – both taken from the MCU – are available and separate jumper pins for choosing either one have been included for each of the PMBus connectors. As mentioned in section , these clocks are to be used for synchronising the operation of DC/DC converters within a test setup. The clock outputs can be expected to be connected to several inputs simultaneously which might present a large load to the clock sources, the clock signals have therefore been buffered using the Fairchild Semiconductor™ NC7SV34P5X which was also used in the reference design.
4.2.7 AVS (Automatic Voltage Scaling)

![Schematic of the AVS connector arrangement.](image)

The connections for the AVS function is shown in Figure 13. The connections simply make the relevant pins on the MCU available to external devices by connecting them to a header. Since the AVS is to be implemented using the SMBus protocol the pull-up resistors required by this protocol have been added.

4.2.8 RS232

![Schematic of the RS232 connector arrangement.](image)

The RS232 connections are shown in Figure 14. As mentioned in section 3.5.9 an off-the-shelf RS232 – the Maxim MAX3226 – transceiver is included to allow...
true RS232 communication despite operating from a 3.3V power supply. The MAX3226 uses two internal charge pumps – one producing a 5.5V voltage and one producing a −5.5V voltage – to achieve this (Maxim, 2011). Two 0.1µF-capacitors are connected between the C1+/C1- pins and the C2+/C2- pins as specified in the datasheet (ibid), these provide the capacitances needed by the charge pumps. The voltages generated by the charge pumps are made available on the V+ (V+) and V− (V−) pins, these voltages are not used by any other circuitry in the present design but the pins have been bypassed to ground as recommended by the datasheet (ibid). The power supply input (VCC) is also bypassed in this manner.

The transceiver provides a number of pins which can be used to control it’s operation. The force on FON and force off FOFF pins can – as their names imply – be used to override the internal shutdown function of the IC (ibid). In the present design normal operation is desired and FON has therefore been connected to ground (through a series resistor) while FOFF has been connected to the 3.3V power supply rail as per Table 1 in the device datasheet (ibid; in order not to cause any confusion it should be emphasised that the FOFF pin is inverting, hence connecting it to the supply rail will disable the force off function). The INVAL pin is indicates whether there are valid RS232 voltage levels on the transceiver inputs (ibid), it is not used in the present design and has not been connected at all. The ready (RDY) pin which indicates whether the transceiver is ready to transmit (ibid) has likewise not been connected since it is not used either.

Communication is relayed between the T1IN/T1OUT and the R1IN/R1OUT pins (ibid), one end of the communication channels thus formed has been connected to the MCU while the other is connected to a header to provide physical connectivity to external devices. It should be noted that the communication channels are inverting (ibid).
4.2.9 UART

Figure 15: Schematic of the UART connectors arrangement. The design shown here has been adapted from the reference design (Ericsson, 2009a) and the application notes for the isolator (Texas Instruments, 2010), the parts illustrating the internal configuration of the IC has been adapted from Texas Instruments (2010).

The UART connections are shown in Figure 15. The external side of the isolator is connected so that it will be powered by the external device when one is present as recommended by the datasheet (Texas Instruments, 2010). This needs to be done in order for isolation to be achieved as an external device connected to the board via the header would otherwise be galvanically connected to the other circuitry in the board through the power supply rails. The power supply pins have been bypassed to ground on both sides of the isolator as recommended by the datasheet (ibid).

4.2.10 Sense inputs

Figure 16: Schematic of the sense inputs filtering circuitry, note that the exact component values differ between different inputs. The design shown here has been adapted from the reference design (Ericsson, 2009a).
As mentioned in section 3.5.11 the sense inputs are required to perform two tasks: scaling the input voltage down to a level suitable for feeding to the ADC and filtering out disturbances on the line. The basic form of the circuitry providing these functions for each input is shown in Figure 16. It is easily seen that this circuitry implements a low-pass filter with some DC attenuation, something which can be verified by simulation or by deriving (the derivation is trivial and has therefore been excluded) and plotting the transfer function:

$$H(s) = \frac{R_2}{sR_1R_2C + R_1 + R_2}.$$

This circuitry is replicated once for each input with some variations in the component values to provide the desired variety of input voltage ranges. Both the resistor and capacitor values have been chosen in accordance with values given in the reference design. The resistor values chosen ensure that the output voltage of the filter/attenuator circuits is close to (and not greater than) 3V for a DC input voltage of the maximum allowable value. The capacitor values give a break frequency of about 100 kHz.

Apart from the external inputs there are also three internal ones. Two of these are used for the two sense voltages generated by the circuitry described in section and one is used to monitor the main 3.3V internal supply rail.

4.2.11 General purpose I/O (GPIO)

After all other connections had been added, the remaining MCU pins were connected to headers to provide for the required general purpose in/out pins.

4.2.12 Reset button

A manual reset button has been included. One end of the button switch is connected to the MCU:s reset pin and the other end to ground, thus pushing the button will pull the reset pin down to ground which will reset the MCU. A bypass capacitor has been placed between the two ends of the switch to inhibit switching transients. It should be noted that the MCU reset pin is also connected to a pin on the JTAG connector which makes it possible to use the pull-up resistor shown in Figure 11 for both of the reset functions.
4.2.13 Bootloader select jumpers

Circuitry has been included which enables the user to choose which bootloader to use by placing jumpers, this circuitry is illustrated in Figure 17. Placing a jumper will simply set one of the two bootloader select pins on the MCU to a logical 0 or 1, it will also light a LED to indicate which bootloader has been selected.

4.3 Test logic

Figure 18: Schematic of the test logic connections, the parts showing the internal connections of the ULN2803A have been adapted from Texas Instruments (2006). Note that while only one stage is shown in the figure eight identical stages are included in the actual design.
The design for the test logic stages are shown in Figure 18, although only one stage is shown in the figure eight such stages are included the actual design. Each stage provides a buffered LED with the input of the buffer made available on a header. The darlington buffers shown are implemented using the Texas Instruments ULN2803A (Texas Instruments, 2006) darlington array IC.

4.4 Considerations for the physical design

In the conceptual schematics shown above all parts of the main circuits have been shown being connected to a single ground. In practice this is not a good solution since the fast switching of the digital signals can cause considerable interference to be present at such a ground. Therefore the practical design uses separate grounds – intended to be implemented in the form of separate ground planes on the PCB – for the digital and the analog parts. In the schematics presented above the ground used for each part of the circuit has been indicated with DGND for the digital ground and SGND for the analog (or signal, hence the S) ground. In addition a ground called 0V has been used in the power supply parts of the circuitry to denote the power ground. The digital ground and the signal ground are both connected to the power ground in star-ground fashion. It should be noted that bubble connectors have been used for the ground points in some of the schematics.
5 Discussion

At the time of the writing of this report the layout work has not yet been finished and therefore no physical board yet exists, the discussion will therefore have to be limited to the abstract electrical design and the process leading to it.

A first conclusion which can be made is that the size of the project rather than any of the specific details has been the main hurdle. While many of the individual subparts of the construction have been fairly simple in and of themselves the number of subparts involved has created some difficulties in managing them. While the project at hand has been large enough to cause such problems it ought to be noted that it is hardly a very large project compared to what one can expect to see in many parts of the industry. Seeing how even a comparably small project – mainly carried out by one person – such as this one can quickly cause problems regarding manageability one conclusion which can be drawn regards the utmost importance of structuring a project in a sensible manner. To this end, it has been invaluable to treat the design as a number of smaller subcircuits, each of which is required to perform a well defined task. Furthermore it has been of great value to group these subcircuits in a sensible manner and to create a numbering system to aid in locating exactly where in the design a certain component can be found. This numbering system was found to be of particular value in discussing the design since it meant that a component could be located with reasonable speed when it was referred to in a conversation.

During the course of the project many ideas were considered but discarded since they were considered to be outside the scope of the current task. One such idea which might be worthy of mention is the one of including some means of bluetooth communication on the board. Since most modern handheld devices are capable of bluetooth communication this would allow the board to communicate with such devices thus making it possible to allow at least basic configuration and monitoring to be done using handheld devices. While such functionality would not be essential to the board it could nevertheless be convenient for its users. It would not be strictly necessary to build such functionality into the board proper in order to provide it, since the board includes a range of communication interfaces it could be instead be provided in the form of a dedicated expansion board which could likely be made small enough to simply mount on the associated header.

Some further ideas arose due to discoveries and insights gained during the design work. As mentioned in a footnote to section 3.5.3 it was discovered that the solution used to achieve level translation for the SPI interface might not be the most elegant one since there exists ICs designed especially for this purpose. In future iterations of the design it should be considered whether to exchange the solution now used for one based on such ICs, for example one of those described in Maxim (2002).
References


Appendices

A Pin numbers

A.1 SPI

![SPI Connector Diagram]

Figure 19: Pinout for the SPI connector.

A.2 JTAG

![JTAG Connector Diagram]

Figure 20: Pinout for the JTAG connector.
A.3 PMBus

Figure 21: Pinout for the PMBus connector.

A.4 AVS

Figure 22: Pinout for the AVS connector.
A.5 RS232

1: RX
2: TX
3: Ground
4: Not connected
5: Not connected
6: Not connected

Figure 23: Pinout for the RS232 connector.

A.6 UART

1: VCC
2: GND
3: RX
4: TX
5: Not connected
6: Not connected

Figure 24: Pinout for the UART connector.

B Numbering of schematic pages

- The root schematic only contains a single page – given the number 01 – which shows the overall structure of the design. If further pages were to be added these should be given numbers of the form 0x.

- Numbers of the form 1x have been used for pages belonging to the power supply schematic, the precise page numbering is as follows:
  - 11: Initial conversion from -48V to 5V
  - 12: Conversion from 5V to 3.3V
  - 13: Generation of the 3V reference voltage
- 14: Generation of the sense voltages

- Numbers of the form 2x have been used for pages belonging to the schematic for the main circuit, the precise page numbering is as follows:
  - 21: MCU connections.
  - 22: EEPROM and external SPI connectivity
  - 23: Converter enable outputs
  - 24: Spare I/O
  - 25: JTAG connectivity
  - 26: PMBus and AVS connectivity
  - 27: RS232 connectivity
  - 28: Sense inputs
  - 29: UART connectivity

- The test logic schematic only contains a single page – given the number 31 – which shows the configuration used for the test logic diodes and the associated buffers. If further pages were to be added these should be given numbers of the form 3x.