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Phase Noise Improvement and Noise Modeling of Type-I ADPLL with Non-Linear Quantization Effects

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Abstract—**This paper presents a phase noise improvement method for fine tuning of type-I ADPLL by exploiting its non-linear quantization effects. When quantization step approaches the same orders of magnitude of standard deviation of input noise, quantization effects become nonlinear, and additive noise modeling of quantization effects is no longer applicable. By proper offsetting the input signals in this case, the feedback loop of ADPLL can be very sensitive to frequency phase deviation. It results in a larger loop bandwidth, and in turn smaller in-band phase noise than in linear quantization case. A theoretic s-domain noise model is proposed to quantify the phase noise in nonlinear case. Results are verified in Modelsim simulations. Proposed method offers possibility of achieving lower phase noise by lower quantization resolution and less circuit design efforts.**

Keywords—ADPLL; Quantization; Nonlinear; Noise Model

I. INTRODUCTION

With technology advances in CMOS process, it is more superior to utilize time-domain resolution of a digital signal edge transition than voltage resolution of analog signals due to higher transistor speed and lower supply voltage. Therefore, all digital implementation of phase-locked loop (ADPLL) illustrated in Fig. 1 has been intensively researched in recent years [1-2]. However, one of the most significant problems in ADPLL is quantization noise, due to the limited resolution in time delay detection by time-to-digital converter (TDC) and in frequency tuning by digital-controlled oscillator (DCO) [3-5]. With intensive study of sigma-delta modulation in ADPLL, quantization noise from DCO has been largely reduced [1-3]. Therefore, quantization noise from TDC has been the dominant effect for phase noise of state-of-art ADPLL [6-7]. In phase noise model, most of current researches model the quantization noise as additive white noise source [1,4-5], based on the primitive that input noise is so higher than quantization steps that it is irrelevant to input signal. However, such condition is not intuitively applicable in ADPLL. Because, additive noise is often small in PLLs of interest and phase error is small and the control signal to the DCO is largely quiescent when the loop is locked [8-9], especially for PLLs optimized with sigma-delta modulation. Thus, this paper proposes a new noise model for type-I ADPLL quantization effect in non-linear cases, and makes use of it for phase noise improvement by increasing quantization step to approach the orders of magnitude of standard deviation (std) of input noise.
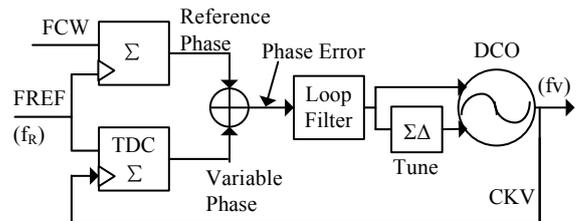

Fig.1. Block diagram of ADPLL structure.

Since zero offset of averaged phase error is a necessary premise to trigger the proposed method, it targets applications in ADPLL fine tuning stage. Remaining sections of the paper is organized as follows: section II introduces nonlinear quantization impact on ADPLL phase noise and the condition to trigger the nonlinear effects in Matlab. Section III proposes a new noise transfer model for nonlinear quantization case. Section IV demonstrates the verification of nonlinear effects and noise model by Verilog-HDL description in Modelsim.

II. NONLINEAR QUANTIZATION EFFECTS

As shown in Fig. 2, a quantizer replaces the additive white noise source in conventional linear phase domain noise model of ADPLL to represent quantization behavior of TDC, and phase error is intentionally shifted by half of quantization step before quantization, and shifted back afterwards. In phase domain, input (quantin) and resolution (quantstep) of quantizer are converted to $\Delta t/T_v$ and Δ/T_v, where Δt is DCO period deviation, Δ is TDC resolution, and T_v is DCO period.

A. Linear Case – Quantization Error Shows Uniform Probability Distribution; Phase Noise Fits Linear Theory.

In linear cases when input noise was much bigger than quantization step, additive white noise model was applicable as verified by quantized phase error, probability distribution (PD) and phase noise illustrated in Fig. 3. In-band power
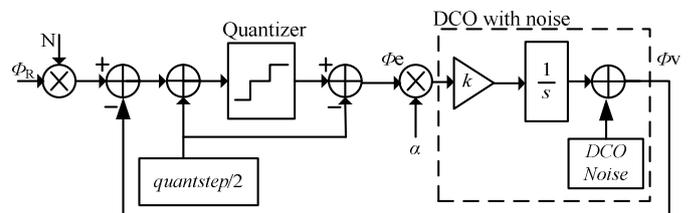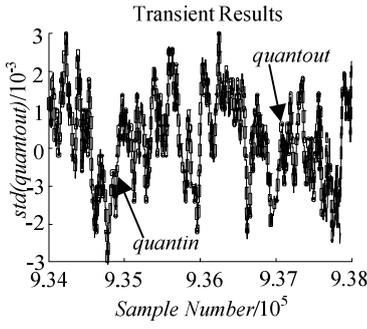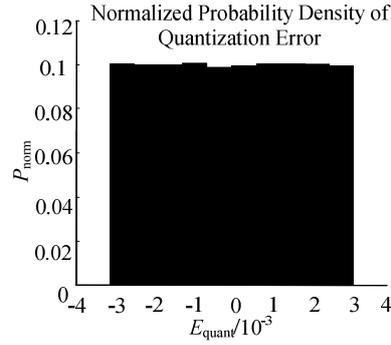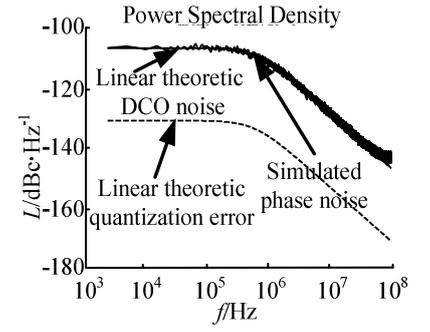

Fig.2. Phase-domain model of ADPLL with noise sources.

(a) Transient results of quantizer input and output

(b) Normalized probability distribution of quantization error

(c) Total phase noise and transferred outputs of DCO noise and quantization error.

Fig. 3. ADPLL Quantization Behavior and Phase Noise in Linear Case.

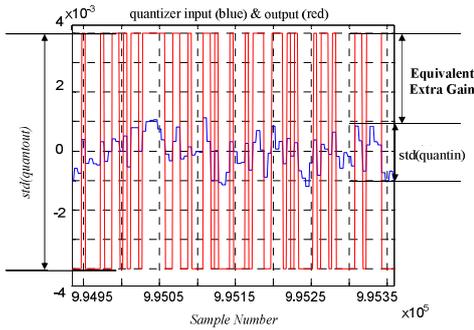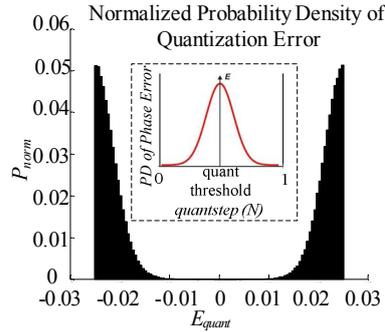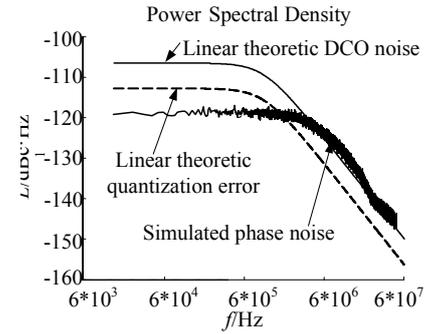(a) Transient results of quantizer input and output

(b) Normalized probability distribution of quantization error

(c) Total phase noise and transferred outputs of DCO noise and quantization error.

Fig. 4. ADPLL quantization behavior and phase noise in non-linear case.

spectral density (PSD) of quantization noise conforms to its theoretic value of $\Delta^2/12f_R$, where f_R is reference frequency.

B. Non-linear Case – Quantization Error Shows 'Canyon-Like' Probability Distribution; Phase Noise can be Lower than Linear Theory.

When quantization step surpassed the std of input noise, PD of quantization error shows 'canyon-like' distribution as illustrated in Fig. 4(b). This can be understood from the PD of phase error in ADPLL locking state as shown in Fig. 4 (c), given the pre-shift of quantstep/2 in Fig. 2. Zero offset of averaged phase error is a necessary condition to trigger this PD. In this case, any deviation from the quantization threshold is detected, and results in transient outputs as shown in Fig. 4(a). It is similar to the loop effects of binary phase detector (BPD) on bang-bang PLL (BBPLL) which detects the lead-lag of two clocks and pushes the phase error trajectory in the opposite direction in consecutive steps [10].

Fig. 4(c) reveals that total phase noise of type-I ADPLL in this case is lower than the theoretic value of linear model. It demonstrates that quantization effect has already affected the loop transfer function and could not be modeled as a single white noise independently added to ADPLL.

The phenomena can be intuitively understood as that since any deviation from the quantization threshold is detected, and compensated with big amplitude output (quantout), the phase

noise is reduced and loop response is speeded up. Fig. 5 and 6 show the in-band noise and bandwidth of phase noise changes versus quantization step increase for three different linear bandwidths (BW$_0$).

The threshold quantization step distinguishing linear and nonlinear cases can be deduced as the same orders of magnitude of std of input noise, because it impacts the PD of quantization error, and hence the relevance of error to input signal. In practical applications, phase noise specification of DCO is offered, thus, a correspondent std of period deviation can be derived by expressions in [1,11]:

$$\text{TH\_quantstep} = (\Delta f)(f_c)^{(-3/2)}10^{(PN/20)} \tag{1}$$

PN is phase noise level in dBc-unit at Δf offset frequency away from center frequency fc. Fig. 6 shows the comparison of theoretic and simulated results, proving its reasonability. From an intuitive understanding, if quantization step further increases to 'extremely' large values, the previous benefits of increased sensitivity to phase error will decrease. Because the compensation is so large that any phase deviation approaching one quantization level will result in quantizer output at the other neighboring quantization level. In other words, the compensation is so big that it already overwhelms the status of phase error by forcing it to periodically toggle between two neighboring quantization levels. In this case, loop loses feedback tuning mechanism and oscillator operates in almost free-running status.
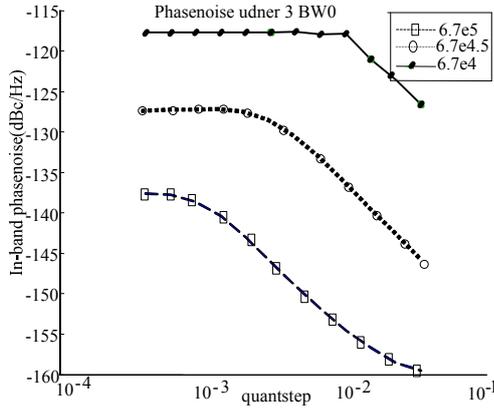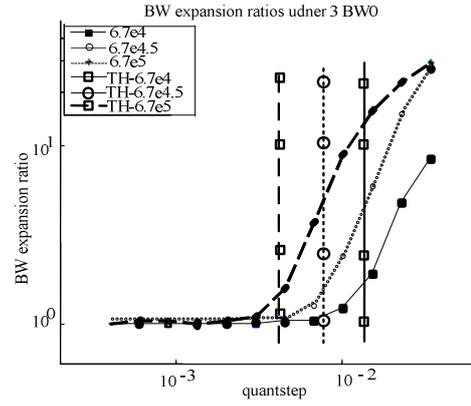
Fig.5. Inband phase noise VS quantstep @ 3 BW$_0$.

Fig.6. BW expansion ratio VS quantstep @ 3 BW$_0$.

III. S-DOMAIN NOISE MODEL FOR NONLINEAR EFFECTS

In non-linear cases, it becomes much more complicated to model the quantization effect than in linear cases. Thus we present an approximated yet practical model for phase noise transfer function. In non-linear cases when quantization step surpasses the standard deviation of quantizer input, the quantizer output toggles between ± *quantstep/2* and has a bigger standard deviation compared to the input as illustrated in Fig. 4(a). This reinforced feedback makes the closed-loop system more active and more sensitive to noise than it is in linear cases. So for type-I ADPLL, this quantization effect can be approximated as a "gain" block whose value is in proportional to the averaged ratio of quantizer output amplitude over input amplitude, similar to the linearized gain factor modeling of BPD in BBPLL [ref]. Thus, the phase domain model with noise source added to a type-I PLL in non-linear cases can be approximated as shown in figure 7.
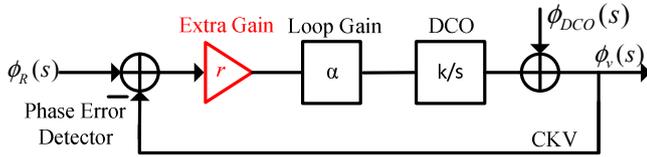

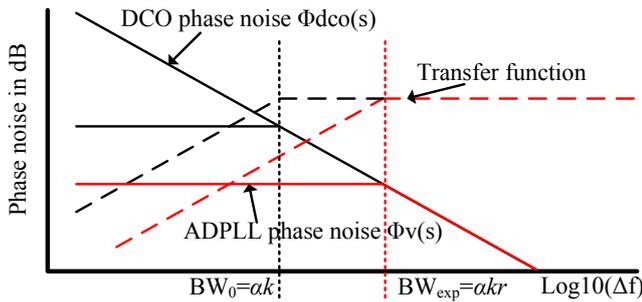Fig.7. ADPLL noise model in nonlinear quantization case.

Fig.8. ADPLL noise transfer function in nonlinear quantization case.

There is only one additive noise source in this model – $\phi_v(s)$ from DCO noise, so phase noise is obtained as $\phi_v(s)$ transferred to the output by closed-loop transfer function:

$$\phi_o(s) = \frac{s}{s + \alpha k \gamma} \phi_v(s) \qquad (2)$$

αk is the same as open-loop gain in linear model, γ is the equivalent extra gain of quantization effect. Expression (2) demonstrates that phase noise of type-I ADPLL in non-linear case can be estimated as DCO noise transferred by a high pass filter with bandwidth of $\alpha k \gamma$. This explains why type-I ADPLL shows bandwidth expansion phenomenon in non-linear cases, and in turn, lower in-band phase noise, as illustrated in Fig. 8.

The extra gain (bandwidth expansion ratio) γ can be approximated with a simple and analytical expression -- dividing the std of output and of input signals. Because quantizer input, i.e. phase error, is a random noise with Gaussian distribution, std can be used to describe the signal powers. So:

$$\gamma = \frac{\text{std(quantout)}}{\text{std(quantin)}} = \frac{quantstep}{2(\Delta f)(f_c)^{(-3/2)}10^{(PN/20)}} \qquad (3)$$

quantout and *quantin* are quantizer output and input signals. $\text{std}(quantout) = quantstep/2$; $\text{std}(quantin)$ can be referred to expression (1).

IV. SIMULATION VERIFICATION AND DISCUSSION

To verify the presented non-linear quantization effect and its noise transfer model of type-I ADPLL, a simulation platform was established by Verilog 2001 behavior model based on Modelsim SE-64 6.5. System parameters are selected to follow the previous values used in Matlab environment: operating frequency (fc) of type-I ADPLL was 2.82GHz, reference frequency was 282MHz, linear bandwidth was 670KHz, and DCO phase noise was -120dBc/Hz @ 1MHz. DCO was described by behavior method based on [11]. Modelsim recorded transition time points of each DCO period, and imported them to Matlab for phase noise calculation.

According to expression (1), ADPLL would operate in non-linear cases when quantization step was selected bigger than approximately 0.002. Fig. 9 demonstrated phase noise in case of TDC=0.04*DCO_period; it exhibited lower phase noise and wider bandwidth compared with phase noise in case of TDC=0.001*DCO_period when quantization step
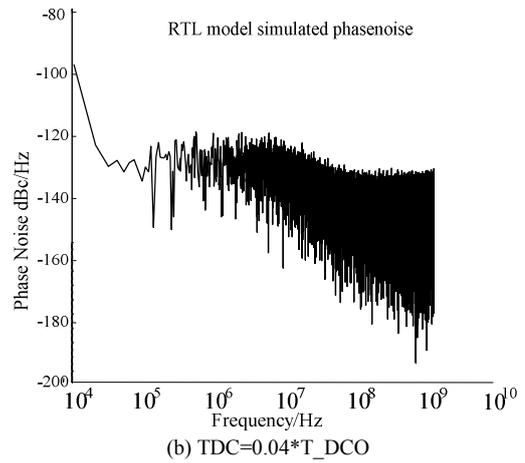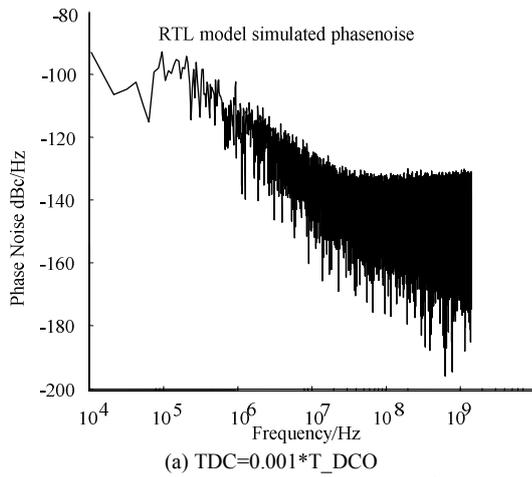
(a) TDC=0.001*T_DCO

(b) TDC=0.04*T_DCO

Fig. 9 Phase noise simulation by Verilog-HDL in Modelsim

was small enough to satisfy linear theory's assumption.

For more overall verification, Fig. 10 demonstrated the estimated bandwidth expansion ratio based on expression (3) and compared with simulation results as quantization step changed. The reason why theoretic extra gain is smaller than simulated one is that in nonlinear case phase noise input to quantizer is already reduced due to a more sensitive feedback control, therefore std(quantin) is smaller than calculation based on phase noise specification in linear case.
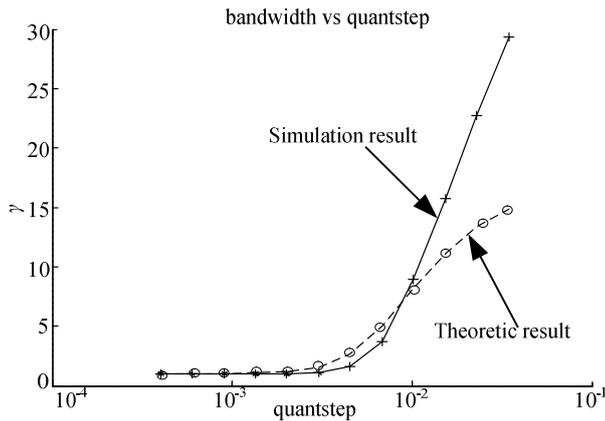

Fig.10. Theoretic and simulated BW expansion ratio VS quantstep.

V. CONCLUSION AND OVERLOOK

Non-linear quantization effect on phase noise and the theoretic noise transfer function model of type-I ADPLL are presented in this paper. When quantization step surpasses a threshold value, conventional model of quantization effect as an additive white noise independent to the system is no longer applicable. The threshold quantization step is derived. New phenomena of bandwidth expansion and phase noise decrease versus quantization step in non-linear cases are presented. An approximating noise model is established to quantitatively explain the nonlinear quantization effects. Subsequent to system analysis in Matlab, above results are further validated by Verilog behavior description in Modelsim. The proposed results provide possibility of achieving lower phase noise by much lower quantization resolution and therefore less circuit

design efforts. As a further step in the future, a complete measurement validation of above results can be realized by replacing DCO in behavior description with CMOS-process implemented DCO. This will improve the current theory and expression when taking into consideration the non-ideal TDC results in actual IC manufacturing.

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