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Electrochemically etched pore arrays in silicon for
X-ray imaging detectors

Doctoral Thesis by

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The picture shown on the cover page is a scanning electron micrograph of an array of tubes formed in silicon by electrochemical etching. The pitch is equal to 3.2 µm.

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ABSTRACT

Digital devices have now been introduced in many X-ray imaging applications, replacing slowly traditional photographic films. These devices are preferred as they offer real time imaging, easy handling and fast treatment of the images. However, the performance of the detectors still have to be improved in order to increase the image quality, and possibly reduce the X-ray dose, a vital parameter for medical use. In this thesis, three different new detector concepts have been investigated. All designs use pore arrays, which are ideal starting structures to form pixellated detectors.

Electrochemical etching of n-type silicon in aqueous hydrofluoric acid solution (HF) has been studied to form these pore arrays. A broad range of pores have been fabricated with diameters varying from 200 nm to 40 μm and with depths reaching almost the wafer thickness, thus leading to very high aspect ratios. The technique was also found to be suitable for the formation of other types of structures such as pillars and tubes on the sub micrometer scale. The etching is based on the dissolution of silicon in HF under anodic bias and a supply of positive electrical carriers (holes). As holes are the minority carriers in n-type silicon, they are usually photo-generated. In this work an alternative technique, based on hole injection from a forward-biased *pn* junction, has been successfully pioneered.

The first X-ray imaging detector concept presented in the thesis consists of a silicon charge coupled device (CCD) in proximity with a scintillating screen. The screen is made from a pore array having reflective pore walls and filled with CsI(Tl), emitting photons at a wavelength of 550 nm under X-ray exposure. The secondary emitted photons are light-guided by the pore walls and then detected by the CCD pixels. Detectors were fully fabricated and characterized. This concept provides good spatial resolution with negligible cross talk between adjacent pixels. The dependences of the detector efficiency on pore depth and on the coating of the pore walls are presented. Although most of the produced detectors had a detective quantum efficiency of about 25%, some detectors indicate that efficient scintillating screens can be achieved approaching the theoretical limit as set by poissonian statistics of the X-ray photons.

The two other detector designs require the formation of vertical *pn* junctions, i.e. in the pore walls. In one concept the secondary emitted photons are detected by photodiodes located in the pore walls. This would lead to high charge collection efficiency as the photons do not have to be guided to one end of the pore. However, high noise due to the direct detection of X-rays in the diodes is expected. The other concept is based on generation of electron-hole pairs in a semiconductor and the '3D' detector, where an array of vertical electrodes is used to separate the charges via an electric field. To uniformly dope the inside of deep pores, both boron diffusion and low-pressure chemical vapor diffusion of boron-doped poly-silicon were shown to be successful techniques. This was confirmed by SIMS profiles taken through the pore wall thickness. Finally, the possibility to form individual junction in each pore was shown. The diodes were electrically characterized, demonstrating good rectifying behavior and sensitivity to light.

CONTENTS

List of publications

Appended papers

1. ***Electrochemical Etching of n-Type Silicon Based on Carrier Injection From a Back Side p-n Junction***
    <u>X. Badel</u>, J. Linnros and P. Kleimann, Electrochemical and Solid State Letters 6, (6) C79-C81 (2003).

2. ***Formation of ordered pore arrays at the nanoscale by electrochemical etching of n-type silicon***
    <u>X. Badel</u>, R.T. Rajendra Kumar, P. Kleimann, J. Linnros, European Material Research Symposium 2004, Superlattices and Microstructures 36, issue 1-3, pp. 245-253 (2004).

3. ***Towards The Formation of 3D Nano-Structures by Electrochemical Etching of Silicon***
    P. Kleimann, <u>X. Badel</u>, J. Linnros, submitted to Applied Physics Letters (in manuscript).

4. ***Improvement of an X-ray imaging detector based on a scintillating guides screen***
    <u>X. Badel</u>, A. Galeckas, J. Linnros, P. Kleimann, C. Fröjdh and C.S. Petersson, Proc. IWORID 2001, Nuclear Instrum. and Meth. In Phys. Res. A 487, pp. 129-135 (2002).

5. ***Metallized and Oxidized Silicon Macropore Arrays Filled With a Scintillator for CCD-based X-ray Imaging Detectors***
    <u>X. Badel</u>, J. Linnros, P. Kleimann, B. Norlin, E. Koskiahde, K. Valpas, S. Nenonen, C.S. Petersson and C. Fröjdh, Nuclear Science Symposium 2003, IEEE proceedings ISBN: 0-7803-8258-7 -- IEEE Transactions on Nuclear Science vol. 51 (3) pp. 1001-1005 (2004).

6. ***Performance of Scintillating Waveguides for CCD-based X-ray Detectors***
    <u>X. Badel</u>, B. Norlin, P. Kleimann, L. Williams, S.J. Moody, G.C. Tyrrell, C. Fröjdh, J. Linnros, submitted to IEEE Transactions on Nuclear Science (in manuscript).

7. ***Formation of pn junctions in deep silicon pores for X-ray imaging detector applications***
    <u>X. Badel</u>, J. Linnros, M.S. Janson and J. Österman, Proc. IWORID 2002, Nuclear Instrum. and Meth. In Phys. Res. A 509, pp. 96-101 (2003).

8. ***Doping of Electrochemically Etched Pore Arrays in n-Type Silicon: Processing and Electrical Characterization***
    <u>X. Badel</u>, M. Domeij, J. Linnros, accepted for publication in Journal of The Electrochemical Society, in press.

Other publications, not included in the thesis

9. *Fabrication of Colloidal Crystals with Tubular-like Packings*
    F. Li, X. Badel, J. Linnros, J. B. Wiley, submitted to Journal of the American Chemical Society (December 2004).

10. *Fabrication and Assembly Behavior of Square Microcapsules*
    F. Li, X. Badel, J. Linnros, J. Wiley, submitted to Advanced Materials (September 2004).

11. *Fabrication of silicon dioxide nanocapillary arrays*
    R.T. Rajendra Kumar, X. Badel, G. Vikor, J. Linnros, R. Schuch, submitted to Sensors and Actuators A (August 2004).

12. *Doping of Electrochemically Etched Pore Arrays in Silicon: Processing and Electrical Characterization*
    X. Badel, J. Linnros, Proceedings of the 5th Micro Structure Workshop, Ystad, March 2004.

13. *Monte Carlo simulation of the imaging properties of scintillator-coated X-ray pixel detectors*
    M. Hjelm, B. Norlin, H.-E. Nilsson, C. Fröjdh, X. Badel, Proc. IWORID 2002, Nuclear Instrum. and Meth. In Phys. Res. A, 509, pp. 76-85 (2003).

List of Symbols and Acronyms

AFM   atomic force microscopy
Al   aluminum
ALD   atomic layer deposition
Al_2O_3 aluminum oxide
As   arsenic
B   boron
c   concentration of hydrofluoric acid
C   capacitance
CCD   charge coupled device
CsI   cesium iodide
DQE   detective quantum efficiency
DRIE   deep reactive ion etching
E   energy
E_a activation energy
E_c energy level of the conduction band
E_g band gap energy
E_L energy level of a defect in the band gap
E_v energy level of the valence band
EHP   electron hole pair
d   density or depth, as specified in the text
F^- fluor ions
Ga   gallium
HF   hydrofluoric acid
I   current
In   indium
IWORID international workshop on radiation imaging detectors
J   current density
J_{ps} critical polishing current density
J_{tip} current density at a pore tip
k   Boltzman constant $k = 1.38 \times 10^{-23}$ J/K
KOH   potassium hydroxide
L   distance between the 300 W halogen lamp and the sample
LPCVD   low pressure chemical vapor deposition
lp/mm   line pairs per millimeter
m   mass
MOS   metal – oxide – semiconductor
n   valence number or refractive index, as specified in the text
N   nitrogen
Na   sodium
P   phosphorous
PVC   polyvinyl chloride
Pt   platinum

q	electronic charge (q = 1.6×10^{-19} C)
Ru	ruthenium
SCM	scanning capacitance microscopy
SCR	space charge region
SEM	scanning electron microscopy (or micrograph)
Si	silicon
SIMS	secondary ion mass spectrometry
SiO_2	silicon dioxide
SNR	signal-to-noise ratio
SSRM	scanning spreading resistance microscopy
T	temperature
Tl	thallium
TlI_2	thallium iodide
V	potential (voltage)
V_{bi}	built-in potential
V_t	threshold voltage
W	width
Z	atomic number
α	absorption coefficient
ε	permittivity
ρ	resistivity
3D	three dimensional
3D-RID	three dimensional radiation imaging detectors (European project)

Acknowledgements

Chapter 1   Introduction

In 1895, Wilhelm Conrad Röntgen discovered the existence of unknown and invisible rays during an experiment on discharge of electrical currents in highly evacuated glass tubes [1]. While performing the experiment in darkness, he noticed that a barium platinocyanide-coated screen started to luminesce in the room, and that an object placed between the X-ray source and the screen could alter the luminescence. The radiation responsible for this phenomenon was called "X-rays". In addition, Röntgen observed that the image of an object could result in shadows of different intensities on a photographic film reflecting its internal structure. This was the beginning of X-ray imaging.

Nowadays, X-ray imaging is used in important applications such as non-destructive evaluation of materials and in medical imaging. As observed by Röntgen, the principle is based on the fact that materials have different X-ray absorption coefficients. For instance, at equal thicknesses, X-rays are more easily transmitted through human tissue and paper than through bones, stones or lead. Hence, if an X-ray sensitive device is placed behind an irradiated object, an image of the object is obtained by transmission. One of the most commonly used and known devices is the photographic film, which is classified according to its speed (defining the sensitivity) and its spatial resolution. These two characteristics are related to the grain size and a tradeoff has to be made since high-speed films are obtained with large grains whereas high spatial resolution is obtained with small grains. Indeed, a higher lateral resolution requires a proportionately higher dose, i.e. a higher number of impinging X-ray photons per area unit. Images with high spatial resolution can be achieved but only a few percent of incoming X-rays are absorbed in the film. Furthermore, the use of photographic film is time consuming and requires handling of hazardous chemical products due to the development procedure. The cost for films and chemicals is also considerable [2]. Thus, new imaging techniques are needed.

During last decades digital X-ray imaging detectors have been developed to replace photographic films. The principle of these devices is to convert the incoming X-rays into position dependent electric signals, which are then treated to compose an image. These detectors enable real time imaging and easy handling of images, almost as for a video camera for home usage. Although some are already

commercially available, today's detectors still need to be improved in order to enhance the picture quality, usually evaluated in terms of signal-to-noise ratio and spatial resolution. Together with the picture quality, dose reduction is the other vital challenge in medical applications. For dental applications for instance, a signal-to-noise ratio of 50 and a spatial resolution of at least 8 lp/mm are required at an X-ray exposure not higher than 20 mR.

The work presented in this thesis is part of the "three-dimensional radiation imaging detectors" (3D-RID) European project [3], whose goal is to study new types of sensors. Three of the proposed detector concepts have been investigated in this thesis. One of them has been fully fabricated and tested while only a contribution to the other two is presented here. All designs are based on pore arrays, which are ideal starting structures to form pixellated radiation imaging detectors. The thesis contains five chapters, whose purposes and thematics are described below.

Following this introductive chapter, chapter 2 gives some basics of silicon electrochemical etching with an emphasis on pore array formation in n-type silicon. In the literature, three techniques are widely used to fabricate pore arrays: deep reactive ion etching (DRIE), laser drilling and electrochemical etching. Being a rather well-established technique DRIE is often used in industry [4]. It was also used in this work as a common processing tool. DRIE enables a good freedom in mask design and aspect ratios of about 20-25. This can be a serious limitation for some types of detectors, as pores may have to be narrow and very deep to provide high spatial resolution and high sensitivity. Laser drilling is a technique enabling to etch any type of substrates with aspect ratios larger than 25 [5]. Unfortunately, this technique is too time-consuming since holes are drilled one by one. Electrochemical etching of silicon, on the other hand, is a good alternative since it enables to drill relatively fast pore arrays with high aspect ratios. This technique was intensively developed in the nineties to produce porous silicon and the ability to form ordered pore arrays was first demonstrated by Volker Lehmann [6]. In this work, electrochemical etching was developed to form a wide range of pore arrays to be used principally as prototypes for X-ray imaging detectors but also for other applications, not reported in the thesis. The possibility to utilize the technique to form pore arrays and other type of structures such as pillar arrays on the sub-micrometer scale is demonstrated. Electrochemical etching is based on the dissolution of silicon in hydrofluoric solutions with a supply of electronic holes. For the first time, the use of hole injection from a *pn* junction instead of photo-generation was shown to be a successful alternative to perform the etching.

After etching of the pore arrays, additional processes are needed to make the structures as fully-working devices. Depending on the detector concept, various kinds of processes had to be developed. Chapter 3 concerns CCD-based X-ray imaging detectors using scintillating screens. Silicon CCD's (charge coupled device) are one of the key elements in today's X-ray imaging detectors. As silicon is more sensitive to visible light than to X-rays, the CCD is often coated with a scintillating layer [7]. A scintillator is a material which converts incoming X-rays (or other radiation such as charged particles) to secondary emitted, visible photons. The

scintillator should absorb most of the incoming X-rays and emit at a suitable wavelength matching the silicon CCD sensitivity. Cesium Iodide doped with Thallium - CsI(Tl) - is a commonly used scintillator. Typically, a 250-μm thick CsI(Tl) layer absorbs about 80 % of X-rays coming from a standard dental X-ray source while a 5-cm thick silicon crystal would be necessary to absorb the same amount of X-rays. For obvious reasons, thick detectors cannot be used for dental applications. Moreover, solid state detectors are based on depleted semiconductors and the required bias for depletion increases with thickness. As can be seen in Fig. 1.1a, X-rays striking the detector are first absorbed in the scintillator, emitting secondary photons that are then detected in the silicon CCD. The problem of this detector concept is the loss of the CCD's high spatial resolution due to light spreading in the scintillator. Thus, structured scintillating screens, generally in the form of CsI columns, are used to maintain good spatial resolution and sensitivity [8]. In this work, structured scintillating screens were formed by filling a pore array, initially etched in silicon, with CsI(Tl). Cladding materials on the pore walls can be used to enhance the wave-guiding efficiency of the secondary photons towards the CCD pixels (Fig. 1.1b). In this chapter, the detection principle, the ideal performance, the processing and the characterization of such detectors are described.

Chapter 4 presents two detector concepts, both requiring the formation of *pn* junctions in silicon pore walls. The first concept is in fact a modified version of the previous detector where the light emitted from CsI(Tl) is detected by photodiodes inserted in the side walls instead of using a CCD to detect the fraction of light coming out of the pore end. This modification would increase the overall efficiency of the detector as coupling problems would be avoided and light collection would be increased [9, 10]. In this work, the formation of *pn* junctions in the pore walls has been studied, using boron diffusion and deposition of boron-doped poly-silicon.

X-ray

CsI(Tl)

CCD pixels

(a)

X-ray

Cladding material

Silicon

CsI(Tl)

CCD pixels

(b)

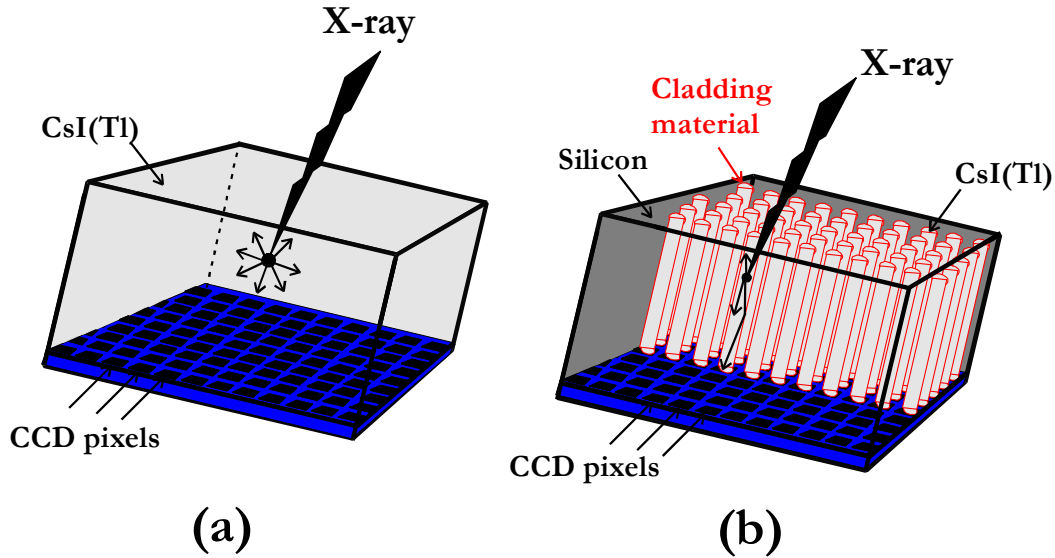**Figure 1.1** Schematics of CCD-based detectors using (a) a plain CsI(Tl) film and (b) a structured scintillating screen, enabling to maintain good spatial resolution due to internal reflection in the CsI(Tl) columns. The principle is based on (i) absorption of X-rays in the scintillator, (ii) emission of secondary photons from the scintillator and (iii) detection of these secondary photons by a CCD.
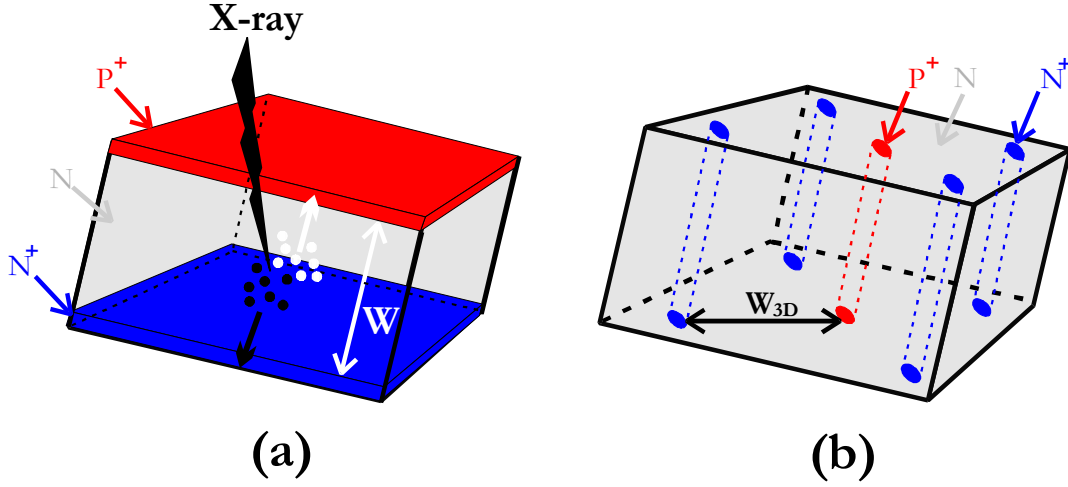
Figure 1.2 Schematics of solid state detectors: (a) planar detector concept and (b) '3D' detector concept. The detection principle is based on (i) generation of electron/hole pairs in the semiconductor, and (ii) collection of these charges due to separation via an electric field. As the pore-to-pore distance can be made much smaller than the thickness of the semiconductor ($W_{3D} \ll W$), the 3D concept allows to work with a low bias to deplete the semiconductor and enable rapid charge collection while keeping an almost equivalent sensing volume.

The pore walls were analyzed by scanning electron microscopy (SEM), scanning spreading resistance microscopy (SSRM), and secondary ion mass spectrometry (SIMS), proving the possibility to form uniform vertical *pn* junctions in the pore walls. Once the *pn* junctions and the filling of the pores have been realized, such a device has to be coupled to a readout circuit. However, in a parallel study, simulations showed that a large noise is expected due to the direct detection of X-rays in the silicon diodes [11]. Hence, the development of this detector concept was not pursued until the end. This detector concept is later termed the "CsI-photodiode" structure.

The other part reported in chapter 4 deals with solid state detectors and the contribution made to the development of a "3D" detector. This concept was first presented by Sherwood Parker as an alternative to planar detectors [12]. For the planar and the 3D detectors, the principle of detection is based on (i) generation of electron/hole pairs in a depleted semiconductor, and (ii) collection of these charges at electrodes as a result of the electric field in the depletion region (Fig. 1.2). The main advantage of the 3D detector is to reduce the distance between the electrodes, which enable fast charge collection and to work with a low bias while keeping a large detecting volume. Such devices also have to be coupled to a readout circuit. These detectors have not been completely realized during this thesis but the electrical characterization of *pn* junctions formed in the pore walls has been performed. Also, a development of the electrochemical etching technique towards narrow hole fabrication has been achieved.

Finally, chapter 5 gives a guide to the eight appended papers included at the end of the thesis and concludes by some outlook and new insights.

Chapter 2　Silicon electrochemical etching

2.1. Etching of non-patterned silicon

2.1.1. From porous to electropolished silicon

Studies on silicon electrochemical etching already started in the fifties (Uhlir and Turner), and it is in 1958 that one of the first papers reported electropolishing of silicon by anodic etching in HydroFluoric acid solutions (HF) [13]. It was also observed that, depending on the experimental parameters, a brown layer could form on the silicon surface. It was later recognized as a layer of randomly distributed and interconnected pores, namely porous silicon. Figure 2.1 shows SEM images of both porous and electropolished silicon viewed from the top. Furthermore, an intermediate regime, also called transition regime [14] and characterized by the formation of pillar-like structures, can be observed. Depending on the pore size, porous silicon is classified in three categories: micropore (< 2 nm), mesopore (2-50 nm) and macropore (> 50 nm, as in Fig. 2.1) [15]. In the following text, the etched face of the silicon substrate will be called the front side (in contact with the HF solution) and the other face, the back side.
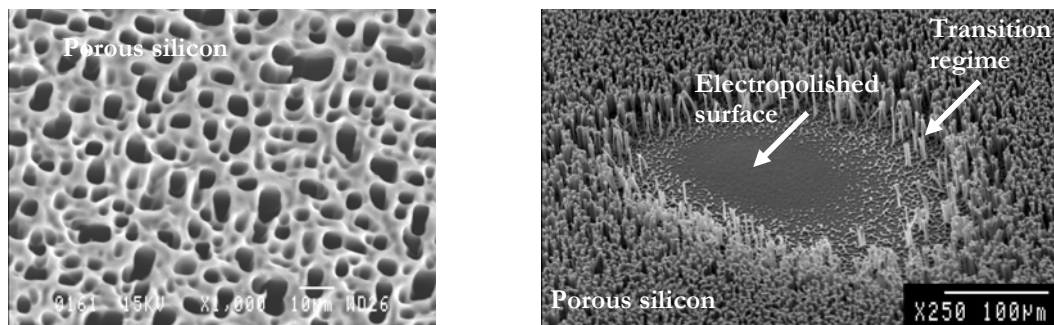

Figure 2.1 SEM images illustrating the three typical electrochemical etching regimes in silicon: porous formation, transition regime with pillar-like structures, and electropolishing. Due to the non-uniform current distribution in the etched area shown on the right (edge of a sample), all three regimes are observed simultaneously.

2.1.2. Chemical reactions and valence number

The chemical reactions responsible for silicon dissolution during electrochemical etching do not only involve silicon atoms and species of the HF solution (also called electrolyte), but also holes (positive charge carriers). Indeed, a charge transfer is needed at the silicon/electrolyte interface for the chemical reaction to happen. Thus, etching occurs readily in p-type silicon as holes are the majority carriers. Both random and ordered pore arrays can be formed [16-20]. For etching of n-type silicon, however, holes have to be generated by some external means. The most common way is photo-generation but an alternative is to inject the minority carriers from a *pn* junction formed at the back side of the wafer, as pioneered in this thesis *(see section 2.3 and appended paper 1)*. In addition, etching of low-resistivity n-type silicon is possible at electrical breakdown conditions [21]. Only n-type silicon was used in this thesis work as the formation of ordered structures, such as pore arrays, is more developed in n-type silicon than in p-type silicon at the moment. Etching of silicon in HF can take two extreme pathways, leading either to porous or electropolished silicon. It is rather well established that porous silicon is formed by consuming two electrical carriers to dissolve one silicon atom whereas electropolishing require four carriers [13]. In the transition regime, between 2 and 4 carriers are consumed. The number of electrical carriers exchanged during the dissolution of one silicon atom is called the valence number, *n*, which can be calculated as follows:

$$n = \frac{I \times t}{q \times \dfrac{\Delta m}{d_{Si}} \times N_{Si}} \qquad\qquad \textbf{Eq. 2.1}$$

where *I* is the current (A), *t* is the etch time (s), *Δm* is the dissolved mass of Si (mg), $q = 1.6 \times 10^{-19}$ C, $d_{si} = 2330$ mg/cm^3 and $N_{si} = 5 \times 10^{22}$ at/cm^3. The dependence of *n* on the current density can be found in Ref. 22 and in section 2.3.3 where hole injection from a *pn* junction is discussed.

Figure 2.2 gives a representation of a possible chemical dissolution reaction involving two charge carriers. The initial silicon surface is hydrogen-terminated, as it is the case in HF [22]. The reaction first occurs between Si atoms and F$^-$ ions, involving only two charge carriers to form SiF$_2$. SiF$_2$ is then dissolved by HF molecules of the solution, forming SiF$_4$; this is a divalent reaction [14, 22]. Later, SiF$_4$ is dissolved in the solution to become a form of the stable product H$_2$SiF$_6$. The second possible reaction (the tetravalent reaction) could start similarly but, instead of being dissolved by HF, SiF$_2$ would be dissolved using two more charge carriers to break the two last silicon back-bonds. Other reaction paths may be possible [23] but the study of these reactions was not the purpose of this thesis. The difficulty in finding the correct reaction schemes can be understood by the large number of species contained in the aqueous HF solution.

$$Si + 2F^- + 2h^+ \rightarrow SiF_2 \qquad\qquad SiF_2 + 2HF \rightarrow SiF_4 + H_2$$
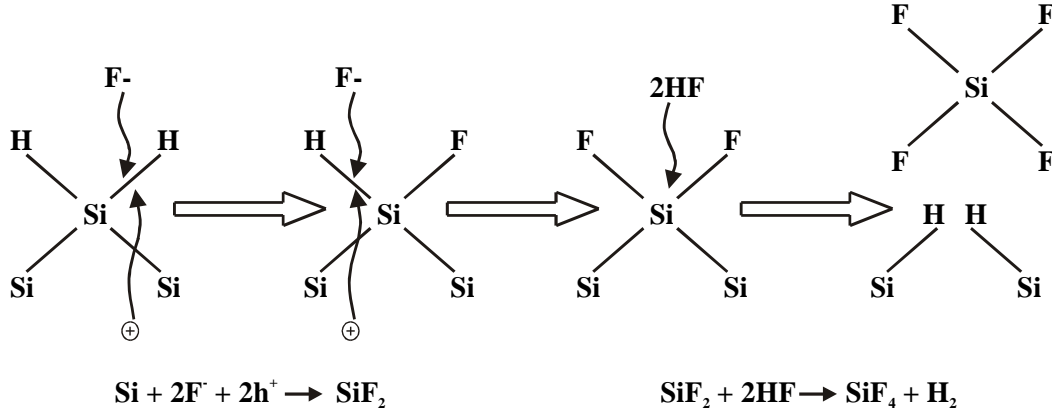
Figure 2.2 Divalent chemical dissolution reaction of silicon in an HF solution [14].

2.1.3. Experimental setup and parameters

A sketch of an electrochemical etching cell, as used in this work, is shown in Fig. 2.3. The light source is located at the backside of the sample, which is usually the case for pore array formation in n-type silicon [6, 24-26]. The cell is made of PVC, which is resistant to HF. Two Platinum electrodes are mounted. Unless specified (as "V_{ref}"), the values given in this chapter refer to the bias between the counter electrode and the sample back side. Generally, a difference of about 0.7 V was measured between the two electrodes. A sapphire window allows observation of the sample surface during etching and possible illumination of the sample front side [27]. As explained in the previous section, etching of moderately and lowly-doped n-type silicon requires first to generate holes in the silicon bulk using, for instance, a light source. Then, a positive bias V, with respect to the solution potential, is applied to the sample back side. The presence of holes at the electrolyte/silicon interface allows for chemical reactions, resulting in etching of the silicon surface whereby charge transfer occurs and a current I is measured. In this setup, the etched area is 2 cm² but etching of full wafers is possible [25, 26]. Electrolytes were prepared by mixing de-ionized water, ethanol (acting as a wetting agent), and hydrofluoric acid (HF50%). The HF concentration, in percentage of weight (wt%), was calculated as follows:

$$[HF]_{wt\%} = \left(\frac{1}{2} \times \frac{V_{HF50\%} \times \rho_{HF50\%}}{V_{H2O} \times \rho_{H2O} + V_{ethanol} \times \rho_{ethanol} + V_{HF50\%} \times \rho_{HF50\%}} \right) \times 100 \qquad \textbf{Eq. 2.2}$$

with $\rho_{HF50\%}$ = 1.16 kg/l, ρ_{H2O} = 1 kg/l and $\rho_{ethanol}$ = 0.79 kg/l
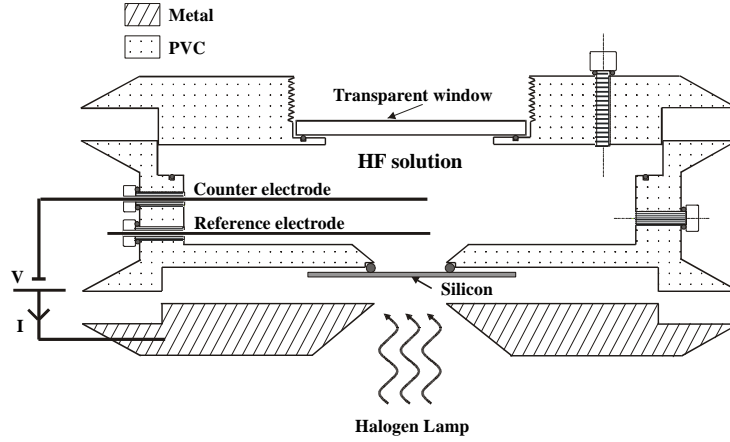
Figure 2.3 Electrochemical etching setup.

Other important parameters for electrochemical etching are:

- The light intensity, determining the number of generated holes in the bulk, and the light wavelength (not particularly studied here).
- The properties of the silicon substrate: resistivity, orientation and type.
- The temperature (T).
- The applied bias (V).
- The etching current density (J).

2.1.4. JV characteristics

Figure 2.4 shows typical JV characteristics (current density – voltage) for n-type silicon illuminated at different light intensities. The first peak observed on these curves is commonly termed J_{ps} and corresponds to the critical polishing current density [13]. J_{ps} delimits the three different regimes: porous silicon formation $(J < J_{ps})$, the transition regime $(J \approx J_{ps})$ and the electropolishing regime $(J > J_{ps})$ [6, 14, 28]. As the reaction can be limited either by the number of holes or the number of HF molecules available at the silicon/electrolyte interface, the JV characteristic depends on both light intensity and HF concentration. As can be seen in Fig. 2.4, when the number of carriers increases via an increase of the light intensity, the maximum current density reached in the JV curve increases too (if the HF concentration is also sufficient). Here the light source was a 300 W halogen lamp placed at different distances "L" from the sample. Also, the current is both dependent on the applied bias and on the light intensity. Thus, the bias can be set independently from the current for $J > J_{ps}$. The dependence of the etching current density on the HF concentration is shown in Fig. 2.5. High HF concentrations allows for high etching current densities (if the hole supply is also sufficient). The J_{ps} value decreases with decreasing HF concentration. Thus, electropolishing is more easily reached for low

HF concentration since it requires low current (low light intensity). The critical polishing current can be estimated from the empirical expression given by V. Lehmann:

$$J_{ps} = Cc^{3/2} \times \exp\left(- E_a / kT\right) \qquad \textbf{Eq. 2.3} \ [6]$$

where c is the HF concentration (in wt%), T the temperature (in Kelvin), k = 1.38×10^{-23} J/K, C = 3300 A/cm², and E_a = 0.345 eV. The dependence in c was found different than $c^{3/2}$ by other authors [23]. Note the high sensitivity to thermal variation indicated by this formula: a 10°C raise from ambient temperature results in a 54% higher J_{ps}.

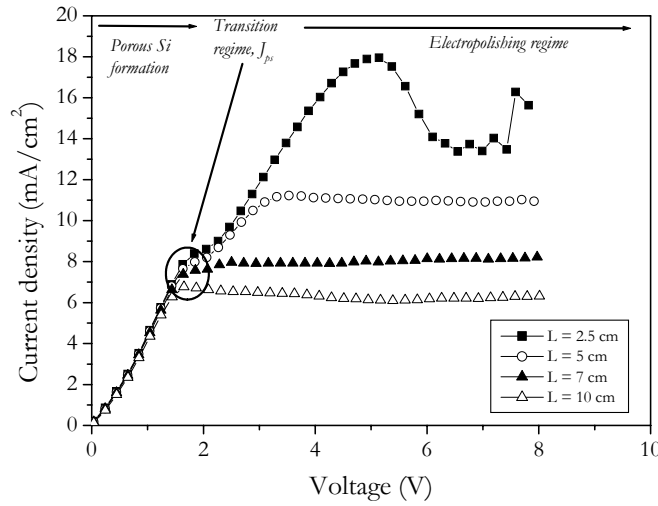**Figure 2.4** *JV* characteristics of an n-type silicon sample (1-10 Ωcm) for various light intensities, changed by varying the lamp/sample distance *"L"* (300 W halogen lamp, 1.5 wt%).
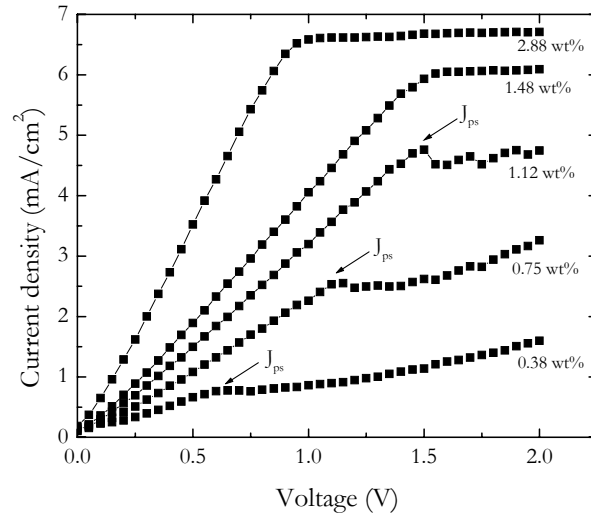
Figure 2.5 *JV* characteristics of an n-type silicon sample (1-1.5 Ωcm) using different HF concentrations. The sample was illuminated with IR diodes and the temperature was kept at 15°C.

2.2. Formation of macropore arrays in n-type silicon

2.2.1. Sample preparation

The front side of the silicon wafer has to be pre-patterned in order to form pore arrays [6]. As illustrated in Fig. 2.6, it consists first of a lithographic step performed in an oxide (SiO_2) or nitride mask in order to define the initial pore opening and the pore pitch (repetition rate). Table 2.1 indicates the pore array geometries used in this work. Both standard 1:1 lithographic tool and a stepper with a 1:5 reduction were used. The stepper allows for high spatial resolution, enabling oxide openings as small as about 500 nm. Then, pits are formed in these openings by anisotropic etching in warm KOH solution (80°C, 30% KOH, 1 μm/min). Etching in KOH results in inverted pyramids since the (100)-oriented silicon planes are etched faster than the (111)-oriented ones (Fig. 2.7) [29]. These pits are used to initiate the pore growth during electrochemical etching. Also, an Al grid may have to be deposited at the backside of the sample in order to apply a uniform potential (Fig. 2.6). This was only done for high resistivity wafers (typically larger than 20-40 Ωcm). For moderately and highly-doped silicon wafers, the backside ohmic contact was realized by applying a eutectic InGa to the surface.
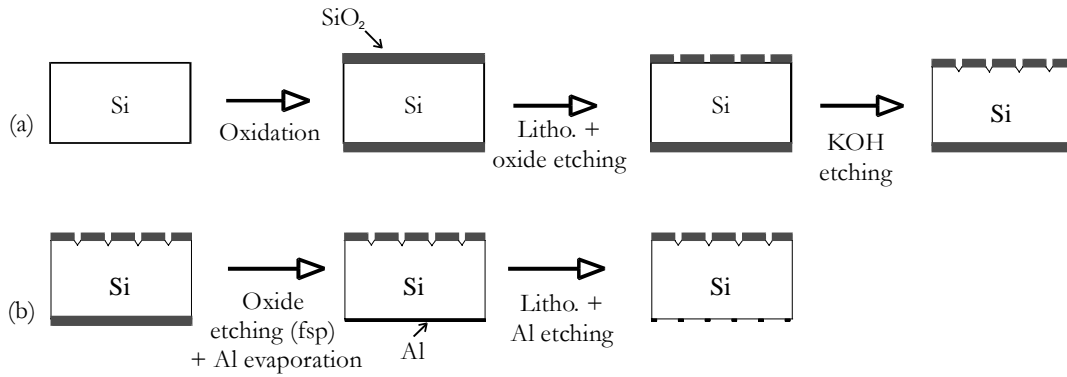
Figure 2.6 Process flow for the preparation of samples prior to photo-electrochemical etching: (a) frontside, (b) backside (fsp means "front side protected").

Table 2.1 Description of the patterns used for lithography.

Pattern	Pore repartition	Pore pitch (μm)	Opening (μm)
S	quadratic	45	40
T	quadratic	30	25
U	hexagonal	30	5 or 10
V	hexagonal	50	5 or 10
W	hexagonal	6	1 or 2
X	hexagonal	10	1 or 2
Y	quadratic	1.4	0.7
Z	quadratic	1	0.5
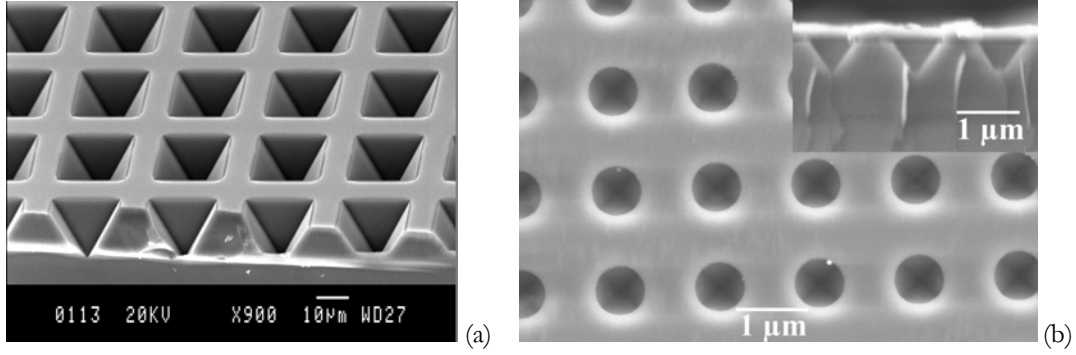
Figure 2.7 SEM of inverted pyramids formed in silicon by warm KOH etching: (a) pattern T, (b) pattern Y.

2.2.2. Formation mechanism

Although several electrochemical etching models have been presented [30, 31], etching of pore arrays in low and moderately-doped n-type silicon is well described by the model proposed by Lehmann [6]. This will be used here for quantitatively explaining the macropore formation mechanism.

Under anodic bias, the n-Si/electrolyte interface is considered as a reverse-biased Schottky junction: a space charge region (SCR) forms in the n-Si electrode along the surface following its profile (Fig. 2.8). Holes generated in the n-Si electrode either recombine in the bulk or participate in the chemical reaction, being accelerated by the electric field of the SCR. The current lines are bent towards the pore tips where the electric field strength is high. The representation given in Fig. 2.8 is for a SCR width equal to about half the pore pitch. Although this looks like an ideal situation, it has been shown that etching of pores spaced by more than twice the SCR width is possible [32-34]. The pore walls are therefore passivated by the combined effect of the SCR and the limited diffusion of the minority carriers [6]. If etching occurs under stable conditions, the pore tips are polished and the current density at the pore tip is assumed to be equal to the polishing current density ($J_{tip}=J_{ps}$). Consequently, for a given pattern (pitch), a modulation of the etching current density results in a modulation of the pore diameter.
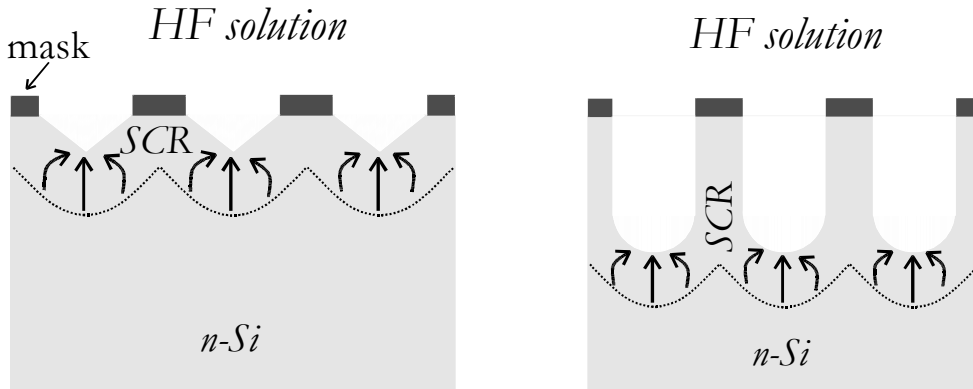
Figure 2.8 Formation mechanism of pore array in n-type silicon (case of pore pitch approximately equal to twice the SCR width) [6, 33]. The arrows represent the current lines.

2.2.3. Influence of various parameters

- *Silicon properties (resistivity and orientation)*

The silicon resistivity is of primary importance for proper formation of macropores since it determines the SCR width. The SCR widths given in Fig. 2.9 were calculated for a potential barrier (ΔV) arbitrarily set to 0.1, 1 and 10 V. As can be seen, high resistivity wafers results in a large SCR. Thus, high resistivity silicon is preferred for thick pore walls. Also, it is generally observed that pores grown in high resistivity wafers are large and vice versa [35]. Consequently, a compromise has to be made on the wafer resistivity in order to form narrow pores with a large pitch. Several pore pitches and diameters had to be realized in this thesis. Hence, different silicon resistivities were tested. Figure 2.10 shows successful examples where the silicon resistivity is well adapted to the pore array geometry. For a pitch of 30-50 μm, high resistivity wafers (2-5 kΩcm) corresponding to a SCR width of about 25-40 μm at 1 V are used. Similarly, for pitches of 6 and 1.4 μm, resistivities of 20-40 and ~ 1 Ωcm are used corresponding to SCR widths of 2.5-5 μm and 0.5-0.7 μm, respectively. For comparison, Fig. 2.11 illustrates problems obtained for a resistivity not adapted to the pore array geometry. If the SCR width is too narrow as compared to the pore spacing, etching may occur in the pore walls due to the presence of carriers. On the other hand, if the SCR width is too large as compared to the initial pits, carriers are not deviated to the pits by the electric field. These results prove the importance of the SCR width and therefore the silicon resistivity. These experiments show also the wide range of macropores that can be achieved by electrochemical etching: from 100 μm large [24] to ~ 200 nm [appended paper 2]. Recently, the formation of ~ 30 nm large pores ("mesopores") in ~ 2 Ωcm n-type silicon by electrical breakdown has been published [36], indicating that the technique can be scaled down far into the sub micron regime.
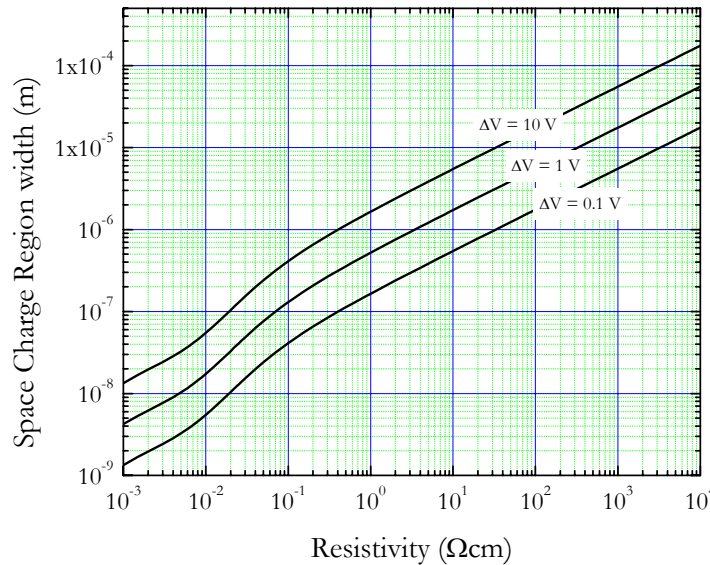
Figure 2.9 Dependence of the SCR width on silicon resistivity.

The orientation of the silicon crystal is also a crucial parameter since pores grow preferentially along the (100) and (113) directions [37]. Thus, pores grow perpendicularly to the surface in a (100)-oriented substrate but not in a (111)-oriented one.
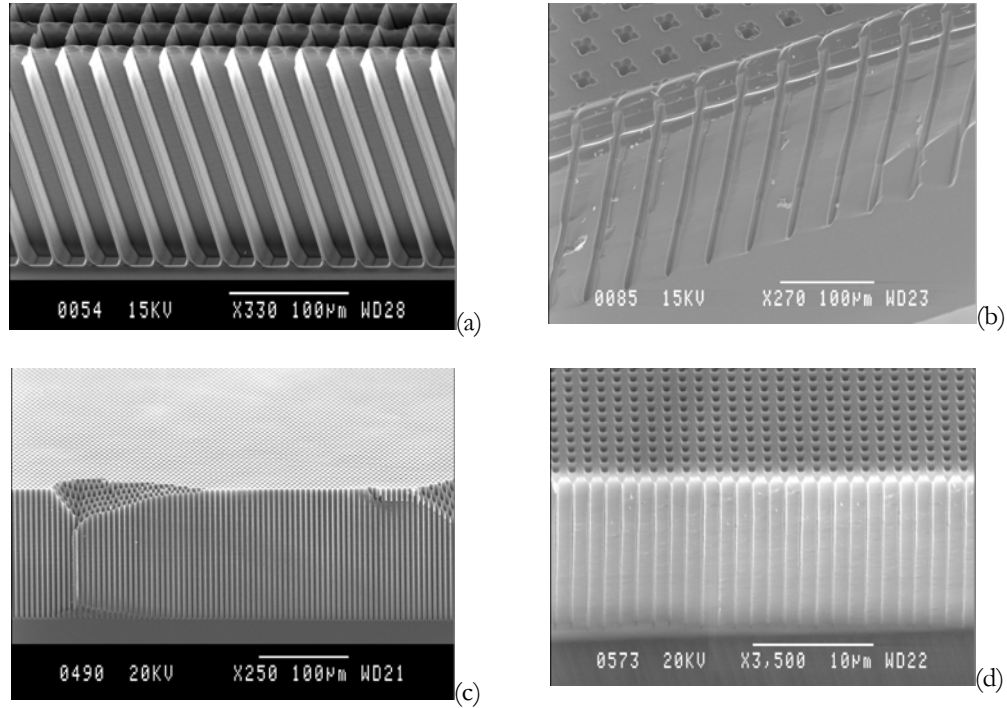
Figure 2.10 Etching of pore arrays with resistivities adapted to the pore array geometry: (a) Pattern T, 2-5 kΩcm, 30 μm pitch (4.2 wt%, 1.5 V, 17.5 mA/cm², 6 h); (b) Pattern V, 2-5 kΩcm, 50 μm pitch (5.45 wt%, V_{ref} = 0.8 V, 1.25 mA/cm², 7 h); (c) Pattern W, 20-40 Ωcm, 6 μm pitch (5.45 wt%, 2 V, 10 mA/cm², 3 h); (d) Pattern Y, 1 Ωcm, 1.4 μm pitch (5.45 wt%, V_{ref} = 0.8 V, 0.5 mA/cm², 0.5 h).
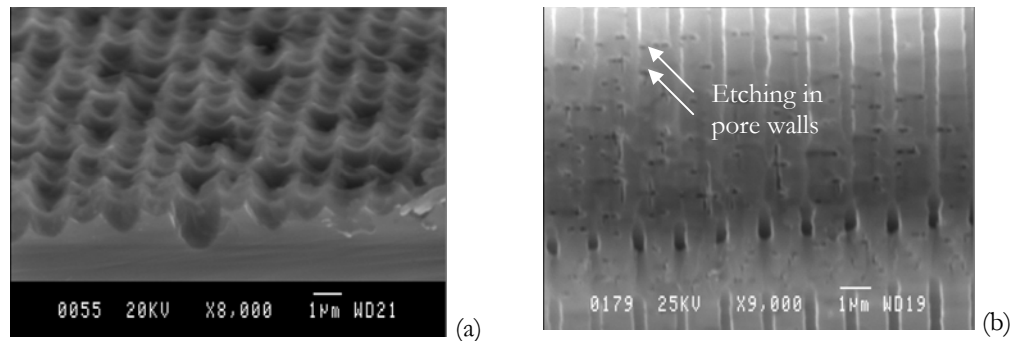
Figure 2.11 Problems occurring with non-adapted resistivities (pattern Y, etching parameters are identical to those of Fig. 2.10d): (a) ρ = 20-40 Ωcm, the SCR width is too large as compared to the initial pits and (b) ρ = 0.1-1 Ωcm, the SCR width is too narrow as compared to the pore spacing (zoom at half the pore depth).

- *Current density (J)*

As explained in previous section, the pore diameter is determined by the etching current density. This is illustrated in Fig. 2.12 where two samples were etched under similar conditions except for the current density and the etch time. As can be seen, the sample etched at high current density has flat pore bottoms and thin pore walls, which is a result of more electropolishing. This effect offers the possibility to modulate the pore diameter as a function of depth [38]. However, this variation cannot be pushed to too large values since a too large increase of the current would lead to total electropolishing of the sample (no structure would be left) while a too large decrease would not enable to satisfy the condition $J_{tip} = J_{ps}$ in all pores. The dependence of the etched area on the current density can be mathematically written as follows:

$$J_{pore}(= J_{ps}) = J \times \frac{A_{cell}}{A_{pore}} \qquad \textbf{Eq. 2.4} \text{ [33, "Lehmann's formula"]}$$

with A_{cell} the area of an unit cell, A_{pore} the area of a pore section, J the etching current density and J_{pore} the etching current density in one pore, which is equal to J_{ps} for stable etching conditions.

The modulation of the pore diameter as a function of time can be utilized to calculate the etch rate as a function of pore depth. This is shown in Fig. 2.13 for a sample with pattern V, to which a sinusoidally varying etching current as a function of time was applied. Clearly, the pore growth rate is not constant along the pore depth. Etching is rather fast at the beginning, about 1.15 µm/min, to finally reach saturation at about 0.5 µm/min. The slow etch rate at the pore bottom may be explained by a slow transport of HF molecules to the pore bottom (mainly diffusion) as compared to the transport of F$^-$ ions, subject to diffusion and migration. This may disturb the balance between HF molecule and F$^-$ ions, thus changing the J_{ps} value and the etch rate. Expression 2.4 predicts a variation of the pore diameter $\varnothing$ as a function of the current density (with $\varnothing$ scaling as $J^{1/2}$). This is verified here since at about half the pore depth (Fig. 2.13), $\varnothing_1 = 13.5$ µm for $J_1 = 1.35$ mA/cm² and $\varnothing_2 = 16.8$ µm for $J_2 = 1.95$ mA/cm², leading to the ratios: $(J_1 / J_2) = 0.69$ and $(\varnothing_1 / \varnothing_2)^2 = 0.645$.

(a)   (b)
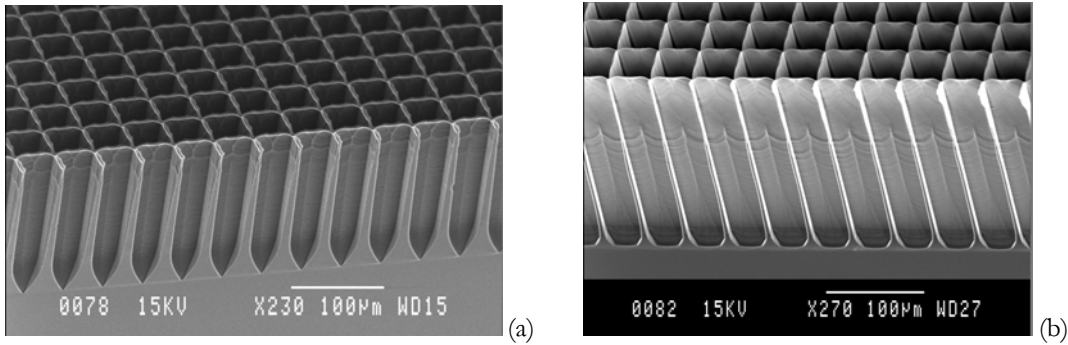
Figure 2.12 SEM of macropore arrays formed at: (a) 15 mA/cm², 3.5 h, (b) 17.5 mA/cm², 6 h (pattern S, 4.2 wt%, 1.5 V, 300 W halogen lamp at L = 4.5 cm).
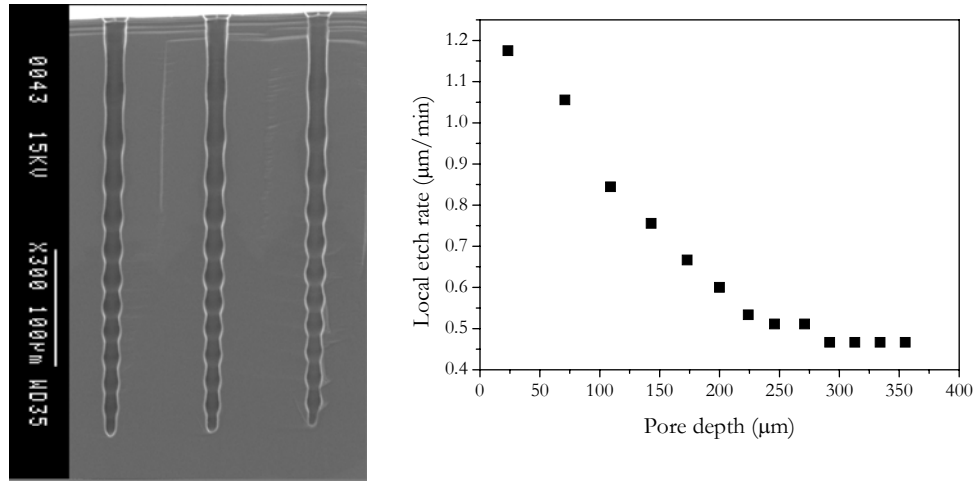
Figure 2.13 SEM of a modulated pore diameter (pattern V, 5.45 wt%, 0.8 V, 9.33 h, sinusoidal variation of J: $1.35 < J < 1.95$ mA/cm² with a period of 45 min). The graph shows the local pore growth rate (depth etched during 1 period divided by the time period) as a function of pore depth.

Note that for a constant etching current and a long etching time, the pore diameter can get enlarged at the top of the pore. This was often observed for pore arrays of type V, which have large pore walls; this means that etching occurs not only at the pore tip but also in the pore walls. This slow dissolution of the silicon pore walls reveals that carriers manage to diffuse in the walls or that they are directly generated in the walls. Nevertheless, this lateral dissolution is very slow: ~ 2 μm enlargement for a 200-μm deep etch.

- *Applied bias (V)*

The effect of the applied bias is shown in Fig. 2.14. A star-like shape of the pores is obtained at high voltages, which is in agreement with observations made in Ref. 35. Clearly, voltages in the range of 1.5 V should be used to grow proper pore arrays. The high electric field at the pore corners may be responsible for this behavior. A similar phenomenon was observed in moderately-doped silicon samples for the formation of sub-micron pores (patterns Y & Z). This is illustrated in Fig. 4 of appended paper 2, where a high bias leads to the so-called "pore wall breakdown" [39] characterized by etching of the main pore walls. On the other hand, a too low bias does not enable to concentrate properly the holes at the pore tips; as a result, holes may diffuse into the walls and rather large pores are formed.
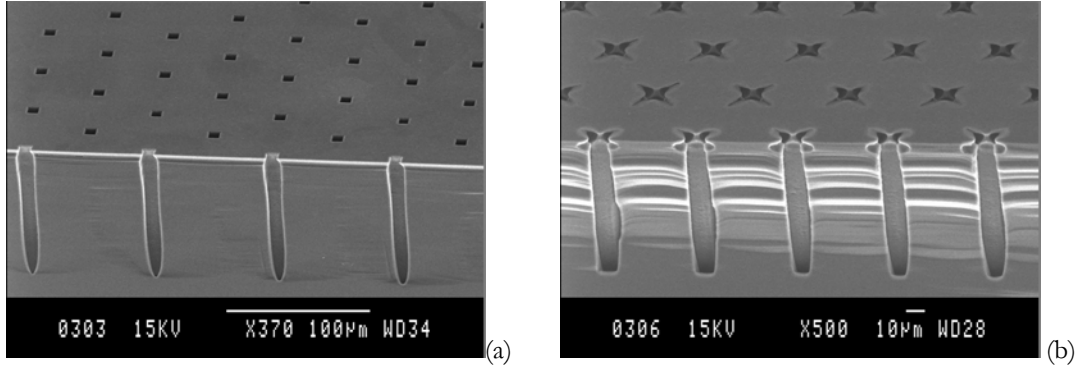
Figure 2.14 Macropore arrays formed at: (a) 1.5 V and (b) 3 V (2-5 kΩcm, 5.45 wt%, 1.4 mA/cm², 1.66 h, pattern V)

- *HF concentration*

Different HF concentrations can be used to form similar pore arrays. As will be seen, this influences the etch rate. However, the etching current density has to be adjusted since J_{ps} depends on the HF concentration (Eq 2.3). If correct parameters are known to form pore arrays at a HF concentration $c = c_1$ and a current density $J = J_1$, the current density to be used at a HF concentration $c = c_2$ can be estimated as:

$$J_2 = J_1 \times \left(\frac{c_2}{c_1} \right)^{3/2} \quad \textbf{Eq. 2.5}$$

Figure 2.15 shows two examples where the proportionality in $c^{3/2}$ is almost respected. The experimental parameters were similar to those given in Fig. 2.10a except for the etching time, the HF concentration and the current density. According to Eq. 2.5, the current densities to be used for a concentration of *5.45 wt%* and *6.6 wt%* would be *25.8 mA/cm²* and *34.7 mA/cm²*, respectively. These estimated current densities are slightly higher than the experimental ones. This could then explain why the sample etched in *5.45 wt%* at *22.5 mA/cm²* has rather thick walls, and why the sample etched in *6.6 wt%* at *32.5 mA/cm²* has the bottom of the pores not properly polished. Examples shown in Fig 2.15 prove also that extremely deep pores can be achieved. In principle, pores could be etched through the whole wafer thickness. However, this is not advised in our case for experimental reasons as the electrolyte would then break through to the back side of the sample. It is interesting to note the high etch rate, 1.23 μm/min, obtained for the sample etched in 6.6 wt% as compared to the sample etched in 4.2 wt%, 0.64 μm/min. Thus, it could be sometimes beneficial to utilize high HF concentrations. However, the etching current has to be increased in accordance (Eq. 2.5) and the supply of minority carriers should therefore be sufficient. This may not always be the case, depending on the available light source (light intensity).
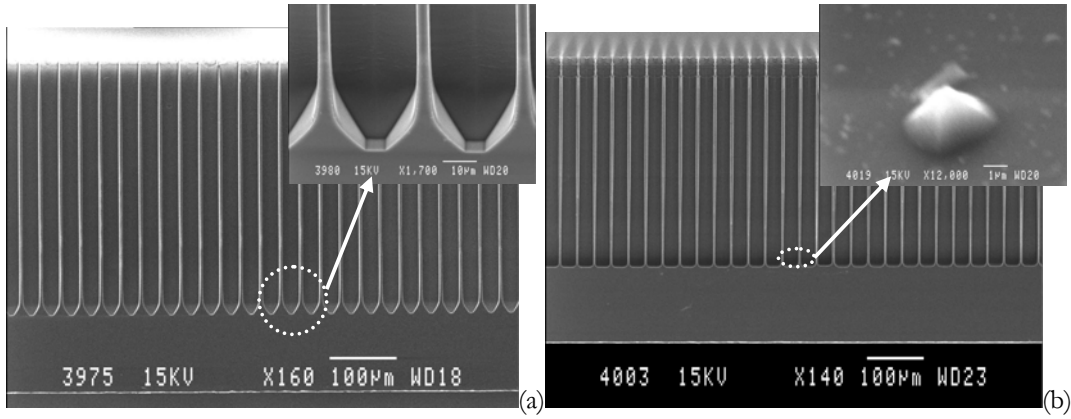
Figure 2.15 Etching at different HF concentration/etching current combinations: (a) c = 5.45 wt%, J = 22.5 mA/cm², t = 7 h; (b) c = 6.6 wt%, J = 32.5 mA/cm², t = 5 h (pattern T, all other parameters are identical).

- *Uniform pattern*

It is crucial to have a uniform pattern on the front side surface since the current lines are very dependent on the pit positions. The absence of one or several pores provokes a surplus of holes, making neighboring pores slightly larger, as pointed out by the arrows in Fig. 2.16.
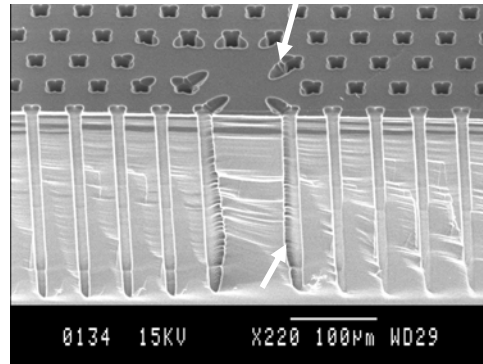
Figure 2.16 Illustration of effects occurring for non-uniform patterning (pattern V).

2.3. Hole injection from a *pn* junction

2.3.1. Sample preparation and principle

Here the goal was to show the possibility of using a *pn* junction as an alternative to photo-generation. This idea was already mentioned in 1979 in ref. 40, but had never been demonstrated.

pn junctions were made at the backside of high-resistivity (3.8-5.5 kΩcm) n-type silicon substrates by boron diffusion from a solid source at 1150°C for 105 min, resulting in a 6-μm thick p$^+$ layer with a maximum B concentration of 2×10^{20} cm^{-3}. For etching of pore arrays the process flow includes etching of inverted pyramids, as presented in Fig. 2.6.

During anodic etching, the diode is under forward bias and holes are injected from the p$^+$ side of the junction into the valence band of the n$^-$ side. These carriers either recombine with electrons in the bulk or diffuse towards the silicon/electrolyte interface to participate in the dissolution reaction. Electrons injected from the n$^-$ side into the p$^+$ side of the junction, together with electrons recombined in the bulk, call for an electron supply. These electrons could be injected from negative ions of the electrolyte into the conduction band of silicon [appended paper 1].

2.3.2. Pros & Cons

Extension of this technique to n-type silicon of lower resistivity (20-40 Ωcm) has not been successful using the same process flow. The high temperature process used to form the junction apparently lowers the lifetime of the minority carriers in the bulk; thus limiting the electrochemical etching process by reducing the achievable current density. A similar observation has been made when etching oxidized silicon wafers of low resistivity. The achievable etching currents are much lower after than before oxidation at high temperatures. However, it is possible to form *pn* junctions using a low-temperature process (around 600°C) such as epitaxy of boron-doped silicon. This was performed on 20-40 Ωcm silicon samples and etching was successful. In conclusion, high temperature processes such as diffusion or implantation followed by annealing cannot be used for low resistivity n-type silicon, limiting the technique to some extent.

The light source is of course not used here, making the setup simpler and preventing the sample and the solution to warm up, as it can be the case with a halogen lamp. However, the possibility to control the minority carrier concentration at a constant bias during etching is a nice feature of photo-electrochemical etching, which is not directly possible here. However, with a front contact on the n$^-$-doped Si, the electrical setup resembles a transistor structure. Thus, one could control the injection of holes from the p$^+$-layer separately from the etching cell bias. This would enable better control of the etching reaction.

2.3.3. Dissolution valence and pore arrays

A series of experiments was performed to calculate the valence numbers in a 2.2 wt% HF solution according to expression 2.1. Depending on the current density, the values vary between 2 and 4 (Fig. 2.17), as expected [13]. The J_{ps} value is about 8 mA/cm², which is rather close to the value of J_{ps} ($\approx$ 10 mA/cm²) estimated from expression 2.3. The ability to etch pore arrays has also been proven (Fig. 2.18). Pores shown in Fig. 218a are 26 ± 1 µm large and 167 ± 13 µm deep along a 1.6 cm wide section, indicating a rather good etching uniformity; thus a homogeneous hole diffusion length, larger than the wafer thickness. The etching currents needed for stable formation are lower than for photo-electrochemical etching, which may be due to the dependence of J_{ps} on temperature, since here the samples are not heated by the halogen lamp (Eq. 2.3). As a consequence, the etch rate is also slightly lower than for photo-electrochemical etching (about 0.5 µm/min here).
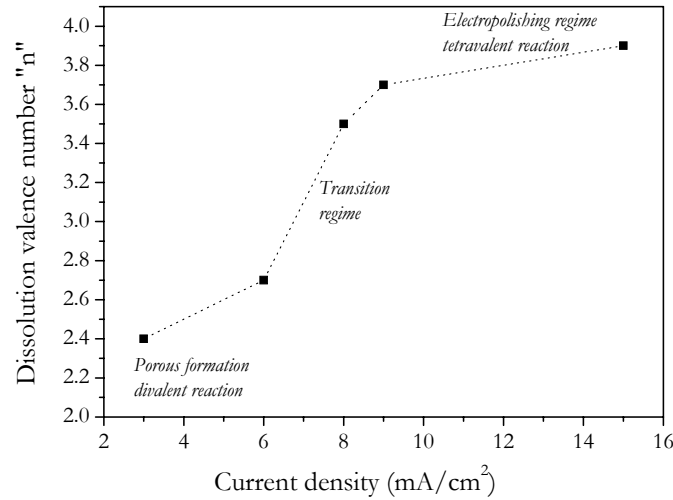

Figure 2.17 Dissolution valence n as a function of current density J for a 2.2 wt% HF solution, using carrier injection from a *pn* junction.
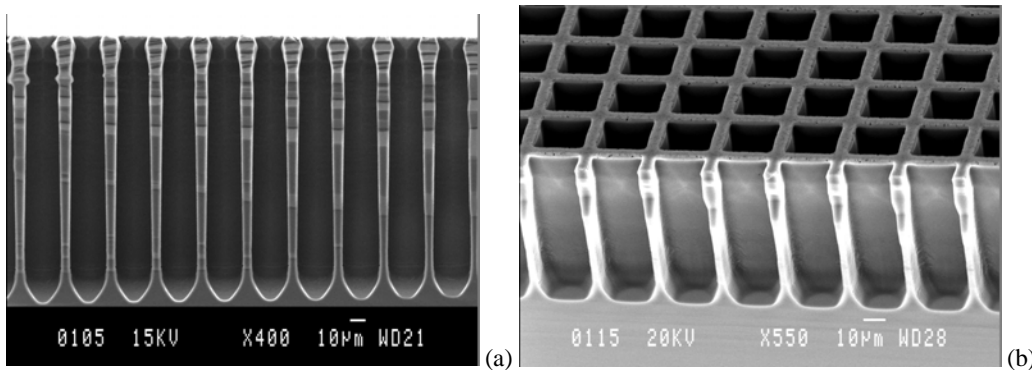

(a)   (b)

Figure 2.18 Etching of pore arrays (pattern T) using hole injection from a *pn* junction. (a) 4.2 wt%, 10 mA/cm², 6 h, (b) 4.2 wt%, 15 mA/cm², 2.25 h.

2.4. Formation of pillar arrays

2.4.1. Goal

Not only pore arrays can be formed in silicon by electrochemical etching. In a parallel work, the formation of structures such as walls, tubes and pillars have been investigated. Several techniques have been proposed to form pillar arrays. However, most of them are rather complicated (composed of several steps) or requires advanced equipments (based on plasma etching) [41-43]. Here the main goal was to establish a cheap and simple technique to fabricate pillar arrays in silicon on the nanoscale. This work is reported in appended paper 3 and is based on a previous study that can be found in ref. 44. The technique developed here provides a simple and powerful tool for "nano-machining" of bulk silicon. Structures may be used to study photoluminescence of silicon, as photonic crystals or to fabricate various types of sensors related to microfluidics.

2.4.2. Sample preparation

As for the formation of pore arrays, the front side of the sample has to be pre-patterned. However, here it consists only of a lithographic step since the resist is directly used as a mask during electrochemical etching. Buffered-HF was used instead of HF to avoid resist lift-off. The initial structures were defined with a stepper. As the process flow is only composed of two steps: Lithography and Electrochemical Etching, the technique was called "LEE".

2.4.3. Etching mechanism

The etching mechanism is illustrated in Fig. 1 of appended paper 3. The principle is rather similar to macropore formation where the structures formed on the wafer surface deflect the current lines, as the pore walls do for etching of pore arrays. The photo-generated holes are directed towards the sides of the structures by the electric field of the SCR. Thus, the goal is to obtain electropolishing of the area surrounding the structure. As narrow pillars have to be formed, most of the sample has to be polished and the etching current density must be rather close to J_{ps}. It was found that the size of the structure scales with the SCR width thus the resistivity, as shown in Fig. 2.9. First the formation of structures in ~ 0.08 Ωcm silicon was studied. Very well defined pillar arrays with diameters of about 400 nm were produced, as shown in Fig. 2.19. Tubes and walls can be formed as well. As for the formation of pore arrays, the diameter of the pillars can be controlled by the etching current. However, a too large current would lead to electropolishing and no structure would be formed as the whole surface is electropolished. On the other

hand, a too low current would lead to formation of "parasite" structures between the pillars. This follows from the proportionality between the etched area fraction and the current density with respect to the electropolishing current density (J_{ps}). Thus, pillar formation requires more accurate control of the current compared to pore etching.
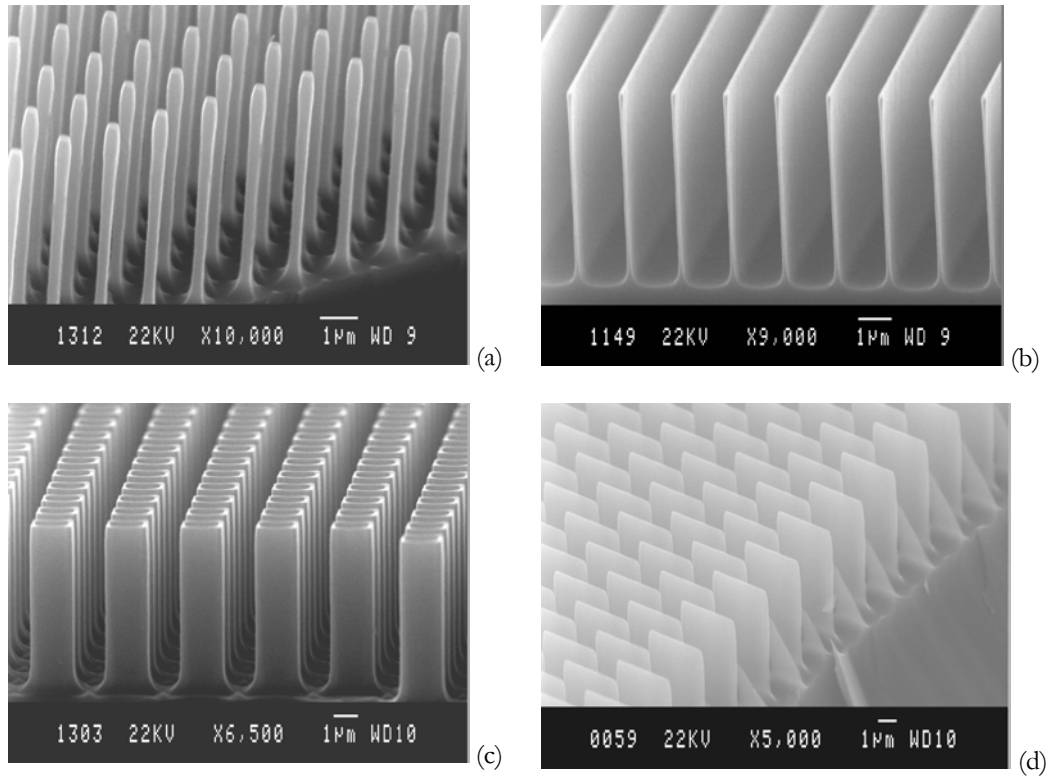
Figure 2.19 Examples of electrochemically etched three-dimensional structures on the sub-micrometer scale: (a) Array of ~ 400 nm large pillars, (b) ~ 200 nm thick walls, (c) Array of tubes, (d) Array of walls.

Chapter 3   CCD-based X-ray detectors using scintillating screens

3.1. Detection principle

3.1.1. CCD

In 1969, George Smith and Willard Boyle from Bell Laboratories invented one of the most commonly used imaging devices today: the CCD [45]. A CCD, charge coupled device, consists of a series of light-sensitive elements arranged in a matrix of lines and columns. Each element (or pixel) is a MOS capacitor (metal–oxide–semiconductor) enabled to convert photons into electrical charges and to store these charges. Charges are then transferred pixel by pixel to an amplifier moving from one MOS capacitor to another. The detected time sequence of charges is later used to recompose the image. The CCD principle is based on charge carrier photo-generation, charge storage in a MOS capacitor and charge transfer in a subsequent read-out cycle.

- *Photogeneration*

Incident photons of energy E, absorbed in a semiconductor of band gap E_g, can generate electron-hole pairs (EHPs) if E is larger than E_g (band-to-band transition), or if E is high enough to allow a transition using forbidden gap energy levels E_L (from which the electron can be excited to the conduction band either thermally or by a second photon), as seen in Fig. 3.1. If one of these conditions is satisfied, the photon energy can be consumed to transfer one electron to an upper energy level [46]. Usually, the concentration of defects or impurities giving rise to the E_L is low and, therefore, processes involving this transition can be neglected. The vacant place left by the electron is called a hole, and can be considered as a positive charge carrier. For silicon, photo-generation is effective in the range 1.1 eV - 10 keV. At wavelengths above 1.1 μm *(E < 1.1 eV)*, the photon energy is not high enough to excite electrons from the valence band to the conduction band. On the
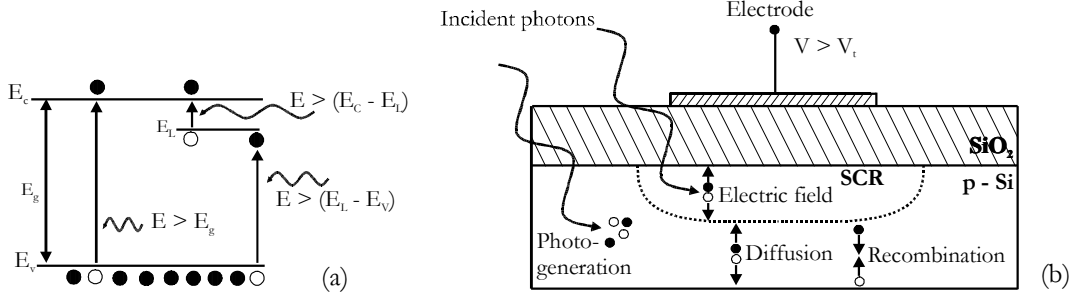
Figure 3.1 (a) Band diagram of a semiconductor illustrating carrier photo-generation, (b) Cross-sectional view of a p-Si MOS capacitor under illumination.

other hand, at energies above 10 keV, the interaction probability between a photon and silicon becomes too low due to the low absorption coefficient of silicon at these wavelengths.

- *Charge storage in a p-Si MOS capacitor*

A MOS capacitor, characterized by its threshold voltage V_t, constitutes the basic element of a CCD. Depending on the potential applied to the electrode (made of poly-silicon here), the MOS can operate in three regimes: accumulation, depletion or inversion. When a positive bias V $(V > V_t)$ is applied on the electrode of a p-Si MOS capacitor, the inversion regime is reached and a large space charge region (SCR) forms under the oxide (Fig. 3.1). Photons impinging on the MOS pass through the SiO_2 layer and the electrode, both transparent, and are then absorbed in the silicon, where EHPs are generated. If absorption occurs in the SCR, EHPs are separated by the electric field; as a result, holes are transferred to the rear side of the capacitor while electrons go to the SiO_2/Si interface. If absorption occurs outside the SCR, charges either recombine (opposite effect of photo-generation) or contribute to the signal after diffusion to the SCR. Electrons are stored under the oxide as long as a high enough positive bias is applied to the electrode. The MOS structure is usually coated by an anti-reflective layer to increase its efficiency [47].

- *Charge transfer or Coupling*

Charges stored in a MOS capacitor can be transferred and read out using different sensor architectures. In all cases, charges are transferred to a storage area, moving from one MOS capacitor to another. Each MOS capacitor usually has three electrodes whose potentials are cycled in order to move the charge packet. Electrons migrate to the electrode having a more positive potential than the one where they are presently stored. For instance, charges can be moved first vertically to a so-called *register line* (line by line), and then horizontally to a so-called *transfer pixel*. Finally,

charge packets are sent to a charge amplifier and an Analogue/Digital converter. Subsequently, information is sent pixel by pixel to a computer. As this type of charge transfer can take relatively long time, other architectures have been proposed. An alternative is to use two identical arrays: one for light detection and another one, light protected, for registration and readout of charges; this is called the *frame transfer*. Another approach is to place an extra line of MOS capacitors between every line of the CCD array in order to store the charges of the closest pixel; this is the *interline transfer*. This shortens the distance to the storage area but reduces the CCD's spatial resolution by about 50 % due to the area taken by these extra MOS capacitors.

- *Limits and applications to X-rays*

Although a CCD presents good imaging characteristics (high spatial resolution and low signal-to-noise ratio), different effects can lower its performance. One of them is the thermal generation of carriers, which contribute to the detected signal. This signal is called *dark current* or *noise*, and can be significantly reduced by cooling down the CCD. Another problem, called *fading*, is the loss of charges during charge transfer, which may be due to interface states trapping carriers at the SiO_2/Si interface. Another negative effect is the *blooming*, which occurs when the maximum number of electrons that can be stored in one pixel is reached. As a result, some of the photo-generated charges leak to adjacent pixels. Finally, it is worth noting that a silicon CCD is most sensitive to light in the range 400-1100 nm. Consequently, a silicon CCD is often combined to a scintillator (emitting visible light under X-rays) in order to be used in X-ray imaging sensors [7]. CsI(Tl) and CsI(Na) have been used in this thesis since their emission wavelengths match quite well the spectral sensitivity of silicon CCDs. These two scintillators are presented in next section.

3.1.2. CsI(Tl) and CsI(Na)

A scintillator is a medium that emits secondary photons of energy E_1 when exposed to ionizing radiation of energy E_2. For instance, CsI(Tl) emits green light (550 nm) when exposed to X-rays. The general characteristics required on a scintillator are (i) high atomic number and density (related to the stopping power), (ii) transparency to its own emission light wavelength, (iii) high light yield (usually expressed as a number of photons/MeV), (iv) good energy resolution, and (v) stability against moisture, mechanical, temperature and radiation effects. Cesium Iodide (CsI) doped with Thallium (Tl) and doped with Sodium (Na) are presented here. The dopant, also called activator, is usually written in brackets. The origin of luminescence in CsI crystals is not completely understood [48-50]. Although CsI is a scintillator itself, dopants are incorporated to increase the light output and to monitor the emission wavelength. Experimentally, CsI(Tl) presents two radiation peaks at 485 and 550 nm while CsI(Na) emits at 420 nm.

Table 3.1 Characteristics of CsI(Tl) and CsI(Na).
λ: Wavelength of the main emission peak; Z: effective atomic number;
d: density (g/cm³); n: refractive index; Y: light yield (photons/MeV).

Material	λ (nm)	Z	d	n	Y
CsI(Na)	420	54	4.51	1.74	150000
CsI(Tl)	550	54	4.51	1.74	60000

Bulk CsI is commonly grown using either the Kiropoulos (extension of the well-known Czochralski technique) or the Stockbarger techniques [51]. The former consists of pulling the crystal from the melt, starting the crystallization with a seed to orient the growth. The later uses furnaces where a crucible containing the charge is first melted and then cooled down. The cooling rate is a crucial parameter to control and ranges typically from 20°C/h [52] to 70°C/h [53]. The dopant is directly introduced in the melt and segregation phenomena of Tl in large crystals can be avoided using the zone leveling technique, where a molten zone is passed repeatedly one way and then the other way along the crystal. CsI(Tl) can also be deposited as thin films using vapor deposition [8]. Vapor deposition is performed with a "two boat evaporator system" where two sources, containing respectively CsI and TlI_2, are operated at different temperatures according to the desired composition ratio of Tl into CsI. The challenge in growing doped-CsI is to maintain a uniform dopant concentration in the crystal, which is essential for optimal light emission efficiency [8]. According to most of the publications found, the amount of Tl needed to obtain high light output should not be less than 4×10^{-2} mole %. The initial powder of CsI(Tl) used in this work contained 1000 ppm, respectively 1×10^{-1} mole %. The general characteristics of CsI(Tl) and CsI(Na) are summarized in Table 3.1.
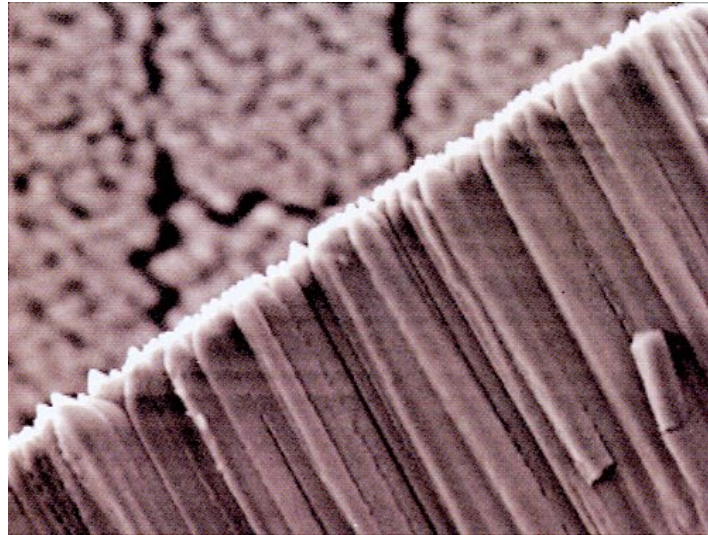

Figure 3.2 Columnar CsI(Tl) film. Proper evaporation conditions allow the growth of dense array of fine CsI(Tl) needles (10 to 20 μm in diameter) [56].

3.1.3. Structured scintillating screens

As explained earlier, a silicon CCD is a device sensitive to visible light but less to X-rays. To form an X-ray imaging detector, a silicon CCD can be coated with a scintillator. Unfortunately, while a thick layer is preferable to absorb most of incoming X-rays, a thin layer is preferable for good spatial resolution due to light spreading in the layer as the emission of secondary photons is isotropic. Thus, a tradeoff has to be made on the scintillating layer thickness. However, structured scintillating screens can be used in order to maintain both good spatial resolution and good sensitivity. A first approach is to use a columnar CsI(Tl) film, which is formed by evaporation on a pre-patterned substrate or on a optical fiber plate (Fig. 3.2) [8, 54-56]. Light emitted from CsI(Tl) propagates along the columns, thus reducing light spreading. Nevertheless, cross-talk between adjacent columns is still possible and there is a tendency for the columns to widen or spread near the top. In this thesis, another type of scintillating waveguides has been investigated. The scintillating screen is formed by filling a pore array with a scintillator. The pores are etched in silicon, and the pore walls are either oxidized or metallized in order to improve the reflection (Fig. 3.3). For optimal spatial resolution, each waveguide matches the lateral dimensions of a CCD pixel [57, 58]. The operation principle is quite similar to scintillating optical fibers [59, 60] and is based on (i) absorption of X-ray photons in CsI(Tl), (ii) emission of secondary photons from CsI(Tl), (iii) wave-guiding of the secondary photons to the CCD pixels, and (iv) light detection by the CCD.
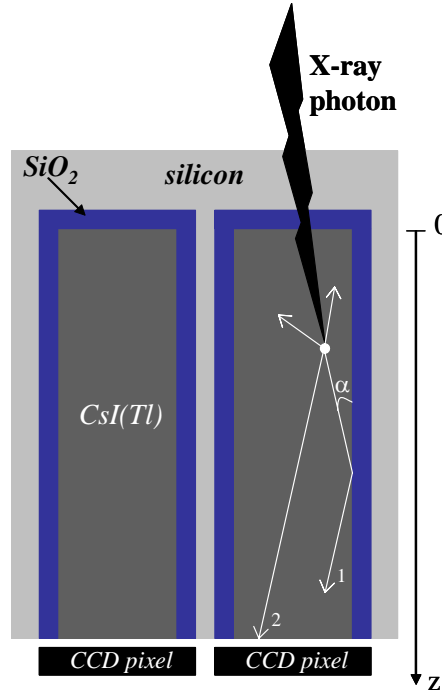
Figure 3.3 Principle of scintillating waveguides. All rays having an incidence angle α smaller than the critical angle ($\alpha_C = 33°$) are totally reflected (ray 1). Other rays may be directly detected by the CCD pixel without any reflection (ray 2) or may be partly reflected, the other part being transmitted into the pore wall and possibly in next pixel. Rays emitted to the rear side of the detector (opposite side of the CCD) have a low probability to reach the CCD pixel.

3.2. Ideal performance

The goal of this section is to study the viability of the proposed concept for dental imaging applications.

3.2.1. Efficiency calculation

Using an oxide layer, good guidance property is expected since the refractive indexes of CsI(Tl) and SiO$_2$ are 1.74 and 1.46, respectively. At the impact point between one X-ray photon and the scintillator, secondary photons can be emitted in any direction (Fig. 3.3). All photons or rays having incidence angles smaller than the critical angle ($\alpha_c = 33°$) are totally reflected without any loss of power. On the other hand, only a part of photons having incidence angles larger than the critical angle are reflected, the other part being transmitted into the SiO$_2$ layer. Cross-talk between adjacent columns due to the refracted part can degrade the spatial resolution of the detector. However, a 2.3-µm thick silicon layer in the pore wall would absorb 80 % of photons ($\alpha_{Si} = 7 \times 10^3$ cm^{-1} at 550 nm). The small fraction transmitted to the next pixel may only give minor cross talk effect as such rays would continue into the next wall, where, again, 80 % would be absorbed. For the reflected part, the reflection coefficient is a function of the incidence angle and the refractive indexes of CsI(Tl) and SiO$_2$.

These optical considerations enable to calculate the *wave-guiding efficiency* in the pores, corresponding to the percentage of visible photons emitted from the CsI(Tl) scintillator, which can reach the CCD pixels. We have calculated this efficiency numerically using a computer code based on ray tracing. To perform the calculation, the waveguide is first divided into several elements along the z-axis (Fig. 3.3). The impact point is chosen to be at the middle of each element (height = Δz and width equal to the pore diameter). For a matter of simplicity, a cylindrical pore shape is considered. As an example, for 250-µm deep oxidized pores with a diameter of 40 µm, around 9 % of the photons emitted by the scintillator would reach the CCD pixels. Using a metal layer, the *wave-guiding efficiency* is mainly dependent on the reflection coefficient of the metal. Each impact on the pore walls attenuates the propagation of the photons. Total reflection is not possible unless the metal has a reflection coefficient of 1 (ideal case). In addition, a *relative efficiency* taking into account both the *wave-guiding efficiency* and the absorption of X-rays in the guides can be calculated ($\alpha = 65$ cm^{-1} was used, 30 keV).

These calculations have been performed for a pore diameter of 25 µm and for different types of coatings, as shown in Figs. 3.4 and 3.5. As expected, with a metal coating having an ideal reflection coefficient of 1 all photons emitted from the scintillator would be guided down to the CCD pixels. However, for the oxide and the metal coatings having a reflection coefficient less than 1, the *wave-guiding efficiency* decreases rapidly in the first 50-100 µm as the number of directly detected photons (ray 2 in Fig. 3.3) decreases (the solid angle becomes smaller and smaller as the depth increases). As can be seen, the *wave-guiding efficiency* and the *relative efficiency* tend

to reach a constant value for deep oxidized pores. Indeed, in this case the main part of the photons contributing to the signal is that of totally reflected photons (ray 1 in Fig. 3.3). As, by definition, these photons are reflected without loss of power, a constant value is reached. However, the *wave-guiding efficiency* is continuously decreasing for metal coatings with reflection coefficient less than 1, as in this case there is loss of power at every reflection at the pore walls. Note that the optimal pore depth depends on the reflective coefficient. The relative efficiency for a reflection coefficient of 1 is shown in a separate figure (Fig. 3.5) due to scaling matter. Indeed, as the *wave-guiding efficiency* is in this case equal to 100 %, the result is not dependent on the pore diameter and the curve represents simply the absorption of X-rays in CsI(Tl) which reaches higher value than those in Fig. 3.4. As can be seen, a 250-μm thick CsI(Tl) layer absorbs about 80 % of incoming X-rays.

The same type of calculation has been performed for two different pore diameters (25 and 40 μm) and for both oxide and metal coatings, as shown in Fig. 3.6. The same behaviors are observed but the wave-guiding efficiencies and, consequently, the relative efficiencies are higher for the large pore diameter.

Figure 3.4 (a) Wave-guiding efficiency and (b) relative efficiency (including X-ray absorption) as a function of pore depth for pore wall coating with an oxide or a metal having a reflection coefficient (r) of 0.53, 0.8 and 1. The relative efficiency for r = 1 is not shown here but in Fig. 3.5 for scaling matter. The pore diameter was arbitrarily set to 25 μm and the absorption coefficient is $\alpha= 65$ cm^{-1}.

Figure 3.5 Relative efficiency as a function of pore depth for a pore diameter of 25 μm and a metal coating with a reflection coefficient of 1. As all photons emitted from CsI(Tl) are detected by the CCD pixels in this case, the graph represents simply the absorption of X rays in CsI(Tl). The absorption coefficient is $\alpha= 65$ cm^{-1}.
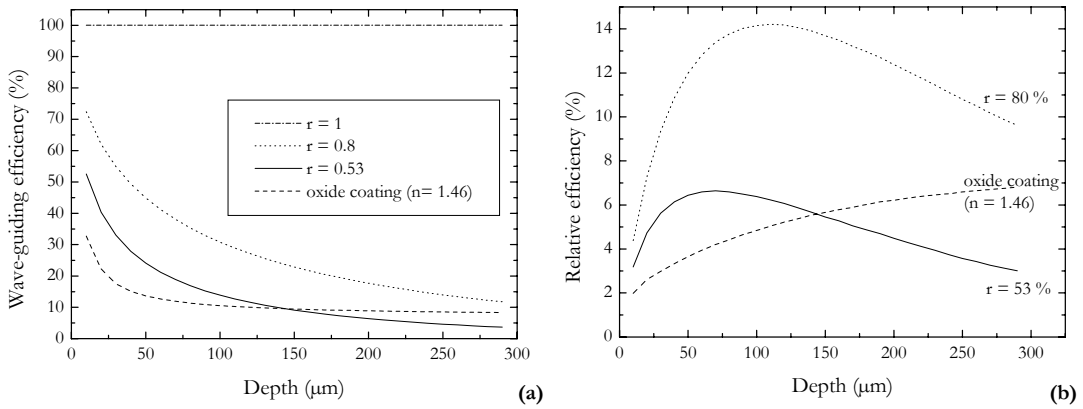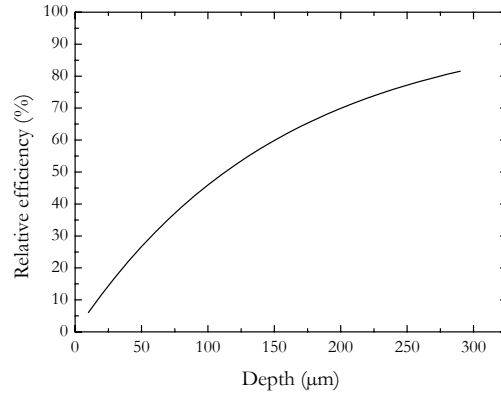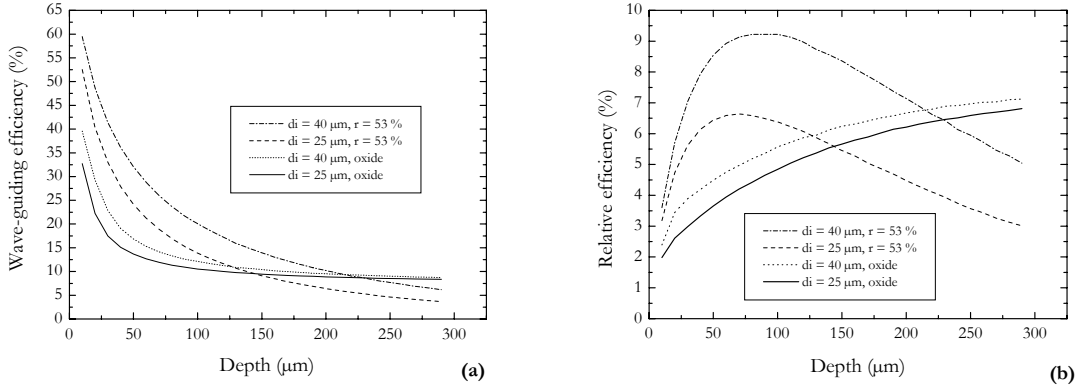
Figure 3.6 (a) Wave-guiding efficiency and (b) relative efficiency (including X-ray absorption) as a function of pore depth for two different pore diameters (di = 25 and di = 40 μm) and two different coatings (oxide and metal with r = 0.53). The absorption coefficient is $\alpha = 65$ cm^{-1}.

These curves show that for a metal-coated pore there is an optimum pore depth (e.g. ~ 80 μm for d = 40 μm and r = 53 %, from Fig. 3.6). On the other hand, for oxidized pores the relative efficiency increases with depth. A pore depth of only ~ 100 μm has, however, important drawbacks on the SNR as will be treated later.

3.2.2. Criteria of evaluation

As mentioned earlier, the goal in developing new X-ray imaging detectors is to improve the image quality and, for medical applications, to reduce the X-ray dose. The two main parameters determining the image quality are the signal-to-noise ratio (SNR) and the spatial resolution. For dental applications, a SNR of 50 and a spatial resolution of at least 8 lp/mm are recommended. The dose should be kept to a minimum, 20 mR being considered as a normal exposure.

Here we can perform a simple calculation to check if these requirements can be achieved with a pixellated CsI(Tl) layer and standard conditions used in dentistry. A standard dental X-ray source operating at 60 kV would give a photon fluence of 1.2×10^{10} X-ray photons/cm^2/R, which is actually the case in our experimental conditions (see section 3.3 later). Considering only the statistical Poisson noise of the incoming X-ray photons, the SNR is defined as:

$$SNR = \frac{N}{\sqrt{N}} = \sqrt{N} \qquad \textbf{(Eq. 3.1)}$$

where N is the number of X-ray photons impinging the detector on one pixel.

If we assume to have a detector where 100 % of incoming X-rays are absorbed in each pixel, we can calculate the ideal SNR as a function of the pixel size (i.e. the active area) for a certain X-ray exposure. This is shown in Fig. 3.7 for an X-ray exposure of 10, 20 and 50 mR. This is an ideal case where the CCD pixel size is equal to the diameter of the CsI guide, and perfectly aligned. The SNR increases
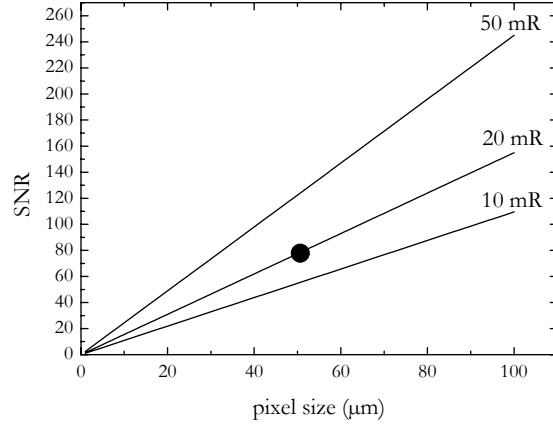
Figure 3.7 Ideal signal-to-noise ratio as a function of pixel size using our standard dental X-ray source at 60 kV (photon fluence of 1.2×10^{10} photons/cm²/R) for 100 % X-ray absorption and for three different exposures (10, 20 and 50 mR). The point shows that at 20 mR with a pixel size of 50 μm, a SNR of 75 can be obtained. A square pixel is considered and the CCD pixel size matches perfectly the diameter of one CsI guide.

linearly as a function of the pixel size since the number of photons (N) absorbed in one pixel is proportional to the pixel area, i.e. the square of the linear pixel size.

Assuming a square pixel with a width W (approximated to the pitch here), the maximal spatial resolution can be defined as $(2\,W)^{-1}$. Thus, the spatial resolution would be equal to 10 lp/mm (line pairs per millimeter) for a pixel size of 50 μm. As can be seen, this resolution is achievable at 20 mR for a SNR of ~ 75 (see the point in Fig. 3.7). Thus, the requirements given above are in principle achievable for an ideal pixellated scintillating layer with 100 % X-ray absorption.

Although the main source of noise is usually due to Poisson statistics of the incoming X-ray photons in scintillator-based detectors, there are other sources of noise. There is also the Poisson statistics of the secondary emitted photons from CsI(Tl). Depending on the uniformity of the Tl concentration in the CsI guide, the number of emitted photons may vary. In addition, there is the electronic noise, which may be due to the CCD and the electronic system. The treatment of fixed pattern noise (non uniformity in the detector response) is discussed in section 3.3.

Finally, note that one of the major advantages of the detector concept developed at KTH as compared to columnar CsI(Tl) films is that cross-talk between adjacent columns can be completely avoided due to absorption in the pore walls. As mentioned above, the upper limit of the spatial resolution of the detector is determined by the pore spacing and the size of the CCD pixel. Any mismatch would degrade the spatial resolution of the detector, but, in principle, very high spatial resolution can be achieved. The influence of the pore depth on the detector efficiency has been investigated experimentally and results are reported in appended paper 6 and in section 3.4. The pore wall thickness, or pore diameter, determines the active area. Thin pore walls are preferable for a large active area. However, the Si layer in the pore walls must be thick enough to absorb the refracted part of the rays that are not totally reflected and, therefore, guarantee a good spatial resolution. Pore arrays as depicted in Fig. 2.10a lead to an active area larger than 80 %.

3.3. Fabrication procedure

The fabrication procedure for a pixellated scintillating screen, as developed at KTH, is described in this section and is composed of (i) pore array formation by deep reactive ion etching or electrochemical etching, (ii) oxidation or metal deposition to accomplish a reflective coating for the pores to work as light-guides, (iii) filling with CsI(Tl) and polishing.

3.3.1. Pore array formation

Both electrochemical etching, as presented in chapter 2, and deep reactive ion etching (DRIE) are suitable techniques to form pore arrays in silicon. In general, these two techniques can be seen as complementary. On one hand, electrochemical etching allows high aspect ratio (up to 250) for a wide range of pore diameters (30 nm to more than 100 µm), but the mask has to be designed with regard to the silicon resistivity (or vice versa). Also, the pattern should preferentially be repetitive in order to have uniform distribution of the current lines. DRIE, on the other hand, allows more flexibility in terms of pattern but is limited to a maximum aspect ratio of about 20-25. In practice, the etching parameters depend on the used pattern, requiring optimization for the particular structure used.

DRIE is a kind of plasma etching where silicon atoms are chemically etched away due to the interaction with the species of the plasma. Following a photolithographic step defining the pattern in an oxide or a photo-resist layer, the process alternates between etching in a SF_6 plasma and passivation in a C_4F_8 plasma [4, 61]. Each cycle lasts for about 10 seconds. A polymer film is deposited on the wafer surface during the C_4F_8 plasma cycle and is used to protect the pore walls during the etching cycle. Pores grow perpendicularly to the silicon surface independently of the type (p or n), the resistivity and the crystallographic orientation, which may, on the other hand, affect the etch rate. As compared to electrochemical etching, DRIE leads to rougher pore walls. Figure 3.8 shows a pore array formed by DRIE.
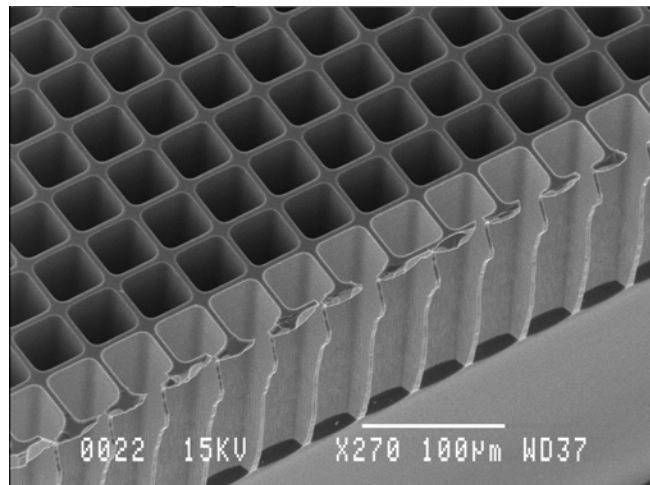

Figure 3.8 Pore array formed by deep reactive ion etching.

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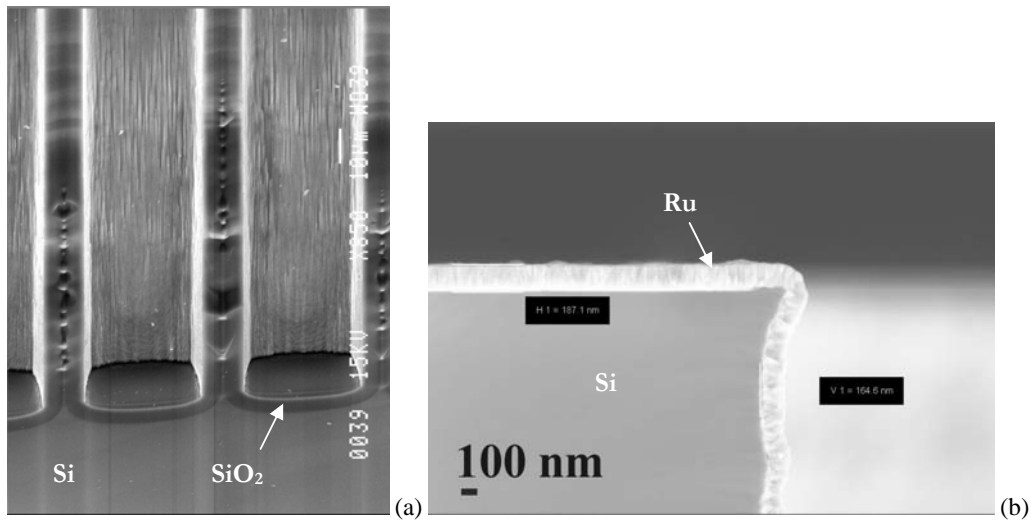
Figure 3.9 (a) Bottom of oxidized pore walls, (b) Top of a metallized pore wall (170 nm of Ru).

3.3.2. Reflective coatings on pore walls

As indicated in Fig. 3.3, the performance of the detector relies on efficient guiding of the secondary emitted photons towards the CCD pixels. Both oxide and metal coatings have been used to reflect the light emitted from the scintillator. For instance, a 2 μm-thick silicon dioxide layer (SiO_2) can be grown by wet oxidation at 1100°C for 9 hours. Other oxidation times were experimented but no significant change on the detector efficiency was noticed. Figure 3.9 shows a 5 μm-thick SiO_2 layer at the bottom of deep reactive ion-etched pores. Alternatively, atomic layer deposition (ALD) was employed to deposit Ruthenium (Ru) on the pore walls [62, 63]. A thin Al_2O_3 film is usually pre-deposited by ALD on the surface in order to improve adhesion of the metal layer. Typical thicknesses are in the range of 100 nm, as shown in Fig. 3.9. ALD is a good technique to provide conformal deposition on large areas and was performed at the Univ. of Helsinki through collaboration with Metorex. The reflection coefficient of the Ru layer, deposited on a planar substrate here, was measured to be 53 % at 550 nm, the emission wavelength of CsI(Tl). This is fairly low and limits the light guiding efficiency to a few reflections, corresponding to an ideal pore depth < 100 μm.

3.3.3. Pore filling with CsI(Tl) and CsI(Na)

The technique employed to fill the pores is described in appended paper 4. The idea is to melt CsI powder into the pores. Thus, apart from its appropriate emission wavelength and good X-ray absorption, CsI was chosen for its low melting point as compared to silicon (621°C and 1410°C, respectively). The forces effective

in this process are gravity and the capillary force, demanding the CsI melt to wet a bare or oxidized silicon surface. The sample is immersed in the CsI liquid (621°C) for a few minutes to ensure a complete filling of the pores and then cooled down at around 10 °C/min. The dependence of the detector efficiency as a function of cooling rate shows an optimal value at about 10 °C/min. A spring maintains the sample in thermal contact with the sample holder (Fig. 3.10), also avoiding a floating of the sample on top of the melt. This setup is installed in a hermetic chamber to perform the process in nitrogen (N_2) ambient. Once the cooling phase is over, any residual CsI(Tl) on top of the sample is removed mechanically. This polishing procedure requires special precautions because of the fragile structure of the matrix and because CsI dissolves in most liquids. Silicon oil or ethylene glycol may be used. SEM images of filled pore arrays are shown in Fig. 3.11. As can be seen, CsI is a very soft material. This does not make easy the evaluation of the filling quality, since any void in the CsI crystal may be due to a non-complete filling or may have fallen out during sample cleaving. Photoluminescence can be used to reveal the defects present in the CsI waveguides [57]. As gas bubbles were suspected to create voids in CsI, some experiments were performed under vacuum. Unfortunately, sublimation of CsI occurred before 600°C and the scintillator was deposited on the glass window of the chamber. Thus, all experiments were done in nitrogen ambient in order to properly fill the pores. It has also been observed that CsI is not always in complete contact with the pore wall. The diminution of the CsI volume during cooling, due to the different thermal expansion coefficients, may explain this gap.
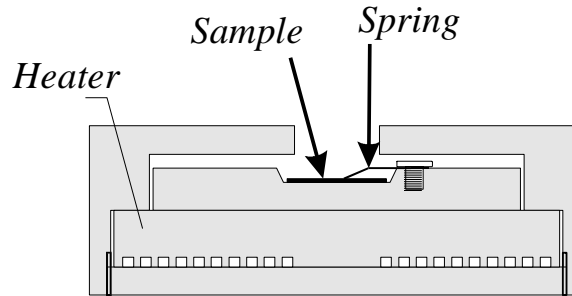

Figure 3.10 Sample holder used for filling pore arrays with CsI(Tl) and CsI(Na).
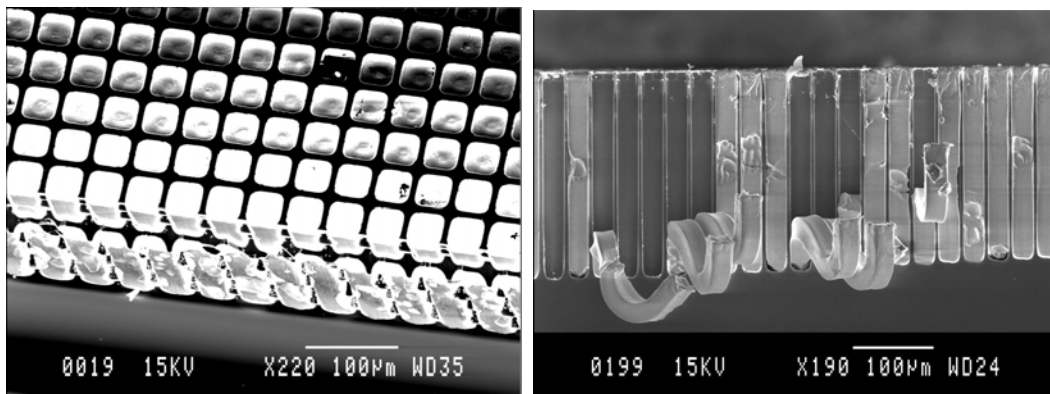

Figure 3.11 SEM of pore arrays filled with CsI(Tl).

3.4. Characterization

3.4.1. X-ray testing

As illustrated in Fig. 3.3, the scintillating screens are then mounted (upside down, if considering the pore openings as the upper side) on top of a silicon CCD in order to evaluate the performance of the detector. An optical fiber plate is placed between the CCD and the scintillating screen in order to protect the CCD from direct X-ray exposure. Also, optical oil can be used to improve light coupling between the scintillating screen and the optical fiber plate. The spectral sensitivity of the used CCD is well adapted to the wavelength range 500-750 nm [64]. The X-ray source is a standard dental source (Planmeca Prostyle Intra dental X-ray unit) operating at 60 kV, giving a photon fluence of 1.2×10^{10} photons/cm²/R [65, 66]. The spectrum shows a peak at 30 keV and spreads from 15 to 55 keV. Since the scintillating screens do not cover completely the CCD, part of the images could be used to measure the performance of the CCD without the gain induced by the secondary photons emitted from the screen. A gain correction of each individual pixel signal is performed in order to reduce fixed pattern noise in the image. A gain map, essentially a matrix of correcting coefficient factors, is obtained. Fixed pattern noise can originate from structural defects of the scintillating screen as well as from non uniformity in the CCD [64]. Fig. 3.12 shows both the original and the corrected image (original image divided by the gain map) from the detector. The output signal of the detector is measured as the mean signal of the histogram taken over a region of interest. The signal-to-noise ratio is calculated as the mean signal divided by the standard deviation for a certain area of the image [64].
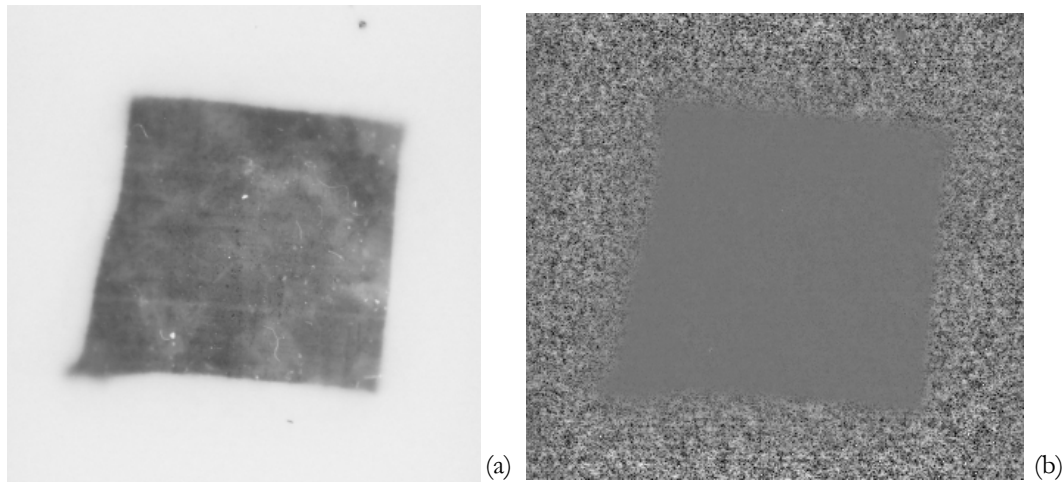

(a)   (b)

Figure 3.12 X-ray image without object (a) before and (b) after gain correction, showing a much reduced fixed pattern noise. The square (distorted due to non-uniform cleavage) corresponds to the image produced by the scintillating screen in proximity of the CCD. The periphery is the image from the CCD only.

3.4.2. Detector efficiency

- *Influence of CsI doping*

Both CsI(Tl) and CsI(Na) were used to fill the pore arrays. Although CsI(Na) has a higher light output, higher efficiencies have been obtained with CsI(Tl) for similar type of pore arrays. One of the reasons may be the more appropriate emission wavelength of CsI(Tl) to the CCD sensitivity since the relative sensitivity of this particular CCD is ~ 5 % and 75 % at 420 and 550 nm, respectively [64].

- *Influence of the reflective coating*

The efficiency of oxidized and metallized pore arrays has been compared. First, the *relative efficiency* is calculated taking into account the number of X-rays absorbed in CsI(Tl) and the *wave-guiding efficiency*, as described in section 3.2. Then, a *total efficiency* is defined as the multiplication between this *relative efficiency* and the active area of the detector. Ru and SiO_2 have been used (appended paper 5). Theoretical calculations for a pore diameter of 38 µm predict an optimal efficiency for a pore length of about 80 µm for pore walls coated with Ru, whereas a plateau is reached at about 300 µm for oxidized pore walls (Fig. 3.13). Indeed, as oxide is used to guide the secondary photons, for very deep pores most of the X-rays are absorbed in CsI(Tl) and the main part of the collected photons is that of totally reflected rays. On the other hand, a peak is observed for metallized pore walls since very deep pores lead to a large amount of absorbed X-rays in CsI(Tl), but also losses in the wave-guiding process. This is largely due to the fact that the reflectivity of metals is far from ideal. An example is Ru, where the reflective coefficient is as low as 53 %, clearly leading to a fast loss after only a couple of reflections. Experimentally, all scintillating screens using metallized pore walls showed lower performance than those using oxidized pore walls (Fig. 3.14). This was finally not surprising since all the tested screens had pore depths larger than 200 µm, which is preferable for oxidized pore walls.
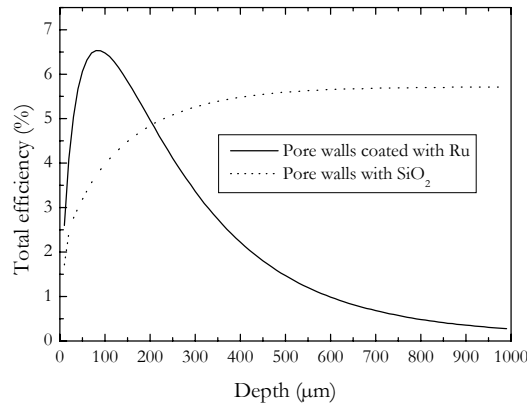

Figure 3.13 Theoretical predictions of the total efficiency of scintillating screens using either Ru (reflection coefficient set to 53%), or oxide as a reflective coating on the pore walls. The total efficiency is given as a function of pore depth for a pore diameter of 38 µm and a pitch of 45 µm.

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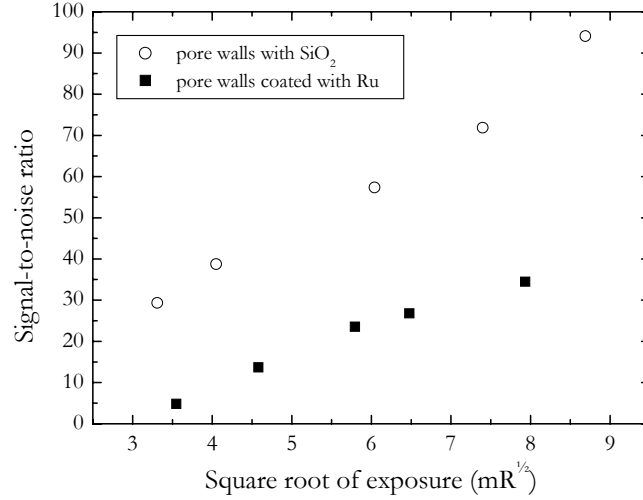
Figure 3.14 Measured signal-to-noise ratio as a function of square root of exposure for screens having pore walls coated with SiO_2 (blank circles) and Ru (filled squares). Data correspond to two of the best detectors of each type.

- *Influence of the pore depth*

The study of the detector performance as a function of pore depth has not been possible for metallized pore walls in this thesis. However, this study has been done with a large series of electrochemically-etched samples having oxidized pore walls (appended paper 6). The pore pitch is either equal to 30 μm or 45 μm, corresponding to pore wall thicknesses of about 4 μm and 6 μm, respectively. Data are shown in Fig. 3.15 and were compared to the ideal signal-to-noise ratio "SNR_{ideal}" (or input SNR), which is calculated from the Poisson statistics of the incoming X-ray photons as:

$$SNR_{ideal}^2 = N_0 \times [1 - \exp(-\alpha \times d)] \qquad \textbf{(Eq. 3.2)}$$

where d is the CsI(Tl) thickness (or pore depth), $\alpha = 65$ cm^{-1}, and N$_0$ is the number of incident X-ray photons in the integration time, which is obtained by multiplying the X-ray photon fluence, the pixel area and the X-ray exposure. Note that a correcting factor, sometimes called the "Swank factor", has to be included in this calculation in order to take into account three effects: (i) the incident X-ray energy distribution, (ii) the absorbed energy distribution due to variable absorption processes in CsI and (iii) the unequal light propagation from different part of the scintillator. However, this correcting factor is equal to 1 at 30 keV for CsI [67].

As the CCD pixel pitch is 45 μm and the pore walls cover part of the effective pixel area, an active pixel area of 39×39 μm² and 37×37 μm² was

considered for the arrays with 45 and 30-µm pore pitch, respectively (two pore walls may cover the CCD pixel in the case of arrays with a 30-µm pore pitch). As can be seen in Fig. 3.15, SNR_{ideal} increases rapidly for the first 200-µm to finally reach a maximum value for deep pores. This trend is also observed for the experimental 'SNR_o' (output SNR). This graphical comparison between SNR_{ideal} and SNR_o is a way of evaluating the detective quantum efficiency (DQE), usually defined as the square of the ratio between SNR_{ideal} and SNR_o [68]. Apart from one sample (sample Y in Fig. 3.15b), the other detectors have SNR_o values about two times lower than the SNR_{ideal}, implying a DQE of about 25 %. This indicates that there are losses in the detection. However, as sample Y shows a SNR_o value close to the theoretical limit, both good light output from CsI and good light collection efficiency in the waveguide can be achieved. Scanning electron microscopy was used to compare sample Y to the other samples, but no particular difference has been noticed. Electrochemically etched pore arrays are equivalent except for the pore depth; thus, we expect that good light collection is achieved in every sample. However, we suspect that the quality of the CsI(Tl), most probably the distribution of the Tl concentration in the crystal during melting and the re-solidification process, is better for sample Y.

(a)

(b)
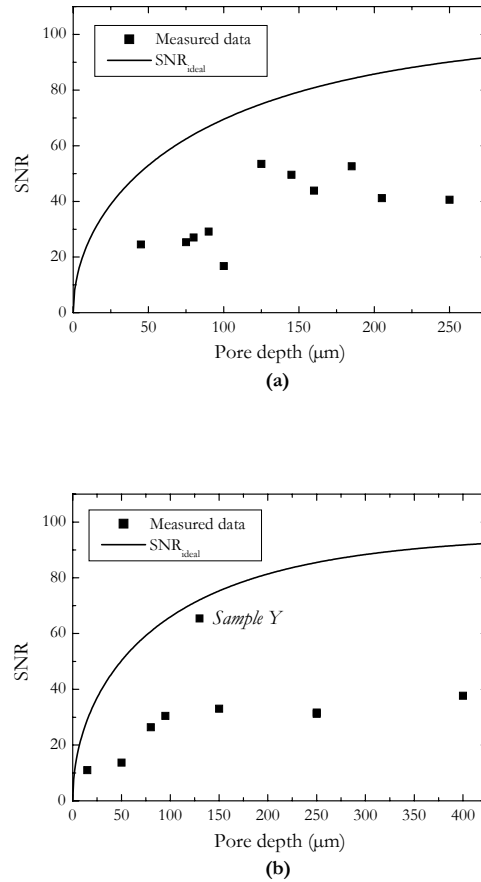
Figure 3.15 Signal-to-noise ratio as a function of pore depth for screens having oxidized pore walls and a pitch of (a) 45 µm and (b) 30 µm. Detectors were exposed to an X-ray exposure of 55 mR.

The output signal of sample Y was compared to a ~ 1-mm thick CsI(Tl) crystal (Fig. 3.16). The response of the detector is linear up to about 100 mR. For higher exposures, the detector would saturate as it is the case for the ~ 1-mm thick CsI(Tl) crystal at ~ 25 mR. At 16 mR, there is a factor 6 between the signal obtained from sample Y (signal = 32) and the CsI(Tl) crystal (signal = 190). In sample Y (130-μm deep pores, 30 μm pitch), about 10 % of the secondary emitted photons are detected (according to computer calculations) by the CCD pixels and ~ 60 % of incoming X-rays are absorbed (assuming $\alpha = 65$ cm^{-1}). Similarly, in the 1-mm thick CsI(Tl) crystal it can be assumed that 50 % of the secondary emitted photons are detected by the CCD and that 100 % of incoming X-rays are absorbed. This would lead to a factor of about 8.3, which is then rather close to the experimental result and proves that the light collection efficiency in the guides is as good as can be expected.
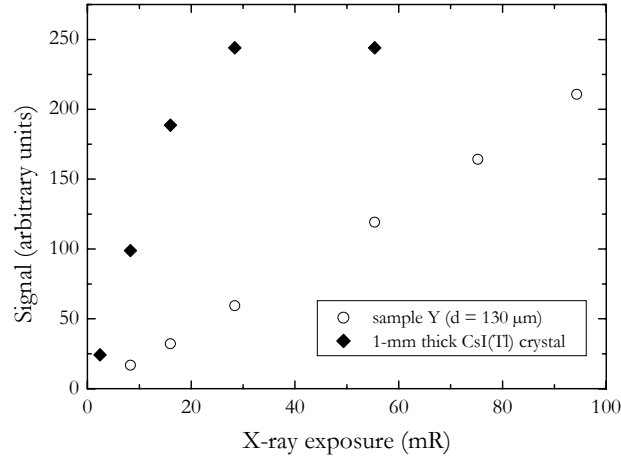
Figure 3.16 Signal as a function of X-ray exposure for sample Y (30-μm pitch, 130 μm deep pores) and for a ~ 1-mm thick CsI(Tl) crystal.
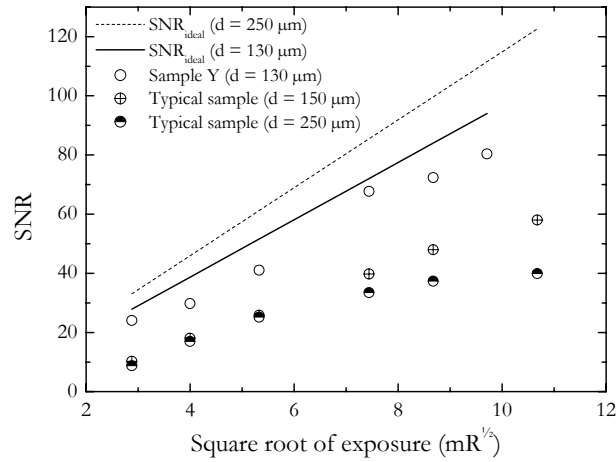
Figure 3.17 Comparison of SNR$_{ideal}$ with the measured SNR of screens having oxidized pore walls. The pore pitch is 30 μm and the pore depth is labeled as "d".

The dependence of the SNR on X-ray exposure is shown in Fig. 3.17 for detectors having the same pore pitch (30 μm) and different pore depths. In principle, the SNR depends on the pore depth and should be the same for identical pore arrays. Thus, for samples having a slight difference in pore depth (130 and 150 μm), the SNR values are expected to be quite similar. As can be seen, this is not the case, and this may be explained by the difference in CsI(Tl) quality from one sample to another. The linear dependence of the SNR on square root of the X-ray exposure is characteristic of Poisson noise. As mentioned in section 3.2, for dental applications the required SNR is 50 and the dose should be kept as low as possible, 20 mR being considered as a normal exposure [65]. For sample Y, a SNR of 50 is obtained at ~ 35 mR. However, sample Y has a pore depth of only 130 μm and a pore pitch of 30 μm, not matching perfectly the CCD pixel pitch. Hence, higher efficiency can in principle be obtained.

3.4.3. Imaging and spatial resolution

Images of different objects have been acquired in order to prove the viability of the detector concept (Fig. 3.18). These images clearly indicate that the structured scintillating screen improves the image quality as compared to the image given by the CCD only (periphery of the images). The spatial resolution can be evaluated using a metallic pattern as object. Here, a spatial resolution of ~ 8-10 lp/mm is achieved, depending of the subjective evaluation of the eye from images like Fig. 3.18c. A more accurate criterion would be based on MTF data (see next page).

Figure 3.18 X-ray images of (a) metallic screws, (b) an integrated circuit, and (c) a metallic pattern, enabling to estimate the spatial resolution (here ~ 8-10 lp/mm).

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The modulation transfer function (MTF) calculations were based on a method presented by Fujita [69] using the image of a 10-μm wide slit, a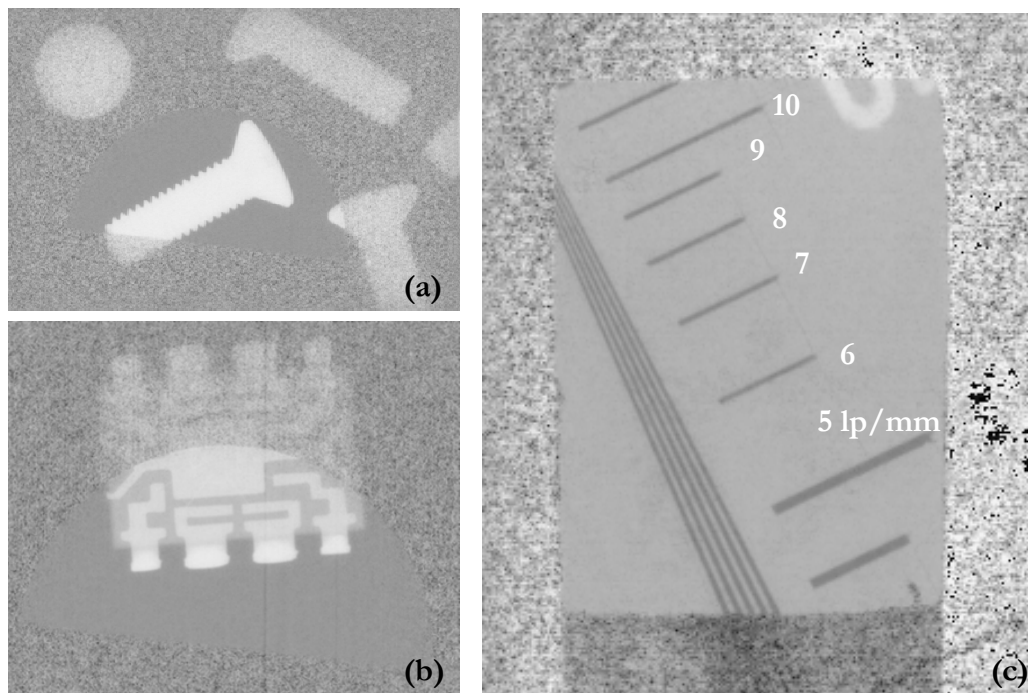s shown in Fig. 3.19a. The MTF is calculated as the Fourier transform of the slit profile, also called the line spread function (LSF). In this method, the profile is taken along a column, i.e. in the direction almost parallel to the slit, rather than along a row (i.e. almost perpendicularly to the slit). Consequently, the profile of the slit is more spread and a smaller effective pixel size has to be considered. This enables to get a profile with more densely spaced data points. The correction factor is estimated from the slit angle. Practically, this angle is obtained by measuring the number of pixels separating maximums of profiles taken along neighboring columns. In the case of the image shown in Fig. 3.19a, the maxima of two neighboring vertical profiles are spaced by 22 pixels. As the actual detector pixel size is 45 μm, the corrected pixel size is 2.04545 μm. The LSF shown in Fig. 3.19b is in fact the average signal from three neighboring profiles, which has also been normalized (and shifted to a common maximum). The MTF can then be calculated from these original data or from the data of the Gaussian fit, as presented in Fig. 3.20. This is achieved by a normal Fourier transform into the spatial frequency plane. The MTF represents the modulation of the signal as a function of the spatial frequency in cycles per mm (or spatial resolution in lp/mm). Usually, the spatial resolution of a digital imaging device is estimated at a modulation of 10 %. As can be seen, this is achieved at a spatial resolution of approximately 8 lp/mm here. The difference between the MTF obtained from the Gaussian fit and the original data is negligible except at high spatial resolution values, where the data of the Gaussian fit gives a smoother MTF. Higher spatial resolution could, in principle, be achieved but this would require a perfect match between the pore pitch and the CCD pixel pitch.
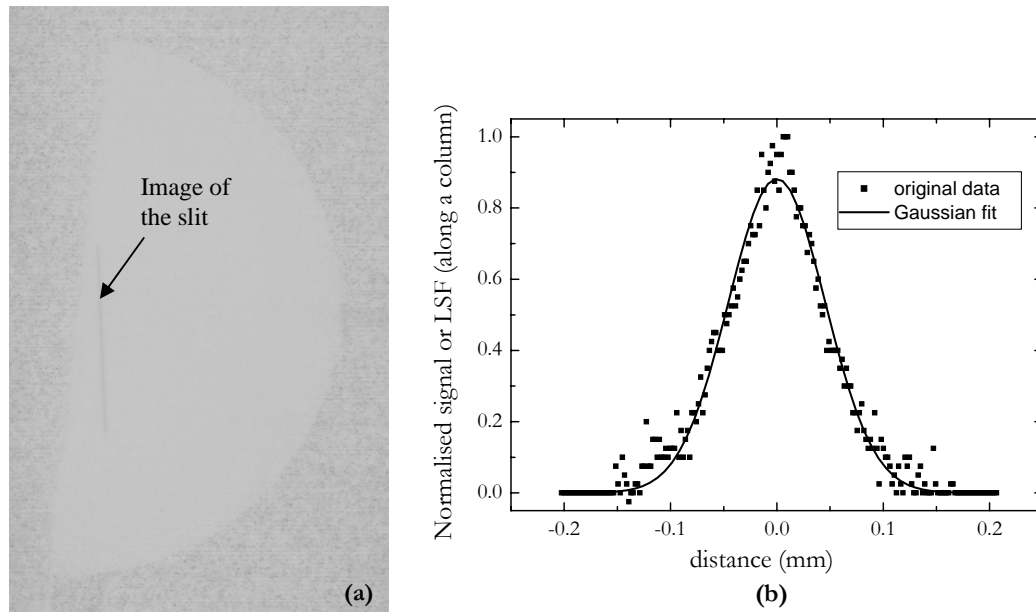
Figure 3.19 (a) X-ray images of a 10-μm wide slit and (b) line spread function (LSF) extracted from the image of the slit. The profile shown is taken along a column and the values of the x-axis are therefore corrected. The scintillating screen was a pore array with a pitch of 30 μm. As the CCD pixel pitch is 45 μm, the conditions are not optimal.

(a)

(b)
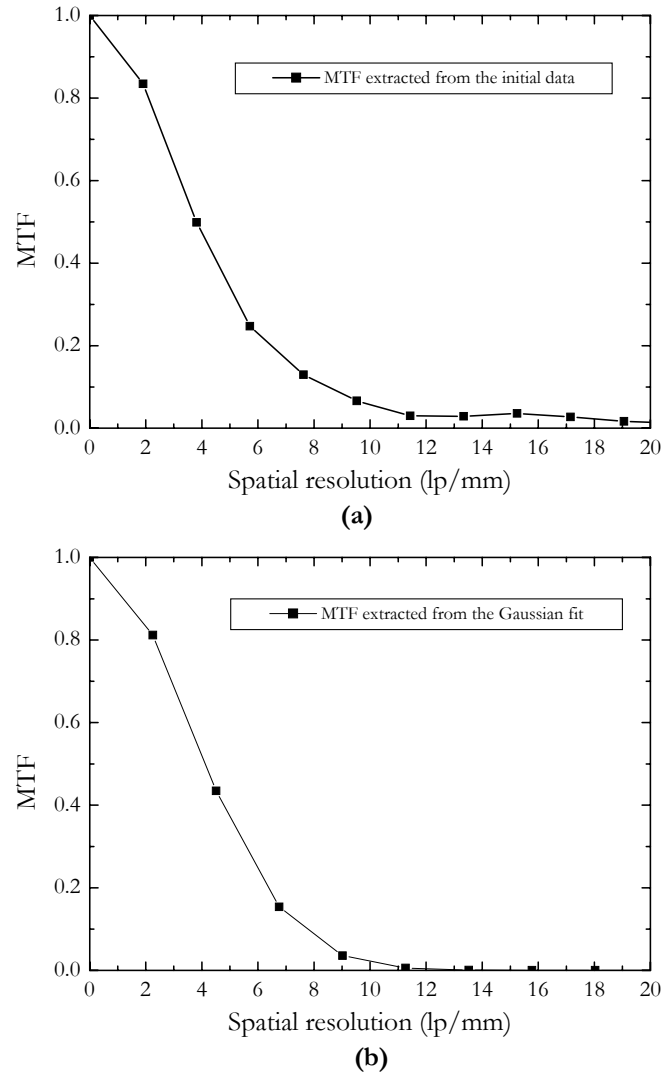
Figure 3.20 MTF extracted from the image and the data presented in Fig. 3.19 using (a) the original data and (b) the data of the Gaussian fit. The spatial resolution obtained at 10 % modulation is estimated to ~ 8 lp/mm.

Chapter 4   Pixellated detectors with vertical *pn* junctions

4.1. Detector concepts

4.1.1. CsI-photodiode structure

- *Principle of detection*

As an alternative to the previous detector concept, a new design including *pn* junctions in pore walls has been proposed (Fig. 4.1). Most of the X-ray photons pass through the top silicon layer and are absorbed in the CsI(Tl) columns, emitting photons at a wavelength of 550 nm. These secondary emitted photons are then captured by photodiodes located in the pore walls. The electrical signal, i.e. the accumulated charge in each pixel, then needs to be readout by a special read-out-chip in proximity with the CsI-photodiode structure (normally bump-bonded). This concept differs from the CCD-based detector since the secondary emitted photons do not have to be guided along the pore depth. This approach would increase the charge collection efficiency since the secondary photons are detected very close to where they are generated. One of the challenging steps in the detector fabrication is the formation of vertical *pn* junctions, working as photodiodes in the pore walls. The detector concept is quite general and filled with other materials, sensitive to other radiation, it may have several imaging applications. One such application is as a neutron imaging detector, as explored in the 3D-RID project. In this case a neutron converter, LiF, is used [70, 71].

- *Photodiode*

A photodiode is a light sensitive device, which is basically a *pn* junction operated under reverse bias [46, 47]. It can be composed, for instance, of an n-type substrate and a p-type (boron doped) region located at the surface. A space charge region (SCR) forms at the *pn* metallurgical junction under reverse conditions. When photons strike the diode, electrical charges (electron/hole pairs) are generated (see

photo-generation in section 3.1). If the charges are created in the SCR, they are separated by the electric field and then drift to the contacts to finally create a signal in the external circuit (*photocurrent*). If the charges are created in the neutral n or p-type regions, they may recombine. However, if they are generated within a diffusion length from the SCR, they can diffuse into the SCR and be accelerated by the electric field, thus contributing also to the photocurrent (Fig. 4.2). The photocurrent is relatively small as compared to the forward current of the *pn* diode, but significantly higher than the reverse current in darkness (Fig. 4.3).
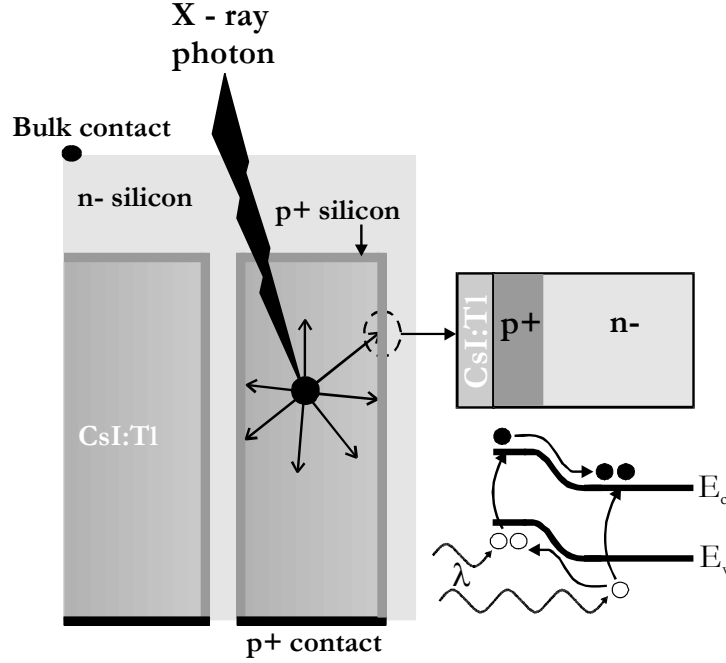
Figure 4.1. Principle of the "CsI-photodiode" detector.
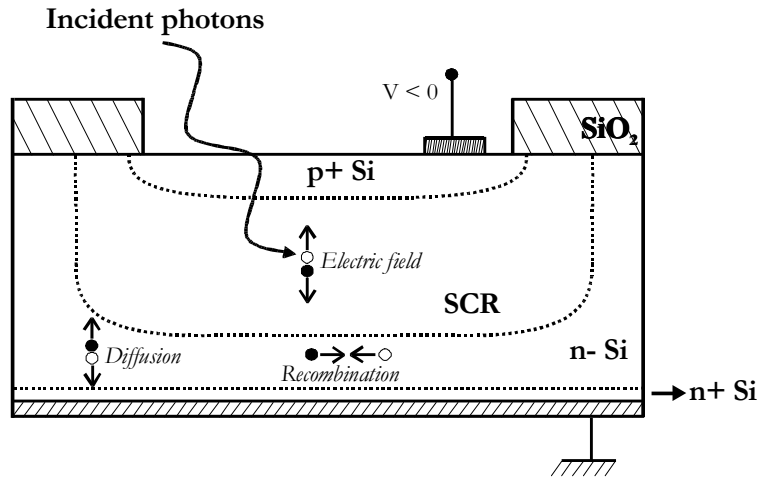
Figure 4.2 Cross-section of a *pin* photodiode under illumination.

The geometrical characteristics and the doping levels of the photodiode control its efficiency, spectral sensitivity, and response speed. For instance, the efficiency depends on the SCR width, which should preferably be large in comparison with the absorption length of the particular wavelength used for detection. The SCR width W of a silicon *pn* junction is expressed as:

$$W = \sqrt{\frac{2 \times \varepsilon_{Si} \times \varepsilon_o}{q} \times \left(\frac{1}{N_A} + \frac{1}{N_D}\right) \times (V_{bi} - V)} \quad \textbf{(Eq. 4.1)}$$

where $q = 1.6 \times 10^{-19}$ C, V is the applied bias, V_{bi} is the built-in potential in the diode (in the order of 0.6 V for a silicon diode), $\varepsilon_{Si} \times \varepsilon_o$ is the permittivity ($\varepsilon_{Si} \times \varepsilon_o = 11.9 \times 8.85 \times 10^{-12} = 1.053 \times 10^{-10}$ F/m), N_D and N_A are the doping levels in the n and p-type regions, respectively.

A low doping of the n-region, as compared to that of the p-region, will induce a large depletion layer. Therefore, the efficiency of the photodiode can be increased using a very low doped region (almost intrinsic) between the p^+ layer and the n^+ region (needed for ohmic backside contact); it is called a *pin* diode (Fig. 4.2). On the other hand, for high response speed, a thin SCR is needed in order to reduce the transit time of carriers. Thus, there is a tradeoff on the SCR width between high efficiency and optimal response time. It is also necessary to have thin p^+ and n^+ layers in order to reduce absorption in these regions. An example of the spectral response of a silicon photodiode is shown in Fig. 4.3. For this photodiode, maximum detection efficiency is achieved around 875 nm.

Figure 4.3 (a) Dependence of the photodiode reversed current on light intensity and (b) example of the spectral response of a silicon photodiode [72].

4.1.2. Semiconductor-based detectors

- *Planar detector*

Semiconductors can also be used as detecting materials in X-ray imaging sensors. Figure 4.4 shows a relatively simple planar detector, which consists of a *pn* junction operating under reverse bias [73]. The electrical charges, created in the semiconductor under X-ray exposure, are separated by the elect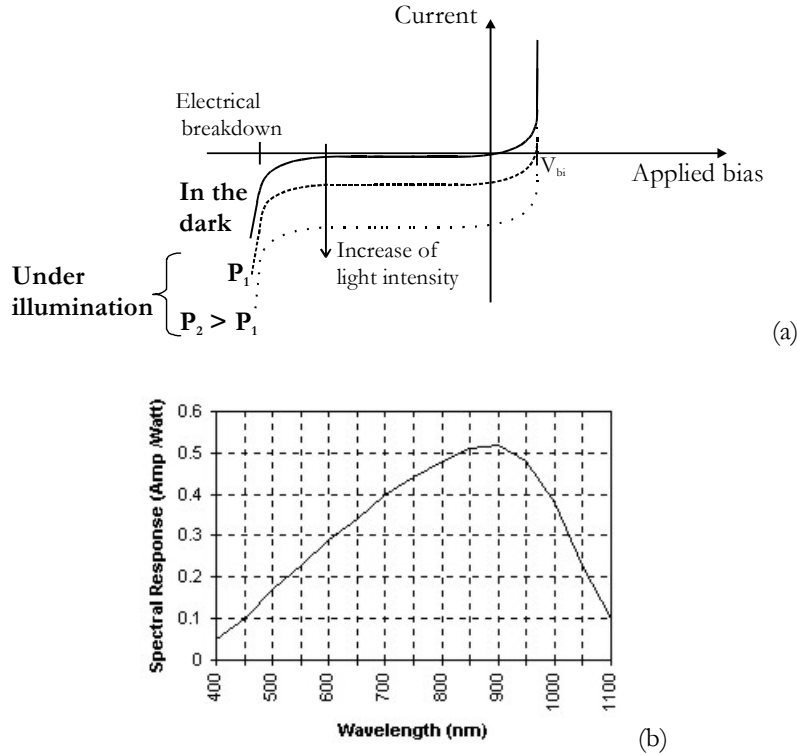ric field of the SCR and are then collected by electrodes, placed on the front and the back sides of the semiconductor. The potentials applied to the electrodes serve to deplete the semiconductor, ideally on all its thickness. Several semiconductors can be used to detect X-rays. The properties of some of them are given in Table 4.1, where the absorption length required to absorb 80 % of X-ray photons coming from a standard dental source (30 keV) is given. High atomic number and density values are needed for a high stopping power, as the absorption of X-rays essentially scales with the electron density in a material. The mass absorption coefficients, used to calculate the absorption lengths presented in Table 4.1, were taken from Ref. 74. Another important selection factor is the status of the material technology and the possibility to grow high quality crystals (high purity, high resistivity). Thus, despite poor stopping power, silicon is often used as it has the most advanced technology. Competitors of silicon, such as GaAs, CdTe (or even CdZnTe) and SiC, still suffer from their poor crystal quality and less-advanced processing technology. However, the growth of these materials is currently under development and recent advances on crystal quality have been reported [75, 76]. There are also other materials that may be used in X-ray imaging detectors, such as lead iodide (PbI_2), which presents promising properties [77, 78].

- *'3D' detector*

One of the drawbacks in the planar detector concept is the high voltage required to deplete the entire semiconductor thickness, which is in the order of 200 V for a 200-μm thick, low-doped silicon detector. Furthermore, due to the damages created in the material during X-ray exposure, a potential of 2000 V would be required to deplete the same 200-μm thick planar detector after 10 years of use [79]. The bias needed to fully deplete the detector is proportional to the square of the distance between the electrodes (see Eq. 4.1), and the collection time is proportional to the distance.

A new detector design has been proposed by Sherwood Parker [12] to reduce the distance between the electrodes while keeping a large sensing volume. The detector was termed '3D', as it is based on a three-dimensional structure, namely a silicon pore array having electrodes in each pore (Fig. 4.4). The electrical charges generated in the semiconductor under radiation are separated by the electric field, now in the horizontal direction, and collected at the electrodes made in the pores. This design enables to significantly reduce the distance between the electrodes without reducing the detector sensitivity. Consequently, after 10 years of operation,

a 200-μm thick '3D' detector with 20 microns spacing would only require 20 volts and not 2000 V, as it is predicted for a 200-μm thick planar detector [3]. Also, the need for high-quality material is significantly relaxed as the doping density can be significantly higher. As opposed to the previous concepts, very deep and narrow holes should be made for optimal active area and volume. Apart from drilling the holes, one of the challenging processes in the fabrication of a '3D' detector is the formation of junctions in the pores. In 1982, T.R. Anthony already studied such type of structures using laser drilling to make pore arrays in silicon and diffusion from liquid and gaseous sources to dope the pore walls [80]. In more recently published works, diodes were fabricated either by metal deposition on laser-drilled pore walls in order to form Schottky contacts [81], or by filling pores made by DRIE with p- and n-type doped poly-silicon in order to form *pn* junctions [12, 82]. In this work, the formation of *pn* junctions in electrochemically etched pore arrays was studied and is presented in next sections.

Table 4.1 Characteristics of some semiconductors used for X-ray imaging.

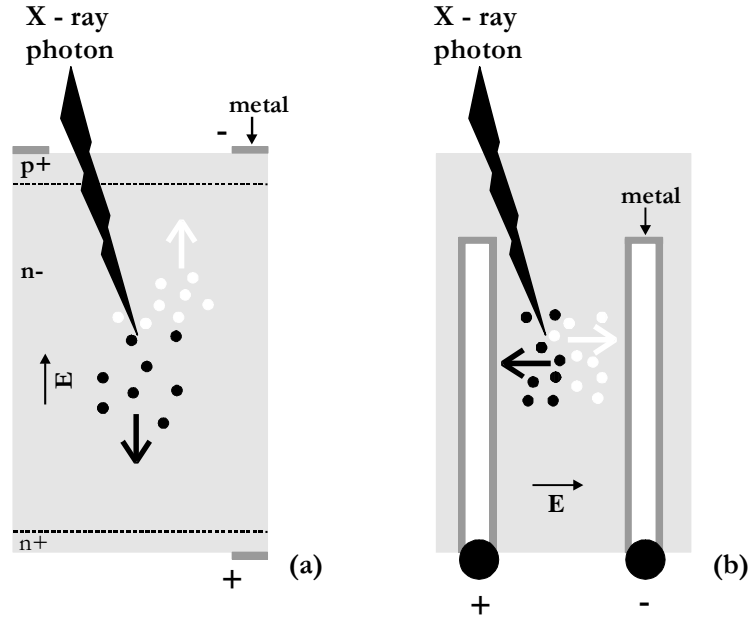|	Si	GaAs	CdTe
Atomic number Z	14	$Z_{Ga} = 31$ $Z_{As} = 33$	$Z_{Cd} = 48$ $Z_{Te} = 52$
Density (g/cm³)	2.3	5.3	5.8-6.06
Band gap (eV)	1.12	1.43	1.5
Thickness (μm) required for 80 % absorption at 30 keV	~ 5000	~ 220	~ 125

Figure 4.4. Schematic of semiconductor-based detectors: (a) planar detector, (b) '3D' detector.

4.2. Doping techniques and characterization

In a first study, the formation of silicon *pn* junctions in thin pore walls (about 3-5 µm thick) was investigated to fabricate the CsI-photodiode structure. Two techniques were employed: diffusion [80, 83] and deposition of doped poly-silicon [84, 85]. In the literature, another technique has been reported for the doping of trenches or pore walls: plasma immersion ion implantation (PIII). PIII is a technique where the sample is immersed in a plasma containing the dopants and biased in order to attract the charged ions. The technique is rather advanced, requires good control of the parameters and enables doping of trenches with aspect ratio up to 12 [86-89].

4.2.1. Boron diffusion

Boron diffusion was performed by mounting vertically the pore array wafers facing boron source wafers in a furnace [90, 91]. The initial pore arrays were formed in n-type silicon by electrochemical etching. A first diffusion was performed at 1150°C for 105 min in a nitrogen atmosphere. During the temperature ramp down in an oxygen atmosphere a thin oxide layer formed. This was to prevent out-diffusion of boron. The oxide was then removed in hydrofluoric acid. Figure 4.5 shows a scanning electron micrograph of the sample after diffusion. A ca. 3-µm thick layer, brighter than the bulk, can be seen at the bottom of the pores, and is most likely the diffused boron layer [92]. Scanning spreading resistance microscopy (SSRM) was used to confirm this observation. SSRM is an extension of the atomic force microscopy (AFM), which enables to image the topography of a sample by scanning its surface with a probe [93]. In SSRM, the spreading resistance is measured while scanning, and the doping distribution in the structure can be recalculated and imaged at the same time [94]. The doping distribution measured by SSRM is shown in Fig. 4.5, suggesting the presence of a ca. 3-µm thick, highly conductive layer at the pore bottom, in good agreement with the observation made by SEM. As can be seen from Fig. 4.5, the pore walls are completely doped with boron; thus, no *pn* junction has really been formed in the walls. However, this proves that doping by diffusion is possible.

The uniformity of the doping along the pore depth was analyzed by SIMS [95]. A cross-section of the sample was polished and mounted on the edge to enable SIMS sputter profiling. The profiles shown in Fig. 4.6(B) indicate that the doping levels are in the same order of magnitude along the pore depth ($\sim 5 \times 10^{19}$ cm^{-3}). For comparison, the same diffusion was performed in a planar sample (Fig.4.6(A)). A 6-µm thick layer with a maximum boron doping of 2×10^{20} cm^{-3} was measured. This higher doping level, together with the larger thickness, suggests that the transport of boron to the pore bottom limits the doping at this temperature. A second diffusion was performed at 1050°C for 70 min in a nitrogen atmosphere. The SIMS profile measured in a planar sample showed a boron layer reaching up to 2 µm with a
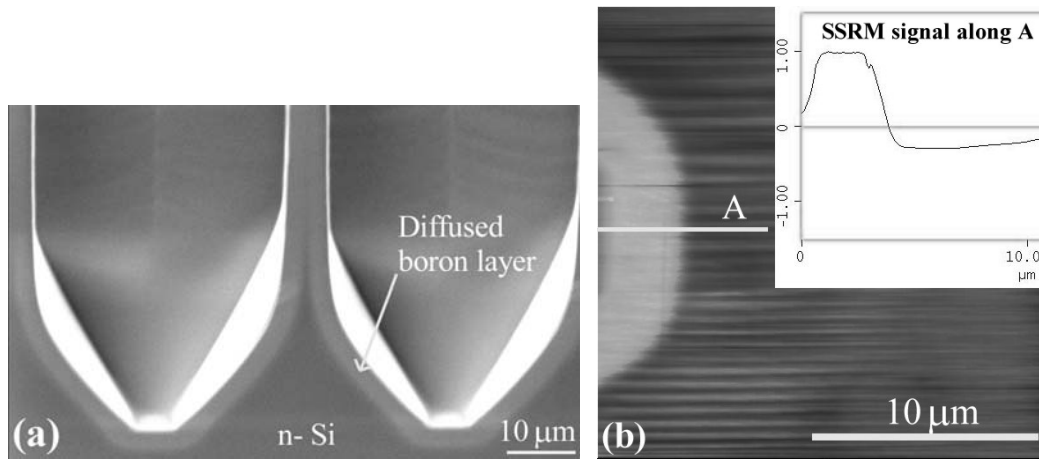
Figure 4.5 Bottom of pores after boron diffusion at 1150°C for 105 min observed by (a) SEM and (b) SSRM. These images reveal the presence of a highly conductive layer at the bottom of the pores. Note that the SSRM image has been rotated 90°, so that the pore bottom is visible as a light area (small resistance) on the left side. The profile along A is shown in the inset.

maximum boron doping of 2×10^{19} cm^{-3} (profile b, Fig. 4.6(A)). The SIMS profiles, taken along the pore depth, are shown in Fig. 4.6(C). The p$^+$ layers located on each side of the pore walls are clearly revealed in profile c. This time, the doping levels measured along the pore depth are in the same range as that measured in the planar sample. Thus, doping is not limited by the transport of boron in the pores in this case. Indeed, the key to uniform doping along the pore depth using diffusion is a sufficiently low temperature, such that the incorporation of dopants becomes surface reaction controlled.

4.2.2. Low-pressure chemical vapor deposition (LPCVD)

LPCVD of boron doped poly-silicon was performed at 600°C under a pressure of 150 mTorr in the presence of SiH$_4$ and B$_2$H$_6$ for 90 min [96]. The deposition was also done on a planar sample, whose SIMS profile is shown in Fig. 4.6(A), profile c. The layer is about 400 nm thick with a boron concentration of 5×10^{19} cm^{-3}. The boron doped poly-silicon layer deposited on a DRIE-etched pore array is shown in Fig. 4.7, indicating that the deposition is conformal. The presence of a *pn* junction at the pore bottom was also observed by SSRM and scanning capacitance microscopy (SCM). SCM is also a variant of the AFM technique, where the capacitance variation between the probe and the sample is measured while scanning [97]. As with SSRM, this enables to image the doping distribution in the structure. Pores having *pn* junctions in their walls can also be filled with CsI(Tl), as shown in Fig. 4.8.
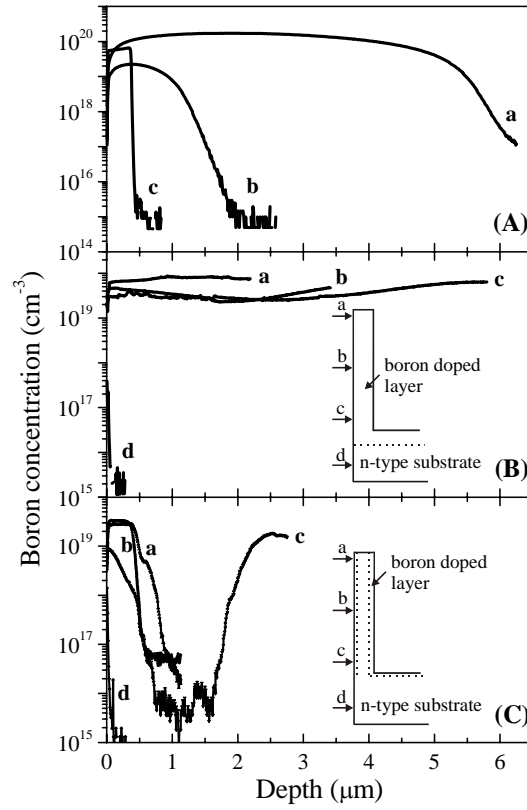
Figure 4.6 (A) Boron profiles for planar samples after diffusion at 1150°C for 105 min (a), diffusion at 1050°C for 70 min (b), LPCVD at 600°C for 90 min in presence of SiH_4 and B_2H_6 under 150 mTorr (c). (B, C) Boron profiles at different pore depths for etched matrices after diffusion at 1150°C for 105 min and after diffusion at 1050°C for 70 min, respectively.
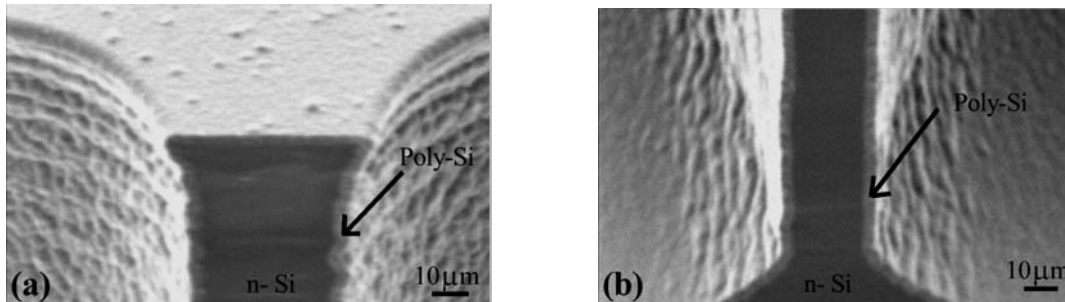
Figure 4.7 SEM images of a DRIE matrix after boron doped poly-Si deposition showing (a) the top of the pore and (b) the pore bottom.
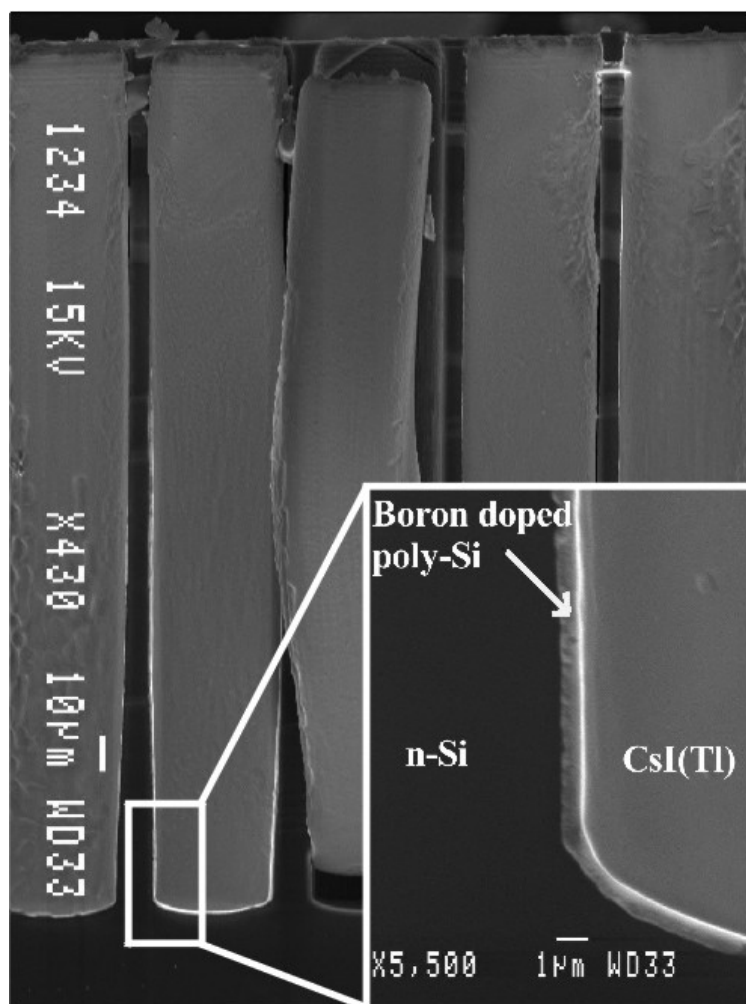
Figure 4.8 CsI(Tl)-filled pores with vertical *pn* junctions made by deposition of boron-doped poly-silicon.

4.3. Electrical characterization of vertical *pn* junctions

As mentioned earlier, simulations of the "CsI-photodiode" detector showed that a too large noise would be obtained [11]. Thus, the formation of *pn* junctions in pore walls was oriented to the fabrication of '3D' semiconductor-based detectors, i.e. towards pore arrays with small-diameter pores. A second study was carried out to electrically characterize *pn* junctions formed in thick pore walls by boron diffusion.

4.3.1. Formation of individual junctions

After doping of the pore arrays, the p^+ layer covers completely the front side surface connecting all pores electrically. For the use as an imaging, pixellated detector, the p^+ layer of each pore must be disconnected from neighboring pores. Two process flows were investigated to disconnect the junctions from one pore to another, as described in Fig. 4.9. The first consists of removing a few μm of silicon at the top of the sample using reactive ion etching directly after diffusion (Fig. 4.9, left side, last step). The second uses an oxide mask at the top of the pore walls as a barrier against boron diffusion. This masking layer remains after electrochemical etching in case of relatively short etching (Fig. 4.9, right side). Thus, the initial oxide layer would preferably be thick for both deep etching and use as a diffusion barrier. The samples of this study are shown in Fig. 4.10 and are called devices X and Y.

Figure 4.9 Illustration of the two process flows used to form individual *pn* junctions.

Figure 4.10 SEM of (a) device X and (b) device Y.
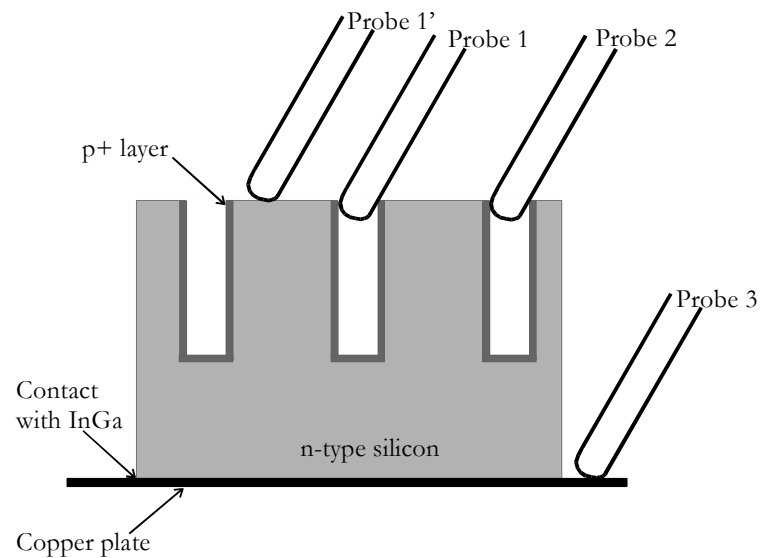
Figure 4.11 Configuration used to characterize the junctions.

Table 4.2 Specifications of devices X and Y.

	Device X	Device Y
P+ layer (Na, cm^{-3})	2×10^{19}	2×10^{19}
n-type substrate (Nd, cm^{-3})	1×10^{12}	1.3×10^{12}
Pore spacing (μm)	50	40
Pore diameter (μm)	12	10
Pore depth (μm)	275	115

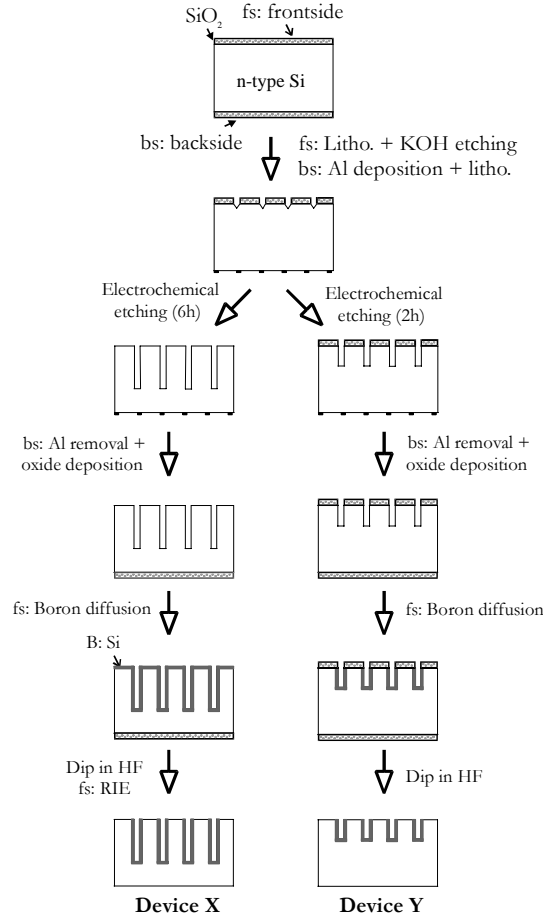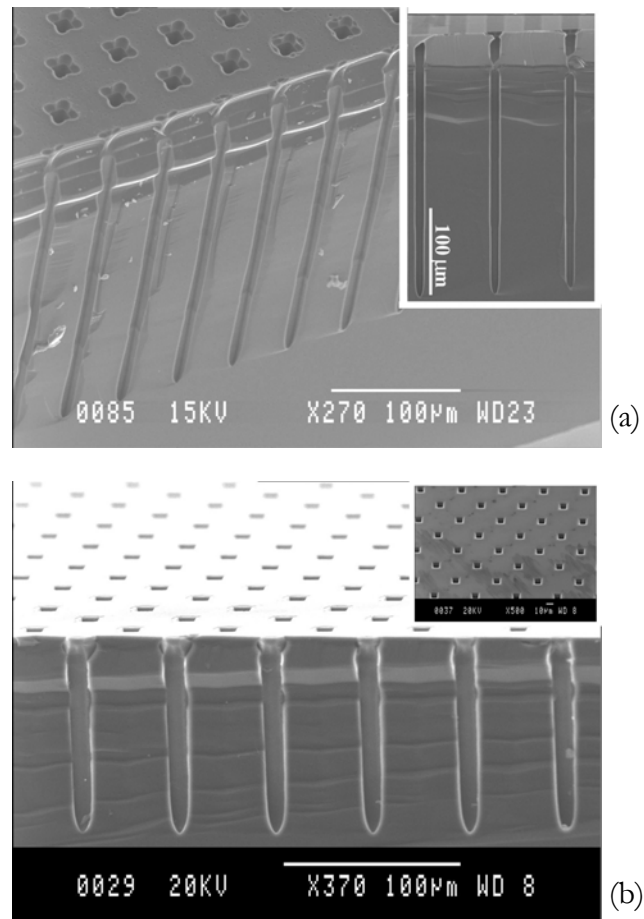Specifications of devices X and Y used in the discussion below are given in Table 4.2. The configuration used to characterize the junctions is depicted in Fig. 4.11. The ohmic backside contact is realized by applying eutectic (liquid) InGa at the silicon surface and the contact to the p$^+$ layers is achieved by probing down into the pore (probe 1). The probe can also be placed between two pores in order to contact the n$^-$ silicon. In addition, two junctions can be connected back-to-back by contacting two neighboring pores. Only the configuration using probes 1 and 3 is discussed here.

4.3.2.   *CV* and *IV* characteristics

- *CV characteristics*

Figure 4.12 shows the $1/C^2 = f(V)$ characteristics for devices X and Y (measured using probes 1 and 3). Usually, such graphs enable to extract the built-in potential at the junction and the doping level of the lowly-doped region, using the following equation valid for a one-sided *pn* junction with a lowly-doped n-type region [46]:

$$\frac{1}{C^2} = \frac{2 \times (V_{bi} - V)}{A^2 \times q \times \varepsilon_{Si} \times \varepsilon_o \times N_D} \quad \textbf{(Eq. 4.2)}$$

where A is the active area, $q = 1.6 \times 10^{-19}$ C, V is the applied bias, V_{bi} is the built-in potential in the diode (in the order of 0.6 V for a silicon diode), $\varepsilon_{Si} \times \varepsilon_o$ is the permittivity ($\varepsilon_{Si} \times \varepsilon_o = 11.9 \times 8.85 \times 10^{-12} = 1.053 \times 10^{-10}$ F/m), and N_D is the doping level of the low-doped n-type region.

However, the extraction of V_{bi} and N_D is only possible if the effective detected area is well known. Unfortunately, this area is not easy to estimate in our case. Moreover, the width of the SCR at 0 V bias is already larger than half of the distance between pores for both devices X and Y. The SCR at 0 V is 29 μm wide

for device X and 26 μm wide for device Y, as calculated from expression 4.1. In other words, the pore walls of both devices X and Y are already fully-depleted at 0 V. Thus, the *CV* characteristics were used in opposite mode to extract the area from which the signal emanates in reverse bias. From the curves presented in Fig. 4.12, the measured capacitances correspond to a diameter of 800 μm for device X and 1.1 mm for device Y. This suggests that the measured signal encompasses several diodes, apparently connected together via the SCR under reverse bias. Note that the SCR would shrink and tend to vanish under forward bias.
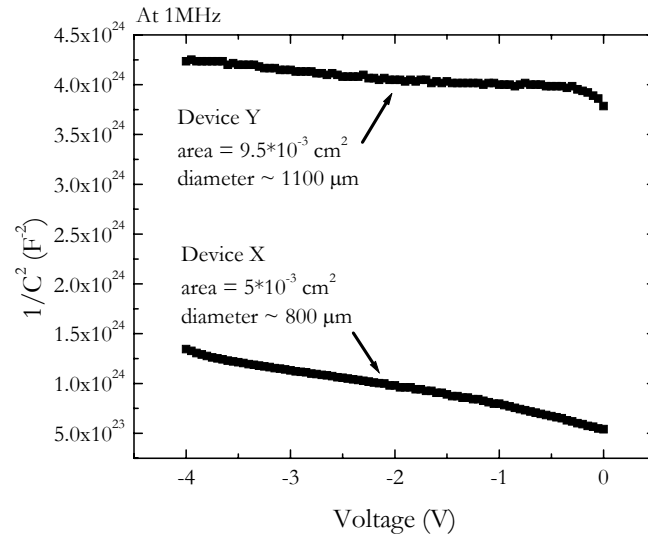
Figure 4.12 Extraction of the active area under reverse bias via the *1/C² = f(V)* characteristics.
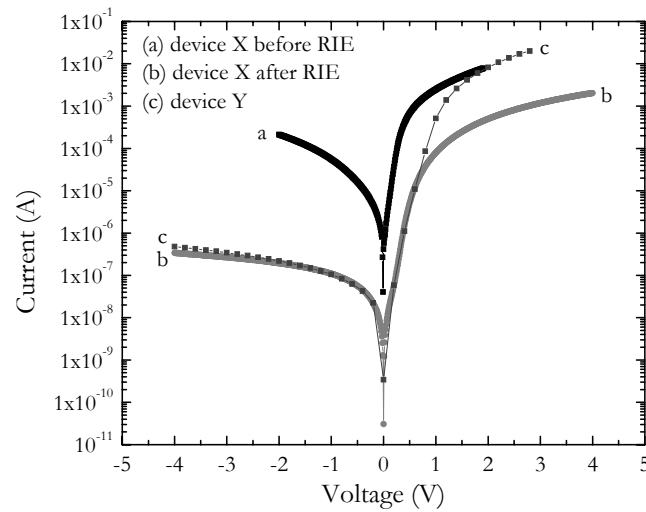
Figure 4.13 *IV* characteristics for devices X and Y.

- *IV characteristics*

Figure 4.13 shows the *IV* characteristics for device X before and after RIE. The forward and reverse currents measured before RIE (curve a) are orders of magnitude higher than that measured after RIE (curve b). Before RIE, all p$^+$ layers are connected at the top of the sample; thus, a large area contributes to the measured current. After RIE, on the other hand, the current would ideally come from one single diode (one pore). This is probably true in forward bias but, according to the previously presented *CV* measurements, the current measured in reverse bias originates from a larger area (800 µm in diameter). Yet, the reverse current is significantly reduced after disconnection of the diodes. Curve b illustrates well the rectifying behavior of device X with a reverse current of about 400 nA at - 2 V and a forward current of 1.5 mA at + 2 V. The *IV* characteristic of device Y (curve c) shows also a good rectifying behavior with a difference of about 5 decades between the forward and the reverse currents (420 nA at - 4 V and 25.5 mA at + 3 V). The threshold voltage for both devices is about 0.5 V, which is characteristic of a silicon *pn* diode.

IV curves were also taken for high reverse bias, showing a dramatic increase of the current at about - 10 V for device X, as can be seen in Fig. 4.14 (curve a). This sudden increase of the leakage current may be due to defects created at the surface of the sample during RIE. These surface defects may need a high reverse bias before they are reached by the SCR and start to contribute to the leakage current. The reverse current measured for device Y does not increase suddenly at - 10 V. Thus, although both process flows enabled the disconnection of the p$^+$ layers, the process without RIE gives superior device characteristics. Furthermore, the RIE process may have attacked the top of the pores in a lateral direction (the rim of pores), thus making difficult the realization of subsequent contacts to the p$^+$ layers. Also, there is a risk that the bottom of the pores has been damaged. As a conclusion, the process flow of device Y is a clearly better alternative.
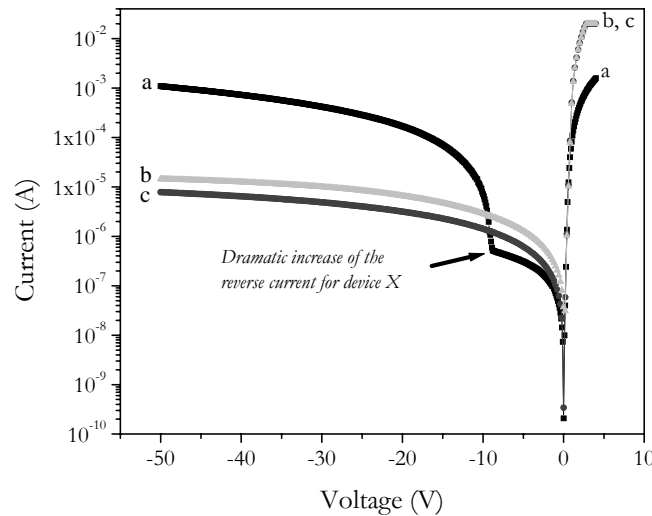
Figure 4.14 *IV* characteristics under high reverse bias for device X after RIE (curve a) and for device Y (curve c: in the dark, curve b: with illumination).

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- *Effect of light and other parameters*

Figure 4.14 illustrates also the sensitivity of device Y to light under reverse conditions. The diode was only illuminated with a weak halogen lamp, but an increase of the reverse current by a factor 2-3 can still be seen. This indicates that the structure could work as a detector for light or ionizing radiation.

The measurements performed on these devices are further discussed in appended paper 8. As regard to the functioning of the diodes, it has been shown that the junctions are in the high-injection regime under forward bias (V > 1V). This means that the measured serial resistance is much lower than the resistance calculated from the bulk. Measurements with probe 1' (see Fig. 4.11) yield linear *IV* curves and high resistances (no injection of carriers), demonstrating that the diodes are well disconnected from one pore to another. The ideality factors were found to be rather high (~ 2.6). These high values were attributed to surface recombination, as suggested by simulations. Passivation of the surface via oxide deposition, for instance, may improve the ideality factor. Connections of two neighboring pores in a transistor-like configuration showed that the current flowing from one pore to another could be controlled by the substrate bias. This demonstrates that a *pnp* structure has, indeed, been formed between pores; however, the base is very large and a gain of only 0.8 was observed.

Chapter 5   Summary

5.1. Guide to the appended papers

The appended papers of this thesis are organized in three categories, supporting the results presented in chapters 2, 3 and 4, respectively. Silicon electrochemical etching has been studied in papers 1 to 3, CCD-based X-ray detectors using scintillating screens in papers 4 to 6 and pixellated detectors with vertical *pn* junctions in papers 7 and 8. The purpose and the main achievements of each article are summarized below. As a first author in seven of the appended papers, the contribution of the author comprises planning, sample preparation, characterization, data analysis, simulations (apart for the program used for wave-guiding efficiency calculations which was developed by Pascal Kleimann) and writing of the manuscript. As a second author in paper 3, these tasks were shared more or less equally with the first author.

Silicon electrochemical etching

- *Paper 1*

This paper reports a new method for electrochemical etching of low-doped n-type silicon. As the chemical reaction responsible for etching of silicon is only possible in the presence of electronic holes (positive charge carriers), etching of low-doped n-type silicon requires an external hole supply. Usually, photo-generation is used and the technique is termed "photo-electrochemical etching". Here, electrochemical etching of n-type silicon using hole injection from a *pn* junction has been demonstrated for the first time. The technique is well adapted to high resistivity wafers as the diffusion length should be sufficiently large for the holes to reach the Si/electrolyte interface. The possibility to form pore arrays and other type of structures is shown.

- *Paper 2*

Formation of macropore array on the sub micron scale is reported in this paper. Pore diameters of ~ 150-200 nm have been achieved at a pitch of ~ 1-1.4 μm for depths up to 30-50 μm. The etching parameters were varied and their effects on the

pore shape were studied by scanning electron microscopy. Different resistivities were tested and a rather good relation to the macropore formation model proposed by V. Lehmann is shown [6]. Such pore arrays can be used as templates for the formation of advanced materials or as devices for ion-guiding. Since this study, another group has shown that pores as small as 30 nm could be etched in a breakdown regime [36], entering the category of "mesopores".

- *Paper 3*

Here the goal was to develop a cheap and easy technique to provide a silicon "nano"machining tool. Electrochemical etching of n-type silicon has been studied to form structures on the nanoscale (pillars, tubes and walls). Only two process steps are required: Lithography and Electrochemical Etching ("LEE" process). The lithographic step was made with a stepper, a common tool in silicon technology, in order to define sub-micron structures in a resist layer. The size of the etched structures is shown to scale with the silicon resistivity. Walls with a thickness of about 150 nm and pillars with a diameter of ~ 350 nm were achieved. This technique could be extended to the formation of structures on the nanoscale (< 100 nm), using appropriate resistivity and more advanced lithographic tools.

CCD-based X-ray detectors using scintillating screens

- *Paper 4*

This paper is chronologically the first (also first of all papers) of the three papers dealing with scintillating screens for CCD-based detectors. At this time, deep reactive ion etching was used to form the pore arrays and oxide was used as a cladding material on the pore walls. The study focuses on the detector fabrication with an emphasis on the filling process. The technique used to fill the pores is to (i) melt CsI(Tl) on top of the pores at 621 °C, (ii) wait until the pores are filled with the liquid and (iii) cool down to solidify CsI(Tl) in the pores. A hold time of about 5 minutes at the melting point and a cooling rate of about 10 °C/min were found to give relatively good filling. Characterization of the best detector showed an improvement of the signal-to-noise ratio as compared to previously processed prototypes. The study confirmed also that good spatial resolution in the range of 8-10 lp/mm could be achieved with this detector concept.

- *Paper 5*

In this paper the possibility to use a metallic layer on the walls of CsI(Tl)-filled pores was investigated. The use of a metal would change the wave-guiding property of the CsI(Tl) guides, and hopefully improve the detector efficiency. The deposition of metal (Ru in this case) was performed by Metorex, an industrial partner of the 3D-RID project. Pore arrays with pore depths in the range of 200-250 μm were used as it was believed that most of the incoming X-rays should be absorbed in CsI(Tl) for an optimal efficiency. Both oxidized and metallized pore walls were tested. These experiments showed that oxidized pore walls provide higher efficiencies, at least for the samples studied. Indeed, a more complete calculation of

the detector efficiency finally showed that the optimal pore depth for Ru-coated pore walls would be ca. 80 μm. This is largely due to the relatively low reflection coefficient of Ru which is only ~ 53 %. For oxidized pore walls, pore depths in the range 200-250 μm are preferable. The wave-guiding properties of metallized and oxidized pores are discussed.

- *Paper 6*

This is the last paper concerning CCD-based detectors. The goal is to provide a better understanding and complete characterization of scintillating waveguides using oxidized pore walls. As we specifically wanted to know how well the pores would waveguide the secondary photons, pore depths were varied from 40 to 400 μm. The filling procedure was performed by AST (Applied Scintillation Technologies), an industrial partner of the 3D-RID project. The dependence of the detector efficiency on pore depth is shown and indicates that the detective quantum efficiency of most of the detectors is about 25 %. This suggests that there are losses in the detection, which could be due to either poor wave-guiding of the secondary emitted photons or low light output from CsI(Tl). One detector, however, shows a much higher efficiency, approaching almost the theoretical limit. This proves that detectors with good wave-guiding efficiency and good CsI(Tl) crystal quality can be realized. It is concluded that the wave-guiding seems to work well, whereas the light output of CsI(Tl) for most detectors is significantly deteriorated, most likely because of loss of Tl during the melting process.

Pixellated detectors with vertical pn junctions

- *Paper 7*

The formation of *pn* junctions in pore walls was investigated for a new detector concept as an alternative to the CCD-based detector. The insertion of photodiodes in the walls of CsI(Tl)-filled pore arrays would result in high detection efficiency, as the secondary emitted photons do not have to be channeled to one end of the pore. Two doping techniques were tested to form these *pn* junctions: boron diffusion from a solid source and low-pressure chemical vapor deposition of boron-doped poly-silicon. The samples were analyzed by scanning electron microscopy, scanning spreading resistance microscopy and secondary ion mass spectrometry. The study shows that uniform vertical *pn* junctions can be formed with both techniques. The fabrication of a complete such detector was stopped as simulations showed that the direct detection of X-rays in the photodiodes would lead to a high noise. The results, however, have a more general use as it is demonstrated that pores of very high aspect ratio can be "coated" with a *pn* junction.

- *Paper 8*

This paper investigates the formation of *pn* junctions in the walls of rather thin pores (diameter of ~ 10 μm for a pore pitch of 50 μm as used in the '3D' detector concept). Two process flows are proposed to disconnect the junctions from one pore to another. The final *pn* junctions were electrically characterized and compared.

The *IV* characteristics of the vertical *pn* junctions are discussed. The study shows that individual *pn* junctions can be formed in each pore, and that the reverse current of the junction is dependent on the light intensity, as in a photodiode or charged particle detector. The pores were also connected in a transistor-like configuration, demonstrating that the current flowing from one pore to another can be controlled via the bias of the substrate.

5.2. Conclusion and outlook

The work presented in this thesis is a contribution to the development of radiation imaging detectors. To form these detectors, pore arrays have been etched in silicon and processed to realize the final detectors (or at least part of them). Among the etching techniques available today, electrochemical etching of n-type silicon was studied particularly since it offers the possibility to etch pores with high aspect ratios for a wide range of diameters. In this work, the formation of well-ordered structures, such as pore arrays, walls, tubes and pillars, was extended to the sub micrometer scale. It could potentially be extended to the nanoscale for the formation of structures below 100 nm. As an example, pore arrays formed on the nanoscale could be used for detectors with high spatial resolution. In addition, the technique itself was developed, and for the first time the use of a backside *pn* junction to inject holes as required for etching of low-doped n-type silicon was demonstrated. The formation of structures was shown and the pros & cons of the technique have been discussed. In parallel to the advances made to silicon electrochemical etching, various processes were implemented for the subsequent treatment of the pore arrays. This includes oxidation and metal deposition on the pore walls, realization of *pn* junctions in the pore walls by diffusion or low-pressure chemical vapor deposition, and filling of the pores with other materials such as CsI(Tl). The results from the post processing of the pore arrays show that uniform doping and deposition as well as filling of the pores can be obtained, even for very high aspect ratios.

The first detector investigated in this thesis uses a scintillating guide screen in proximity to a silicon CCD. The screen is formed by filling with CsI(Tl) a pore array having reflective pore walls. The study shows that good spatial resolution can be achieved with negligible cross-talk between adjacent pixels. Here, a spatial resolution of ~ 8 lp/mm was obtained. Most of the produced detectors had a detective quantum efficiency of about 25 % but the possibility to produce detectors approaching the theoretical limit for X-ray absorption was shown. Thus, quite efficient detectors can in principle be produced which would enable a dose reduction for medical applications. However, the procedure used to fill the pores with CsI(Tl) is critical and still requires careful control in order to obtain good CsI(Tl) quality in the pores with uniform Tl concentration. Oxide was preferred as a reflective material as it produces smooth pore walls and enable total internal

reflection in the CsI(Tl) columns. No efficiency enhancement has been observed using metallized pore walls in this work. However, as shown by efficiency calculations, the detector efficiency could be increased using a highly reflective metal coating.

Two more types of detectors were studied in this thesis, both requiring the formation of *pn* junctions in silicon pore walls. One detector consists also of a pore array filled with CsI(Tl) but, instead of detecting the secondary emitted photons by a CCD, the light is captured by photodiodes formed in the pore walls ("CsI-photodiode" structure). The other concept is called the "3D" detector, where the pore array is used to form an array of electrodes in the detecting material (silicon here). Although the detectors were not fabricated to completion, the formation and the characterization of *pn* junctions in silicon pore walls have been studied, as it is one of the crucial steps for the fabrication of these two detectors. Boron diffusion from a solid source and low-pressure chemical vapor deposition of boron doped poly-silicon were shown to be suitable techniques to obtain uniformly doped pore walls. Two process flows were proposed and shown to be successful in order to form individual *pn* junctions. Indeed, the p$^+$ layers have to be disconnected from one pore to another after diffusion. Electrical characterization of the *pn* junctions formed by boron diffusion is provided and the diodes demonstrated good rectifying behavior and sensitivity to light. For the further realization of such detectors, there is still the difficult task of making contacts to the p$^+$ layers. Nevertheless, as mentioned earlier, the CsI-photodiode structure will not provide much improvement as a large noise is expected due to the direct absorption of radiation in the photodiodes. For the "3D" concept, the possibility to bump-bond the pore arrays on a readout chip is currently in progress within the 3D-RID project. Here, one of the limitations is that silicon has a rather low absorption coefficient for X-rays. Other materials with higher stopping power, such as GaAs or InP, could be used. The processing technology of these two materials is under development and the possibility to etch InP by electrochemical etching has recently been shown [98].

Finally, electrochemical etching is a very interesting technique to form various structures in silicon, from the micro to the nanoscale. This has potential for new devices in silicon but also for making new functional materials by impregnating these structures by various materials or particles [99-101]. Thus, it is important to develop this technique further to see the possibilities as well as limitations.

As for the most promising approach for an X-ray imaging detector, the scintillating screen-CCD concept, it seems that it is possible to approach the theoretical limit of detection. This is set by Poisson statistics of the X-ray fluence. Whether such a detector could be marketed, depends on the control of the CsI-filling process that can be reached, but also on price and performance of competing detectors.

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