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Theory and Implementation of CMOS Class-D Digital Audio Amplifier for Portable Application

Master of Science Thesis
In Electronic System Design

by

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Abstract

The audio power amplifier plays an essential role in every system that generates audible sound. General power amplifies are voluminous, heavy, expensive, unreliable and have very poor energy utilization, all due to a low efficiency.

In the last few years the use of digital technology in audio electronics has become widespread and, nowadays, there is an increasing interest in the development of completely digital audio systems. Moreover, the growing market demand for small size multimedia systems with high output power and large number of audio channels is driving the need for high efficiency power amplifiers. Recently, a great effort has been made to develop fully digital power amplifiers, usually referred to as power DACs. These amplifiers convert the PCM (Pulse Coded Modulation) digital signal into a sigma-delta modulated 1-bit data stream or a PWM (Pulse Width Modulation) signal. The high frequency two-level signal is then amplified using an open loop power buffer and low-pass filtered. This approach is relatively simple, but the output analog signal is adversely affected by supply noise and non-idealities within the power buffer. A good performance can be obtained using more complex digital structures and algorithms for noise and distortion reduction. However, a more efficient approach for building a low cost power DAC relies on the use of a feedback power buffer. A single-chip power DAC with a feedback power buffer has been recently proposed.. The digital input signal is converted in a noise-shaped one-bit signal Pulse Density Modulation (PDM) modulator. The PDM bit stream directly feeds a class-D amplifier, and a simple LC filter reconstructs the audio signal. In this thesis we proposed CMOS digital audio amplifier based on delta sigma ($\Delta\sum$) modulator a power efficient switching (class D) output-stage with out intermediate frequency. The technology is UMC 0.18 micron CMOS. Various topologies of digital audio amplifiers are investigated at 0.18 micron. Therefore we designed the digital Amplifier in 0.18 μm standard digital CMOS Process with operation frequency 2.75 KHz, the amplifier can operate from 1V to 1.8V. UMC 0.18 micron offers Low and Zero threshold voltage transistors, in addition to the Regular threshold voltage transistors.

However previously not much work have been done or reported a CMOS power amplifier in particular low voltage. As a supply voltage is reduced to 1V, the performance of the amplifier, such as the output power and the efficiency are degraded. In this thesis the design considerations of CMOS amplifier under low supply voltage and power are detailed. The total harmonic distortion at the load is less than 0.07% with a dynamic range (DR) is 85dB. We can obtain an efficiency of 76% with the load resistance of 4.3Ω. The maximum out put power is this case can be 350mW from a single 1.8 power supply. In this work we have demonstrated the implementation of Class-D amplifier with high end audio performance in low voltage environment.

Acknowledgments

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PART 1: INTRODUCTION

This part of the report aims to give a basic understanding of the concepts that are common throughout the thesis project. After a short introduction, the basic concepts concerning Power Amplifiers; then a description of the Audio Amplifiers follows.

The motivation and the general thesis outline are described in this introduction part. This Part provides a basic smattering of the main concepts that are the ground of this master thesis-project work and summarizes how the work has been accomplished.

Part 1 and 2 aim to give a general overview of power Amplifiers, Digital CMOS amplifiers, and their integration, while Part 3 and 4 depict why and how the project has been developed, which results have been achieved, and in which environment it will fit.

1.1 Motivation

Portable system require at lower supply voltage that require compactness, high speed, and long battery life. At the same time, dimensions have become smaller. Mini sets, car radios and PC multimedia equipment have only little space available, leading to an increasing conflict between manageable power dissipation and market demands for high output power and many output channels. In these cases, low power consumption is necessary to lengthen battery life. To meet these demands, highly integrated, power efficient audio amplifiers are essential. New innovative circuit design techniques are required for high speed with low power consumption. Power-minimum high-speed circuit design methods with charge recycling are being developed to drastically reduce the power consumption of low-voltage CMOS circuits.

Although CMOS technology provides single chip solution, it also suffers from a poor quality factor of monolithic passive components, low breakdown voltage of the transistors and large process variation. The Supply voltage has been scaling down with the technology but the required power at load remains or even increases.

In anther way we have convectional method for audio reproduction from digital source can be use by using classical class AB amplifier[1] with high peak power, however, have very poor efficiency at moderate signal levels. This approach is also consists of two chips implementation in different technology which require more hardware can be disadvantage Also, good bass reproduction is getting more and more important, requiring much power of the amplifier.

As audio is increasingly derived from the digital source the motivation is to find a digital alternative to analog power amplification. In our project we demonstrated how audio can be generated from the digital source.

During the history of audio registration and reproduction, which started more than a century ago, there has been a steady improvement in quality. The first record player, which was in fact a rotating drum, used only the mechanical excitation of the needle to produce sound. The movements of the needle were transferred to a diaphragm in a horn, thus forming a true ‘audio amplifier’. Later in time, the movements of the needle were first transformed into electrical signals. These signals were amplified by means of vacuum tubes and fed to a loudspeaker. With the introduction of the transistor, vacuum tubes were replaced by transistors, [2] and later by integrated circuits. These developments led to audio amplifiers with less weight, using less power and sounding better. (Regarding this last aspect it is quite unfortunate that many people are misled by the term ‘warm feeling of tube amplifiers’, thinking it refers to sound quality rather than to dissipation).

Fundamentally, only little has changed in the final stages of the audio reproduction chain for decades. The widespread use can not be justified by superior performance; in fact the principle of electric-acoustic conversion is limited by numerous fundamental problems that make this ultimate stage in the audio chain the weakest – by far. One essential limitation is the striking inefficiency. Generally, a given amount of acoustic power requires orders of magnitude higher power input delivered by the power amplifier. The power amplifier has the task of amplifying the audio signal to a level that, combined with sufficient current to move the coil, produces the desired acoustic level from the loudspeaker. The poor loudspeaker efficiency is very unfortunate, since power amplifiers generally have to be capable of delivering large amounts of undistorted power, to produce the subjective levels demanded by the consumer.

The field of audio power amplification has equally suffered from a lack of real breakthrough inventions for decades. Thus, sound reproduction today is founded on a few power amplifier principles that are characterized by a linear operation of the output transistors. The advantages include topological simplicity and good performance, but the linear amplifier principles suffer [3] from low efficiency, which is critical since the power amplifier handles considerably amounts of power. Accordingly, power amplifiers are in general provided with massive heat sinks of extruded aluminum to cope with the heat development. Negative side effects of inefficient power amplification include high volume, weight, cost and reliability problems. Moreover, the power amplifier has low energy utilization, which is clearly not an attractive feature in this energy-conscious area.

This Master of thesis project will focus on design consideration and implementation digital CMOS audio amplifier for low power digital devices cellular phones, handheld computers, personal digital assistances (PADS), and earphone in general for electronics portable devices, for which analog linear amplification is inefficient.

1.2 Problem definition

1.2.1 Audio signals

Essentially, an audio amplifier is a normal voltage amplifier optimized for the amplification of audio signals. The limited frequency response of the ear sets the bandwidth limits: 20Hz - 20 kHz, although most people are not able to hear 20 kHz. Most power is concentrated in the mid frequencies, and occasionally in the low frequencies. Generally, the amplitude probability density function of audio signals is Gaussian. This means that the ratio between maximum and average power is large: 10…20dB. In average, it is 15dB, which is 12dB below the power of a rail-to-rail sine wave. [40]

1.2.2 Amplifier Power

The ear has a very large dynamic range. To give an example: the ratio between the acoustic power of a rock concert and the sound of breathing can be as large as 10^{11}. This makes large demands on the dynamic range of the audio amplifier. To get an idea about the order of magnitude of amplifier output powers, refer to Table 1.1. The SPL’s have been taken from [4]. Table 1.1 displays some situations in which audio power amplifiers can be used. The first column gives the Sound Pressure Level (SPL) in dB. 0dB SPL is the hearing threshold and defined as 0.00002 N/m^2. The second column shows what sound sources would produce an equivalent SPL - just to give an idea. Now suppose we want to reproduce these SPL’s with an audio amplifier and a loudspeaker. Assuming that the loudspeaker has an efficiency of 90dB/W@1m (a normal value for large loudspeakers) and that the SPL decreases with the squared distance, the needed loudspeaker power at a certain hearing distance can be calculated (third column). In practice, these values can be a little too high, because of reflections against walls or ceiling.

SPL [db]	Sound pressure Level (SPL) is equivalent to:	Power in LS for that SPL @ distance from LS	Necessary amplifier rating
50	Low level back ground music at 1m	~ 100µW @ 1m	1.5mW
60	Normal Speech at 1m	~ 1mW @ 1m	15mW
80	Orchestra in concert hall	~ 1W @ 3m	15W
110	Rock band	~ 2kW @ 4.5m	30kW

Table 1: Amplifier power needed for different sound pressure levels

Finally, audio signals have an average power that is considerably lower than their peak power, so for undistorted sound the maximum sine power rating of an amplifier should in average be 12dB higher than the average power delivered to the loudspeaker. The resulting calculated amplifier peak power is displayed in the fourth column of Table 1.1.

From Table 1.1 we conclude that audio amplifiers must operate over a wide range of power levels. The ratings in column 4 are an indication of the amplifier powers found in transistor radios (100mW-1W), midi sets (10W-100W) and professional PA equipment (1kW-10kW). These values depend on many factors; they are mainly meant to create a feel for amplifier powers.

1.2.3 Efficiency or dissipation

The efficiency of an audio amplifier is hardly important in systems that use audio amplifiers. In battery powered equipment, the dissipation should be minimal for the longest battery life time. In systems where cooling is a problem, the maximum dissipation is an important design criterion. In literature, however, the most common measurement graphs depict the efficiency of an audio amplifier as a function of output power as shown in Figure 1.1. A problem with these kinds of charts is that it is difficult to see how much the amplifier actually dissipates. The dissipation of an amplifier in relation to the output power P_o and the efficiency h is:

$$P_{diss} = P_o\left(\frac{1}{\eta} - 1\right)$$

which makes it not very easy to see that the right amplifier in Figure 1.1 dissipates 50% more than the left one at full power (which seriously affects heat sink design).

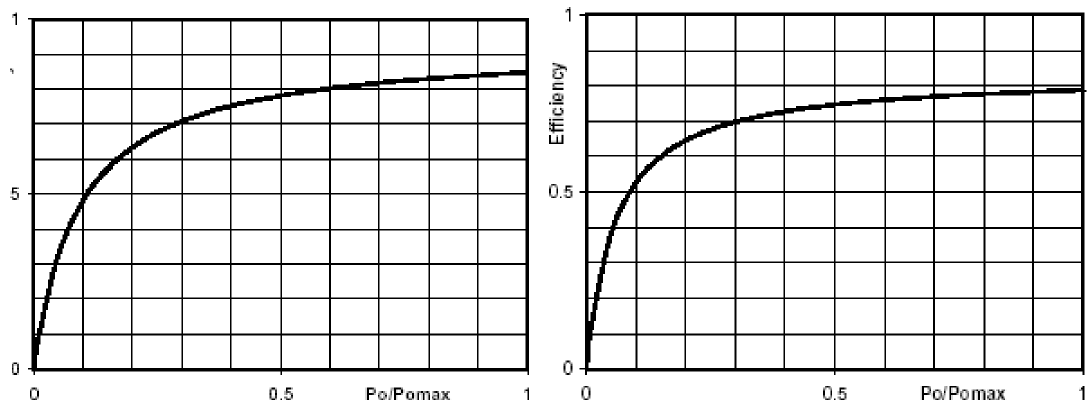

Figure 1: Simulated efficiency of two hypothetical audio amplifiers with different dissipation [4].

The fact that the left amplifier has a 50% higher quiescent power dissipation (which seriously affects the battery life of e.g. a portable radio) is not visible at all, since the efficiency is always zero at zero output power. Apart from that, the average power of an audio signal is on average 12dB lower than a full power sine wave, so the majority of the graph displays useless information. From now on we will therefore use graphs as displayed in Figure 1.2. The dissipation for the whole power range is clearly visible thanks to the logarithmic x-axis, and also the maximum- and quiescent power dissipation can easily be observed.

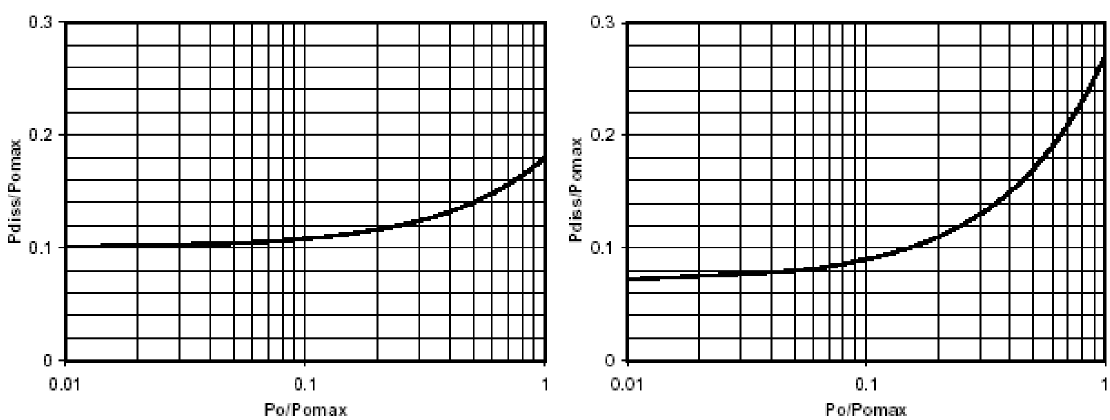

Figure 2: Dissipation of two amplifiers in Figure 1 [4]

1.2.4 Distortion

Making a high efficiency audio amplifier would be a lot simpler if its distortion was not important. A class D amplifier on a low switching frequency can have an excellent efficiency, but its distortion will be too high. The design of class G amplifiers is complicated by switching distortion, etcetera. Therefore, a low distortion is an important condition when judging efficiency. There are several types of distortion that can be measured:

Total Harmonic Distortion (THD)

When a sinusoidal signal is applied to a non-linear amplifier, the output contains the base frequency plus higher order components that are multiples of the base frequency. The Total Harmonic Distortion is the ratio between the power in the harmonics and the power in the base frequency. This can be measured on a spectrum analyzer. Most distortion analyzers, however, subtract the base signal from the amplifier's output and calculate the ratio between the total RMS value of the remainder and the base signal. This is called THD+N: Total Harmonic Distortion + Noise. Normally, the noise will be low compared to the distortion, but the noise of a noisy amplifier or the switching residues in a class D amplifier can give garbled THD figures. For a THD+N measurement, the bandwidth must be specified. For class D measurements, a sharp filter with a 20 kHz corner frequency is necessary to prevent switching residues -that are inaudible- to show up in the distortion measurements.

InterModulation distortion (IM)

When two sinusoids are summed and applied to a non-linear amplifier, the output contains the base frequencies, multiples of the base frequencies and the difference of (multiples of) the base frequencies. Suppose a 15kHz sinusoid is applied to an audio system that has a 20kHz bandwidth, and the THD+N needs to be measured. All the harmonics are outside the bandwidth and will be attenuated, resulting in too low a THD+N reading. The same situation occurs when the distortion analyzer has a 20 kHz bandwidth. In these cases, an IM measurement can be a solution. The first standard was defined by the SMPTE (Society of Motion Picture and Television Engineers). A 60Hz tone and a 7 kHz tone in a 4:1 amplitude ratio are applied to the non-linear amplifier. The 60Hz appears as sidebands of the 7 kHz tone. The intermediation distortion is the ratio between the power in the sidebands and the high frequency tone. Another common standard is defined by the CCITT, and uses two tones of equal strength at 14 kHz and 15kHz. This generates low frequency products and products around the two input frequencies, depending on the type (odd or even) of distortion.

Interface InterModulation distortion (IIM)

In this test, the second tone of an IM measurement set-up is not connected to the input, but to the output (in series with the load impedance) [5],[6].

Transient InterModulation distortion (TIM)

When a square wave is applied to an amplifier with feedback, its input stage has to handle a large difference signal, probably pushing it into a region that is less linear than its quiescent point. When a sinusoid is added to the square wave, the nonlinearity induced by the edges of the square wave will distort the sinusoid, giving rise to TIM, also called transient distortion or slope distortion [7]. There are many ways of testing TIM and it remains unclear how much it adds to the existing measurement methods. If the maximum input signal frequency during normal operation of an amplifier is limited to 20 kHz, a 20 kHz full power sinusoid is the worst case situation. When that generates little distortion, TIM will not occur [8].

Cross-over distortion

Cross-over distortion is generated at the moment the output current changes sign. at that moment, the output current gets supplied by another output transistor. The process of taking over generates distortion, visible as spikes in the residual signal of a THD measurement. This kind of distortion is notorious for its unpleasant sound (a small percentage error is quickly noticeable). Because it’s usually present around zero amplitude, the impact on small signals can be relatively large.

Which distortion is important?

There is no consensus as to which distortion measurements are essential. In the ongoing search for the critical attributes that determine the ‘sound’ of an audio amplifier, many other mechanisms can play a role like reactive harmonic distortion [9], the spectrum of the distortion [10], non-linear crosstalk [IEC268-1], memory effects [11], granularity distortion [14], and external influences like speaker cables [13], decoupling capacitors and the phase of the moon. It is unclear to what extent these concepts influence the ‘sound’ of an amplifier. Also, alternative measurement methods have been described, like measuring the difference between input and output of an amplifier for audio signals [15], or analyze the output signal in Volterra space [12]. Based on experience and for practical reasons, the frequency transfer characteristics and the THD+N over power and frequency range are important. Observing the residual signal in a THD measurement and an IM measurement are also good practice.

1.2.5 Other specification

It's usually easier to select an amplifier than to design it from scratch. But to select the CMOS amplifier, you need to know which specifications are important to your application. An audio amplifier has many parameters which characterize its performance. The question is which specifications are critical to for portable and mobile application and which ones are not. To answer these it has been determined based on the three things:

1) The performance of the amplifier design,
2) which parameters determine that performance,
3) What the values need to be for those parameters.

There is more to say about audio amplifiers than will fit in one article, so we there will be several Tech Tips on this subject. In the following paragraphs we will discuss some key concepts needed to understand amplifier specifications and relate them to performance.[4]

Gain

The gain of an amplifier is the ratio of the output signal to the input signal. This is usually fixed, or variable in a small range. The output resistance must be low to ensure a proper control of the loudspeaker. There are three categories of gain: voltage gain (Av), current gain (Ai) and power gain (AP). Any amplifier has a value for all three gains, but typically you must specify just one of them. Depending on the application, Av and Ai may be expressed as a simple ratio or as the log (base 10) of the ratio:

$$AV = \frac{V_{out}}{V_{in}} \quad \text{or} \quad AV = 20\log\frac{V_{out}}{V_{in}}$$

When using the log of the ratio, the result is referred to as dB. Strictly speaking, dB actually refers to the log of the power gain:

$$db = 10\log\frac{p_{out}}{P_{in}} = 10\log\frac{\frac{(v_{out})+(v_{in})}{R_{out}}}{\frac{(v_{out})(v_{in})}{R_{in}}} = 10\log\frac{R_{in}}{R_{out}} + 20\log\frac{v_{out}}{v_{in}}$$

But having Av expressed as a logarithm is very useful, and referring to it as dB is part of the culture.

Bandwidth and Frequency

The bandwidth (BW) of an amplifier is the range of frequencies, from lowest to highest, over which the amplifier delivers sufficient gain. The meaning of "sufficient" depends on your application, but one common meaning is when the gain (20 Log Av) has dropped by 3dB. IC amplifiers of the "op-amp" variety (operational amplifiers) will work from DC up to some frequency, the "break-point", where gain has dropped by 3dB. Amplifiers which amplify DC as well as AC are said to be "direct-coupled".

How much bandwidth does an audio amplifier need? It depends on what you mean by "audio". In a telephone circuit, 300 Hz to 3300 Hz is adequate bandwidth. In high-fidelity audio, 20 Hz to 20 kHz would be required. In some applications, 100 kHz is considered to be an "audio" frequency. Amplifiers are called audio amplifiers to distinguish them from either DC amplifiers used in instrumentation applications and from high-frequency (1 MHz and up) amplifiers used in radio frequency (RF) applications.

Gain bandwidth

Amplifiers have a property referred to as the "gain-bandwidth product" or GBW. The GBW of a given amplifier is a constant. If you set the amplifier to a gain of Av (ratio, not dB), then the bandwidth is given by: $BW = \frac{GBW}{AV}$

For example, suppose the GBW is 100,000. At a gain of 10, the amplifier will have a bandwidth of 10,000 Hertz. At a gain of 100, the amplifier will have a bandwidth of only 1000 Hertz.

1.2.6 Trade –offs: Speed and Power

GBW is an example of a "trade-off". A trade-off occurs when making one thing "better" makes another thing "worse". In designing electronic circuits there are always various trade-offs to be made. GBW is a trade-off between gain and bandwidth. Speed and power-dissipation is another trade-off. When designing an amplifier, it may be possible to increase the GBW (the "speed") if you are willing to have it "run hotter" by dissipating more power.

Bode Plots

A Bode Plot is a graph showing how gain and bandwidth are related in an amplifier. It is very useful, and is very commonly found in books and magazine articles on electronics. A typical Bode Plot is shown in Figure 3.

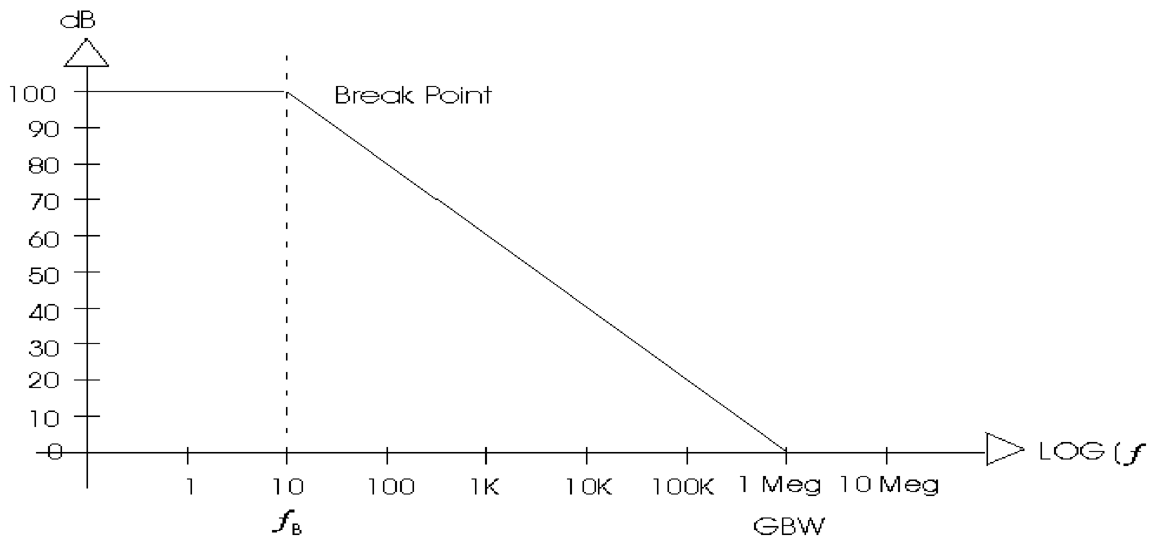

Figure 3: A typical Bode Plot

The vertical axis (Y-axis) is in dB. Remember that when dealing with amplifiers, dB is defined by equation given above. The horizontal axis (X-axis) is the Log of the frequency, so each mark on the horizontal axis represents a frequency 10 times higher than the previous mark. The distance from one mark to another, from f to 10f, is called a "decade". The distance from f to 2f is called an "octave".

Break-point, Roll-Off and Feedback

Figure 2 shows the maximum voltage gain (Av) of an amplifier as a function of frequency. There are two important things to see on the graph. First is the "break-point" which occurs at the "break-frequency" fB. Av is constant until the break-point. The second thing is that after fB, Av starts to "roll off" at a constant rate of

20 dB per decade. The point where the graph crosses through the horizontal axis is the GBW. A roll-off of 20dB / dec is typical of many amplifiers. Figure 2 also shows that the amplifier starts out with a gain of 100 dB, which is a gain of 100,000. That's more gain than you need for most applications. So high-gain amplifiers in general, and op-amps in particular, use "negative feedback" to reduce the gain to a usable level. A total discussion of negative feedback is beyond the scope of this article. We will just say that negative feedback takes some of the output signal and connects it back to the input in such a way that the signal fed back subtracts from the input. The effect is to cause the amplifier to operate at a lower value of gain while the GBW stays the same. With no feedback, the amplifier is said to be "open-loop". With negative feedback, it is said to be "closed-loop".

1.3 Thesis Scope Outline

In this thesis, there are 4 Parts. In part Chapter 1, the motivation, the problem definition and the classification of audio amplifiers is detailed. Therefore many audio fragments are analyzed with respect to amplitude- and frequency distribution. Existing and new test signals are compared to these characteristics to determine if they are suitable to compare present amplifiers, and to predict how new ones will perform. Part 2, gives an overview of already existing digital amplifiers. They can be divided into linear amplifiers and switching amplifiers. The advantages and crucial limitations of both types are analyses. Some of the basics of power amplifier will be detailed in part 2 to provide background information for the readers. The problem with the low efficiency of anther types can be solved by basing the output stage on a class D amplifier configuration covering a technology which in many ways is like the one known from the switch mode power supply and motor controls. In a class D amplifier stage the power transistors operate in only two conditions: 'on' or 'off', and theoretically it is about a non-dissipative conversion technique if you could get 'ideal' Switching components (output transistors). Part 3 will discuss the design considerations of the digital audio Amplifier used for portable applications. In this chapter the realization of pulse density modulation in place of Pulse width modulation have been states or considered. It is done with a $\Delta\sum$ modulator, which generates analog-digital converter a stream of bits 0’s vs. 1’s of constant pulse timing at constant clock rate. In general $\Delta\sum$ modulators generate a one bit or a few bits representation of a digital signal. An input signal is sampled at a frequency far higher than the Nyguist frequency (twice the maximum signal frequency). We can get a high resolution through with implementation of $\Delta\sum$ analog to digital converters. This is because of the over sampling is done above the Nyguist rate and the noise shaping uses of negative feedback to control the spectrum of the quantization error is varied in proportion to the input signal. The details of proposed digital Class- D amplifier out put stage is also described Part 3. The thesis ends with a conclusion in part 4 and talks about the potential improvement of the circuit and the future work.

Part 2: Basics of Power Amplifiers

When ever there is Audio there are power amplifiers. We can rate the performance of Audio amplifiers in terms of power gain, the efficiency and the linearity. Different power amplifiers mode should be thoroughly understood before improved circuit topology can be designed. Understanding the language used in the world pf amplifiers and the basic operating principle of different modes of Amplifiers is required. In Part 2 different class of power amplifiers and their correspondence features will be described.

2.1 Introduction

The field of audio power amplification has equally suffered from a lack of real breakthrough inventions for decades. Thus, sound reproduction today is founded on a few power amplifier principles that are characterized by a linear operation of the output transistors.[1] The advantages include topological simplicity and good performance, but the linear amplifier principles suffer from low efficiency, which is critical since the power amplifier handles considerably amounts of power. Accordingly, power amplifiers are in general provided with massive heat sinks of extruded aluminum to cope with the heat development. Negative side effects of inefficient power amplification include high volume, weight, cost and reliability problems. Moreover, the power amplifier has low energy utilization, which is clearly not an attractive feature in this energy-conscious area.

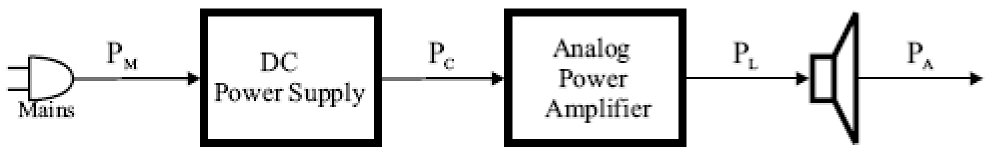

Figure 4: Power Flow in audio reproduction chain

Consider the model of essential power flow in a typical audio system, shown in Fig. 4. To illustrate the low power utilization, a typical 100W power amplifier is considered. The power flow at two specific output levels is given below.

Situation	Pm	Pc	Pl	pd
Typical	15W	10W	100mW	1mW
1/3 of max	115W	90W	30W	300mW

Table 2: Power flow at specific output

Clearly, the transducer is the fundamental source of the efficiency problems, i.e. an efficiency improvement by and order of magnitude would virtually eliminate the need for power amplification, as we know it today. However, most of the power is dissipated in the power amplifier due to low efficiency in this stage.

2.2 Classification of Amplifier

Digital modulation offers superior performance, such as noise insensitiveness and integration of low cost CMOS process over analog modulation, and is widely used in wireless systems. To facilitate discussion on the tradeoff between power efficiency and spectral efficiency in digital modulation, literature classifies power amplifiers as either linear power amplifiers or nonlinear power amplifiers [2].

2.2.1 Linear Amplifier

When a linear power amplifier is used to amplify a signal, there is linear relationship between the input signal and the output signal. This is important for the non-constant envelope modulation scheme because the signal information, which is embedded in the envelope, will be lost if the power amplifier is not linear enough. Among all classes of power amplifiers, class-A, class-AB class-B class-G, Class-H and the cool-power amplifier can be viewed and discussed here as a linear power amplifier.

Class A

A class-A power amplifier is the simplest power amplifier. It can be viewed as a small-signal amplifier except the signal level is a substantial fraction of the bias level. A typical circuit topology is shown in Fig. 5.

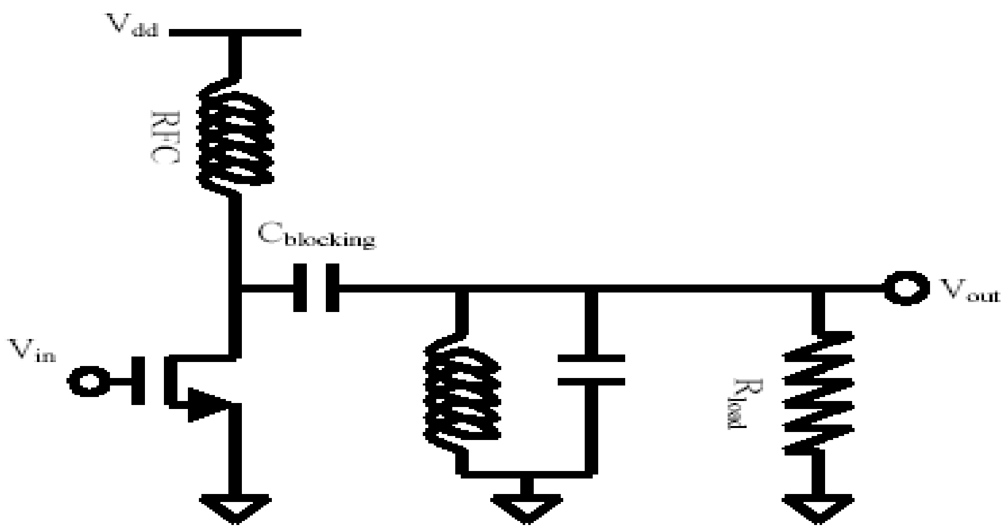

Figure 5: Typical configuration of a class-A power amplifier

It consists of an RF choke, a DC blocking capacitor, a parallel LC tank and a transistor. An RF choke (RFC) is used to feed DC power to the drain and provide a constant current to the transistor. Also, the use of inductive load doubles the voltage swing at the drain of the transistor which lowers the supply voltage by a factor of two [3]. The DC blocking capacitor prevents current flow to the output loading in order to eliminate DC power consumption. Due to the non-linearity of the transistor, the parallel LC tank filters the out-of-band emission so that only a single tone sine wave is observed across the output loading. The NMOS transistor shown in Fig. 5 is operated in the saturation region or pinch-off region for the whole input cycle. The transistor is biased to V_{dd} so that it operates in the saturation region for the entire period. Since both the transconductance (g_m) and the output resistance (R_{out}) of the transistor remain the same throughout the entire input cycle, the gain, $g_m R_{out}$, is approximately the same throughout the period and the linearity is the best among the other classes of power amplifier. Figure 6 shows the waveforms of a class-A power amplifier.

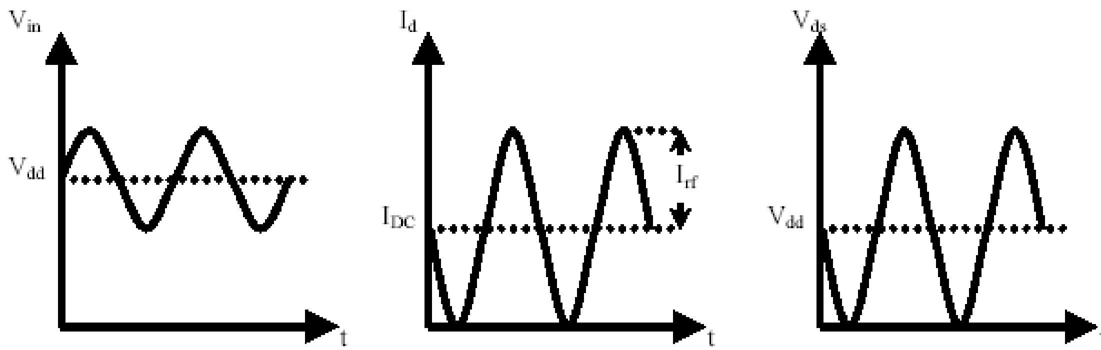

Figure 6: Voltage and current waveforms of an ideal class-A power amplifier

However, due to the 100% duty cycle or 360° conduction angle, the transistor always draws current during the period and the voltage across the transistor is always larger than zero. In other words, the transistor dissipates power constantly throughout the cycle. High linearity is achieved with the price of poor efficiency in a class-A power amplifier.

The efficiency can be derived with the fact that the transistor is biased at V_{dd} and the amplitude of the output voltage swing is as large as V_{dd}. Also, the DC supply current, I_{DC} is the same as the RF current, I_{rf} Therefore, the DE of a class-A power amplifier is:

$$DE = \frac{P_{rf}}{P_{DC}} = \frac{\frac{1}{2} I_{rf} V_{dd}}{I_{DC} V_{dd}} = \frac{1}{2}$$

The inherent DE of a class-A power amplifier is limited to 50%. Any non-ideal effects, such as losses associated with the parasitic will further reduce the efficiency. Therefore, the class-A power amplifier is chosen only when the requirement of linearity is stringent.

Amplifier Class B

It is noticed that the efficiency can be improved if the transistor does not conduct current for the entire cycle, but only draws current at a certain period of time. For example, if the transistor conducts half of the cycle, it is categorized as class-B power amplifier. Because the transistor has a 180° conduction angle, the transistor is biased at the threshold voltage and the transistor is in cut off region during half period of time, as shown in Fig. 7.

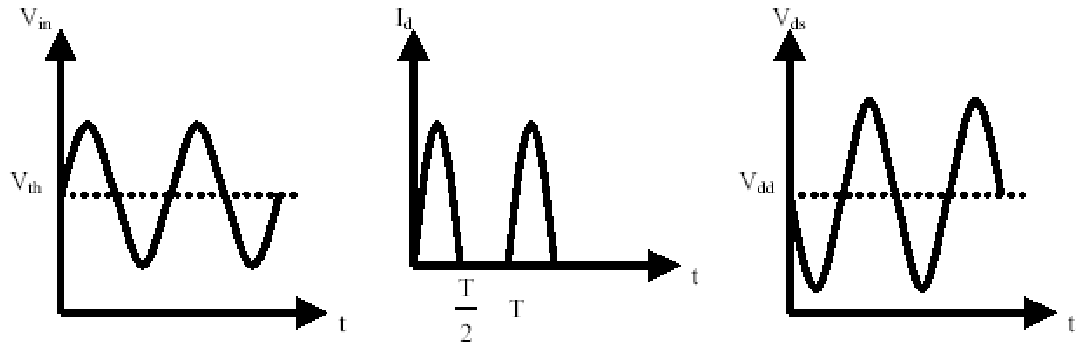

Figure 7: Voltage and current waveforms of an ideal class-B power amplifier

In practice, a class-B power amplifier is usually realized in push-pull configuration, as shown in Fig. 8, to maximize efficiency.

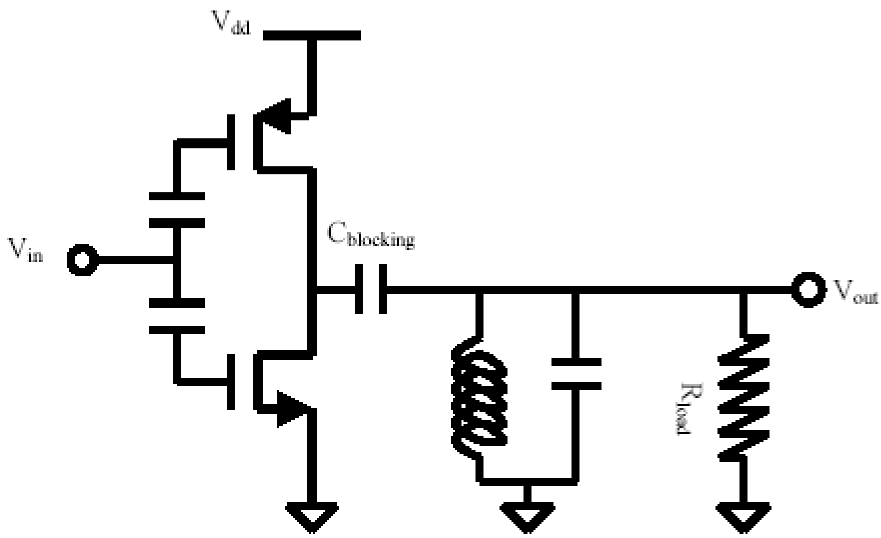

Figure 8: Complementary Class B power amplifier

On the first half of the cycle, the current is 'pushed' to the output loading through the PMOS transistor. On the other half cycle, the current is 'pulled' from the load to NMOS transistor. However, due to the absent of high speed PMOS device, this configuration is seldom used for RF applications.

As shown in Fig. 9, a transformer-coupled class-B power amplifier utilizes two NMOS transistors.

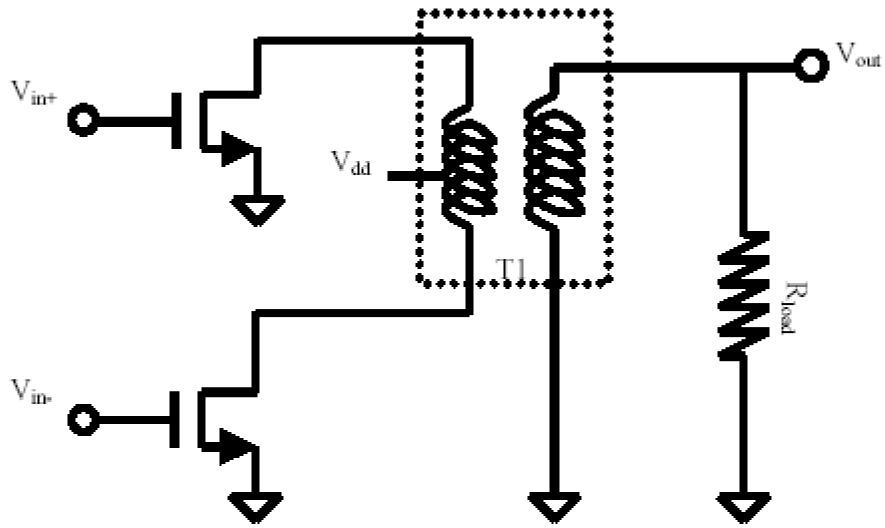

Figure 9 A transformer coupled class-B power amplifier

Since two NMOS transistors are used, it is more suitable for high-speed applications. The transformer is used to combine the differential-ended drain current into a single-ended current. With a 50% duty cycle, the DE can achieve 78% [3]. However, the linearity is inevitably degraded due to the switching between the cut-off region and the pinch-off region of the transistors. In practice, a class-B power amplifier is difficult to implement because the two transistors may have different threshold voltages and they may be ON or OFF at the same time.

Amplifier class AB

When the transistors are ON at the same time for some instant, the amplifier is defined as a class-AB power amplifier. The corresponding waveforms are shown in Fig. 10.

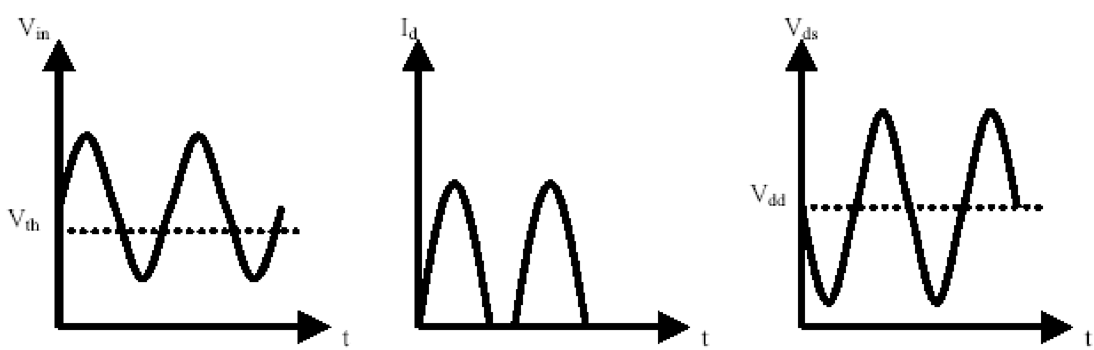

Figure 10: Voltage and current waveforms of an ideal Class-AB power amplifier

As its name implies, all parameters associated with a class-AB power amplifier lie between class-A and class-B. For example, the efficiency is between 50% and 78%. The performance of linearity is somewhere between class-A and class-B. Since the duty cycle of the transistors is ranged from 100% to 50%, the transistors are biased above the threshold voltage.

The circuit topologies of a class-AB power amplifier can be either a simple transistor configuration as class-A or a push-pull configuration as class-B. Class-AB power amplifiers are widely used in a system with a non-constant envelope modulation scheme [4] since it can provide better linearity with acceptable efficiency.

Class-G Amplifier

The output signal for audio, however, is close to zero most of the time, with only few excursions to higher levels. Thus the average voltage drop across the output transistors is large, causing the poor efficiency figures for audio. An amplifier in class G uses multiple supply voltages. At lower power levels, the lower supply voltage is used. When the signal becomes too large for this supply, the higher power supply takes over, and delivers the output power. In this way the average voltage drop across the output transistors is reduced and the overall efficiency can be improved [23, 24, 26]. There are two basic ways in which class G amplifiers are realized. The difference is the way of switching between the supply voltages. Figure 11 shows the upper half of a possible output stage. The upper transistor is switched on during signal peaks increasing the power supply of the lower transistor -that controls the output voltage- from Vdd1 to Vdd2. Another way to use this circuit is opening the lower transistor totally during signal peaks, giving the higher MOST the role of output transistor.

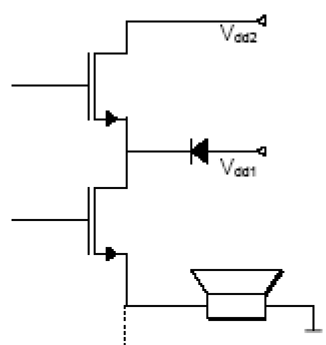

Figure 11: Serial Class G Amplifier

A disadvantage of this circuit is that there are always two elements in series. At low output voltages, the diode decreases the efficiency. During signal peaks the two transistors are in series, so that the output current has to pass two VDS voltage drops. Figure 12 shows a ‘parallel’ topology that does not suffer from these problems. It needs special precautions in the driver circuitry, however, to prevent high VGS reverse voltages across the upper left output transistor.

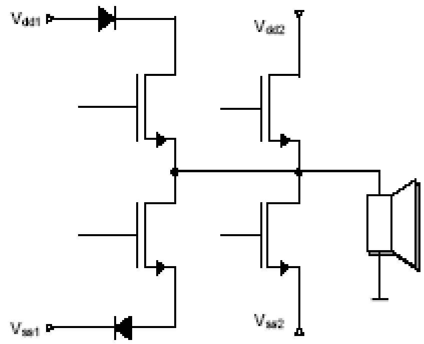

Figure 12: Parallel Class-G Structure

In general, the need for multiple supplies may be a problem. If a transformer is used in the power supply, multiple taps are a good solution, but if a car battery is used, it is more problematic. Another problem with this type of amplifiers is the distortion caused by the switching between the two amplifiers. By using a comparator with hysteresis and delay to decide between the supplies [23], the number changes can be reduced, but this is a very inelegant way to reduce the total distortion. Another way to limit switching distortion is by switching between the two amplifiers gradually. However, this cuts down the efficiency a little.

Class-H Amplifier

Here is not necessary to use two power supplies like in class G. Because the signal peaks generally last only a short time, the energy can be supplied by a capacitor. This technique is referred to as 'Class H' [22]. See

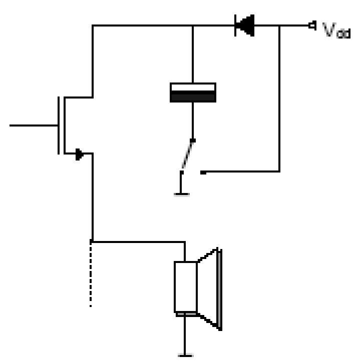

Figure 13: Class-H Amplifier

During low output voltages, the switch is in the position as drawn in Figure 13. During signal peaks the switch lifts the lower side of the elco to the power supply, such that the upper output transistor sees a voltage of approximately 2Vdd. The time that the signal is 'high' should not be too long; a large elco is required for high power at low frequencies. Switching according to the envelope of the signal, as is sometimes done with class G amplifiers, is riskier as it is impossible to tell how long an envelope will last. The advantage of class H is that only one power supply is needed. As such it is ideal for car audio applications. To prevent the need for four lifting elcos, it is then built like a bridge amplifier with a signal dependent common mode level. Figure 14 shows a class H bridge amplifier. The common mode level is normally half the supply voltage. When the load voltage must be higher than Vdd, the common mode level of the bridge is increased such that one half of the bridge remains at a constant voltage close to ground and the other half gets the lifted supply voltage. See Figure 15 for the waveforms of the two bridge halves for a sinusoidal output.

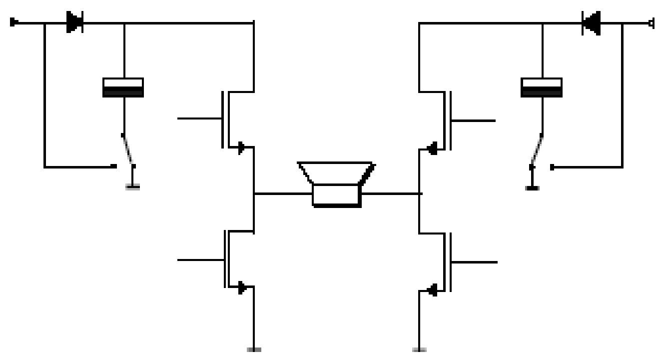

Figure 14: Class-H Bridge Amplifier

For normal audio signals, and even for a rail-to-rail sine wave, only one lifting circuit would suffice. In practice this is not implemented, because it’s a bad habit to test audio amplifiers with near rail-to-rail square waves, which give the lift elco not enough time to recharge.

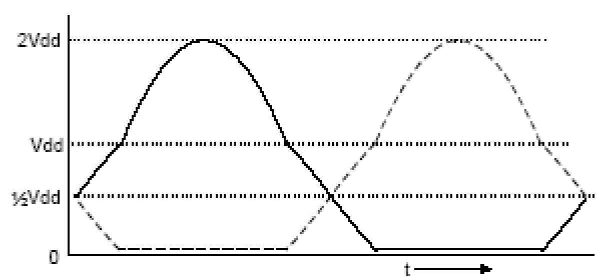

Figure 15: Waveforms of both bridge halves for a sinusoidal Output

The Cool Power Amplifier

The ‘cool power’ technique is very similar to the techniques in the last two paragraphs. The circuit normally operates single-ended: one side of the loudspeaker is connected to an amplifier, and the other end to an elco. The ‘quiescent output voltage’ of the amplifier is half the supply voltage, so it charges the elco to the same value. Because audio signals have no DC component, this voltage will hardly change. During signal peaks that are higher than half the supply voltage, the loudspeaker is disconnected from the elco, and connected to a second amplifier to work in a bridge configuration [25]. See Figure 16 and Figure 17:

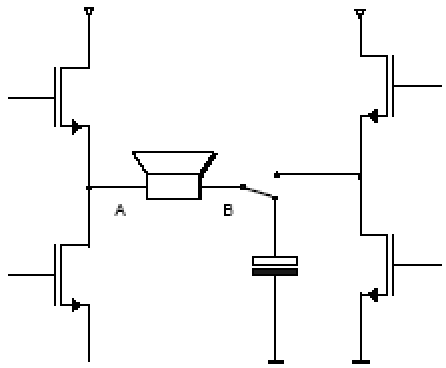

Figure 16***: ‘Cool power’ amplifier.***

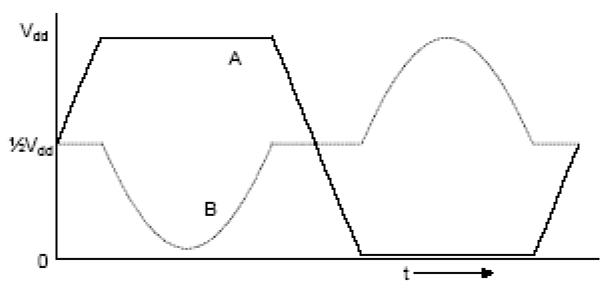

Figure 17: Waveforms of the bridge halves of the cool power amplifier for a sinusoidal output.

Like the class H amplifier, it provides good possibilities for automotive applications, as it needs only one power supply. Contrary to the class H amplifier, there is no limit to the duration of the high power signals. However, it is favorable to design the heat sink for average music/speech signals.

2.2.2 Limitation of Linear Amplifiers

The main limitation of linear amplifier is increasing the number of supply voltage is complex, while the benefit is limited owing the quiescent power dissipation Saturation voltages and quiescent power dissipation are zero. In the ideal case, a class G amplifier with 2 supply voltages halves the dissipation. Adding an extra 3rd supply voltage halves the dissipation again. At present, it is not attractive to use a higher number of voltages. Every extra supply introduces at least 1 extra elco and switching becomes very complicated. When we consider non-idealities, even a third supply seems unattractive. A quiescent power dissipation of 0.02…0.05Pomax is quite usual for audio amplifiers. This means that at 0.1Pomax, approximately the maximum output power for undistorted playback of audio signals, 20…50% of the dissipation is caused by quiescent dissipation. For compressed music (that can play at a higher average output power without distortion) these figures are even less favorable. Furthermore, the maximum dissipation is barely lower than for two supplies.

2.2.3 Non linear Amplifiers

When a system employs constant envelope modulation scheme, the linearity of a power amplifier is not critical. A non-linear power amplifier can be used so as to obtain higher efficiency. Class-C, class-E and class-F are examples of non-linear power amplifiers with high efficiency.

Class C

The efficiency of a power amplifier is increased from 50% for a class-A power amplifier to 78% for a class-B power amplifier with the condition angle decreased from 360° to 180°. It is observed that efficiency greater than 78% can be achieved if the condition angle is further reduced to a level smaller than 180°. The resultant power amplifier is categorized as class-C. In fact, the circuit topologies can be the same for class-A, class-AB, class-B and class-C. The transistor in a class-A, class-AB, class-B and class-C power amplifiers is operated as a current source. The major difference associated with these four types of power amplifier is the biasing condition. With the reduction in condition angle, the efficiency is traded-off with the linearity from class-A to class-C. The price of achieving high efficiency is the poor linearity performance. Moreover, although the efficiency can approach 100% with conduction angle trends to zero, the output power will be zero since there is no drain current at all. Figure 18 shows the current and voltage waveforms of a class-C power amplifier.

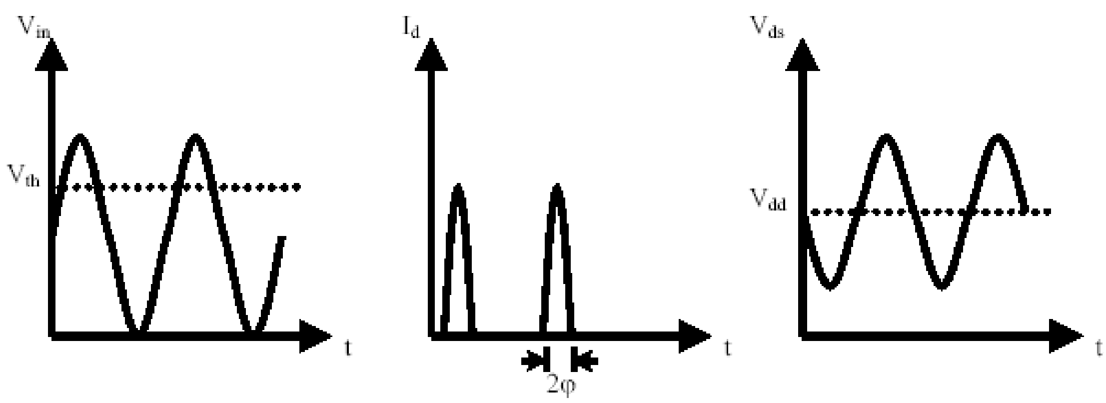

Figure 18: Voltage and current waveforms of an ideal class-C power amplifier

From [12], the DE can be expressed in terms of θ where 2θ is the conduction angle (in radian) for the class-C power amplifier:

$$DE = \frac{\theta - \sin\theta}{4\left[\sin\left(\frac{\theta}{2}\right) - \frac{\theta}{2}\cos\left(\frac{\theta}{2}\right)\right]}$$

The above equation can also be applied to class-A with $2\theta = 2\pi$, class B with $2\theta = 2\pi$, and class-AB with $\pi < 2\theta < 2\pi$.

When the conduction angle is reduced, the input driving power has to be increased in order to maintain the device in the pinch-off regions which is essential to retain the output power level. Among all of the conventional power amplifiers, the input-driving requirement of a class-C power amplifier is the largest. Therefore, a class-C power amplifier is only suitable for a system with constant envelope modulation scheme and low output power. For a system with high output power and a constant envelope modulation scheme, switch mode power amplifier is used which have both high output power and superior efficiency.

Class E

The class-E power amplifier was first invented by Sokal in 1975 [6]. Several criteria have to be fulfilled for a power amplifier to be categorized as class-E. First of all, voltage across the switch remains low when the switch turns off. When the switch turns on, voltage across the switch should be zero. Finally, the first derivative of the drain voltage with respect to time is zero, 0, when the $\frac{dV_{ds}}{dt} = 0$, when switch turns on. The first two conditions suggest that the power consumption by the switch is zero. The last condition, $\frac{dV_{ds}}{dt} = 0$, ensures that the voltage-current product is minimized even if the switch has a finite switch on time. Figure 12 shows a typical configuration of a class-E power amplifier. L_1 acts as either an RF choke or a finite DC-feed inductance [7]. C_2 and L_2 are designed to be a series LC resonator plus an excess inductance L_x at the frequency of interest. C_1 and L_x are designed so that the conditions for a class-E power amplifier operation are met.

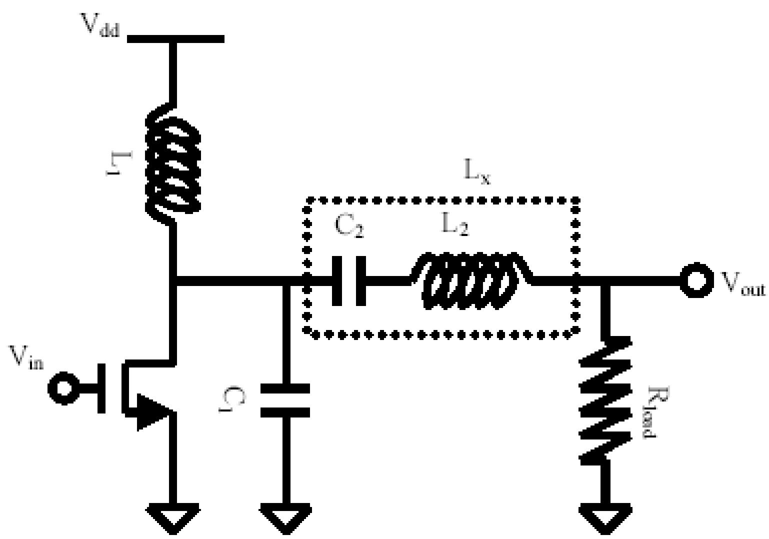

Figure 19 A typical configuration of class-E power amplifier

Figure 20 shows the waveforms of a class-E power amplifier.

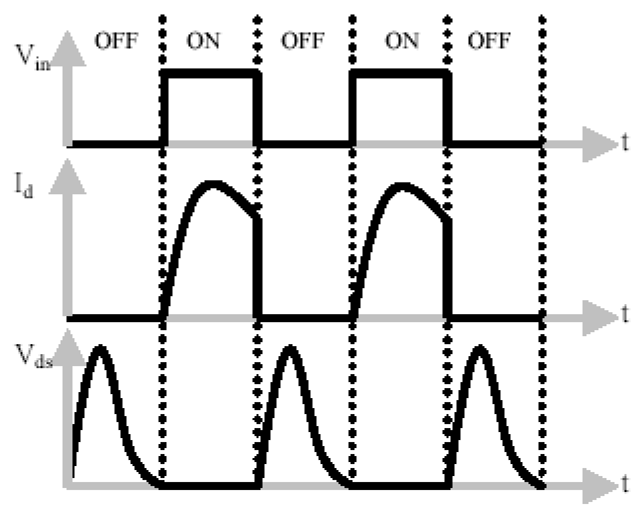

Figure 20 Voltage and current waveforms of an ideal class-E power amplifier

It was observed that there is no overlapping between the voltage and the current waveforms. Class-E power amplifiers achieve 100% efficiency theoretically in the expense of poor linearity performance. However, the peak drain voltage is quite high which increases the stress on the device especially for low breakdown CMOS process.

Class F

The idea of a class-F power amplifier is to exploit the harmonic contents so that the drain voltage and current waveforms are shaped to achieve higher efficiency. A sharper edge of the drain voltage will lower the loss of the switch. Therefore, a square wave is desired at the drain. A parallel LC tank tuned to the third harmonic is included to obtain the third harmonic component and add to the fundamental component to approximate a square wave at the drain of the transistor. The circuit configuration of a class-F power amplifier is shown in Fig.21. L_1 and C_1 are tuned to resonate at the fundamental frequency while L_2 and C_2 are tuned to present non-zero load impedance at the third harmonic frequency to make up the second terms in the Fourier series expansion of a square wave.

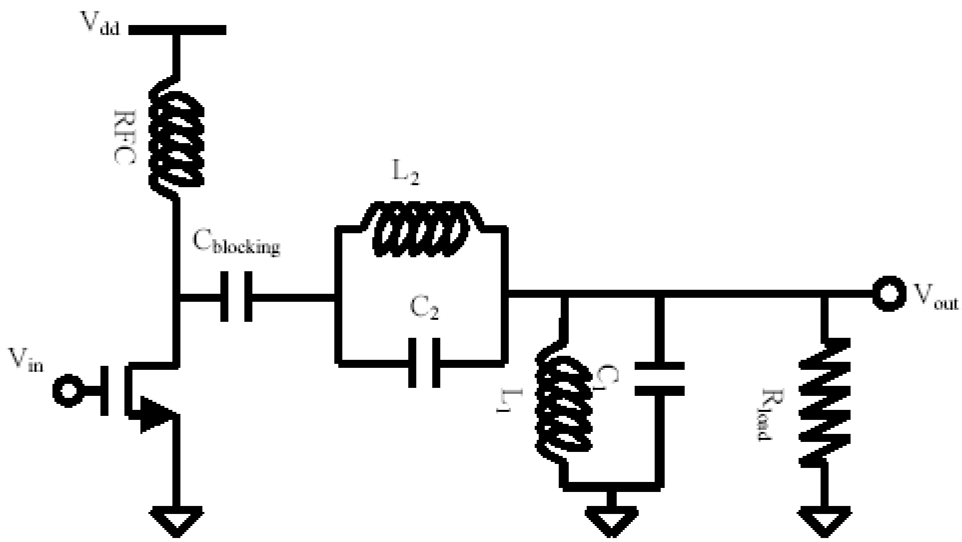

Figure 21 Simple configuration of class-F Power amplifier

Figure 22 shows only the simplest class-F power amplifier with one LC tank tuned to the third harmonic. Additional LC tanks can be added to resonate at other odd harmonic frequencies to obtain a better square wave. The voltage and the current waveforms shown in Fig. 22 will be observed.

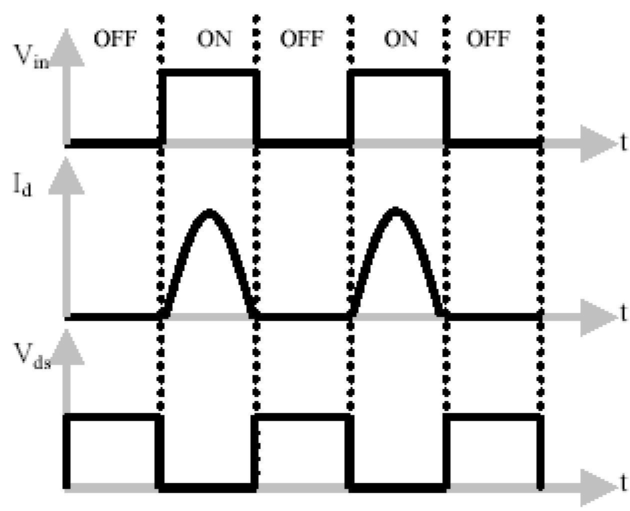

Figure 22 Voltage and current waveforms of an ideal class -F power amplifier

A class-F power amplifier can achieve 100% efficiency ideally. However, the disadvantage, in addition to the highly non-linear performance, is the complicated circuit topology for scaling of 3^{rd} harmonic.

2.3 Switching Amplifiers

Digital modulation offers superior performance, such as noise insensitiveness and integration of low cost CMOS process over analog modulation, and is widely used in wireless systems. To facilitate discussion on the tradeoff between power efficiency and spectral efficiency in digital modulation, literature classifies power amplifiers as either linear power amplifiers or nonlinear power amplifiers [20].

We can also say that digital amplifiers are Switching Amplifiers. With switching amplifiers we mean amplifiers with a switching output stage in which that the transistors in the output stage have a switch function; any simultaneous occurrence of voltage across and current through these transistors is undesirable. Alternatively, switching amplifiers produce audio signals by modulating a rapidly alternating "digital" (or two-state) voltage so that its averaged (or low-pass filtered) voltage represents the desired audio signal. The switching frequency is always much higher than the highest frequency of the desired audio output signal, usually 10 times or more. This rapidly switching output signal is passed through a filter comprised of capacitors and inductors (which are ideally lossless components) before being passed to the speakers. The advantage in using this switching output approach is that the power output transistors, usually MOSFETs as shown in Figure 23, are ideally never operating in mid-conduction and instead operate much like switches either fully "on" or fully "off." When "on" and conducting current to the speaker, each transistor acts like a closed switch, with zero voltage (V = 0) across its terminals and therefore P = V x I = zero, ideally yielding no wasted power. Of course, when "off" the switch is open, I = 0, and the wasted power is also zero.

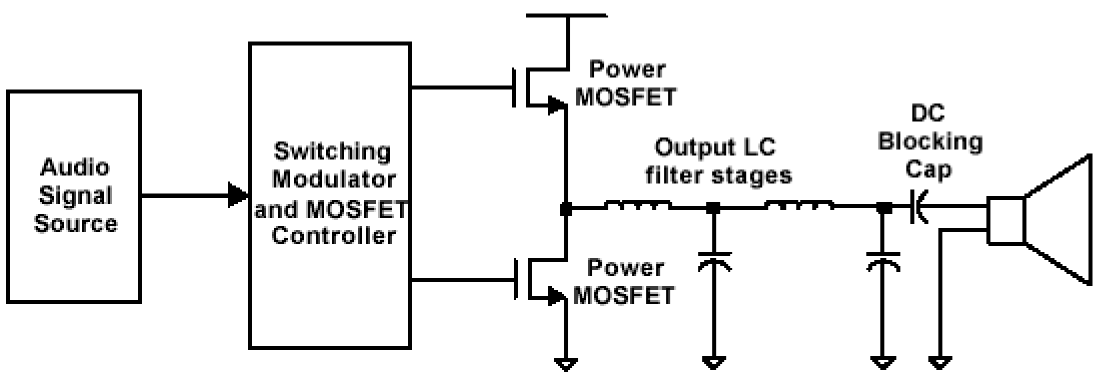

Figure 23: A Typical single-ended Switching Amplifier

As a result, the digital amplifier's efficiency is far better than it's conventional Class-A, AB, or B counterparts and can reach 80% or 90%. In contrast, linear amplifiers are usually less than 50% efficient. The high efficiency of digital amplifiers can be a critical advantage in systems where excessive heat can be a problem, such as in multi-channel surround audio receivers or enclosed systems such as powered subwoofers. Also, in applications where power is at a premium, such as battery-operated portable stereos or laptop/notebook PCs.

2.3.1 Class-D Pulse Width Modulated Amplifiers

Figure 24 shows the most basic and traditionally most common form of switching amplifier modulation, called pulse-width modulation, or PWM. Though the actual implementation actually uses a different technique, having nothing to do with PWM, these waveforms are presented as an example because they are more easily understood as a basis for discussion.

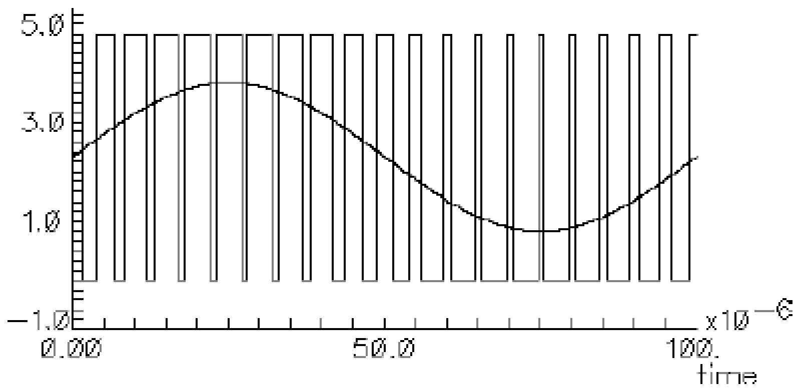

Figure 24: Pulse Width modulation wave form

The rapidly switching waveform traversing between 0V and 5V is the direct, unfiltered signal from the amplifier's power MOSFET output transistors. The smooth, continuous sine wave is the resulting audio obtained after the switching signal is passed through an LC-type filter and then on to the speakers.

2.3.2 Limitations of switching amplifiers

In the previous sections, the main building blocks of switching amplifiers have been discussed. To summaries the limitations that were encountered, it is easy to start with an important audio amplifier specification: low distortion. With feedback directly from the switched output, very good high power PWM signals can be generated. The output filter, however, introduces additional distortion and deviations of the specified frequency transfer when non-resistive loads are connected. Feedback after the filter is difficult, and high feedback factors can not be realized. Even when these problems are overcome, the filter prevents further integration because for sufficient suppression of the carrier frequency, typically a fourth order filter is necessary. It is not possible to eliminate the external two coils and two capacitors without introducing a much larger switching residue.

2.4 Conclusion and Summary

The design of a class D output stage is not a trivial matter. In general, an output stage will not be able to preserve the exact frequency content of its input signal. This chapter provides background for the designer to choose a suitable digital amplifier. Efficiency and linearity are the major considerations when a class of power amplifier is to be selected. It is very important to understand the specifications of the power amplifier in advance because different applications will result in different choices of power amplifiers. A table of summary is shown of the performance of all the classes discussed.

	Ideal Efficiency	**Linearity**	**Practical Efficiency**
Class-A	50%	Good	35%
Class-B	78.5%	Moderate	49%
Class-AB	50% - 78.5%	Good	45%
Class-C	78.5%-100%	Poor	55%
Class-E	100%	Poor	62%
Class-F	100%	Poor	80%
Class-D	100%	Good	90%

Table 3 Performance summaries of different class of power amplifiers

Part 3: Design of Digital Amplifier

Recall that the research goal is to design a CMOS digital amplifier for portable electronics equipment. Therefore, the corresponding specifications should be studied before the design of the digital amplifier. As stated in chapter 1, the output power of the digital amplifier is set to be with intermediate frequency for equipments like head phone application for low or under 1V supply voltage. Among all classes of power amplifiers, the class-D power amplifier is the most attractive candidate in terms of circuit simplicity and high efficiency performance. The circuit technique used for the digital power amplifier to work under low supply voltage will be detailed in this chapter. Different modes of modulations techniques and their relation ship with digital amplification and also, the design considerations of a class-D power amplifier will be discussed. Both the calculated and the simulated results will be presented..

3.1 Design of Digital Amplifier

3.1.1 The class D principle

A typical class D amplifier consists of a modulator that converts an analogue or digital audio signal into a high frequency Pulse Width Modulated (PWM) or Pulse Density Modulated (PDM) signal followed by the output stage, often a half bridge power switch (Figure 25). The output of the switches is either high or low, and changes at a frequency that is much higher than the highest audio frequency. Typical values are between 200 kHz and 500 kHz. The frequency spectrum of the PWM signal in the audio band is the same as the frequency spectrum of the audio signal. An LC filter filters out the high frequency switching components, so that the audio signal is available at the output of the filter. Ideally, the switches do not dissipate and neither does the filter, so the efficiency can be very high.

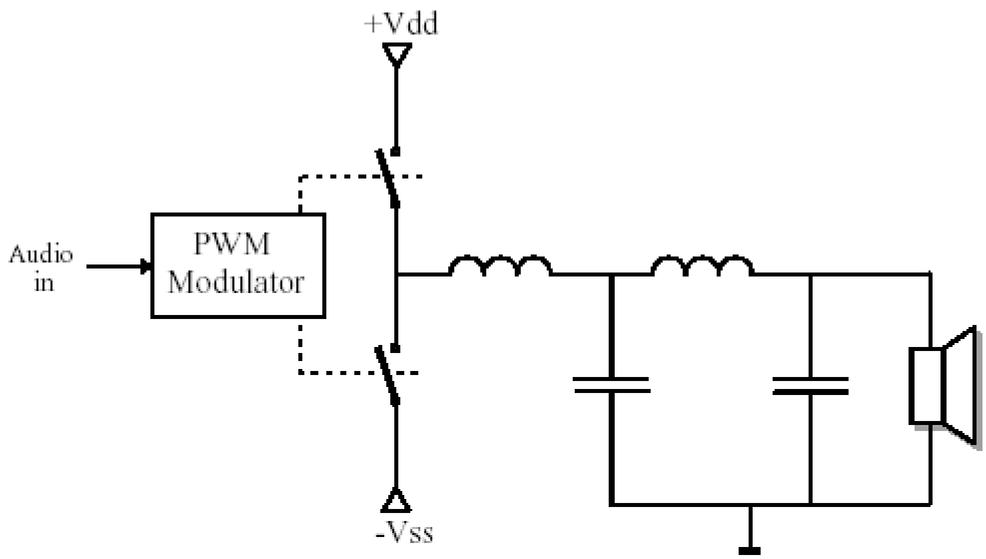

Figure 25: principle of PWM amplifier Output stage

Figure 26 shows a typical class D output stage. It is a class AD stage, which is used for most class D amplifiers. It is a simple inverter: when the input signal is positive, M2 conducts. When it is negative, M1 conducts.

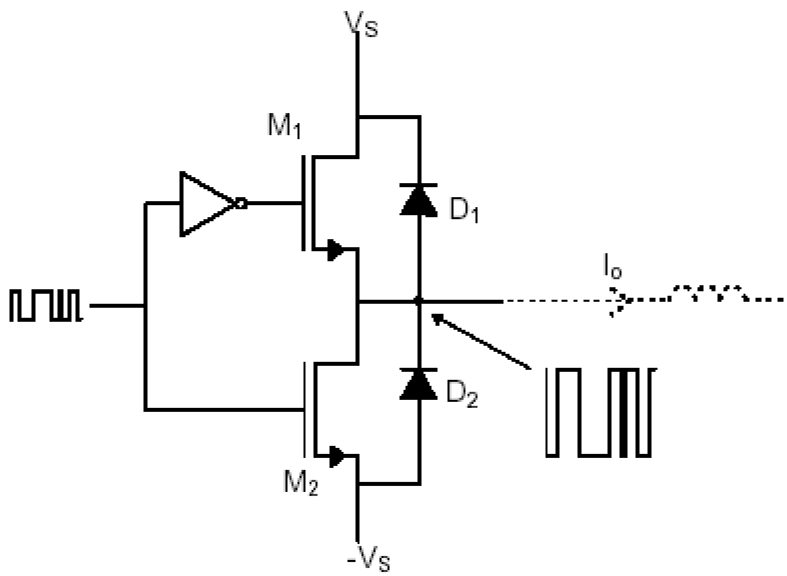

Figure 26: Atypical class D Amplifier

Diodes

The diodes D1 and D2 are needed because the transistors are unidirectional switches. Suppose the output signal is positive, and the output current Io is also positive. When M1 is switched on, this is OK, but when M2 is switched on, the coil in the output filter still tries to keep the current Io, forcing the output voltage below -VS, causing D2 to conduct. With DMOS transistors as switches, the intrinsic diodes can be used. However, the intrinsic diode of a DMOS transistor can have a long recovery time (several hundred ns) or cause latch-up. In that case external (shottky) diodes are a solution, although not a desirable one. It is also possible to build DMOS transistors with a fast-recovery intrinsic diode [34].

Switching speed

High switching speeds are necessary to keep switching losses small. Typical values of today's integrated designs are tens of nanoseconds. Because of the large gate-source capacitances of M1 and M2, this leads to large peak currents. Also, the high speed switching in combination with wires and (gate) capacitances can cause ringing, overshoots, and delays. For a low distortion it is important that the switching times of M1 and M2 are equal [29]. Tunable coils between M1 and M2 can provide a solution. However, both the fact that these coils can not be integrated and that they need to be tuned make this an unattractive solution. With high speed switching, the risk of common conduction of M1 and M2 increases. The introduction of a 'dead zone' in which both transistors are turned off is a common solution, although this introduces extra distortion in the audio signal. Another option is a handshake procedure to check if the other transistor is turned off.

Power supply

In pure feed forward systems a stable power supply is extremely important, because any deviation from the nominal value shows up in the output signal. For an output signal of 16 bit accuracy, the power supply should have a 16 bit stability. Common solutions are feedback from the pulsed output or feed forward correction by referring the triangle waveform to the supply voltage (see section 3.3.5). Another supply issue arises from the use of NMOS devices that are preferable thanks to the lower Ron per area. The gate of M1 needs a voltage that is higher than VS. A bootstrap capacitor or a charge pump can provide such a voltage [56].

Cross-over distortion

M1 and M2 have a certain Ron resistance. D1 and D2 have a certain voltage drop when conducting. Suppose the output current is positive. During conduction of M1, the voltage will be a little lower than VDD because of Ron1. During conduction of D2, the voltage will be a little lower than -VS due to the voltage drop. So all the time the voltage is lower than it should be. When the output current is negative, the same reasoning shows that the output voltage is too high. This results in crossover distortion. It can be solved by connecting the transistors to a tap of the output inductor [29] or a separate supply voltage.

Output stage dissipation

Most of the dissipation in a class D amplifier is generated in the output stage. The dissipation consists of three main components: Conduction losses, switching losses, and capacitive losses. Conduction losses are the result of the on-resistance of the switches. Refer to Figure 25. The conduction losses can be expressed as: $P_{cond} = I_o.R_{on}$

where I_o equals the output current and R_{on} the on-resistance of the switches. Io has some high frequency ripple. At higher output powers it is relatively small, since it is undesirable to dimension the maximum current rating of the switches much higher than the maximum output current of the amplifier. Switching losses are a result of the simultaneous presence of voltage across and current through the switches. Suppose the output current Io is positive and M1 is switched from conducting to non-conducting. The coil in the output filter tries to keep its current Io at a constant value, bringing down the output voltage of the power stage below -VS so that D2 starts conducting. During the time the voltage goes down, Io has to be supplied by M1. Figure 27 shows the corresponding waveforms.

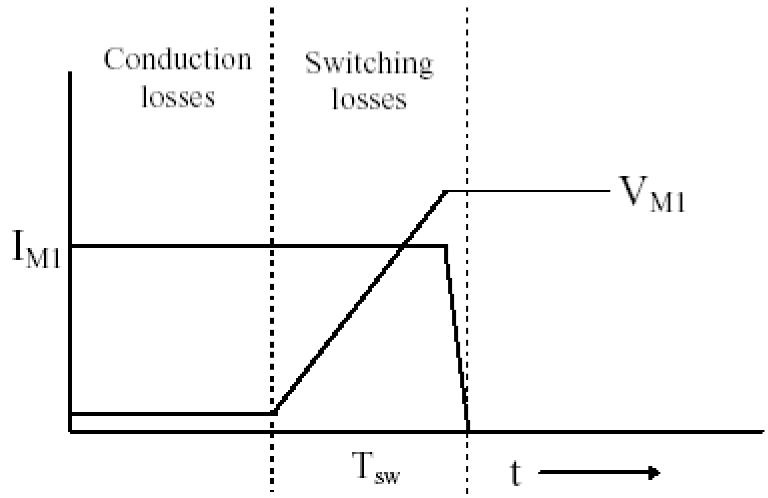

Figure 27: Voltage over Mi and current Over M1 during switching from high to low output voltage

If we assume the voltage across M1 to rise linearly from 0 to 2VS, the dissipated energy during the switching time T_{sw} approximately $1/2*2V_s*I_0*T_{sw}=I_0V_sT_{sw}$. There are two transitions per period of switching, so the switching losses at a switching frequency f_{sw} can be expressed as:

$$P_{switch}=2V_sI_0T_{sw}f_{sw}$$

The third source of dissipation is (internal) capacitances that are charged and discharged. When a capacitance C with zero initial charge is charged to a voltage V, the final energy $1/2CV^2$ has also been dissipated during the charging process. This can be prevented with the aid of inductors like in the output filter, but the driving circuitry of the gate capacitances, for instance, does not work that way. This brings the capacitive losses to:

$$P_{cap}=C_{\sin}V_c^2f_{sw}$$

where f_{sw} is the switching frequency, C_{int} are the internal capacitances and V_c is the voltage to which these capacitances are charged. In a practical system there is more than one capacitance present, and they may work at different voltages. In a class D output stage, all three dissipation sources are significant. The model

parameters were matched to the class D stages that were used in our experiments. This yielded 16ns switching time, a total on-resistance of 0.65□, and internal capacitances of 500pF. With these values the dissipation at higher output powers could be predicted with less than 10% error. Possible errors include negligence of the drain-source capacitances, which are charged and discharged at the switching frequency. If this is done by the coil current, the process is lossless. If it is done by the output transistors, it is not. The actual situation depends on the output power, the switching time and the ripple current. The dissipation model is useful for sizing the output transistors. If very large transistors are utilized in an output stage, the conduction losses will be small, resulting in a lower maximum dissipation. The capacitive losses, however, will be considerable, resulting in a higher quiescent dissipation. This is a common trade-off in class D amplifiers, which could be circumvented by using small transistors at low output currents and larger transistors at high output currents. Reduction of the switching time T_{sw} is always favorable, as it decreases the switching losses.

3.2 *Modulators and Feedback with Digital Amplification*

There are numerous modulators, and it is not our objective to give an extensive overview. In this section, only the basic topologies are discussed. A low cost digital audio power-amplifier suitable for direct processing of digital sources has been of great interest to the consumer electronics industry over the last few years. Here we review some current solutions for a digital power-amplifier based on Pulse-Width- and Sigma-Delta Modulation.

3.2.1 Pulse-Width Modulation

Pulse-Width Modulation (PWM) is an established technique in industrial applications for motor control and power supplies. PWM is based upon pulses having a fixed cycle-time and a variable pulse-width with the width being proportional to the mean value of the input signal. A fundamental system to create pulse-width modulated signals is shown in Figure 28. The input signal is compared with a linearly ascending reference signal. The period of the reference signal defines the cycle-time of the PWM pulses. If the input signal is higher than the reference, the pulse is switched to the HIGH level, otherwise to the LOW level. Usual forms for the reference signal are ascending, descending and also double-sided ramp [5].

Analogue PWM Systems

The switching times in all analogue PWM systems are derived from a continuous input signal not held constant over a pulse period. This is called natural sampling [5],[6]. Complete PWM based audio amplifiers in integrated form are offered by some semiconductor manufacturers, including Texas Instruments [7] and Philips. These systems only use analogue components; thus input and output signal are analogue. In the analogue domain a PWM signal can be generated by comparing the audio signal to a triangle or saw tooth waveform. This technique, called natural sampling, is the basis of almost all analogue modulators. See Figure 28. When the momentary value of the input signal is larger than the triangle, the output of the switch is high. It is easy to see that in this way the pulse width at the output is proportional to the input voltage. The modulator does not introduce harmonic distortion, only (multiples of) the carrier frequency and (multiples of) harmonics of the modulating frequency around the carrier [1].

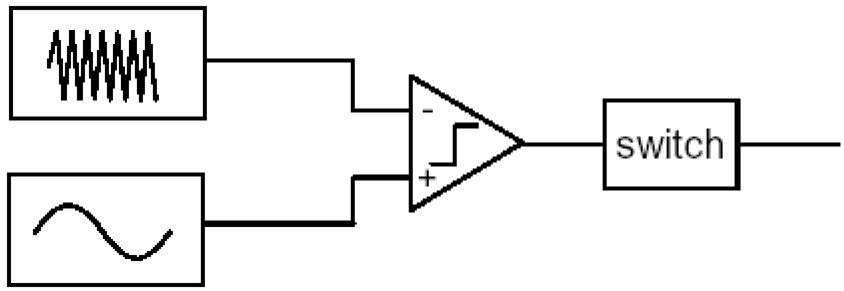

Figure 28: open loop class- D modulator

The main problem is the lack of feedback. Output stage inaccuracies, nonlinearities, timing errors and supply voltage variations all contribute to the distortion. We will discuss feedback here, as it is so closely related to the modulator. Figure 29 shows a modulator with feedback. Both inputs to the comparator have triangular waveforms. Figure 30 shows the waveforms for zero and positive output voltage. At zero output voltage, the feedback signal intercepts the reference triangle in such a way that the duty cycle is 50%. When the output voltage is not zero, the rising and falling slope of the feedback triangle are different, leading to a larger (or smaller) duty cycle.

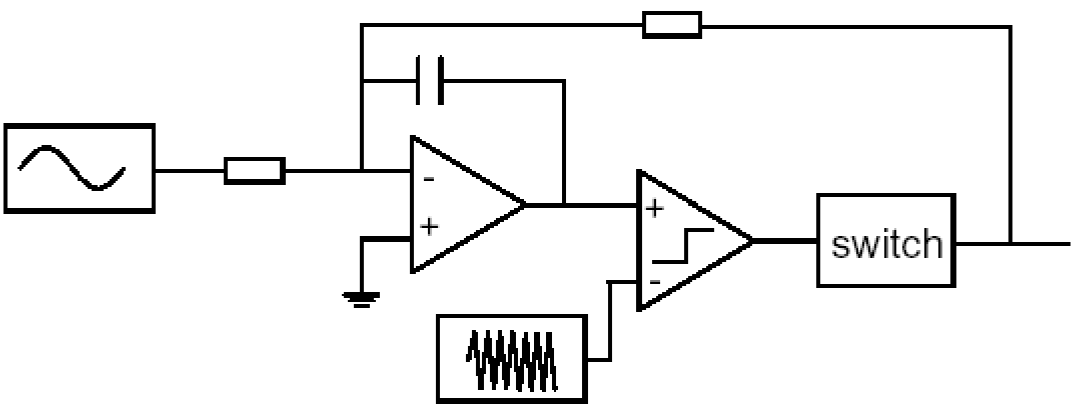

Figure 29: modulator with feedback

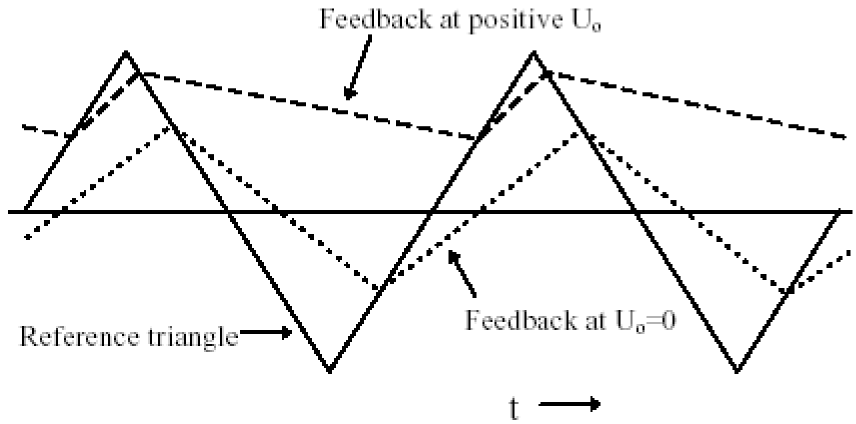

Figure 30: signals at the input of the comparator of the input modulator

The slew rate of the feedback signal must always be smaller than the slew rate of the reference triangle. Otherwise, the amplifier starts oscillating at a very high frequency. This constitutes a compromise between switching frequency and loop gain. The slew rate requirement can roughly be translated to the demand that the loop gain of the amplifier at the switching frequency is smaller than ½. Thanks to the integrator, the open loop frequency transfer of the amplifier is first order, so that the loop gain at a certain frequency has a maximum that is related to the switching frequency. A way to get more loop gain at low (audio) frequencies is by introducing a range with second order frequency response in the loop. As long as the loop gain is back to first order at 0dB, stability is ensured. This can be done in the modulator by adding a second integrator before the comparator while bypassing it for high frequencies [40, 38]. In practical realizations of a feedback modulator, the triangle is generated by adding a square wave to the input of the integrator [41]. The feedback properties of this type of modulator can also be used when the input signal is generated by a digital modulator [40]. Because in that case the bit stream is already clocked, the negative input of the comparator can be tied to ground. Other techniques, like the one cycle control technique [35] or pulse edge delay error correction [39] are similar to this modulator in their attempt to control the integral of the switched output voltage. The high frequency oscillation that occurs in a feedback modulator when the feedback signal is too large, is exploited in the self-oscillating class D modulator [41]. See Figure 3.28. The comparator is equipped with some hysteresis to control the switching frequency. Other factors that influence the switching frequency are the integrator time constant and the output voltage. For large output voltages, the frequency approaches zero. This can cause aliasing problems that can be overcome by using a comparator with a variable hysteresis dependent on the input voltage. In that way the oscillator frequency is kept constant over a wide range of output voltages [31].

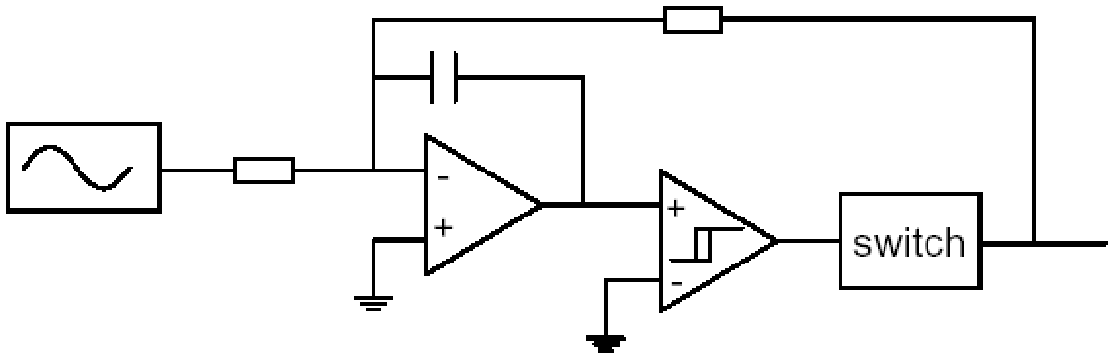

Figure 31: self oscillating class D modulator

In the situations above, feedback is successfully taken before the output filter. The combination with feedback after the filter is more troublesome.

Digital PWM Modulators

A digital Pulse-Width Modulator can process digital input data directly. The basic PWM scheme is implemented as an algorithm in a DSP or as logical functions in a FPGA to convert from Nyquist rate PCM to a suitable PWM signal. Digital PWM modulators offer a lower switching frequency than PDM modulators. The Pulse Amplitude Modulated (PAM) samples are converted to PWM. This could be done by giving each pulse a length that is proportional to the original amplitude. However, for CD quality the internal clock frequency would have to be 44.1kHz*216= 2.9Ghz, which is way too high. Furthermore, the frequency spectrum of the PWM signal would not equal that of the PAM signal. This can be calculated, but for a better understanding it is best to realize that natural sampling yields the best results because it does not introduce harmonic distortion. In natural sampling, the audio signal is compared to a triangle or saw tooth waveform (see the analogue modulator section below). When we convert a digital PAM signal directly to PWM, it looks as if, looking in the analogue domain, we compared the sawtooth waveform to a step-like representation of the signal instead of the signal itself. This is called uniform sampling. See Figure 32. It introduces harmonic distortion, which depends on many factors including the signal frequency, the switching frequency and the modulation depth [1].

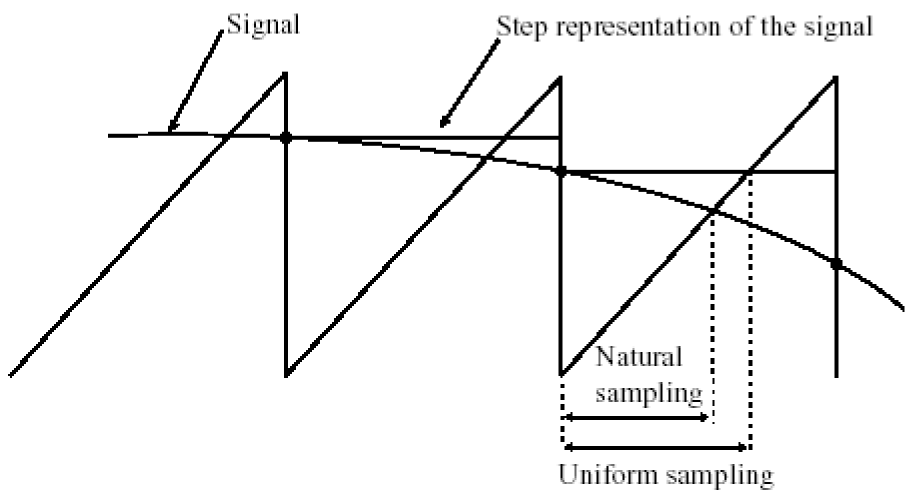

Figure 32: natural sampling versus uniform sampling

To approximate natural sampling, linear or higher order interpolation between two or more samples is used to approach the natural PWM pulse width [33, 39, 41]. When the pulse width has been calculated, the sample instant can be the beginning or the end of the pulse (single sided modulation) or the middle (double sided modulation). There are more aspects that deserve attention, but a full discussion of these would be beyond the scope of this chapter.

3.2.2 Non-linear Distortion

Fundamentally PWM is a non-linear process. The spectrum of the output pulse-series contains the pulse repetition frequency and its harmonics plus the spectral components caused by the modulation. A complete derivation of the PWM-spectrum can be found in [5],[6]. In a digital modulator the PWM pulse does not represent the mean-value of the continuous input signal, but one sample value. This causes further distortions [5],[6], which reach into the base-band of the audio-signal. The spectrum of the audio base-band from a PWM-simulation is shown in Figure 33. The leftmost line represents the original input tone, all further ones result from the non-linear process. One method of linearization is to get nearer to the naturally sampled PWM. This can be done by polynomial interpolation investigated in [8] and [6] and thus allows an estimation of the sampling time of natural PWM. Another approach developed in [9] is based on the spectral properties of the pulses. A target pulse width with a specific frequency-spectrum is chosen. The aim is to achieve the best equality in the range of the audio base band in the spectrum of all pulses. This is done by adaptive FIR filters and a recursive coefficients estimation algorithm. In a third method used for a commercial amplifier solution a non-linear model of the PCM to PWM conversion is derived [10]. This model is used directly to form FIR filters for different powers of the input-signal, which cancel the spectral properties caused by the non-linear behavior. This method is used

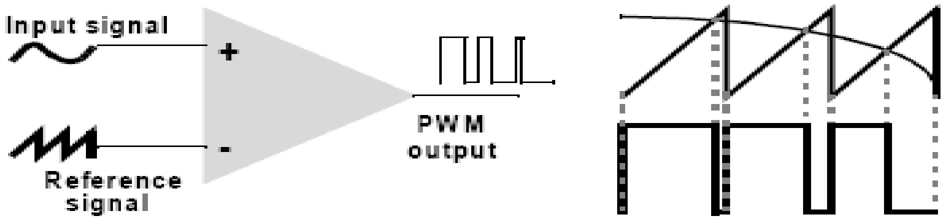

Figure 33: Generation of PWM [5]

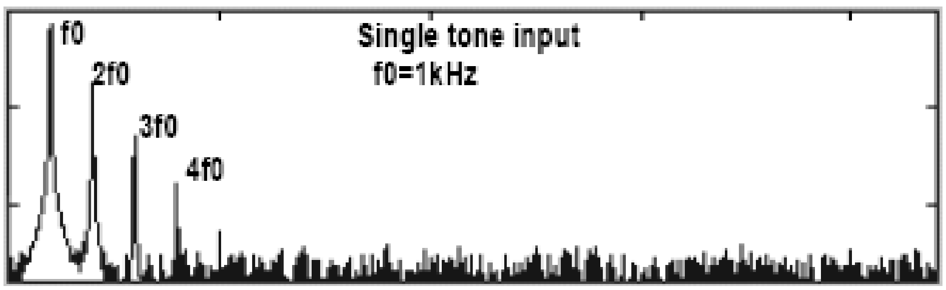

Figure 34: Spectrum of uniformly sampled PWM[5]

Limited resolution of digital systems

The maximum clock-frequency of the digital processing limits the resolution in creating the PWM pulses. To sample a signal quantized to 16 bits, 65536 different pulse-widths would be necessary. With a sampling-frequency of 44.1 kHz and trailing edge modulation the clock frequency has to be 44100*65536=2.89 GHz. For this reason the quantization is limited to a lower number of bits and noise-shaping is applied [12].

3.2.3 Sigma-Delta Modulation (Σ-Δ)

A basic first order sigma delta (Σ-Δ) modulator (or loop) is shown in Figure 5. Similar to PWM the original Nyquist rate PCM signal can be recovered by low pass filtering the bit stream. A sigma delta loop necessarily over samples the input signal, and the spectra of the bit stream output indicates that the original base band information has only a low level of quantization noise, where at frequencies above half of the Nyquist sampling rate, the quantization noise has been increased. This is referred to as noise shaping. Therefore unlike PWM the Σ-Δ modulator already contains a quantization noise-shaping. To achieve improved noise-shaping higher order loops can be used, although due to the non-linear nature of the loop, this higher order design is not trivial [13].

Solutions of Digital Power Amplifiers using Σ-Δ

In theory the Σ-Δ modulator can be used directly to convert over sampled Nyquist rate PCM data into a power bit stream, which can be filtered by analogue low pass filters. The key modification is to replace the quantize by a power-switch consisting of transistors. However the main problems of the implementation are the high switching frequencies. Consider a 64 times over sampled Σ-Δ modulator with a sampling-frequency of 44100 Hz, a clock frequency of 2.8224 MHz can be calculated. The highest possible pulse repetition frequency that can occur then is 1.4112 MHz. The losses in the power-stage are too high at such a frequency and therefore strategies to reduce the pulse repetition frequency have been investigated. One straightforward method is the pulse group modulation [11]. The output of a Σ-Δ modulator is divided into sections of N bits and these bits are ordered according to their sign. This produces a PWM from the Σ-Δ output. As the Σ-Δ modulator bit-stream represents uniformly sampled data, the typical distortions of PWM are introduced as well. A feedback of the erroneous signal over a low pass-filter is suggested in [14]. Another method investigated controls the number of consecutive changes in the state of the Σ-Δ bit stream. This method is called bit-flipping [15]. When the number of consecutive changes exceed a certain number, the current bit is inverted to save one transition. This method can be varied in the maximum number of transitions and the number of bits to be inverted. Another problem in the implementation of ΣΔ for power amplification is the dependence of the noise-spectrum on the input signal and the generation of idle-tones [16]. Chaos in the noise-shaping filter and dithering can be used to reject these unwanted frequencies [17].

3.2.4 PDM modulators

PDM modulators have resulted from the digital signal processing domain. In more and more equipment, the signal is available in digital form. For a switching amplifier it must be converted into a 1 bit signal at a high frequency. Sometimes, as with DSD audio data, this is even the native format. The output stage acts as a 1 bit D/A converter. Because the length of each bit is constant, and only the presence or non-presence of a bit is controlled, this is called Pulse Density Modulation (PDM). To convert a multi-bit signal to a 1-bit signal, over sampled noise shaping is used. Figure 35 shows a general noise shaper [62].

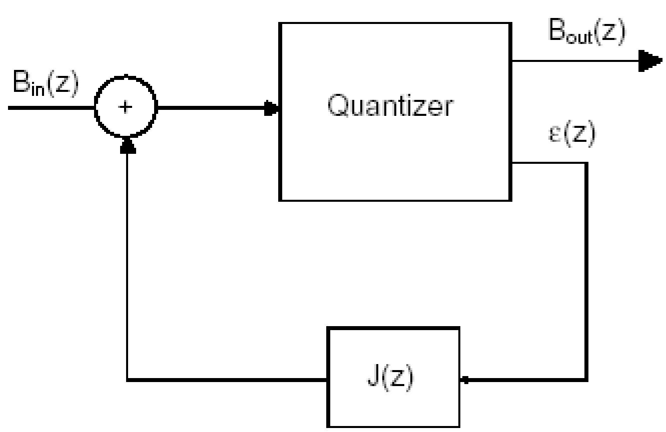

Figure 35: Noise shaper

The input signal $B_{in}(x)$ has a larger number of bits than $B_{out}(x)$. (When the input signal is analogue, a similar structure in the analogue domain constitutes a sigma delta modulator [30,62]). The block called

'Quantize' reduces the number of bits by simply passing only the most significant bits to $B_{out}(x)$. The least significant bits, which are the error, are added to the input after passing through a transfer function J(z). It is easy to calculate B_{out} :

$B_{out}(x)$ = $B_{in}(x) - \mathrm{e(Z)(I\text{-}J(x))}$.

Suppose $J(Z) = Z^{-1}$, one clock delay. The system is now a first-order noise shaper. $B_{in}(x)$ is a 16 bit signal at 256 f_s and $B_{out}(x)$ is a 1 bit signal at 256 f_s , In that case, the quantize transfers 1 bit to the output. The other 15 bits are the error signal. B_{out} : equals:

$B_{out}(z)$ = $B_{in}(z)x) - \mathrm{e(z)(I\text{-}z^{-1})}$.

With Z = $e^{2\Pi j(\frac{i}{256 f_s}}$), we see that for low frequencies (audio) the error in the output signal approaches zero. The error reaches a maximum for f=128fs. See Figure 36.

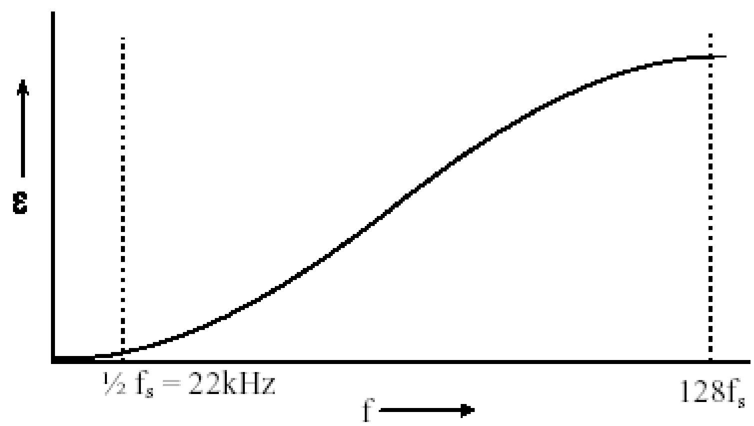

Figure 36: Noise distributions as a function of frequency

Applying Bout to a 1 bit D/A converter and filtering above 20kHz reconstructs the original signal. In the time domain such a noise shaper is a way to convert resolution in the amplitude domain to resolution in the time domain. It outputs bits at high speed in such a way that the average is the intended output (which has a higher amplitude resolution). This way it is also easy to see that although the D/A converter is only 1 bit, it should have a 16 bit accuracy. To convert the audio signal to 256fs, an oversampling interpolating filter must proceed the noise shaper. A two times oversampling filter works as follows [32]. Suppose the spectrum of the signal sampled at fs looks like Figure 37. This signal is converted to a sampling frequency of 2fs by inserting a sample of value zero after every original sample. See Figure 38. Because every sample is a Diracpulse of proportional height, the frequency spectrum stays exactly the same.

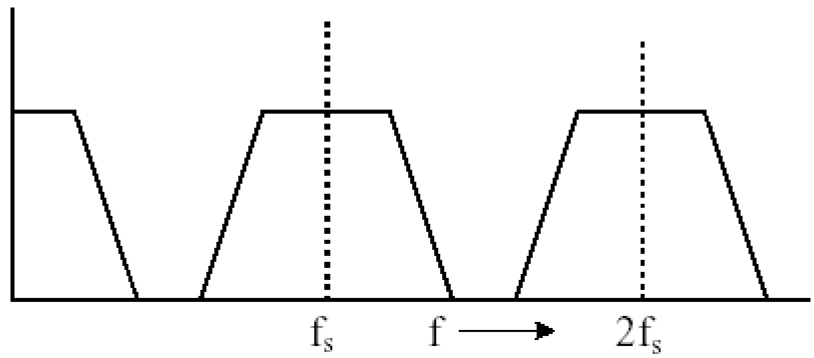

Figure 37: Spectrum of signals

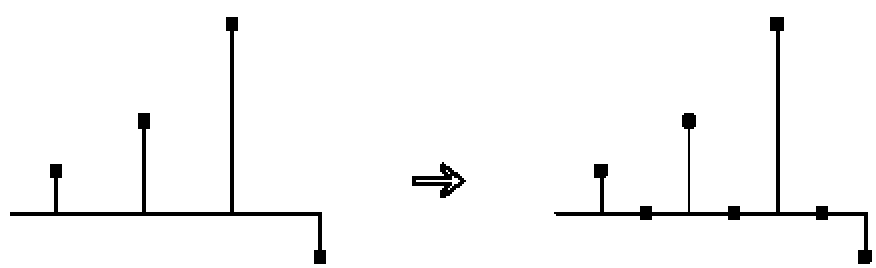

Figure 38: inserting zero samples

Next, the signal is applied to a digital filter at 2fs that filters out the middle replica, see Figure 39. After that, the frequency spectrum of the signal looks exactly like it has been sampled at 2fs. These techniques, oversampling interpolating filtering and noise shaping are essential for all digital PDM systems, although the exact realization may vary.

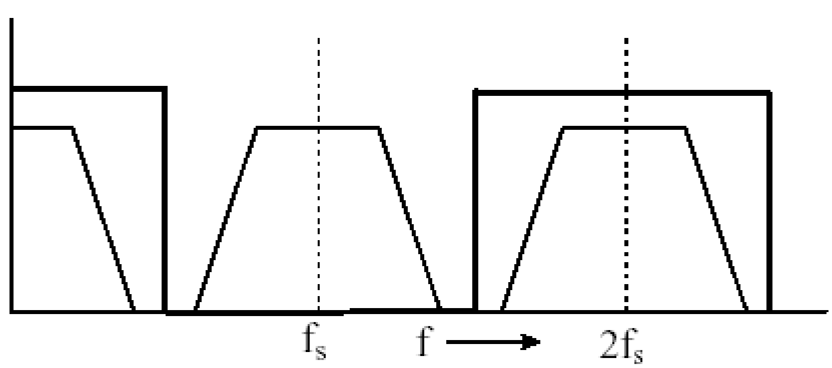

Figure 39: Filtering and the middle replica

In [62], the 256 times over sampling for a CD player D/A converter is done in two stages. A four times over sampling filter is followed by a 64 times linear interpolator. The direct use of a 256 times oversampling filter is also possible, but the filter would be very large. A linearly interpolating filter is easier to build, and at 4fs the distortion that it creates has only little effect in the audio band. Then, at 256fs, a second order noise shaper suffices to get a 1 bit signal with 16 bit resolution in the audio band. Unfortunately 256fs=11MHz which is too high for power switching. Another possibility is to use only 32fs with an eighth order noise shaper [27]. Noise shapers with a higher order than three are prone to instability, and it is necessary to manipulate the system when it becomes potentially unstable [33]. Extensive simulations are necessary for evaluation. Even in this case, the switching frequency is 1.4MHz. The high switching frequencies are a general problem of PDM modulators. Bit-flipping techniques can reduce the average frequency at which the output changes somewhat [36].

3.2.5 Comparison of both methods and conclusions

Both PWM and Σ-Δ have their advantages and disadvantages in the usage for power amplification. PWM offers the lowest possible switching-frequency, but without proper linearization the audio base band will be distorted if applied to uniformly sampled data.

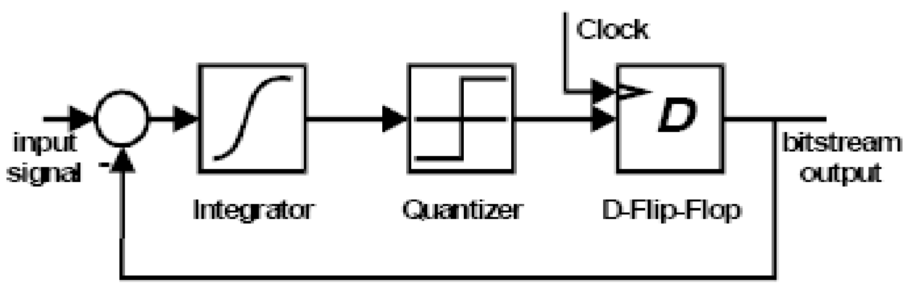

Figure 40: Basic-Sigma delta modulator[16]

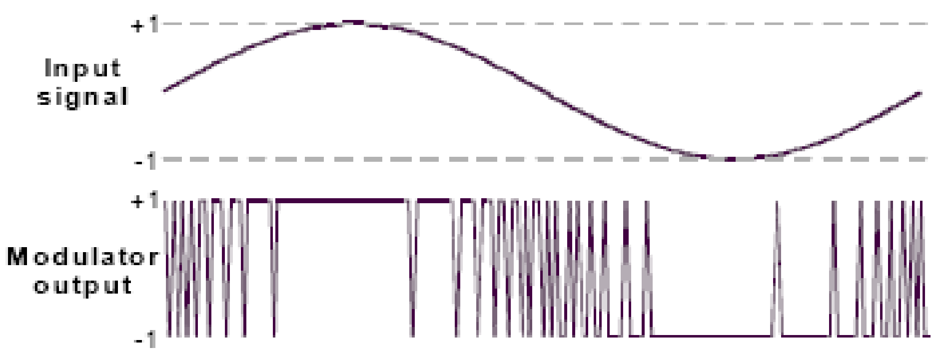

Figure 41: modulation of Sinusoidal signals[16]

The linearization methods based on interpolation and non-linear modeling require high computational power. The Σ-Δ modulator is a more linear method, if the presence of idle patterns is reduced by dithering or by the use of chaotic modulators [27]. Σ-Δ produces a bit stream, where the pulses are distributed uniformly over the over sampling period. This causes high switching frequencies in the power-stage. The number of bit-transitions can be reduced by controlling or re-organizing the current bit-stream. So far linearized PWM provides good audio quality at moderate switching frequencies and thus was chosen for the implementation in one of the first fully digital implementation by the Danish company TOCATTA [23]. Less consideration has been given to the real behavior of the power switches, the reconstruction filter and the loudspeaker as a strong non-linear load. In [23] the design of an approximately ideal output stage as a hybrid element is described, but the effort to produce such a device is very high. The introduction of feedback from the filtered or unfiltered output would provide a possibility to control the distortions caused by these elements. This would ease the demand on the circuit design drastically. The use of feedback implies a conversion from the analogue to the digital domain to be processed by the modulator system. This causes a delay in the feedback path which is harmful for the stability of the system. Another possibility is to make a model of the output circuitry and to provide a correction of the input-signal in the digital processing. A third method used in [29] is to implement the Σ-Δ modulator containing the power-stage in the analogue domain and to provide an error-feedback. The investigation of the switching-stage, the output circuitry and the influence of a non-ideal power supply is our current work. Other possible ways to reduce the pulse-repetition frequency

in order to optimize the effort of signal-processing and output-performance are also being investigated. The introduction of feedback to bring further linearity into the conversion process and to reduce the cost of switching elements should also be of benefit.

Part 4: Design of ∆Σ modulation based Class-D Digital Amplifier

This part depicts the basic features of the implementation that has been achieved. The basic aim of the implementation was to design CMOS digital audio Amplifier for portable application, but to demonstrate and test the issues defined in the previous Chapters. Only the basic aspects are analyzed, since an exhaustive discussion about the audio amplifiers design and implementation would be quite aboard. Here in this part we described the digital Σ-∆ modulator of the proposed Class-D audio amplifier is describe in section 3.1, its class-D output stage is presented in section 3.2, while full investigation is discussed in section 3.3, the proposed class D audio amplifier for portable application is implemented in a 1.8-V 0.18 μm CMOS process and the performance is discussed in section 3.5.

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4.1 Implementation

This chapter depicts the basic issues of the implementation that has been carried out in order to demonstrate what has been discussed and analyzed in the previous part.

In this thesis several attempts have been done to implement a digital power amplifier capable of directly coupling to digital source, thereby eliminating the need for the first converting the digital audio-signal to analog. The digital amplifier (figure 42) performs power amplification directly from the PCM digital audio-data and uses class D output stage for improved power efficiency. Class-D systems have a switching output stage whose transistors are always turned fully off, there by achieving a high power efficiency ideally is 100 %)

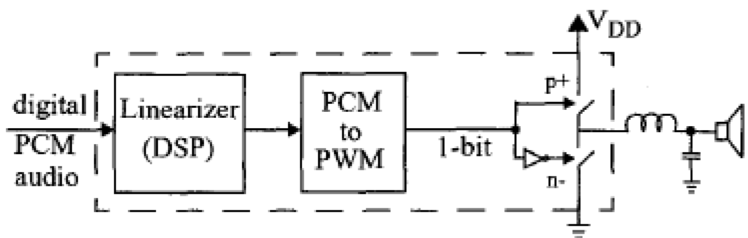


Figure 42: Typical digital amplifier architecture

In a Class-D amplifier, the audio signal is converted in to a high frequency pulse width modulated PWM signals whose pulse width varies with the amplitude of the audio signal. The varying-width pulses switch the output transistor of the class D output stage at a fixed frequency. A low pass filter (LPF) then converts the output pulses into an amplified audio signal that drives the speaker.

Direct PCM to PWM conversion (a process known as uniformly sampled pulse width modulation or UPWM) introduces harmonic and non harmonic distortion in the output spectrum of the amplifier. (27,30). A number of methods have been proposed to correct the non linearity of UPWM in order to minimize distortion in the audio band (27,29,30,31).How ever proposed algorithms required DSP computation and complex hardware to implement. In place of PDM algorithms in this work we proposed ΔΣ modulation to generate a bit stream switching signal whose pulse has a fixed width where the output signal is determined by the short-term pulse-density average. ΔΣ Modulation offers a number of benefits over convectional PWM. Particularly attractive is its advantage of shaping the quantization noise and pushing outside the audio band where it can be filtered out by LPF preceding the speaker), there by resulting in an improved harmonic-distortion performance.

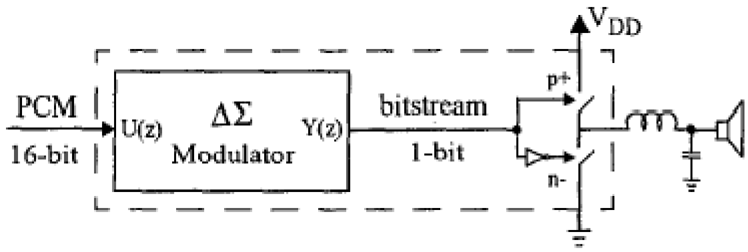


Figure 43: proposed digital class-D amplifier architecture

As an alternative to PWM digital amplifier, a ΔΣ based amplifier switches the transistor in the Class-D output stage at a high frequency. There by dissipating more power. This is why PWM has been preferred in the implementation of digital amplifier. However with the High speed of modern technology and when operating from low voltage, this may no longer be an issue. In addition to the above direct ΔΣ modulation is proposed to generate the switching signal and offers improved harmonic distortion. ΔΣ modulation performance with a low clock frequency rate by avoiding the hardware complexity of UPWM linearization. Using ΔΣ modulation produces a higher switching frequency.

4.2 Design of ΔΣ Class-D Audio Amplifier

Class-D amplifiers are, as said, amplifiers that involve modulation. The filtering retrieves the average signal. So if we want to reproduce the audio band (20-20000 Hz), we need to use such a high frequency, that the average signal can still reach 20 kHz. Several modulation techniques exist. The simplest is Pulse Width Modulation, where at a fixed frequency, the audio amplitude is compared to a triangle-shaped wave and the duty-cycle of this comparison contains the original amplitude. Pulse Density Modulation is essentially the same as sigma/delta modulation. The amount of fixed-width pulses per time unit is analogous to the audio amplitude. Pulse Position Modulation is, as the name implies, a modulation method where the position or phase of the pulse in the duty cycle carries the information and hence largely compatible with PWM, but the energy content per cycle is always equal. There are many derivative forms of modulation, which are all a combination or variation to the forms described above. All the forms of modulation can also be synthesized digitally.

As said, class-D and sigma/delta audio are quite alike. They both have only 2 levels, a high frequency modulation scheme and noise shaping characteristics. It therefore makes sense to use a class-D amplifier with 1 bit audio: just apply a power stage after the bit-stream, amplifying it directly, filters it and you're done. Unfortunately, it is not as simple as that since the bit-stream runs at a very high frequency. If you want to switch a power stage at such a high frequency, you create large errors due to the dead-time needed to prevent shoot-through. One of the solutions that has been applied, is recalculating the digital data to an 8 bit word (using noise shaping) and using the 8 bit info to create 256 possible duty cycles, and then running the power stage at 300 kHz with the discrete duty-cycles.. Another possibility is to still try and amplify the bit-stream directly, but apply a PWM feedback over the PDM pulses. Using this feedback, errors have the effect that the pulse is widened to still have the same area (amount of energy). Hence, several pulses are 'smeared' together, and thus the switching frequency is lowered as well. The high-end solution would be to accept the higher distortion and still run at a very high frequency, but that would imply a powerful driver as well to drive all those gates so fast. 1-bit isn't "Delta-Sigma" (which is an encoding strategy) – 1-bit in this case is Pulse Density Modulation (PDM). The samples are represented with a frequency modulated square wave, with pulses of equal duration. This is as compared to Pulse Width Modulation, where the duration of the pulses is modulated rather than the frequency of the pulses. One could say that PDM is a frequency domain approach, while PWM is a time domain approach. A new inverter topology based on high frequency power conversion and Sigma-Delta Modulation is proposed. Sigma-Delta technique is particularly an attractive idea in audio power amplifying area. Analysis of this technique is presented. Power modulation is a way to obtain power amplifiers with better efficiency than conventional lineal power amplifiers. A quasi-resonant converter with Sigma-Delta modulation in-put, has been integrated to reduce switching losses, allowing high frequency operation. Audio power amplifier and isolated high power supply are integrated in one unit and analyzed. Simulations are performed to backup the analysis.

In this thesis the proposed ΔΣ modulator based digital class-D amplifier architecture, is function in the 3rd order topology shown in figure 44. The noise transfer function (NTF) can be calculated by using the following transfer function:

$$NTF = \frac{(z-1)^3 + b_3\partial z(z-1)}{z^3 - (k_1 - b_3\partial)z^2 + (k_2 - b_3\partial)z - (1 - a_2)}$$

Where $k_1 = 3 - a_1 b_3 - a_2,\qquad k_2 = 3 - a_1 b_3 - 2a_2 + b_1 b_2 b_3,$

and ∂ is the coefficient of the resonator feedback. The single bit quantization is used to simplify the post processing of the modulator output signal while achieving the low harmonic distortion. To guarantee stability the loop-filter coefficients must be chosen such that the [NTF] > 1.5 over all frequencies. In order to reduce the digital hardware complexity, the coefficients must to have a power of two value, which can be implemented only adders and fixed shift value. The modulator is optimized to achieve the desired resolution which is less than 16 bits in audio at low frequencies of 5.6MHz. By using this above analysis the loop filter coefficients are given in the table 4.

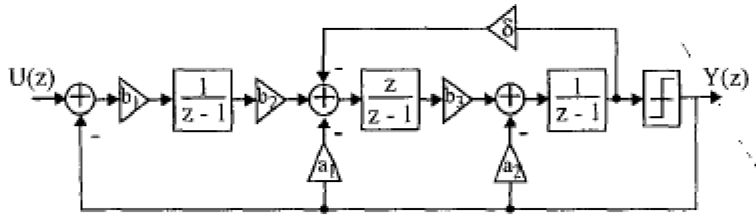


Figure 44: 3rd order single-bit ΔΣ modulator

$a_1 = 2^{-2}$	$b_1 = 2^{-2}$	$b_3 = 2^{-1}$
$a_2 = 2^{-2}$	$b_2 = 2^{-2}$	$\partial_1 = 2^{-13}$

Table 4: Coefficient value of the ΔΣ modulator

For the simulation we use 3rd filter and the result shown that a single bit out put with a small coefficient values and Dynamic range is >96 db.

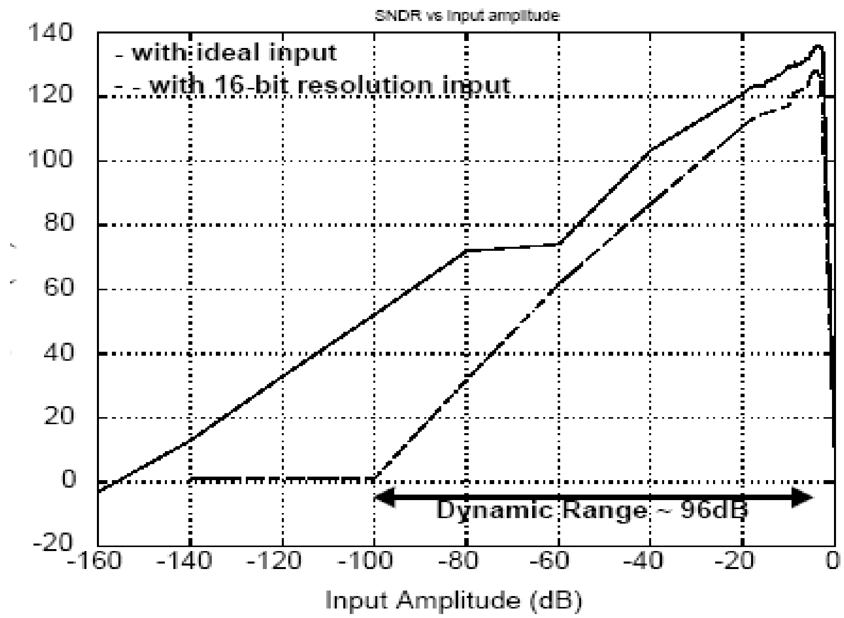


Figure 45: MATLAB Simulation of 3rd order filter

4.2.1 Class-D output -Stage

Typically Class-D amplifiers are amplifiers that involve modulation. Typical properties of Class-D amplifiers:

- they incorporate only two voltage levels, typically in both supply lines.
- since the devices are switched fully on, only devices with a very low on-resistance are used: MOSFETs
- since the ‘average’ signal must still be at least 20 kHz, the amplifiers run on high frequencies. 300 kHz is a common trade-off between accuracy and device losses due to gate capacitances
- Hence, an output filter can not be omitted.
- Power outputs vary between 1W and 1kW

- Efficiency is at least 78%, depending on power output. Due to the switching, either the device is fully off (I=0) or fully on (V=0), in any case the dissipated power in the device P=V*I is nearly zero.
- class-D amplifiers are found mainly in low-power applications.

Based on the above characteristic of Class-D amplifier; in our design digital audio amplifier uses Class-D at the out put stage. In the proposal of the Class- D output stage, the output switch which is illustrated in figure 19 is implemented using full bridge-tied-load (BTL) differential-drive configuration, as shown in figure 20. This BTL configuration or H-bridge effectively doubles the voltage across the load which normally is the speaker. Furthermore in a low voltage application CMOS transistor can be used instead of convectional DMOS devices. The discontinues mode of operation of a class-D output stage results in a theoretical power efficiency of 100% when an ideal switching characteristic is assumed. In practice however, the combination of switching and conduction losses sets an upper bound of the amplifiers power efficiency.

In a CMOS inverter the main power dissipation mechanism are due to:

- The charging and the discharging of the load capacitance:

  $$P_c = f_c C_L V_{DD}{}^2$$

  where f_c is the average switching frequency and

  C_L represents the total load capacitance

- The short circuit current when the NMOS and PMOS devices are simultaneously are on during the input signal transistors

  $$P_s = I_{mean} V_{DD}$$

  Where I_{mean} is the mean value of the short-circuit current

- The on- resistance of the transistor

  $$P_r = \frac{I}{T}\int_0^T i_L(t)^2 R_{ON}\, dt$$

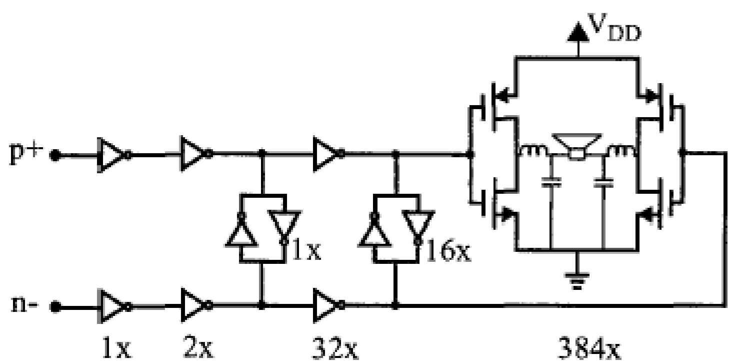
  Where $i_L(t)$ is the instantaneous load current and

  R_{ON} is the resistance of the transistors.

The static power dissipation P_r due to the transistor on resistance is ignored in digital circuit analysis because of the load impedance of this circuit is mainly capacitive. How ever the load of the out put inventers in an audio is considerably small (typically 4 to 36Ω). Therefore the static power dissipation become s the dominant factor of in limiting the overall power efficiency. The dynamic power efficiency is the total $P_c + P_s$

According to the size of the transistors in the output switching stage is determined by the required on resistance to meet the power efficiency specification. For efficiencies in the order of 80% the W/L ratio these output transistors must be very large.

Due the large width of the out put transistors, a fully differential multiple stage buffer architecture was designed to drive the H-bridge. When designing such output stage circuit , it is critical to ensure that the signals in each branch of differential path have equal rise and fall times and, hence, reach the switching threshold-voltage of the invertors $V_M = V_{DD} / 2$; as exactly the same instant. This guarantees that, when one side of the H- bridge is pulling high, the other side is pulling low and vise versa. If this condition is not properly met, both sides of the H-bridge is pulling in the same direction during part of the switching transition (small rise fall times) is described as it helps reducing the short circuit power dissipation of the inverter In order to meet the requirement described above and to minimize distortion, weak cross-couple inverters (well-matched devices) are inserted between the two differential lines of the output stages shown in figure 46.



Unit size Inverter dimensions

W_p	13 μ_m
W_n	5 μ_m

Figure 46: Class-D output-stage circuit

In order to minimize distortion the feed-forward provided by the cross-coupled invertors helps minimizing the signal skew. Simulation shows that the differential signals are well matched by crossing each other at switching threshold Vm and having a rise/fall time of less than 1ns. (Corresponds to the fast switching time)

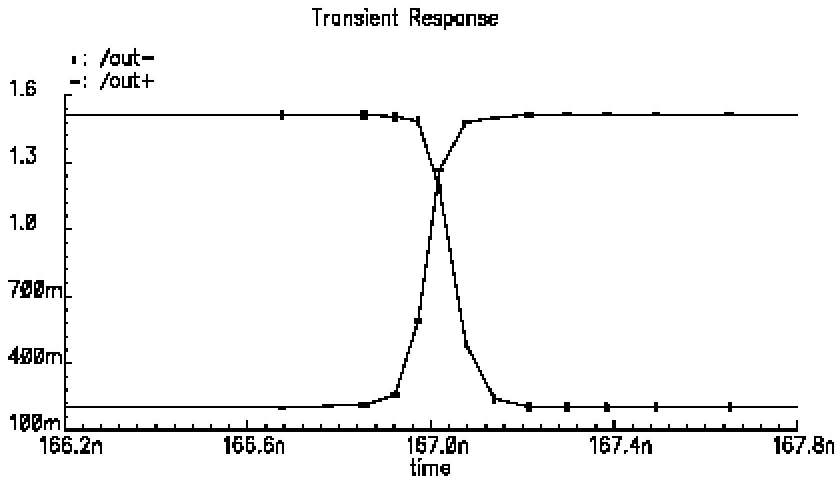
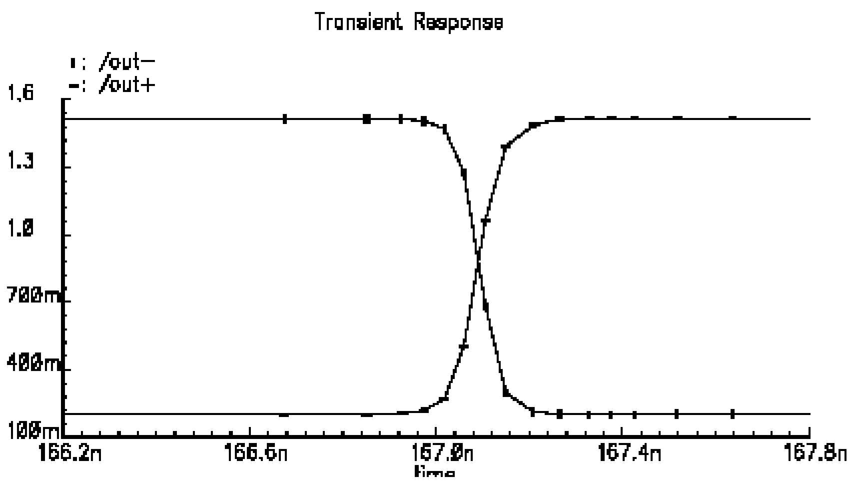


Figure 47: Matching effect due to addition of cross coupled inverter



The final design of the output stage is presented in figure 44. A balanced LC-type differential LPF is connected between the H-bridge output and the load (speaker).

4.3 Simulation Results

The following table indicates that the simulation with varying of different impedance in the load with 1.8 supply voltage can be seen as summary result in table 3.

Load impedance	4.3 Ω	8.2 Ω	36 Ω
THD	0.07%	0.07%	0.07%
SNR	74db	77dB	71dB
Power into load (max)	350mW	200mW	80mW
Efficiency	76%	66%	79%

Table 5: Simulation result

:

Part 5: Conclusions and final remarks

This part contains the conclusions that have been drawn during the thesis work and how the work can be continued. In particular, there are certain aspects of the analysis that need to be further analyzed, the implementation needs to be refined and the testing activity needs to be concluded. Furthermore, this parts includes references, have taken that deepen certain aspects of the thesis.

:

5 Conclusions and final remarks

This chapter points out the achieved results and the conclusions that have been drawn at the end of this master thesis project. Furthermore it provides some guidelines for what can be done further to complete, deepen, and enrich what has been described throughout this report.

5.1 Summary

- This master of thesis presents the design and simulation results of a digital audio amplifier in a 0.18-μ m standard digital CMOS process. It demonstrates:
- The feasibility of implementing fast-switching Class-D amplifier for a low- voltage low-power application with high efficiency.
- The system is implemented with in minimum overhead and no analog mask options are required for the design.
- The use of direct $\Delta\Sigma$ modulation instead of the traditional PWM mapping scheme, enables high-quality audio with out the complexity of the hardware- intensive linearization algorithms.
- Simulating 1-V power supply voltage on this audio amplifier demonstrates enormous potential for of application includes low-power digital devices as wireless and portable electronics equipment such as cellular phones, handheld computers, personal digital assistances (PADs) earphones, etc.

5.2 Achieved results

This thesis is concerned with 3 main subjects: classification of audio amplifiers, test signals for measuring and predicting amplifier efficiency (chapter 1), an overview and analysis of existing amplifiers and their efficiency (chapter 2), an overview of design of digital amplifier (Chapter 3), and the analysis and design of new amplifiers (chapter 4). We can be brief about the overview of high efficiency amplifiers given in chapter 2. It can serve as a reference for other people working in this field. Unfortunately, books about audio amplifiers are very rare, so chapter 2 is a good beginning.

The design of digital amplifiers has concentrated on new concepts. In this thesis the proposed $\Delta\Sigma$ modulator based digital class-D amplifier architecture, is function in the 3rd order topology with low operating voltage has been considered. As mentioned in the beginning of this thesis, the audio amplifier was one of the few remaining analogue components in the audio chain. The input of audio amplifiers was analogue. A digital input would simplify circuit design, as it eliminates the need for a separate D/A converter. Especially here the combination with class D amplifiers is advantageous, because, the digital audio signal was converted to analogue by a D/A converter, en then back to digital by the class D modulator. The strong point of this amplifier is the small output ripple. To keep this advantage for a digital input signal, strong filtering is unavoidable. Big advantage compared to class D is that this can happen in the small-signal domain. D amplifiers are usually specified by their maximum efficiency. This is not a real problem, as long as the quiescent dissipation is also specified. Because of the shrinking dimensions of IC-processes, the channel length of transistors decreases, and the amount of gm per parasitic capacitance increases. This is also favorable for power applications because it enables faster switching. Faster switching diminishes switching losses, creating possibilities for very high frequency class D amplifiers.

In this thesis work we also tried to see that both PWM and ΔΣ have their advantages and disadvantages in the usage for power amplification. PWM offers the lowest possible switching-frequency, but without proper linearization the audio base band will be distorted if applied to uniformly sampled data. The linearization methods based on interpolation and non-linear modeling require high computational power. The ΔΣ modulator is a more linear method, if the presence of idle patterns is reduced by dithering or by the use of chaotic modulators [13]. ΔΣ Produces a bit stream, where the pulses are distributed uniformly over the over sampling period. This causes high switching frequencies in the power-stage. The number of bit-transitions can be reduced by controlling or re-organizing the current bit-stream. The output would provide a possibility to control the distortions caused by these elements. This would ease the demand on the circuit design drastically.

5.3 Future work

Low Voltage low power is increasily important in modern CMOS process which leads to continuselay decreasing supply voltage. Therefore we propose the further study and the implementation of the ΔΣ modulator for digital amplifier to focus on the low voltage and details. The next generation ADCs will be expected to work under lower voltage and power, and to provide higher resolution as well as larger conversion bandwidth. Here we have focused the studies on the implementation of digital Amplifier for portable application; the future work can be for a vast range of applications like instrument measurement, wireless transceiver, medical care solutions, military applications, and environment monitoring. The future research will can also focus on ultra-low voltage Sigma Delta ADC using low/zero- VT process. Switched-Capacitor circuit is the most robust structure to realize a Sigma Delta ADC. However SC circuit faces a severe design challenge when using an ultra low supply voltage. For example, when the supply voltage is lower than the sum of threshold voltages of PMOS and NMOS transistors, a complementary MOS switch will not function correctly.

Finally a continuation of this work can be proposed as one of the future work it is also important to note about the lay out of this digital amplifier which is also one of the targets.

Tables of figures

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