Fabrication, Characterization and Simulation of Graphene Field Effect Transistors operating at Microwave Frequencies

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Abstract

With the end of Si based Metal Oxide Semiconductor Field Effect Transistor scaling paradigm approaching fast as predicted by the Moore’s Law, and the technological advancements as well as human needs in many ways pushing for faster devices, graphene has emerged as a powerful alternative solution. This is so because of its very special properties like high charge carrier mobility, highly linear dispersion relation, high current carrying capacity and so on. However, since we have a finite resistance at Dirac point, the on/off ratio in graphene devices is sufficiently low, making graphene devices not so suitable for logical applications. At the same time, the 1/f noise, which is understood till now to originate from surface disorders like those observed in a two-dimensional electron gas system like graphene and is a major unwanted outcome in mesoscopic regime devices, reduces very much at high frequencies, making these devices good candidates for high frequency analogue applications. Motivated by these observations, this work explores fabrication and characterization of graphene field effect transistors operating at microwave frequencies, and compares a double gated device performance to a mono-gated device having the same geometry, dielectric layer thickness and gate length. A simple electrostatic finite element simulation model has also been developed to support our experimental observations by fitting simulated gate coupling capacitance values to the measured data. The model helps us in understanding the level of interface trap charge densities introduced into the device channel during fabrication, and the effect of quantum capacitance on device performance, and is in line with the experimental observations. Our results show that a double gated graphene FET has superior performance compared to a mono-gated FET.

Key words: Graphene field effect transistor, microwave frequencies, transit frequency, quantum capacitance.
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<tr>
<td>ALD</td>
<td>Atomic Layer Deposition</td>
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<td>AFM</td>
<td>Atomic Force Microscopy</td>
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<td>CVD</td>
<td>Chemical Vapour Deposition</td>
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<td>DUT</td>
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<td>GFET</td>
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<tr>
<td>MIBK</td>
<td>Methyl Iso-butyl Ketone</td>
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<td>MOSFET</td>
<td>Metal Oxide Semiconductor Field Effect Transistor</td>
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<td>NEMS</td>
<td>Nano-electromechanical Systems</td>
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<td>PMMA</td>
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<td>RF</td>
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Chapter 1. Introduction

This chapter discusses the basic properties of the recently discovered [1.1] and much explored electronic material called Graphene. We start with a general overview of the structure and associated properties of graphene as investigated by various researchers in the opening paragraphs and then would proceed to briefly outline some of the specific properties of this material in the later paragraphs. This is aimed at building some basic understanding of this material in the reader’s view, because this entire work revolves around the theoretical and experimental aspects of the graphene devices operating at high frequencies. These devices essentially utilize some of the basic properties of graphene described here, so that an initial outline of these properties would support the flow of this thesis report, as one reads through it.

1.1 Graphene & its properties

Graphene is a term coined to represent a highly ordered two-dimensional atomically thin sheet of Carbon atoms which has a fundamental shape of honeycomb lattice structure. This was conceptually very first realized as early as in the year 1947 by P. R. Vallace [1.2]. At each of the corners of each of these honeycomb unit cells stand six carbon atoms. These carbon atoms are bonded to each other through sp\(^2\) type of chemical bonding, as in a benzene ring, so that in the simplest way a mono-layer of graphene can be basically visualized as an ordered two dimensional sheet of hexagonal rings. Such a structure possesses many remarkable properties due to its unique physical make. Since graphene is a purely two dimensional material, one of the first implications of this is that it is atomically thin, and the thickness of a mono-layer may be only a few angstroms. This effective thickness may vary from point to point because ripples with no preferred orientations appear as stable states at all temperatures with long life times in mono-layer graphene [1.3]. However, contrary to one’s primary notion of it being a fragile thing, such a structure is highly stable and mechanically strong, mainly due to the reason that carbon-carbon sp\(^2\) covalent bonds are fairly stable, so a large sheet of carbon atoms made up of such a regularly ordered array of covalently bonded carbon atoms is really strong. Mechanical strength tests have shown that the Young’s modulus of graphene is about 1 TPa [1.4], which is even larger than many of the known materials like steel, aluminium and iron. The carbon-carbon bond length in mono layer graphene is about 1.42 Å [1.5].

Intrinsic mono layer graphene is very much different from any other known three dimensional material, and the charge carriers in such a system behave like a purely two dimensional electron gas. The energy-wave vector correlation (E-k) in the Brillouin Zone is also linear for intrinsic graphene near what is known as the Dirac point at low energies, which leads to zero effective mass of electrons and holes. Dirac point is the point where the energy bands; viz., the conduction and valance bands, merge at the six corners of the
Brillouin Zone in Graphene [1.6]. Figure (1.1) below shows the Dirac cones in Graphene in the k-space. [1.7]

![Image](image.png)

Figure 1.1: (a) The six Dirac cones in mono-layer intrinsic graphene. (b) the simple schematic showing E-k relationship map in k-space at each of these Dirac points.

This results into very high theoretical charge carrier mobility values in graphene, however, in practical applications, due to its interaction with other materials like gate dielectric and substrate as well as due to inevitable introduction of impurities due to device fabrication process and other reasons, this mobility value becomes limited. Even then, both calculated and measured values of charge carrier mobilities in graphene devices are orders of magnitude higher than its other conventional counterparts like Silicon Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). Graphene also has very high current carrying capacity, which makes it a good candidate for high power applications where required current densities are much more than those achieved with Silicon MOSFETs. However, due to a linear dispersion relation at the six Dirac cones of the hexagonal k-space map of an intrinsic graphene sheet and zero band gap, graphene FETs cannot be turned off as they show a certain minimum conductivity even at zero gate voltages. This limits their use in logical devices and circuits. At the same time, graphene FETs make a suitable candidate for further scaling down of FET devices as graphene is atomically thin. Graphene FETs also present a good option for high frequency devices as charge carrier conduction is much facilitated in graphene sheets due to low carrier effective mass, as already outlined above. One of the other reasons is also that these devices do not require high on-off ratios also.

In the light of the above facts, in the following sections of this chapter, we briefly highlight some of the useful aspects of mono-layer graphene system, which have formed the basis of our understanding its nature and developing our simulation model along with explaining the outcome of our experimental results, which are subjects of later chapters of this work.
1.2 Conductivity related behaviour of mono layer Graphene

The special physical and band structure of Graphene renders to it a very characteristic conductivity related behaviour also. Unlike most of the conducting materials like metal and semiconductors, graphene mono-layer has a point-to-point varying conductivity value, which also means that the charge carrier mobility values also change from one point to the other in these systems. As has now been confirmed by various experimental as well as theoretical works [1.8, 1.9], something called as charge puddles exist on the surface of graphene, which means that a mono-layer graphene as has been later modelled in the simulation part of this thesis also, can be roughly visualized as having a chess board type of structure. Alternate black and white squares in a chess board can be considered as alternately positioned positive and negative charge puddles. Due to these puddles, the conductivity behaviour of graphene system is also quite typical compared any other known charge carrier system. [1.10]

A spatially inhomogeneous screened Coulomb potential is caused in graphene mono layers due presence of charged impurities in the substrate materials. Such charged impurities are almost always there due to fabrication process steps and exposure to ambient environment. At low carrier densities, the mono-layer graphene sheet charge system breaks into puddles of electrons and holes [1.10]. Some researchers argue that the minimum conductivity level observed in graphene mono layer systems even at zero gate voltage is also an outcome of the presence of these charged impurities, because their presence results into large scale density inhomogeneities in the system. They believe that these inhomogeneities occur up to such an extent that the local 2D density fluctuations become higher than the average density at low carrier density levels. This highly localised density fluctuation thus forces the system to break into alternate electron and hole puddles, yielding a finite conductivity even at zero gate voltage, because these random charged impurity centers cause scattering of charge carriers. [1.11] In case of very high quality samples, wherein such random charged impurity centers may be not so strong, it is also suggested that some scattering also occurs due to presence of point defects, however, as we would see later in experimental section of this work, since our samples turned out to be highly doped, our simulation model does not account for a conductivity definition based on point defect based scattering.

1.3 Electric field effect in mono-layer Graphene

Electric field effect is defined in transistor devices where a vertical electrical field is generated by applying voltage on a gate sitting underneath or on top of a semiconducting channel formed between the source and gate ends of the transistor device. The fundamental concept behind this effect is that application of a gate voltage results into a shift in Fermi level of the channel, which results into the modulation of current flowing through the channel. In all cases, both electrons and holes act as charge carriers in FETs. In graphene FETs (GFETs), ambipolar electric field effect is observed. [1.1] In an uncharged and
unbiased free graphene sheet, charge carriers do not experience any external force, and so they are free to move in all possible random directions, which results into a net zero current. However, upon application of a voltage difference between source and drain ends, where the gate is positioned on top or bottom of the graphene sheet which in turn, acts as the channel material in GFETs, the charge carriers experience a drive from drain to source resulting into a non-zero channel current. When the gate voltage is applied, these charge carriers experience an additional driving force due to the electric field created by the gate voltage. This electric field causes Fermi energy shift in the graphene channel, and thus ‘modulates’ the net charge carrier movement; i.e., current through the channel. This explains the basic principle behind the graphene field effect devices.

1.4 High frequency measurements on Graphene FETs

Since mono-layer intrinsic graphene does not possess a band gap, its applications in logical circuits and device applications are not that beneficial. However, due to high carrier mobilities and fast switching possibilities, RF applications of GFETs look promising. Of late, great interest is being shown by the graphene community in RF analogue application of GFETs. Such high frequency GFETs require device characterization to be carried out at operating frequencies, which may range between several mega hertz to many giga-hertz. In our case, we have measured the devices between 10 MHz to 40 GHz using a measurement instrument called as two-port Vector Network Analyzer (VNA). VNAs are used to apply high frequency voltage signals to devices under test (DUT). The two ports of the VNA connect the network analysis system to the terminals of the DUT, as these ports are the calibrated media with contact probes at their ends, which connect the DUT to the measurement circuit. A two port VNA measurement system characterizes a DUT at high frequencies by applying a signal to its source-drain as well as the gate ends, and simultaneously measuring and recording the measured information in the form of S-parameters. S-parameters represent the abbreviation of scattering parameters, which basically measure what portion of a signal applied on to a port gets reflected back and how much of it gets actually transmitted across to the other side, through the device. Clearly, the sum total of both the transmitted and reflected signals in such a case would then be one, because these are the only two components of the overall applied signal. Loss of signal strength in modern set ups is very low, so it may be considered negligible in most of the cases for practical purposes, however, depending upon the experimental conditions, it may be non-negligible also in some cases.

S-parameter matrix measurements can be of one port, two port or even three port types. The S-parameter matrix in an N-port measurement scheme contains $N^2$ elements. In case of two-port S-parameter measurements therefore, these parameters are of four types, namely $S_{11}$, $S_{12}$, $S_{21}$ and $S_{22}$, which form the $2 \times 2 = 4$ elements of the parametric matrix. It is indeed a matrix calculation because high frequency signals are AC signals and therefore these parametric measurements represent the measurement of a vector network, where
both real and imaginary parts of the parameters represent different quantities being measured. Some of these quantities are various types of intrinsic capacitances, RF transconductance and output transconductance values at different frequencies and intrinsic impedance and so on.

S11 represents the ratio of reflected signal to the applied on port-1 and is basically the reaction of port-1 towards the signal applied on itself. Likewise, S22 represents the ratio of reflected to applied signal at port-2 and quantifies the reaction of port-2 to itself. S12 represents the reaction of a signal applied at port-2 and measured at port-1. S21 represents similarly, the signal applied at port-1 and passing through port-2 \[1.12\][1.13]. Generally, S-parameters can be classified as large signal S-parameters and small signal S-parameters. In case of small signal S-parameters, the applied signals have only linear effects on the network. In this work, we are concerned with small signal S-parameters only.

1.5 Quantum Capacitance in Graphene FETs

Here we discuss some basic concepts about quantum capacitance in graphene FETs, a more detailed theoretical investigation and discussion on the same will follow in the later chapter on Modeling & Simulation, where we study our own devices in this perspective. Quantum capacitance is an important parameter in the electrostatic design of FET devices. Quantum capacitance in GFETs can be compared to the inversion layer capacitances in Si MOSFETs. In a Si MOSFET, since the charge carrier density is exponentially dependent on potential in both the weak inversion as well as in the depletion regions, the inversion layer capacitance is hardly noticeable in Si MOSFETs because it is really small compared to other capacitive components; viz., depletion layer capacitance (C_D) and interface trap charge density related capacitance (C_{it}), whereas in the strong inversion region beyond threshold, its magnitude becomes comparatively much higher. So a prominent and comparable role is played by inversion layer capacitance, the analogue of GFET quantum capacitance, only in the narrow region of weak inversion where it is comparable in magnitude to C_D and C_{it} in Si MOSFETs. In GFETs, since there is no depletion layer formation, the only capacitance components available are geometrical capacitance (C_g, as also in any Si MOSFET), C_q and C_{it}. So, on a comparative scale, C_D in a Si MOSFET can be replaced by C_q in a GFET [1.14]. Therefore the equivalent circuit for a Si MOSFET and a GFET can be shown as shown in figure 1.2 below.
Quantum capacitance thus plays an important role in the overall GFET performance compared to a Si MOSFET, especially in the cases where the dielectric layer around the mono-layer graphene channel is very thin. One reason for this importance being assigned to quantum capacitance in the case of GFETs is that in a graphene layer, the charge carriers are almost always degenerate, although not at and close to the Dirac point, the point of minimum conductivity. This is not true for Si substrate based MOSFET devices. [1.15] So unlike Silicon MOSFETs, quantum capacitance is an effective electrostatic design parameter in case of GFETs. In later section of this work therefore, we will seek to develop a numerical simplification of the mathematical expression for quantum capacitance in GFETs under certain simple assumptions, and arrive at the gate voltage dependence of quantum capacitance. Later, as the simulation results would be discussed, such a gate dependent quantum capacitance turns out to be a major component of the overall gate coupling capacitance in doubly gated GFETs. Also, our simulation results would highlight how quantification of various components of gate coupling capacitance could throw light on how ‘clean’ or ‘dirty’ such a doubly gated structure is, and an approximate indication towards the range of values in which the Fermi velocity of electrons in device channel may fall.

Having outlined and discussed some of the fundamental concepts and aspects of Graphene related technology in this introductory chapter, we now proceed to discuss the experimental and simulation part of our work in the coming chapters.


Chapter 2. Experimental Setup & Techniques

This chapter aims to describe the various experimental aspects of this work. First, we begin by defining the goal of the experiment. We then describe our experimental set up and outline the measurement instruments as well as the circuit scheme deployed to carry out the measurements. The fabrication of samples is also described, followed by a brief comment on measurement techniques.

2.1 Goal of the Experiment

The goal of this experiment is to study and compare the performance of mono-gated and double-gated graphene field effect devices (GFETs) operating at microwave frequencies. This includes the following steps of study.

One part of this overall work includes the development of a finite element simulation model to study the role of quantum capacitance and interface trap density based capacitances in the devices that we fabricated as part of this experiment. This model and its outcomes are discussed in the chapter on Modeling and Simulations.

The operating band of frequencies for this experiment’s purpose was chosen as between 10 MHz and 40 GHz. This was chosen to be so because of the limitations imposed by the corresponding measurement instrument; i.e., the Vector Network Analyzer (Rhode & Schwarz ZVA40), which was used to send microwave pulses down to the device level. Since the frequency range of the ZVA40 stretches between 10 MHz to 40 GHz, we used this frequency band in our experiments. The details of the principle behind these measurements and the corresponding set up are discussed in a later section called Measurement Techniques. To support the experiments and to develop a better understanding of the device behaviour and influences of these capacitances, a simple electrostatic finite element model was also developed using a commercially available finite element simulation package COMSOL Multiphysics 4.3a. The developed simulation model is based on a number of simple theoretical assumptions and attempts to calculate the total gate coupling capacitance in case of both a single (back) gated GFET device as well as a double (back and top) gated GFET device. It is worth mentioning at this very start of this chapter that all the devices fabricated and measured for the purpose this experiment were fabricated on sapphire, an insulating substrate, in order to avoid any unintended back gating effect in any of these devices. This also helps us in preventing the introduction of unwanted charged impurities from the substrate end into the mono-layer graphene channel, which cause localized screened coulomb potential fields, which are the cause of charge puddle formations in graphene as well as distortion of effective charge carrier mobilities. The fabricated samples were then measured using a simple circuit, which can be used in both DC as well as high frequency measurements & characterization of GFETs. This simple circuit is described in later sections along with the measurement instruments used therein. As the later sections of this report would discuss, the simulated data is then fitted to the experimentally measured gate
capacitance data extracted from the S-parameter measurements for each of back gated as well as double gated device cases. As the parameters are tuned to fit the simulated data to the experimental data, a number of effects are revealed to us about the nature of the fabricated device; viz., how clean the fabricated device was, how quantum and interface trap density based capacitances vary when we go from mono-gated device to a double-gated device with all other dimensions remaining the same, how the oxide layer thickness (i.e., the dielectric thickness) affects the overall capacitance and thus the device behaviour, and so on. Finally, based on these results and their conclusions, development of a future work outlook has been attempted.

2.2 Fabrication of Samples

Mainly in our group, two kinds of mono-layer graphene samples were fabricated, one wherein scotch tape based mechanically exfoliated graphene flakes were used, and the other where chemical vapour deposition (CVD) grown graphene sheets were used. In this experiment, the samples were fabricated using CVD graphene flakes, which were not grown by us. The CVD graphene was obtained ready made from external sources. However, in some of the other experiments conducted in the group, samples were also fabricated and measured in similar manner using the same high frequency. One of these devices tagged as SP68 (indicating sample no. 68) was measured for cumulative gate capacitance versus gate voltage fitting data against the simulations developed as part of this work. This was a 200 nm double gated device, and is discussed accordingly in terms of its geometry and materials used for fabrication in the chapter on Simulations in the later part of this thesis.

The device samples fabricated using CVD graphene sheet, around which this thesis work is centered, was tagged as SP71, and consisted of an array of 14x10 active as well as passive (dummy) structures of various types. The CVD grown graphene sheet used for this purpose was obtained readymade to purpose by our group from the Flexible Electronics Laboratory, Suwon, Korea, who have reported various developments in growing sufficiently large and uniform CVD graphene sheets [2.1, 2.2, 2.3]. All the structures were defined in the coplanar waveguide layout. Out of these 140 device structures fabricated on this chip, two starting columns of 10 devices on the left consist of opens and two ending columns of 10 devices on the right consist of short structures. These structures are together called as “dummy” or “passive” structures and have been used to de-embed the measured raw data. The remaining 10x10 array of structures in the middle consists of active devices, which were proper graphene field effect transistors (GFETs), of different gate lengths and channel types, in some cases. A sample map with nomenclatures is shown in figure (2.1). The device gate lengths varied between 100, 200, 500 and 1000 nm. However, due to time constraints, not all of these devices could be measured in the course of this work, and hence only two of these devices, which were completely measured to purpose have been reported here as part of this thesis. One of these devices was a back gated device labelled as SP71KD whereas the other device was a double gated device labelled as SP71KK. As part of this thesis work,
both these devices were completely and systematically measured around the points of maximum high frequency performance possibility in the microwave frequency band and results were analyzed. These results are reported in the last chapter of this work.

Figure 2.1: Sample map of SP71. The two columns of open structures are on the left most side of the chip, whereas two columns of shorts were defined on the right most side of the chip.

Prior to sample fabrication, and after graphene transfer on to the device array chip, a Raman spectra study was carried out to confirm the presence of mono-layer graphene. As can be seen below in figure (2.2), the presence of clear G and 2D in the Raman spectra taken over one the fabricated device structures (SP71 KG 500 nm double gate) after graphene transfer, peaks proves that the CVD graphene sheet was successfully transferred using a poly-methyl-methacrylate (PMMA) positive resist based transfer method. As a confirmation to the Raman spectra theory on graphene mono-layers, a smaller sharp peak around 1600 and a higher sharp peak near 2700 on the x-axis of the spectra plot confirms the presence of mono-layer graphene.

Figure 2.2: Raman spectrum taken around one of the devices SP71-KG (500 nm) to verify if the CVD graphene applied to channel was mono-layer or not. As can be clearly seen, the G and 2D peaks confirm the presence of mono-layer graphene.
The sample for this work, SP71, as mentioned above, was fabricated on insulating sapphire substrate. A sapphire chip with pre-defined markers was taken for this purpose. The markers are small cross structures placed at regular intervals for forming a reference plane, with respect to which further device fabrication steps like alignment of e-beam during e-beam lithography steps and definition of masks for various fabrication steps can be carried out. These crosses, called markers, can be defined using e-beam lithography itself, however, in this work, sapphire chip with pre-patterned markers was taken to start with. On this chip, back gates were patterned using spin coating a positive resist (PMMA, 200 nm thick) on to the substrate wafer and exposing it to e-beam in a Raith Eline e-beam lithography tool. This exposed layer was then developed in Methyl Iso-Butyl Ketone (MIBK) for approximately 15 seconds, followed by rinsing the wafer further into Iso-propanol. The wafer is then blown dry using a pressurized Nitrogen gun. This leaves only the hardened PMMA layer in the defined shape of the gate with a cavity of required gate and contact pad shape and dimensions, as decided while carrying out e-beam exposure of the PMMA. Sometimes, the rinsing of the exposed PMMA layer may be further extended by 5 or 10 more seconds, depending upon the need, as sometimes, PMMA does not get readily dissolved and may take a bit longer exposure to MIBK. Further to this step, back gate metal deposition was carried out in low pressure (vacuum) metal evaporator IONIVAC with the gate stack consisting of Cr adhesion layer+ Au contact layer (~40 nm thickness all in all). A lift off in acetone, followed by a brief sonication completes the back gate formation step. Further to this, the dielectric layer mask definition was carried out using Raith Eline e-beam lithography system, and a 2 nm thick Al seeding layer was deposited using Cambridge Nanotech Inc Atomic Layer Deposition (ALD) system. This 2 nm Al seeding layer was then exposed to ambient air to initiate oxide formation, which resulted into a total of 7 nm of Al2O3 dielectric layer deposition. The thickness measurement was carried out using an atomic force micrograph taken on Bruker dimension icon ScanAsyst Atomic Force Microscopy (AFM) instrument. Au/Pd contacts were also deposited through the same process flow used above to deposit the back gate stack. Palladium (Pd) was used as it is reported in a recent report [2.4] that using Pd in contacts shows sufficient reduction in contact resistance values.

Further to this step, mono-layer CVD graphene transfer was carried on to the chip to form the channel. For this step, wet transfer of graphene sheet was carried out. For this step, a pre-fabricated CVD graphene-on-Silicon available in the lab was utilized (we didn't grow CVD graphene for this experiment). Transfer of graphene mono-layer from the Si wafer to the device chip was carried out as follows. First, an appropriate size (approximately 1 cmx1cm area) of the Si wafer containing graphene was diced using a diamond dicing tool. A 800 nm thick PMMA layer was spun on top of this area and was baked in an electrical oven at 168 C for almost 30 minutes to harden the PMMA. Further, this silicon wafer piece was put into a shallow petri-dish, and water was poured into it very carefully and at a very slow rate, so that it eventually surrounds this Si-CVD graphene-PMMA chip all around, and adding any
further water to the petri-dish leads would lead to water interacting with PMMA-on-graphene layer. At this stage, a very little bit of water is again added carefully, and the petri-dish is left untouched for almost half an hour to one hour’s time to allow the water to seep in between the Si wafer-piece and the PMMA on graphene thin layer. One can observe that after this time, the graphene sticks more to PMMA than to Si surface, because after this seeping-in period, graphene on PMMA is seen floating in the water and is clearly separated from Si wafer surface. We then added a bit more of water, so that there is sufficient separation between the floating graphene on PMMA sheet and the Si wafer piece. The Si wafer piece is then pulled out of the petri-dish carefully without touching the floating graphene on PMMA sheet, and a metallic graphene transfer plate with a sufficiently sized centre hole in it is transferred underneath the floating sheet using a tweezer. A syringe is now carefully used to suck out the water, simultaneously carefully positioning the graphene on PMMA floating sheet with respect to the metallic transfer plate in a way that eventually when all the water is sucked out of the petri-dish, the graphene on PMMA sheet is positioned on to the transfer plate on the hole. This process has to be carried out very carefully, because the graphene sheet lies between the PMMA layer and the transfer plate, and even a slight carelessness may lead to damage to the graphene sheet. After the graphene sheet has been successfully transferred onto the transfer plate, the transfer plate is left to dry out a bit. The sample (chip with the fabricated devices & ALD layer) is now kept under the microscope of a graphene transfer setup shown in figure (2.3) on a hot plate which is electrically heated up to 165 C. This helps in driving out any stray water molecules.
(moisture) present on the surface of the ALD deposited Al₂O₃ [refer the graphene transfer setup figure]. The transfer plate is now inverted and fixed to the transfer fixtures and screws are tightened. In this position, the transfer plate and hence, the graphene on PMMA sheet can not move. The heated sample is now drawn closer to the inverted transfer plate slowly using a screw, through which the hot plate stage can be moved up & down. When the PMMA layer comes in contact with the sample surface we allow it to stay there for a few minutes, so that by heat transfer, PMMA slowly melts away while a carefully kept very small distance between the sample & the transfer plate allows any possible air bubbles to expand and escape, resulting into clear merger of the two surfaces. Also, due to this heat transfer, the thin water layer between the graphene layer & the transfer plate also evaporates, allowing them to separate easily. We now turn off the power supply to the hot plate, allow it to cool down and take the sample off the plate using a tweezer. It is then put into a beaker containing small amount of acetone, enough to completely drown the sample, to remove any remaining traces of PMMA, completing the CVD graphene transfer to the device chip.

After this step, PMMA is again spun on top of this transferred graphene (200 nm thickness) and e-beam lithography is used to define a mask pattern for reactive ion etching (RIE) of graphene in the required patterns. Since graphene at this juncture covers the entire device chip area, whereas it is required finally to be only on top of the active device area; i.e., the channel as well as under the contacts, etching away the excess flake of graphene is required. The reactive ion etching scheme uses oxygen plasma to etch away the graphene. The RIE system used for this was Oxford PlasmaLab 80 Plus.

Next, top contacts are defined using e-beam lithography similar to the bottom contacts. A 40 nm Pd/Au contact layer was deposited in this case, as top contacts, the same way as was done for the bottom contacts described above. The top dielectric layer was deposited again using a similar 2 nm Al seeding layer followed by exposure to ambient air to deposit a 5 nm Al₂O₃ (total 7 nm thick top gate oxide layer). A lift off in acetone was used as a final step for attaining the final mono- (back-) gated device shown in figure (layout) above. PMMA masks used for all such cases were all 200 nm thick.

In case of double gated devices, the only extra step that was involved was another PMMA mask layer deposition followed by e-beam lithography used to define the top gate masks. Similar to the back gate deposition process described above, a 40 nm thick Pd/Au top gate metal deposition was carried out using the IONIVAC metal deposition system.

After final metal lift off step, when observed under the microscope, it was found that not all the devices had fared really well. Two such devices on the chip, namely SP71LC and SP71LH, are shown below in figure (2.4) after the final metal lift off step. As one can observe easily, in case of device LC, the PMMA lift off step using acetone did not go so well, and thus the top metal layers have got curled up. These devices may show not that good contact behaviour, and even the gate dependence behaviour may also be hampered, although this needs to be investigated practically.
Figure 2.4: SP71LC (left) and SP71LH(right) after final lift off. As can be observed, the top metal layer in case of LC has got curled up, whereas LH has come out clean.

2.3 Experimental Set up

By experimental set up, we mean the basic circuit as well as its various components utilized to carry out the electrical characterization of the fabricated sample devices. By components of the circuit we mean the measurement and actuation instruments, such as the voltage sources, vector network analyzer, volt-ampere meters (Agilent 34410A) and so on. A schematic of the measurement circuit in general is shown below in figure (2.5). The simple circuit scheme used here to characterize the GFETs at high frequencies is shown as under in figure (2.6).

Figure 2.5: Simple schematic showing the measurement circuit used in this work. The 100 k-Ohm resistor attached to the gate end is in series.
Figure 2.6: Simple schematic of measurement set up used for high frequency characterization of our devices.

The figure above shows how the sample is connected to the vector network analyzer (VNA) ports which can be used to apply microwave frequency signals on to the sample. In our case, we employed a two-port VNA. Each of the ports sends out a signal through the sample (GFET device) and measures the reflected as well as transmitted components of the signal. For this, two three-pin probes are utilized to connect the VNA to the device end. The centre-pin is the signal carrying “live” pin of the probe, whereas the remaining two side-pins are the “ground” pins. One of the probe connects to the gate end of the GFET, whereas the other connects to the drain-source ends of the device, as shown in above schematic. These probes are also connected simultaneously to the measurement instruments as shown in figure (2.5) above. Basically, we have two voltage sources, one for supplying the gate voltage and one for supplying the source-drain potential. Each of these were Yokogawa GS210 in this case, which can be connected to the computer through a GPIB communication bus, so that desired applied voltages could be applied at these ends by sending a command from the computer. These voltage sources are also in communication with the VNA through GPIB interface. Further, there are two volt-ampere meters also employed as shown in figure (2.5) above to act as measurement instruments. One of these measures the actual gate voltage on the device gate, whereas the other is used to measure the source-drain current flowing through the device. These VAMs are also in GPIB communication with the CPU of the computer (which is used to send the commands) through the VNA. A 100 k-Ω resistor is connected in series to the gate of the device to avoid any high currents to flow through the gate, which may damage the device permanently. Note that as shown in figure (2.6), each of the probes connect the VNA to the sample via a bias-T, which is a three port network.
element used to set the DC bias point of operation. Thus by using a bias-T, the connected device is able to see both the bias as well as the RF input.

Figure (2.7) below shows the laboratory set up, which was actually utilized in characterizing the fabricated GFET devices.

Figure 2.7: The probe station setup used for characterizing the fabricated samples. The top two devices with live display are VAMs for showing measured gate voltage as well as source-drain currents respectively. The two devices with live display in the middle are the gate voltage source (bottom) and source-drain voltage source (top). The foreground shows the optical microscope integrated probe station setup, with the 40 GHz VNA in the background.
Figure 2.8: the probe station setup for microwave frequency sample measurements. The sample (DUT) is mounted on the horizontal X-Y stage and the two 3-pin probes shown on right and left are used to connect it to the microwave frequency source. These probes are connected to individual bias Ts.

Figure (2.8) above shows the zoom-in of the probe station workpiece table, where the sample is mounted. The optical microscope mounted just above the sample table helps us in aligning the probe tips correctly with the contact pads of the device so that smooth and damage-less contact between the DUT and the probe tips could be established. The probe

Figure 2.9: Rhode & Schwarz ZVA40 Vector Network Analyzer with attached probes.
tips are themselves connected to the ends of a x-y movement ratchet, which enables us to move the probes in x, y and z all possible axial directions. The workpiece table is also mounted on a x-y stage which can be used for moving and positioning of the sample. This entire setup (workpiece table+probe tips) are together mounted on a damping stage, which helps us in keeping the device free of any external mechanical disturbances, such as any stray vibrations or noise. This makes sure that the contacts between the probes and the device are always stable. Likewise, figure (2.9) shows the VNA with the two attached probes.

2.4 Measurement Techniques

The measurement techniques for these GFETs are mainly of two types. DC measurements were carried out to characterize the device, giving us information on how much maximum current it could carry as well as the position of the Dirac point. Basically, DC measurements show how the device responds towards changes in gate voltages for a fixed bias as well as the changes in bias voltages for a fixed gate voltage. Since the plots of these response curves show the intrinsic device behaviour, these plots are referred to as device characteristics. The former one is referred to as transfer characteristic ($I_{ds}$-$V_{gs}$ plots) whereas the latter is called as output characteristics ($I_{ds}$-$V_{ds}$ plots).

Further to this, microwave frequency measurements were made to determine the transit frequency of the fabricated devices, and to evaluate net gate coupling capacitance, RF transconductance, RF output conductance and stray contact pad capacitance values, giving out a total map of the device in terms of its intrinsic characteristics. For this, de-embedding procedure was also carried out by using dummy (open and short) structures fabricated along with the device on the same chip, having the same gate lengths and device layouts, as shown in figure (2.1) above. Microwave measurements essentially mean two port S-parameter measurements in the context of this work. However, one-port and more complex three-port S-parameter measurements are also possible.
Chapter 3. Modeling & Simulation

3.1 The Finite Element Simulation method

The finite element method is a mathematical method used by scientists and engineers popularly to solve boundary value problems of various kinds; e.g., transient heat transfer problem, mechanical and thermal loads occurring dynamically while grinding a work piece, flow of fluids through pipes of varying geometries and so on. The solutions evolved using these methods are approximate solutions. This method proceeds by dividing the concerned domain in a large number of infinitesimally small units consisting of multiple nodes or nodal points (as it is called) as its corner points. This process of subdivision of domain is called meshing. Multiple domain problems can also be handled the same way, and mesh types may be same or different for each of the domains involved in the problem. This method has the Calculus of Variations at its roots wherein it uses the technique of minimization of an error function to produce a stable solution at all the nodal points mentioned above. This method therefore, basically utilises the fundamental idea that any macro-level body can always be subdivided into a large number of small, finite elements, which can then be solved for simple elemental equations to solve the larger system level boundary problem. These equations approach to a solution by considering the boundary conditions at each of the nodal points of these finite elements, and by minimizing the corresponding error function, try to merge the solutions into a common direction, which is referred to as the convergence of a boundary value solution. When the boundary conditions at two or more nodes are not coherent, meaning that the error function cannot be minimized at these nodes in more than one cases of basic mesh units, the solution does not converge, and the simulation as such is said have failed to converge.

Many commercial softwares are available these days in the market, which simulate various processes in one, two and three dimensions. Some of these packages also have provisions of including a time dimension for modeling of problems such as transient heat transfer. One such software, which provides modules not only for various physics domains like electrostatics, mechanics etc. but also provides a powerful tool option for multiphysics inter-domain and intra-domain solutions of such boundary value problems is COMSOL Multiphysics. This software has been used here to carry out the finite element method based simulation of a graphene field effect transistor (GFET) in two-dimensional geometry under certain simplifying assumptions. These assumptions will be discussed and outlined in further sections of this chapter.

3.2 Simulation geometry, settings & parameters

As outlined in the opening chapter of this work, quantum capacitance plays a major role in the operation of graphene FETs, and hence in electrostatic design of these devices, estimation of overall gate coupling capacitance as well as its components is of importance,
particularly at high frequencies. This is so because the transit frequency $f_T$ of a RF GFET is linearly proportional to its transconductance whereas is inversely proportional to the sum total of all capacitances. Thus, higher the net capacitance, lower the $f_T$. This is the reason why these capacitances are referred to as unwanted or parasitic capacitances, as they reduce the optimum performance of the device and restrict the current through the channel. However, as we would observe, in case of a double gated device compared to a mono-gated device, the total gate coupling capacitance is higher yet other stray capacitances like pad-gate capacitance and so on can be reduced by efficient design of GFETs, which may result into overall reduction in capacitances. At the same time, having two gates makes the gating more effective, effectively increasing the transconductance, so the overall result is a net increase in intrinsic transit frequency ($f_{T_{deem}}$). One of the popular and trusted practices in design of circuits and devices and many more such systems has been the finite element simulation of the DUT within a set of boundary conditions to analyze the behaviour of the device without encountering the need of both invasive and non-invasive testing methods. The main advantage of simulating a DUT is that it saves a lot of valuable laboratory time an material resources needed to fabricate and test the device. Moreover, even if one manages to overcome these difficulties, studying intrinsic device behaviour is still a difficult issue, which simulations help us overcome using a set of problem specific boundary conditions. These boundary conditions are based on some basic assumptions about the physics of the problem, and this reduces the overall complexity of a DUT to the level of a boundary value problem. This boundary value problem is then solved as described above in the opening paragraphs of this chapter.

For simulating our Graphene field effects transistors in this work, we used COMSOL Multiphysics finite element simulation package. A simple electrostatic two dimensional model was drawn in the graphical user interface of COMSOL for different single and double gated device geometries, the cross sectional layout details of which are shown below in Figures (3.1) and (3.2).

![Figure 3.1: Cross sectional geometry of a mono (back) gated GFET device as simulated in COMSOL.](image-url)
Three sets of simulations were carried out, a 200 nm gate length exfoliated graphene double gate FET (SP68), a 500 nm gate length CVD graphene double gated FET (SP71KK) and a 500 nm gate length CVD graphene mono-(back) gated FET (SP71KD). SP71KK and SP71KD were fabricated and characterized as part of this work, whereas SP68 data were adopted only for comparative study purposes. These simulations were targeted at studying the gate voltage dependent capacitive behaviour of these GFET devices in two different ways. One comparative study was targeted at the comparison of an exfoliated graphene device to a CVD graphene device, whereas the other part of this study was targeted at the comparison of a double gated GFET device to a mono-gated GFET device. One of the device geometries as drawn in the graphical user interface of COMSOL Multiphysics is shown in the figure (3.3) below. Note that conductivity, and therefore quantum capacitance is also temperature dependent quantities in graphene mono-layers, a fact which has not been considered in these simulations. [3.1] This is due to the reason that conductivity in graphene mono-layers is very poorly dependent on temperature for non-flat or suspended substrates. [reference]
In either case, the gate stack consisted of a chromium adhesion layer followed by a gold top layer. In case of SP68 (200 nm gate length FET), the gate stack consisted of 3 nm Cr layer followed by 20 nm gold layer deposited using metal evaporation. The dielectric layer was 7 nm thick Al$_2$O$_3$ top and bottom layer each, because while fabricating this device, the oxide layer growth was initiated by a 2 nm thick Al seeding layer deposited through atomic layer deposition (ALD) method, followed by exposure to ambient air resulting into a further growth of total aluminium oxide layer thickness up to 7 nm. The thickness was verified using an atomic force micrograph taken subsequent to each of the fabrication steps. This device was not fabricated and tested as part of this work; however its gate coupling capacitance versus gate voltage data was adopted for fitting with our model. The metallic contacts seen on the far ends of the device in the figure above have been put there to account for bias application condition from source/drain ends. Since the device was doubly clamped, this description of adopting a point of voltage application through a metal-graphene contact on both source and drain ends is justified. The assigned material in either of the metal contacts is chromium adhesion layer on gold.

The channel layer in all of the simulated GFETs was defined as a series of new materials defined in COMSOL, because Graphene as such is not defined in this simulation package. Each of these new materials was called “MLG #” where MLG stands for Mono Layer Graphene and the symbol # indicates the number (position) of the same in the series. Each of these MLGs was assigned with a particular and different electron mobility, electrical conductivity and charge carrier density. Each of these MLGs represents an individual charge puddle along the length of the graphene mono-layer which forms the device channel. The reason behind defining a mono-layer graphene sheet in this way is that since mono layer graphene is a purely two dimensional material, its cross sectional view would present us with a one-dimensional line of a series of charge puddles sitting next to each other. [3.2, 3.3, 3.4, 3.5] In our simulations, we adopted the same approach by defining each of these charge puddles as each of these “MLGs” in such a manner that positive and negative charge puddles (“MLGs” with positive and negative charge carrier densities) are placed alternatively next to each other. Since each of the charge puddles in a mono-layer graphene system may have a size of the order of roughly 20-50 nm as reported in the references cited here as well as elsewhere, in a few cases, citing the reason that charge puddles may vary in size within the same mono-layer graphene system, even the size of our MLGs was varied between 20, 25, 40 and 50 nm. After defining each of these charge puddles (MLGs) with similar yet separate, different material properties, they were all connected and merged as a single material, called graphene by forming a union of them all. This forms a series of p-n junctions, as is the case in real mono-layer graphene systems [3.4].

Since the electrical conductivity in graphene varies from point to point, and various models have been presented in this connection to derive a theoretical expression for the same, the
following conditional definition of minimum electrical conductivity in graphene mono-layer was chosen for our simulations [3.6]

\[
\sigma(n - n_{avg}) = \begin{cases} 
(20e^2/h) \times (n^*/n_{imp}) & \text{if} \quad n - n_{avg} < n^* \\
(20e^2/h) \times (n/n_{imp}) & \text{if} \quad n - n_{avg} > n^*
\end{cases}
\]

where the analytic expressions for \( n^* \) and \( n_{avg} \) are given by:

\[
n^*/n_{imp} = 2r_s^2 C_0^{RPA} (r_s, a = 4d \sqrt{|\mathcal{T}|n^*}) \quad \text{(equation (9), [3.6])}
\]

\[
n_{avg} = n_{imp}^2 / (4n^*)
\]

where, \( n^* \) gives residual carrier density in this self consistent theory of graphene sheet conductivity, \( n_{imp} \) gives impurity concentration at a given point where conductivity is being defined, \( \sigma \) is electrical conductivity as a function of the difference between charge carrier density \( n \) and average charge carrier density \( n_{avg} \). The expression for \( n^* \) has been derived here under the Random Phase Approximation (RPA) in low carrier density limit and details of its derivation can be referred to from this reference. Note that this model is valid for low charge carrier density case only and therefore, our simulation model also is valid only in the low carrier density limit only; i.e., near the Dirac point. In our simulations, a starting value of each parameter was adopted which are listed as follows:

- residual density = \( 7 \times 10^{11} \) /cm\(^2\)
- carrier density = \( 50 \times 10^{10} \) /cm\(^2\)
- impurity density = \( 1 \times 10^{12} \) /cm\(^2\)

These values have been adopted basis the model discussed in [3.6] where these values were adopted from some experimentally reported measurements. Note that we have modified the carrier density a little, as we redefine the model to fit with our experimental data. These values are also supported by data adopted for 2D carrier transport modeling by Hwang et. al. [3.7]

The electron mobility expression was also adopted from the same work for defining the linear tail mobility of charge carriers in graphene sheet as follows:

\[
\mu = \mu_0 \times (n_0/n_{imp})
\]

where \( \mu_0 = 1 \) m\(^2\)/V-s and \( n_0 = 10^{10} \) cm\(^2\) in the low carrier density regime as in [3.6]. We adopted the same expression for our modified carrier density with the assumption that it still remains valid. Each of the charge puddles of a certain dimension defined in the model as described above was assigned one particular randomly selected minimum electrical conductivity and electron mobility value along with a relative permittivity value individually. Note that all these conductivity values are dependent on the average charge carrier density.
and impurity density in each of these puddles, so basically, these quantities were changed from point to point in our simulation geometry material definitions to define the overall variable conductivity/variable mobility based graphene layer definition. The relative permittivity values for all the puddles were chosen to be 2.5, as defined for graphene in general. One example plot of conductivity along the graphene channel under this definition of point-to-point varying conductivity is shown below in figure (3.4). Note that this is just an illustration; therefore the positive puddles have the same conductivity levels whereas alternately placed negative puddles have been assigned varying impurity and charge carrier densities to vary their respective conductivities.

Figure 3.4: A sample plot showing point-to-point varying conductivity model implemented for graphene in our COMSOL model. Each of the peaks are centers of the alternately positioned positive (hole) and negative (electron) charge puddles, which have been defined along the length of the mono-layer graphene sheet.

Each of the peak points in figure (3.4) denote the center of alternately placed electron and hole puddles, and a gradual conductivity variation (slope of the line between any two peaks) denotes the possible leakage or transparency available to charge carriers across the p-n junctions thus formed. This transparency is necessary for realizing an overall “macroscopic” conductivity across the graphene sheet. [3.4]

In order to simulate overall gate coupling capacitance in any GFET device, the following simple electrical circuit model was adopted, shown in figure (3.5) below.

Figure 3.5: equivalent circuit model of a GFET adopted for simulation. $C_{ox}$ represents the capacitance component due to gate oxide layer and we have called it as geometric capacitance throughout our work,
whereas \( C_{it} \) represents the quantum of capacitance effects generated due to the interface trap charge densities present inside the device. \( C_q \) denotes the quantum capacitance, which is the property of a 2D Fermi system [3.8]

Under this model, since the quantum capacitance \( C_q \) is nothing but the response of the device channel with respect to the applied gate voltage, and the unavoidable interface trap charge based capacitance component \( C_{it} \) also adds this “channel response” or “reaction” of the device channel, therefore, \( C_q \) and \( C_{it} \) should be in parallel. On similar lines, since the oxide capacitance is basically the geometrical capacitance associated to the gate(s) and the channel, we would usually refer to it as \( C_g \), the geometrical gate capacitance associated with the GFET device.

The corresponding quantum capacitance was simulated using a few simplifications introduced to the commonly accepted expression for it [3.11], which is discussed as follows. The geometrical capacitance was taken as twice the parallel plate capacitance between the mono-layer graphene channel and one of the gates, because the gates are located equally apart on each side of the MLG channel, and this forms a system of two equal parallel plate capacitors connected in parallel.

The interface trap charge density related capacitance \( C_{it} \) was initially assumed fixed and its value was adopted as 5 \( \mu \)F/cm\(^2\) in accordance with one of the values assumed by Han et. al. [3.9]. However, since we could not ascertain how much was the exact value of \( C_{it} \), and hence, how much would be the resultant Fermi velocity of electrons \( v \) in the Graphene channel, we decided to keep these two parameters independent, and tune them while simulating the device for fitting against the measured device capacitance data. Upon fitting the measured device capacitance data with the simulated one, quantification of \( C_{it} \) and \( v \) would be possible.

The gate voltage dependent quantum capacitance was derived as follows, and supplied to the simulation program for evaluation & plotting:

\[
C_q = \left\{ -C_5 + \sqrt{(C_5)^2 + 8(q^3)(C_1)\frac{abs(Vg)}{(3.14\times10^{-7})^2}} \right\}^{1/2}
\]

where \( C_5 = C_1 + C_{it} \) = geometrical + interface trap density related capacitance. \( abs(Vg) \) denotes the absolute value of applied gate voltage, \( b = (\hbar/2\Pi) \), the reduced Planck’s constant, \( q = \) elementary electronic charge (1.6x10\(^{-19}\) Coulomb) and \( v = \) Fermi velocity of electrons in graphene, adopted to be theoretically 1.15x10\(^7\) m/s initially [3.10], but was later tuned to fit with the experimentally measured data set from the fabricated back gated and double gated CVD graphene devices as part of this work as well as the data adopted for the exfoliated Graphene device SP68, whose data was adopted partially in this work for cumulative gate coupling capacitance fitting with simulation model.

This expression for quantum capacitance was derived as follows. Cheremisin [3.10] has defined quantum capacitance in absence of a magnetic field as:

29
\[ C_q = \frac{(2e^2kT)}{(3.14 b^2v^2)} \ln\left[2(1 + \cos \left(\frac{qV_{ch}}{kT}\right)\right) \]

where \( V_{ch} \) = channel potential. In this simulation, we also assumed absence of any magnetic fields. Under the assumption \( qV_{ch} >> kT \) in this case of mono-layer graphene (Jena et. al., eq (15))[3.11], we can write this as:

\[
C_q = \frac{(q^2)}{(3.14)} \frac{V_{ch}}{(b^2v^2)} \]

\[
= \left(\frac{2q^3}{3.14 b^2 v^2}\right) C_1
\]

\[
\Rightarrow \{ C_q \ast (C_1 + C_t + C_l) \} = \left(\frac{2q^3}{3.14 b^2 v^2}\right) V_g \ast C_1
\]

\[
\Rightarrow C_q^2 + C_q \ast (C_1 + C_t) - \left(\frac{2q^3}{3.14 b^2 v^2}\right) V_g \ast C_1 = 0
\]

\[
\Rightarrow C_q = \frac{-[C_1+C_t]\pm\sqrt{[C_1+C_t]^2-8q^3V_gb^2v^2}}{2}
\]

Equations (a) and (b) are the same.

The assumption of zero magnetic field strength during the operation seems reasonable here because the strength of magnetic field component of the applied signal is very much less than of the order of 1 Tesla or so, for which case, the expression above can be safely adopted. For higher order magnetic field strengths, the initial expression for \( C_q \) changes, because at such high strengths, Landau Level splitting occurs and the physics of such event is different. [3.12]

### 3.3 Results and plots of simulated devices: fitting against measured data

After defining the graphene mono-layer as described above and the rest of the device geometry; viz., source and drain contacts, gate stack and dielectric layer geometries and corresponding materials, electrostatic AC simulation settings were defined. Voltages were swept around the Dirac point as indicated by the measured device data, with respect to which the simulated data was being fitted, whereas the AC signal frequencies were swept between 10 MHz and 40 GHz, as was done in case of real Vector Network Analyzer based high frequency S-parameter measurements as discussed in the relevant chapter already. Note that this model as well as our experimental data analysis was based on the small signal model of electrical circuits.

The simulated model data versus the measured device data was fitted with respect to varying the values of the interface trap density based capacitance \( C_t \) and the Fermi velocity of charge carriers \( v \) (electrons and holes were assumed similar in our simulations) for gate voltage values falling near the Dirac point for the device SP68 (200 nm double gated) is shown as under in figure (3.6). A Dirac point shift related voltage offset of 0.9 V was
introduced into the simulations to fit with the experimental data in this case, because this model does not include implementation and definition of Dirac point shift due to impurity doping in GFETs.

Figure 3.6: total gate coupling capacitance versus applied gate voltage for SP68. The blue circles denote experimentally measured data as against the blue crosses, which denote simulated data.

As one can observe, the experimentally obtained data has a difference in the slopes of its e- and h-branches, owing to the well known ambipolar nature of transport in graphene, which is also one of the factors not included in our simple electrostatic simulations. Therefore, the simulated data has both its e- and h-branches having the same slope, because it actually considers only one kind of charge carriers (say, electrons) being present in the device, causing conductivity effects.

Also, the minimum conductivity plateau observed at the Dirac point in the measured data set denotes sufficient effects of dopant impurities in the device, another effect which was not included in our simulations. However, since we account for the impurity densities in defining the conductivity, charge carrier mobilities and relative permittivity values from puddle to puddle in graphene sheet along with the charge carrier densities, which in turn determine the quantum and the nature of the response of the channel to an applied gate voltage, simulated data seem to emulate an ideal, electron-only, metal-contactless graphene sheet acting as channel in an ideal double gated GFET. Please note that this response of the device channel to the applied gate voltage is defined as the quantum capacitance, and therefore, quantum capacitance values are mainly determined by voltage in the channel, which in turn is determined by the applied gate voltage. The data fit quite closely, within ~1 fF, proving the expression derived earlier in this chapter, which was used to simulate quantum capacitance with respect to applied gate voltage in graphene sheet simulation model correct. The corresponding values of $C_{it}$ and Fermi velocity of electrons in
case of SP68 is approximately quantified as follows for this fit. At these values, the total gate coupling capacitance including gate voltage dependent quantum capacitance is plotted in figure (3.6) above.

\[
\begin{align*}
C_{it} &= 1.14 \times 10^{-6} \text{ F/cm}^2 \\
v &= 5.65 \times 10^6 \text{ m/s}
\end{align*}
\]

Please note that since \(C_{it}\) is an after effect of the interface trap charged densities present in the graphene sheet [3.9], it denotes the extent to which such impurity charge densities have been introduced into the device during its fabrication. Thus, a comparative simulation versus experimental data fit based study between two similar device geometries can thus be used to conclude which one is more ‘clean’ compared to the other, because the simulated data fitting approximately quantifies the order of magnitude of \(C_{it}\) present in the device and reflected in the measured gate capacitance data.

Another simulated device data fitted with respect to measured gate coupling capacitance for a 500 nm gate length double gated device (SP71 KK) is shown as under in figure (3.7). Note that this device was a CVD graphene device compared to SP68, which was an exfoliated graphene device. By CVD graphene device, we mean that the device channel consisted of a mono-layer of graphene which was grown using Chemical Vapour Deposition (CVD). As outlined in the previous chapter which discusses fabrication of samples, the CVD grown graphene sheet used for this purpose was obtained readymade to purpose by our group from the Flexible Electronics Laboratory, Suwon, Korea, who have reported various developments in growing sufficiently large and uniform CVD graphene sheets.[3.13, 3.14, 3.15]. By exfoliated graphene device we mean that the device channel consisted of a mechanically exfoliated mono-layer graphene sheet. In case of SP68, the dimensions of the exfoliated sheet were approximately 14x10 µm².

![Figure 3.7: total gate coupling capacitance versus applied gate voltage for SP71KK. The blue circles denote experimentally measured data as against the green crosses, which denote simulated data.](image-url)
As can be seen in the figure above for SP71KK double gated device data fit, the measured data differ from the simulated data in many ways; e.g., that real device has a much broader minimum conductivity plateau compared to the simulated ideal device, which has quite a sharp point of minima. Similarly, not just in comparison to the simulated ideal double gated GFET of the same geometry but also in comparison to the exfoliated graphene device SP68 shown in figure (3.6) above, one can clearly observe the enhanced difference in mobility values of the charge carriers in this CVD graphene device. However, SP68 and SP71KK cannot really be compared because although they’re similar in many ways, yet they’ve different gate lengths, type of graphene sheets used to fabricate the channel and levels of doping present in their respective graphene sheets, thus also in terms of the Dirac point voltage shift. Therefore, looking at the $C_{it}$ and Fermi velocity $v$ values obtained through simulated data fitting for SP71KK, the only way of comparing these two devices basis this simulation would be to say whether one of them is more ‘clean’ compared to other or otherwise. As our simulation model estimates, the contribution of interface trap charge density to gate coupling capacitance can be quantified at 1.14 µF/cm$^2$ for the exfoliated graphene channel device SP68, as compared to a $C_{it}$ value of 1.43 µF/cm$^2$ for SP71KK, which depicts that charge carriers should suffer lesser impurity collisions inside SP68 compared to SP71KK. As per the simulations, the Fermi velocity of charge carriers in this case for device KK was estimated to be $4.67 \times 10^6$ m/s, which is lower than the estimated Fermi velocity of charge carriers in case of the exfoliated device SP68. This would mean that average charge carrier mobility would also be higher in the exfoliated graphene channel compared to a CVD graphene channel, which is in line with experimental observations reported elsewhere. This proves that our basic approach to simulation is correct, and applies equally well to a CVD graphene FET.

![Figure 3.8: Simulated versus measured data fit for back gated device KD (500 nm gate length).](image-url)
Figure (3.8) above shows a similar gate coupling capacitance versus gate voltage variation data fit plot for another 500 nm CVD graphene GFET device SP71 KD. This device was fabricated on the same chip alongside with SP71 KK, and a comparative study of these two devices was carried out to investigate various device parameters and properties on their high frequency performances. The effects rendered by the overall gate coupling capacitance as well as its individual components are discussed later in chapter 4. As can be seen from the simulated versus measured data fit plot for device KD, no clear Dirac like point of minimum capacitance could be located from the measured capacitance values, because the level of n-type dopants in this device is large enough to degrade the e-branch to sufficiently low values, around $V_{gs} = 1V$ and onwards, the curves remains almost flat. Accordingly, simulated data were plotted by adopting a Dirac point voltage shift of 1V in figure 3.8. Note that since electrons and holes are modelled alike in our simulations, the simulated data also had an e-branch, which has not been shown here. This was done so to maintain the clarity in observing the close fit of measured to simulated data for the h-branch. For this close fit within ~1 fF, the corresponding $C_{it}$ and $v$ values obtained from simulations for the device SP71 KD are as follows.

\[
C_{it} = 4.78 \times 10^{-7} \text{ F/cm}^2
\]

\[
v = 1.29 \times 10^7 \text{ m/s}
\]

These simulated values indicate that the average charge carrier velocity in back gated device KD is more and interface trap charge densities are lesser, meaning that this device is ‘cleaner’ than the other double gated device KK on the same chip. One reason behind this could be that fabrication of a double gated device involves one extra step of top gate stack deposition, during which such impurities may possibly get introduced inside the device. The back gated device is protected by a resist mask in this step. The simulation process thus helps us in quantifying the intrinsic parasitic components with an accuracy reaching up to the order of magnitude of the real values reflected from measured capacitance data. This information may be useful in explaining other aspects of device behaviour and performance, as we would observe in the analysis and discussions sections of the next chapter.

Looking at the complete picture that emerges out of this simulated data result, one can clearly observe that the simulated value of the Fermi velocity of charge carriers in the device channel is in all cases a highly unrealistic figure, because as reported elsewhere [3.1,] by many other researchers, the maximum possible value of Fermi velocity cannot exceed $1.3 \times 10^6$ m/s and is often accepted to be around $((1.1 \times 10^6) \pm (0.1 \times 10^6))$ m/s [3.3]. View this, we modified the approach adopted in carrying out the simulations to account for this discrepancy by limiting the Fermi velocities within realistic limits. For this purpose, we incorporated Novoselov’s approach of varying Fermi velocities in a device channel [3.16]. Under this approach, the Fermi velocity is taken as a function of varying charge carrier densities across the device channel. The approach assumes an initial Fermi velocity value $v_{f0}$ and calculates its value based on Random Phase Approximation (RPA) theory based
variation of dielectric constant $\varepsilon$ of the gate oxide (Al$_2$O$_3$) with respect to the change in charge carrier density based on a cut-off density as shown below:

$$\varepsilon' = \varepsilon + \frac{3.14 + e^2}{4\pi\hbar(v_F)}\frac{1}{e^2n_0}$$

where $h$ is the Plank’s constant and $v_F$ is the net Fermi velocity inside the dielectric material at that point. The variation in Fermi velocity is then given by (eq.(5), [3.16]) as follows:

$$v_F(n) = v_F(n_0)(1 + \frac{e^2}{16\pi\hbar v_F}\frac{\ln(n_0)}{n_0})$$

We assumed a cut off density $n_0 = 1.3 \times 10^{11}$ carriers/cm$^2$ for graphene on alumina system for our simulation purposes, and carried out a test simulation study for SP71KK (500nm double gate) sample data. The simulated values of Fermi velocity then fall between the range of $1.21 \times 10^6$ m/s to $1.29 \times 10^6$ m/s, which is more close to the realistic values reported and suggested in available literature, as outlined before also. The simulated cumulative gate coupling capacitance ($F$) versus applied gate voltage $V_g$ (V) plot is shown as under in figure (3.9) below.

![Fig. 3.9: Simulated cumulative gate coupling capacitance as a function of applied gate voltage for the sample device SP71KK (500nm double gate) under the modified approach adopted from Novoselov’s model of charge carrier density based quantum capacitance. Note that this simulation was carried out for the response of one of the gates on the channel.](image)

Comparing this simulated data to previously measured versus simulated data plot shown in figure (3.7), which represents the measured and simulated data for the effect of both the gates of the double gated sandwiched device, we can clearly observe that the simulated data is of the same order of magnitude as of the measured real device. The interface trap charge density based capacitance element ($C_{it}$) for the device SP71KK in the above modified
simulation approach came out to be 0.42 μF/cm², which indicates a cleaner device at the same time, compared to the earlier simulation results. Although the nature of the plot differs substantially in the two (measured versus simulated) cases because of the reason that this model accounts for the ideal behaviour of the device, whereas the real device suffers from many internal as well as external loss factors, which render non-ideal behaviour to it. However, comparing our simulation results with the simulated results presented by Novoselov et. al. in figure 2(a) [3.16], we observe that our expression for quantum capacitance incorporating Novoselov’s proposed model of varying charge carrier density based quantum capacitance conforms to the expected behaviour of such GFETs. This proves that our theoretical expression derived and presented in equation (b) above is correct, and can be effective in understanding of device behaviour in line with the established theory in the field.
Chapter 4. Results, Discussions, Conclusions & Outlook

Results & Discussions:

This chapter discusses the experimental measurement results obtained and the intrinsic device characteristics obtained under high input RF power settings. In this study, the RF power was 0 dB (1 mWatt), which is quite high for these devices given their overall ultra-thin structure as well as only 7 nm of gate oxide layer thickness. Therefore in a way, this study reflects a worst case operating condition scenario study of RF GFETs. The main objective of this study was to compare the RF performance of a double gated GFET device with the RF performance of a single gated device. The results, as we observe, show that even under these high RF power conditions which might cause thermal damage to the sample, these devices were robust and could perform. We note that a double gated device with the same gate dielectric layer thickness has a higher intrinsic transit frequency and thus, shows a better RF performance compared to a similar mono-(back) gated device on the same chip. We also observe that quantum capacitance already starts playing an important role in the overall performance of the device even with the gate dielectric layer thickness of 7 nm.

In the following sections, we report the detailed analysis of these two devices by comparing their measurement results under similar operating conditions.

Analysis of double gated device SP71 KK (500 nm):

Two devices on this sample SP71 with CVD graphene sheet as channel, labelled KD and KK were characterised in detail at frequencies spanning between 10 MHz to 40 GHz. Note that the major difference between KD and KK was that KD is a single (back) gated GFET device whereas KK was a double gated device. Both devices were similar in all other aspects, such as gate length (500 nm each), top and bottom gate dielectric layer thickness (7 nm each) and device width (16 µm), to name a few. Both devices were doubly clamped by metal layers and had cuts introduced in the graphene sheet under the metal contacts for charge injection. The transfer characteristics at various bias values and output characteristics of the device KK at various gate voltage values are shown below in figures (4.1) and (4.2). The ambipolar nature of graphene is seen in these curves as there is conduction occurring at both positive and negative voltages, indicating both electron and hole dominated transport regimes. This is a special property of GFETs. However, as can be observed in the transfer characteristics, the e-branch and h-branch slopes differ significantly. As can also be seen from transfer curves, the double gated device was doped, yet as we would see in further sections, much less doped compared to the back gated device KD, and a Dirac point for KK is clearly observed at around 1.3 V $V_{gs}$. This indicates that the device is heavily n-doped with impurities. As in the case of the back-gated device KD as we’ll see, no clear Dirac point could be located, which is again due to heavy n-type impurity based doping. Also, as the output
characteristics would show, the double gated device carries a higher current for the same applied gate voltage.

Figure 4.1: transfer characteristics of SP71 KK at relatively low negative (a) and positive (b) bias voltages. The quantity ‘Ids Norm’ represents the normalized current ratio $\frac{I_{ds}}{I_{ds0}}$ in amperes. The Dirac point as well as the characteristic drain induced shift is observed. (c) shows the transfer characteristics captured at relatively higher bias values.
Figure 4.2(a): Output characteristics of SP71 KK at various gate voltages. Drain source current reaches its maxima at negative bias voltages, indicating hole dominated transport in the device. This can also be observed from the transfer characteristics shown above, wherein the hole mobility (slope of the h-branch) is more than the electron mobility (slope of the e-branch). A complete saturation of drain-source current was not observed in this case, however some of the curves seem to approach saturation. Some of the curves, e.g., at Vgs=-600mV and Vgs=400mV, appear to distort at the highest bias, which is probably more so due to device heating than current saturation.

Figure 4.2(b): The device resistance in ohms as a function of gate voltage Vgs in volts for the device SP71KK at low bias (Vds=10 mV). Resistance attains a maxima at around 1.5 V Vgs and then tends to show saturation like behaviour. Approximate resistance for the device is around 120 Ohms.

Further to this, we carried out the DC transconductance (gm) calculations to locate the points along the Ids-Vgs curves where gm reaches a maximum, for both positive as well as negative bias voltages, for the device KK. Transconductance gm was observed to be maximum for device KK at -2.7 mS/µm at Vgs=1.02V for Vds=+1V. The other maxima of gm
was observed to occur at 2.8 mS/µm at \( V_{gs} = 0.60 \text{V} \) for \( V_{ds} = -1 \text{V} \). The \( gm \) plots are shown as under in figure (4.3).

Figure 4.3: DC transconductance \( gm (dI_{ds}/dV_{gs}) \) at two bias points of +1V and -1V, where they were observed to reach a peak \( gm \) value for the device KK. The plots were obtained by numerically differentiating the transfer characteristics at various bias voltages. The observed peak values of \( gm \) are -2.7 mS/µm at \( V_{gs} = 1.02 \text{V} \) and 2.8 mS/µm at \( V_{gs} = 0.60 \text{V} \) respectively. The shakiness in the curves is probably due to the window size selected for numerical integration of the \( Ids-Vgs \) data using MATLAB.

Around these points, both the gate voltage as well as source-drain bias was swept in very small steps and S-parameter data was captured. For de-embedding of these data to get intrinsic device characteristics, open and short dummy structures of the same geometry and layouts fabricated on SP71 chip were measured. The transit frequency of the intrinsic device (\( ft_{deem} \)) was evaluated using the standard de-embedding procedure defined by Dambrine et. al. [reference] and for the double gated device KK, \( ft_{deem} \) was found to reach a maximum value of 14.5264 GHz at \( V_{gs} = 0.91 \text{V} \), \( V_{ds} = 1.05 \text{V} \) at a source drain current of 8.2 mA. On the negative biasing side, \( ft_{deem} \) touched a maxima of 8.1680 GHz at \( V_{gs} = 0.46 \text{V} \), \( V_{ds} = -1.07 \text{V} \) with a source drain current of -7.8 mA. The corresponding \( h21 \) versus frequency plot for these points are shown as follows in figures (4.4) and (4.5).

Figure 4.4: \( h21 \) versus frequency plot for the device KK at operating point maxima \( V_{gs} = 0.91 \text{V}, V_{ds} = 1.05 \text{V} \).
Figure 4.5: $h_{21}$ versus frequency plot for the device KD at operating point maxima $V_{gs}=0.46\,\text{V}$, $V_{ds}=-1.07\,\text{V}$.

Figure 4.6: RF transconductance ($gm_{\text{rf}}$) plots for device KK at 10 MHz and 1 GHz at one of the points of maximum $f_{\text{deem}}$ ($V_{ds}=1.05\,\text{V}$). As can be observed, the $gm_{\text{rf}}$ at higher frequency always remains smaller than that at the lower frequency as the gate voltage increases, suggesting possibly high parasitic capacitances are encountered in this case, comparing with the model suggested by C. Benz et.al.[4.1]

Figure 4.7: RF transconductance ($gm_{\text{rf}}$) plots for device KK at 10 MHz and 1 GHz at one of the points of maximum $f_{\text{deem}}$ ($V_{ds}=-1.07\,\text{V}$). As can be observed, the $gm_{\text{rf}}$ at higher frequency degrades as the gate voltage increases, suggesting that higher non-uniform gate resistance and/or parasitic capacitances are encountered at this bias point, unlike the above case of positive bias point of $f_{\text{deem}}$ maxima.
Figure 4.8: De-embedded transit frequency $f_{T_{deem}}$ as a function of drain-source current at the other $f_T$ maxima operating point ($V_{ds}=1.05\text{V}$) for the device KK. Compared to the other bias case shown below ($V_{ds}=-1.07\text{V}$), in this case the growth and saturation and a small fall-down region is clearly observable. Therefore, adopting this operating point of $f_{T_{deem}}$ maxima would be reasonable.

Figure 4.9: the de-embedded transit frequency ($f_{T_{deem}}$) plotted as a function of drain-source current at the other maximum $f_{T_{deem}}$ operating point $V_{ds}=-1.07\text{V}$ for the double gated device KK. In contrast to the above positive bias maxima point, the growth-saturation-fall down behaviour is not observed in this case.

The combined observations from the above set of plots showing current gain ($h_{21}$) as well as the RF transconductance behaviour of the device KK at high frequencies indicates that the device has high parasitic capacitances as well as low gate access resistance at the point of maximum de-embedded transit frequency (14.53 GHz). This observation is supported by the extracted capacitance data for the device at both of these bias points outlined and plotted above, wherein the pad-gate coupling capacitance is observed to be fairly low at almost all the points (less than or equal to 1 fF) however, the net gate coupling capacitance
\[ C_g = (C_{gs} + C_{gd}) \] is of the order of \(~70-80\ fF\) whereas the extracted intrinsic device resistance \( R \) is of the order of \(~110\ \Omega\). Due to the double gate configuration of the device, an increase in the gate coupling capacitance compared to any mono-gated device case appears reasonable also. Low gate resistance is understood because of the h21 behaviour, where it does not degrade at or before the point of optimum cut off frequency but rather tends to saturate. This is in line as the predicted and explained through theoretical model fitting to measured device data by C. Benz et. al.\[4.1\] Their derived mathematical expression can be briefly summarized as follows:

\[
h_{21}(\omega) \propto \frac{1}{(R_g \times C_g)}
\]

where \( R_g \) is gate resistance and \( C_g = (C_{gs} + C_{gd}) \) is the net gate coupling capacitance in the intrinsic device. Looking at the simulated gate coupling capacitance fitted to the extracted gate capacitance data plot (fig.(3.7)), our simulations suggest that quantum capacitance becomes the most dominating component among the three capacitances; i.e., geometric gate capacitance, interface trap charge density related capacitance and quantum capacitance. The point to note here would then be that even when our gate oxide layer thickness is 7 nm, which is quite thick compared to many other previous reports where it is as thin as down to 1.5 nm, quantum capacitance starts to become a dominating design factor in high frequency GFET design and can not be ignored.

**Brief comments on some of the defective points observed in the captured data set:**

At some of the operating points where S-parameters were captured during the two-dimensional sweep of \( V_{gs} \) and \( V_{ds} \), it was observed that \( f_T \) and \( f_{Tdeem} \) values were suddenly touching exorbitantly very high values; however the number of such points in the entire data set was very less. In case of device KK, all in all 3 points out of a total of 496 operating points swept were found to show such sudden jumps. The analysis of the various S-parameter plots at these and the neighbouring operating points reveals the reasons behind such unexpected behaviour. Here, we outline one point each on the positive and negative bias sides to explain the reasons.

At an operating point \( V_{gs} = 1.14\text{V}, V_{ds} = 1.05\text{V} \), \( f_{Tdeem} \) was suddenly touching a value as high as 39.202 GHz at a source-drain current of 7.163 mA, whereas other points in the vicinity of this operating point, were giving out \( f_{Tdeem} \) values around \(~14\ GHz\). A plot of corresponding \( h_{21} \) (current gain) as well as \( S22 \) against frequency reveals the reason. These plots are shown as under in figures (4.10) and (4.11).
Figure 4.10: h21 versus frequency plot at the operating point showing sudden unexpected jump in $f_T\text{deem}$ values ($V_{gs}=1.14V$, $V_{ds}=1.05V$) for device KK. Much deviation from the expected $1/f$ behaviour (trend lines) is clearly noticed at high frequencies where the ends twist up a bit.

Figure 4.11: The parameter S22 plotted against frequency at the above mentioned operating point, as well as two of the nearest neighbour operating points. A difference in S22 parameters at these three subsequent points indicates that the signal applied at port2 and its reflected response read at port2 itself are quite shaky.

At another operating point $V_{gs}=0.45V$, $V_{ds}=-0.95V$, another such sudden unexpected jump in $f_T\text{deem}$ was observed. The plots of h21 versus applied frequency as well as S22 at this along with the only nearest neighbour point measured subsequent to it, are shown as under in figures (4.12) and (4.13).
Figure 4.12: $h_{21}$ versus frequency plot at the operating point showing sudden unexpected jump in $f_{T\_deem}$ values ($V_{gs}=0.45\,\text{V},\, V_{ds}=-0.95\,\text{V}$) for device KK. Deviation from the expected $1/f$ behaviour is not noticed in this case as in above discussed case.

Figure 4.13: The parameter $S_{22}$ plotted against frequency at the above mentioned operating point, as well as one of the nearest neighbour operating points. A difference in $S_{22}$ parameters at these two subsequent points indicates that the signal applied at port2 and its reflected response read at port2 itself are quite different in this case also.

All other S-parameters at these points and their neighbouring points, viz., $S_{11}$, $S_{12}$ and $S_{21}$ were found to be behaving as expected as no major deviations were observed for them. Initially, before analyzing these S-parameter plots, the first impression was that since the points of sudden jump (peaks) in $f_{T\_deem}$ versus $I_{ds}$ curves are the points where RF transconductances, and hence $Y_{21\_deem}$ are the maximum. RF transconductance and hence
Y21deem (and hence S21) become maximum at these points because at these operating points, the transmission response of port 2 (source-drain) signal applied at port 1(gate) suddenly becomes very high. We plotted S21 and Y21 in vicinity of this suddenly high fTdeem point but S21 looked almost the same, so S21 can not be responsible for this sudden jump. Having plotted S11, S12, and S22 also, it was observed that S22 at this one point of maximum fTdeem is suddenly very different from other points in its vicinity. So, this indicates that apparently while measuring the data using the VNA, due to some reason, port2 was disturbed (suffered some physical jerk or something similar) which could have had possibly caused this jump. Therefore these sudden jumps were apparently a result of external disturbance and not due to some internal device or measurement set up response. These operating points are thus proven to be defective, and were discarded for further data analysis purposes. The final de-embedded transit frequency (fTdeem) values derived and reported here therefore, were basis the other operating point data set minus these defective points.

**Analysis of mono-(back) gated device SP71 KD (500 nm):**

The same procedure of measurement was followed for the back gated device KD, whose transfer characteristics for the some of the bias voltages are shown below in figure (4.14). Output characteristics are also shown in figure (4.15). Please note that both the devices; viz., KK (double gated, described above) and KD (back gated, described in this section) were measured at the same operating points; i.e., transfer and output characteristics were obtained for the same set of values of V_{gs} and V_{ds}, and the number of data points swept was also kept the same, to obtain a comparative study.

![Figure 4.14: transfer characteristics of SP71 KD at relatively low negative (a) and positive (b) bias voltages.](image)

As can be observed, the device shows higher peak current values for negative V_{ds} values, indicating a hole...
dominated charge transport in the device, because n-type impurity doping is evident from the direction of shift of Dirac point in the $+V_{gs}$ direction. The quantity ‘Ids Norm’ represents the normalized current ratio $I_{ds}/I_{ds0}$ in amperes. Compared to device KK, in this case the Dirac point is not clearly observed, however the characteristic drain induced Dirac shift is observed.

Figure 4.14 (c): transfer characteristics of SP71KD at relatively high biases. The two maxima points of bias voltage denote the operating points at which maximum DC transconductance and hence, maximum de-embedded transit frequencies ($f_{Tdeem}$) were observed.

Figure 4.15 (a): Output characteristics of SP71 KD at various gate voltages. Current degradation at higher bias voltages is visible, indicating device heating, and at $V_{gs}=-1V$, the curve is pretty much different from the rest. Drain source current reaches its maxima at negative bias voltages, indicating hole dominated transport in the device. This can also be observed from the transfer characteristics shown above, wherein the hole mobility (slope of the h-branch) is more than the electron mobility (slope of the e-branch). Drain current trends more towards saturation in this case than compared to device KK shown above in figure 4.2.
Figure 4.15 (b): The device resistance in ohms as a function of gate voltage $V_{gs}$ in volts for the device SP71KD at a low bias ($V_{ds}=10$ mV). Unlike device KK, resistance does not attain a maximum nor shows any saturation-like behaviour in this case. Approximate resistance for the device is around 200 Ohms.

Further to this, we carried out similar DC transconductance ($g_m$) calculations as was done in case of device KK above to locate the points along the $I_{ds}-V_{gs}$ curves where $g_m$ reaches a maximum, for both positive as well as negative bias voltages, for both the devices. $g_m$ was observed to be maximum for device KD at 1.7 mS at $V_{gs}=-0.044V$ for $V_{ds}=+1V$. The other maxima of $g_m$ was observed to occur at -1.9 mS at $V_{gs}=-0.3122V$ for $V_{ds}=-1V$. The $g_m$ plots are shown as under in figure (4.16).

Figure 4.16: DC transconductance $g_m$ ($dI_{ds}/dV_{gs}$) at two bias points of +1V and -1V, where they were observed to reach a peak value for the device KK. The plots were obtained by numerically differentiating the transfer characteristics at various bias voltages. The observed peak values of $g_m$ are 1.7 mS at $V_{gs}=-0.044V$ and -1.9 mS at $V_{gs}=-0.3122V$ respectively. The shakiness in the curves is due to the window size selected for numerical integration of the $I_{ds}$-$V_{gs}$ data using MATLAB.

Once again, both $V_{gs}$ and $V_{ds}$ sweeps were carried out simultaneously for the device KD around these points having $g_m$ maxima and S-parameters were captured. Comparatively for the back gated device KD, $fT_{deem}$ was found to reach a maximum value of 7.2882 GHz at
$V_{gs} = 0.14\, \text{V}, \, V_{ds} = 1.09\, \text{V}$ with a source drain current of 6.3 mA; as well as on the negative bias side, $f_{T_{deem}}$ maximum was 9.1277 GHz at $V_{gs} = -0.17\, \text{V}, \, V_{ds} = -1.10\, \text{V}$ with a source drain current of -5.5 mA. These plots are shown as under in figures (4.17) and (4.18).

![Figure 4.17: h21 versus frequency plot for the device KD at operating point maxima $V_{gs}=0.14\, \text{V}, \, V_{ds}=1.09\, \text{V.}$](image1)

![Figure 4.18: h21 versus frequency plot for the device KD at operating point maxima $V_{gs}=-0.17\, \text{V}, \, V_{ds}=-1.10\, \text{V.}$](image2)

Figures (4.19) and (4.20) compare the RF transconductance behaviours of the device at these two bias points whereas figures (4.21) and (4.22) show the dependence of de-embedded transit frequency ($f_{T_{deem}}$) on source-drain current $I_{ds}$ at these bias points.
Figure 4.19: RF transconductance (gm_rf) plots at 10 MHz and 1 GHz at one of the points of maximum fTdeem (Vds=1.09V). As can be observed, the gm_rf at higher frequency is always higher than that at the lower frequency throughout the gate voltage sweep around the point of maximum fTdeem. As discussed in case of device KK, this may suggest comparatively low parasitic capacitances in case of this back gated device KD around this bias point. Gate resistance appears low as in the previous case given the h21 versus frequency plot behaviour.

Figure 4.20: RF transconductance (gm_rf) plots at 10 MHz and 1 GHz at the other point of maximum fTdeem (Vds=-1.1V). As can be observed, the gm_rf at higher frequency initially is less than that at the lower frequency but surpasses it as we sweep the gate voltage beyond the point of maximum fTdeem. This behaviour compared to the behaviour at the other bias point shown in fig. (4.19) above indicates that at this bias point, the high frequency behaviour of the device KD is better as lower effect of parasitic at higher frequencies is observed.
Figure 4.21: the de-embedded transit frequency ($f_{T_{deem}}$) plotted as a function of drain-source current at one of the maximum $f_{T_{deem}}$ operating points ($V_{ds}=1.09V$) for the back gated device KD. In contrast to the other bias point maxima (shown below), the growth-saturation-fall down behaviour is not observed in this case.

Figure 4.22: De-embedded $f_T$ as a function of drain-source current at the other $f_T$ maxima operating point ($V_{ds}=-1.1V$). Compared to the above bias case, in this case the growth and saturation and a small fall-down region is clearly observable. Therefore, adopting this operating point of $f_{T_{deem}}$ maxima would be more reasonable, combined with the fact that it shows better high frequency transconductance around this bias point also, as outlined in the figure 4.20 above.

The combined observations from the above set of plots showing current gain ($h_{21}$) as well as the RF transconductance behaviour of the device KD at high frequencies indicates that the device has lower parasitic capacitances as well as similar low gate access resistance (due
to similar gate stack configuration) at the point of maximum de-embedded transit frequency (9.13 GHz), compared to the double gate device KK. This observation is supported by the extracted capacitance data for the device at both of these bias points outlined and plotted above (figure 3.8), wherein the pad-gate coupling capacitance is observed to be fairly low at almost all the points (less than or equal to 1 fF or so) however, the net gate coupling capacitance $C_g = (C_{gs} + C_{gd})$ is of the order of ~30 fF whereas the extracted intrinsic device resistance $R$ is of the order of ~200 Ω. At the same time, similar to the double gated device KK discussed above, the saturation behaviour of the extrinsic as well as the intrinsic current gain $h_{21}$ particularly at high frequencies in itself suggests low gate resistance, as predicted and explained through theoretical model fitting to measured device data by Benz et. al. and outlined in above sections.

**Comparison of double gated versus mono-(back) gated device:**

A summary of the comparative data obtained through the above measurement procedure are listed below in table 1.

<table>
<thead>
<tr>
<th>Device type</th>
<th>$f_{T\text{deem}}$ (GHz)</th>
<th>$V_{gs}$ (V)</th>
<th>$V_{ds}$ (V)</th>
<th>$I_{ds}$ (mA)</th>
<th>$C_g$ (fF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>KK double gated</td>
<td>14.5264</td>
<td>0.91</td>
<td>1.05</td>
<td>8.2</td>
<td>44.58</td>
</tr>
<tr>
<td>KK double gated</td>
<td>8.2879</td>
<td>0.46</td>
<td>-1.07</td>
<td>-7.8</td>
<td>32.85</td>
</tr>
<tr>
<td>KD back gated</td>
<td>7.2882</td>
<td>0.14</td>
<td>1.09</td>
<td>6.3</td>
<td>32.34</td>
</tr>
<tr>
<td>KD back gated</td>
<td>9.1277</td>
<td>-0.17</td>
<td>-1.10</td>
<td>-5.5</td>
<td>28.64</td>
</tr>
</tbody>
</table>

Table 1. Summary of measured transit frequencies and operating point values for a gate length of 500 nm.

This data shows that the double gated device KK has a maximum intrinsic transit frequency of 14.53 GHz at 0.91V $V_{gs}$ and 1.05V $V_{ds}$ with a source-drain current of 8.2mA, whereas the back gated device KD has a maximum intrinsic transit frequency of 9.13 GHz at -0.17V $V_{gs}$ and -1.10V $V_{ds}$ with a source-drain current of -5.5mA. This tabulated data summary also indicates that a double gated device of the same gate length, geometry, layout and material configuration; e.g., gate dielectric thickness, is capable of carrying higher current densities and has higher de-embedded transit frequency because of better transconductance accompanied by relatively higher gate coupling capacitance and a comparatively lower gate resistance, as observed from resistance versus gate voltage plots. The lower gate resistance is reflected in the end results also as we observe higher currents near points of maximum transit frequency. This indicates a better transconductance for the double gated device as compared to a mono-gated device. Although gate coupling capacitance in case of the double gated device KK is a little more than that of the mono-gated device KD, the overall effective parasitic capacitances do not increase so much as the RF transconductance, resulting in a net increase in intrinsic transit frequency $f_{T\text{deem}}$. 
The reason behind a better performance of KK can also be understood if we look at the gate coupling capacitances in the two cases. Theoretically speaking, despite of having two gates and two dielectric layers above and beneath the channel graphene sheet, the interface trap charge density related capacitance values ($C_{it}$) for the two devices should be the same. This is because the two comparable devices like KK and KD measured and analyzed here were fabricated together under the same lab environment using same process sequences as well as same CVD graphene sheet was used in defining their channels. Having undergone same process conditions of fabrication, $C_{it}$ can be safely presumed to be more or less the same in both the devices. However, since graphene transfer on to the device chip was carried out using PMMA based transfer process, and despite best efforts some traces of PMMA or other such impurities might alter the $C_{it}$ value from point to point across the chip. The atomic layer deposition process in itself might also be a source of impurity introduction into the graphene channel layer. In that case, the differing factors which need to be considered includes the geometric gate capacitance of these devices, the $C_{g}$ component as well as the quantum capacitance. Since the geometric capacitance is a fixed quantity, because it is dependent on the physical dimensions of the device, quantum capacitance accompanied by the $C_{it}$ component remain as the only variables which might be the probable cause behind the difference in behaviour between these two devices. Our basic simulations show that the $C_{g}$ components for the best fit were found to be 1.43 µF/cm$^2$ for the device KK and 0.478 µF/cm$^2$ for the device KD. This indicates that back-gated device KD is apparently more ‘clean’. Given that its theoretical geometrical capacitance is already half as much as that of device KK, and $C_{it}$ component is also reflected as much less as compared to KK, if one of these capacitance components were the dominating ones, the de-embedded transit frequency of KD would be higher than that of KK. However, measured data indicate otherwise, which points towards gate voltage dependent quantum capacitance as playing the major role in determining the overall capacitance of these GFETs. As a matter of fact, quantum capacitance can be seen as the response of the device channel to the applied gate voltage, because against every applied gate voltage value, there develops a certain channel potential, and quantum capacitance is a logarithmic function of this channel potential. As was observed while fitting the simulated capacitance data against the measured device data, in order that the quantum capacitance starts affecting the device behaviour, its values for KK and KD should be of the same order of the smallest component between the $C_{g}$ and $C_{it}$, and in order for it to be a governing factor in device operation, its value should be the smallest among the three.

On comparison with the experimental data after fitting it against simulated data, it was found that quantum capacitance is indeed playing a dominant role here in determining RF response of the device, which is getting reflected in the form of enhanced transit frequency. The simulated maxima of gate dependent quantum capacitance values for the best fit to experimental data were found to be 15.608 fF and 11.292 fF for double gated device KK and back gated device KD respectively. The calculated theoretical parallel plate geometric
capacitances in the two cases were 198.24 fF and 99.12 fF respectively. These figures indicates that quantum capacitance is indeed an important quantity in the operational performance of these devices, given that it is the smallest component among all three and the net gate coupling capacitance is derived as per the following figure (4.23) shown below. In case of device KK, \( C_q \) is comparatively much smaller than the other two components, whereas in case of KD, the comparative magnitude of \( C_q \) is not that low. This observation suggests that \( C_q \) is more effectively governing the behaviour of the double gated device KK than of the back gated device KD, and hence the higher de-embedded frequency value is justified. This outcome of our simulation is also in line with the theoretical studies carried out by Jena et. al. [4.2] where they suggest that for devices with thin gate oxides, the gating of charge carriers in the channel is strong and non-linear due to \( C_q \) becoming comparable to overall \( C_{ox} \).

![Simple equivalent circuit model of a GFET device showing the correlation between the various capacitance components.](image)

Figure 4.23: Simple equivalent circuit model of a GFET device showing the correlation between the various capacitance components. The simulation model developed in this work is based on this equivalent circuit model. \( C_q \) and \( C_{it} \) act in parallel whereas the \( C_{ox} \), which is addressed as \( C_g \) here, the geometric capacitance associated with the device due to parallel plate configuration of the GFET device is in series with these two.

As can be observed from the I-V characteristics, both of these devices do not show high impedance, and as the simulated versus measured capacitance data fit has already shown in the previous section, these devices contain quite a bit of impurity density, meaning that charge carrier mobility in the channel would be limited by collision with impurities apart from phonon scattering due to device heating. Device heating also plays an important role in limiting the current through the device, because heating causes impurity centers in graphene layer to become more active, limiting the overall current carrying capacity of the GFET device. Unlike pulsed bias and gate voltages as has been used in some of the recent reports [4.3, 4.4], we have used a continuous non-pulsed bias and gate voltage for our measurements. As has been shown by recent theoretical studies also [4.5], self heating in GFET devices may degrade current at current densities higher than 1 mA/µm up to 15% and may be responsible for the saturation behaviour experimentally observed in graphene devices. At sub-500 nm gate lengths, contacts also become an important source of heat sinking. As is observed upon comparing the output characteristics of the two devices, the double gated device shows higher current carrying capacity, although its peak current values do not appear to saturate at higher biases. In our opinion, although our devices were 500
nm gate length GFETs and not smaller, still since a double gated GFET device has greater metallic area including both gates as well as source-drain contacts, its I-V characteristics should reflect lesser current degradation despite of higher gate coupling capacitances as compared to a mono-gated device of equivalent dimensions. This explains the observed I-V behaviour, and also indicates that the saturation like behaviour of the mono-gated device is basically an outcome of current degradation that occurs at higher bias values. This is also supported by the simulated device parameter results where the interface trap charge density related capacitance component is although smaller for the mono-gated device, its very much flattened transfer characteristics near the Dirac point and a very distorted e-branch indicate very high levels of device doping, implying higher Joule heating probability and thus more current degradation possibility. As has already been mentioned at the beginning of this chapter, these measurements were carried out at 0 dB power level, which in itself is sufficiently high to smear such thin devices, so this might have also contributed to current degradation.

Also, as the RF input power was quite high, our samples are quite robust.

Conclusions & Outlook:

In conclusion, we fabricated characterized and simulated two graphene field effect transistors of comparable geometry, layout, material composition and gate oxide layer thickness on insulating sapphire substrate. Both DC as well as high frequency (microwave) measurements were carried out on these devices. De-embedding of the measured device data was carried out using dummy structures of the same geometry and comparable dimensions fabricated side by side on the same chip. We note that double gated GFET devices have higher transit frequencies compared to mono-(back-) gated GFET devices, and thus are a more suitable option for high frequency applications. We also note that fitting of the measured gate coupling capacitance data with our simulation model indicates that quantum capacitance plays an important role in determining the high frequency behaviour of these devices even at gate oxide thicknesses as high as 7 nm. The effect of quantum capacitance appears to be more pronounced in case of a double gated device. View this; we argue quantum capacitance may have even more pronounced effects on the high frequency performance of devices as we go down to thinner gate oxide layers and smaller gate lengths. Our simulation model is also able to suggest a possible reason behind the saturation-like behaviour of the output characteristics observed in case of one of the (back-gated) devices fabricated and characterized as part of this work.

Future work may include further improvements in the design of these GFET devices, some of which are as follows. Gate oxide layers may be fabricated with higher dielectric constant like TiO$_2$ and HfO$_2$, which would result into an increase of effective gate coupling capacitance but making thinner gate oxide layers possible. This may enhance the overall effect of quantum capacitance on the high frequency performance of these devices even further, leading to high de-embedded transit frequencies. Shorter gate length devices may
exhibit near ballistic transport of charge carriers, and thus improve on faster switching of these devices also. On the simulation front, many things can also be improved. Some of these may include inclusion of fluid charge carriers into the device model, which may help us in modeling and simulation of transfer and output characteristics of these devices also, thus bringing our understanding of the overall device behaviour closer to reality. Inclusion of both positive and negative charge carriers with different effective masses (electrons and holes) may also help us in simulating charge carrier mobility figures and ambipolar nature of graphene mono-layers. Inclusion of contact material specific metal-graphene contact resistances into the model may also result into a more realistic device simulation. Finally, a more detailed model of a graphene sheet would include impurity concentration based charge screening phenomenon, which may give us a better picture of potential distribution in the channel, which is necessary for a more accurate estimation of Fermi velocity of charge carriers in the graphene sheet, and thus the quantum capacitance in these devices. However, our simulations give an almost accurate Fermi velocity estimate of the same order for charge carriers (electrons) as reported by other researchers [4.2, 4.6], because of the fact that we have simulated the device behaviour mainly around and close to the Dirac point.
Chapter 6. Appendix I: suspended gate geometry GFET based NEMS device: Feasibility study

Introduction: The basic properties of a graphene mono-layer acting as a channel in a GFET help it attain higher mobility values, and thus better conductivity levels in the channel, despite of the fact that the limitations associated with its manufacturing process flow introduces varying impurity levels into the graphene sheet, which in turn, proves out to be a strong mobility killer.[1] Various experimental and theoretical studies have shown successfully this to be correct. Subsequently, this has evolved a great interest among both the industrial as well as academic fraternity, an immense interest towards realizing high performance devices based on graphene mono-layers acting as a channel. This work attempts to study the feasibility of a partial mono-layer based GFET dual gate configuration MEMS pressure sensor, which builds upon the modification of recently reported dual gate GFET device.[2][3] The feasibility study was carried out using COMSOL Multiphysics 4.3a simulation package, and the fundamental results under some basic assumptions on boundary conditions are reported here.

Working principle & device layout: The device layout is outlined in figure 1 below. The device basically is a differential conductivity MEMS sensor, which aims at detecting a mechanical stimulus applied to one of the ends of the dual gate fingers of a partial GFET device. The gate fingers are essentially fixed-fixed beams with a common drain and different source pads on the other side. One of the channels of the two FETs consists of a mono-layer graphene sheet, so that one of the FETs, when in operation under an applied gate voltage, acts as a GFET, whereas the other one acts as a normal FET (non-GFET). Since graphene mono-layer is a two dimensional electron gas system, which has a much higher conductivity even for dirtier (impurity levels ~ 10^12 cm^{-2} or more)[1] than regular oxide channel FETs, the current output response of the two FETs put side-by-side is in principle expected to be fairly different, and this would help us in detecting and measuring the applied stimulus.

In the figure above, the left half of the device is a GFET with a suspended gate, whereas the right half is a normal (aluminium) oxide channel FET with a fixed gate. The two devices are laid side by side with a common drain. While in operation, similar gate voltages are applied to both the gates. As the mechanical stimulus (pressure) is applied on the suspended flat attached to the other end of the suspended gate, it tends to bend the gate beam down, which changes the electric field effect, and thus triggers a change in the conductivity of the graphene channel as the gate comes closer towards...
the channel. In the right hand side oxide channel FET (RHSOFET), the current remains constant, whereas the current changes in the GFET on the left. This constant current in the RHSOFET can be treated then as a fixed reference value with respect to which the change in conductivity (and hence current response) in the GFET on the left can be measured. A change in value of current response in the GFET can be seen as that due to the applied stimulus, and hence the applied stimulus can be measured.

**Simulation results & discussion for the GFET:** The left half GFET was drawn in COMSOL Multiphysics as a 2-D geometry, as shown below in figure 2 and simulated under static conditions (no applied frequency; i.e., DC gate voltage).

![Figure 2: The suspended gate GFET geometry drawn in 2-D in COMSOL Multiphysics. The bottom layer is Sapphire substrate on top of which is a thin layer of Al₂O₃ dielectric placed to support the mono layer graphene. The mono layer graphene is so thin that it can not be seen in this cross sectional view, but it essentially lies on top of the dielectric layer. The top bar shown is the suspended gate. The mono layer is grounded whereas the gate was applied with a gate voltage of 0.5 V.](image)

One of the major issues while designing such a suspended gate geometry device was the consideration of mechanical stability of the mono-layer graphene layer while a gate voltage is applied and the gate approaches it from its initial position of suspension. If the initial suspension height is below a certain value, the electric field force may be so high that it exceeds the Van der Waal’s forces holding the mono-layer graphene sheet to the oxide layer beneath it, thus ripping it apart and permanently damaging the device. Therefore, in order that the device remains mechanically stable, the initial suspension height of the gate has to be chosen such that the electrical field forces do not exceed the Van der Waals forces outlined. Therefore, a simulation sweep was made with varying gate heights between 100 nm and 1000 nm suspension and a constant gate voltage of 0.5 V applied to the gate. Electrostatic force on between the gate and the graphene sheet was calculated using the electrical energy density method, as discussed further in this section below.

The simulated potential field maps for three sample heights of 1000 nm (1 µm), 500 nm and 100 nm are shown below in figure 3. As can be easily observed from these potential maps, at heights below 500 nm, the potential field lines grow very much in density and sharpness between the gate and the graphene sheet, indicating that the electrostatic force may be dominating over the Van der Waals forces, which indeed is the case, as simulation results outlined further would show. Reference Van der Waals force values were adopted from the work of S. Alvo et. al. [4] considering their model.
predicting such forces between nano-sized spherical objects (charge puddles in graphene sheet, which have a finite size and mass) and a flat base surface to be valid.

In order to check whether the entire potential drop correctly occurs between the gate and the graphene sheet (as the case should be), the graphene sheet was partially grounded and a simulation run was carried out. Figure 4 below shows the resultant potential field, where the left hand side
60 nm long portion of the graphene sheet is grounded whereas the remaining length on the right hand side was not grounded. One can easily observe that the entire 0.5 V applied to the gate drops between the gate and the grounded portion of the sheet, indicating that the simulation runs shown in figure 3 above would yield correct maximum force values.

![Figure 4: potential field map showing the partially grounded graphene sheet (blue area, minimum potential), whereas the right hand side non-grounded area is almost at half the maximum potential. This confirms that the potential maps obtained in figure 3 correspond to correct maximum electrical energy density.](image)

The potential drop shown in figure 4 was plotted along the length of the graphene sheet also to affirm this conclusion, and the same is shown in figure 5 below, where the grounded portion of the graphene sheet displays zero potential, whereas the ungrounded portion shows varying potential drop, depending upon the various charge puddle concentration values.

![Figure 5: line plot of potential drop showing variation of potential across various grounded and non-grounded charge puddle regions of the graphene sheet. The ungrounded region shows fluctuation in potential values because of the ungrounded charge puddle concentrations, each of which cancels out some of the potential field generated out of the gate voltage.](image)

The electrostatic force between the gate and the graphene sheet was calculated using the electrical energy density method. By using an inbuilt function (es.We) in COMSOL Multiphysics, the linear and volumetric electrical energy density distribution may be calculated as a function of either applied gate voltage (V) or gate suspension height (nm). Figures 6 and 7 below show the linear and
volumetric electrical energy density distributions along the length of the graphene sheet as a function of gate suspension height (nm).

Figure 6: Linear electrical energy density distribution (J/m) as a function of gate suspension height (nm). Clearly, as the gate goes farther away from the sheet for the same gate voltage (V), energy density reduces as field line intensities thin down.

Figure 7: Volumetric electrical energy density (J/m$^3$) as a function of gate suspension height (nm).

Now the electrostatic force between the two plates of a parallel plate capacitor; i.e., top suspended gate and the graphene mono-layer; can be calculated using the following formula, described under COMSOL Support Manual [EK 2360 Hands on MEMS Engineering course support material, KTH Microsystems Technology Division, Stockholm, Sweden]:

$$F_{el} = \frac{[(es.We)_1 - (es.We)_2] \times \text{(device width)}}{(h_1 - h_2)} \quad \text{Newton}$$

where, (es.We)$_1$ = electrical energy density in position 1;

(es.We)$_2$ = electrical energy density in position 2;

$h_1$ = height of suspension in position 1;

$h_2$ = height of suspension in position 2.
Using this formula, force values were obtained for suspension height sweep between 100 nm and 1000 nm positions in 100 equal steps, and the obtained values are plotted in figure 8 as under. The appendix listed at the end of this report shows a table listing the entire simulated set of electrical energy density and force values against suspension height (called as “gap”, in nanometers).

This plot of simulated electrostatic force (N) as a function of gate suspension height (called gap, nm) for the given geometry.

This plot of simulated electrostatic force tells us how much force acts on the graphene sheet when a gate voltage of 0.5 V is applied on the gate at a particular gate suspension height. This force calculation is necessary, as outlined earlier also, to know if the Van der Waals force holding the graphene sheet to its base (Al₂O₃ layer) would keep it mechanically stable against the electrostatic force which develops between the gate and the graphene sheet. As can be observed from the plot above (figure 8) and the corresponding force values listed in the Appendix at the end of this report, the electrostatic force at a gap of 300 nm is $1.63 \times 10^{-10}$ N, which is almost of the order of Van der Waals force calculated and predicted by S. Alvo et. al. in their numerical model for nano-sized spheres in vicinity of a plane surface ($\sim 10^{-10}$ N)[4]. Therefore, we can conclude that to remain on the safer side and to avoid permanent mechanical failure of the device, the gap distance between the suspended gate and the graphene sheet should be minimum 300+ nm. Therefore, in conclusion, at a design voltage of 0.5 V, the minimum designed suspension height (when the gate is under maximum bending) must be always more than 300 nm. One important point to note is that at higher applied gate voltages, the electrical energy density between the surfaces, and hence the forces may be higher, as was observed for a constant gap distance of 1000 nm, when the gate voltage is swept between -0.5 V and 0.5 V. This is shown below in figure 9. Therefore, if the device is desired to be operated at higher voltages or at different voltage values, separate results need to be obtained accordingly.
Conclusion: In this report, dual gate Field Effect Transistor based MEMS pressure sensor device design is proposed and simulations are made for studying the feasibility and mechanical stability of one half of the proposed device (GFET part), which constitutes of a RSOFET and a suspended gate GFET. Simulation was carried out using COMSOL Multiphysics 4.3a simulation package. The simulation studies show that the suspended gate GFET would be mechanically stable for a gate suspension height of >300 nm under operation for an applied gate voltage of 0.5 V.

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