Wafer-level 3-D CMOS Integration of Very-large-scale Silicon Micromirror Arrays and Room-temperature Wafer-level Packaging

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Front cover images:
Background: Array of app. 10 000 micromirrors made of monocrystalline silicon on a chip of 4.5 mm side length.
Top left: Close-up picture of the array in the background.
Top right: Close-up picture of an array with 1 000 000 tilting micromirrors made of monocrystalline silicon for maskwriting applications.
Center: Close-up pictures of hidden-hinge micromirror arrays made of monocrystalline silicon with three different flexure geometries. The top mirror plate is removed to allow the view on the flexures underneath.
Bottom left: Droplet of liquid in a reservoir, encapsulated at room temperature by wafer-bonding.
Bottom right: Photonic gas sensor, in transparent package with gas inlets and filters. The sensor was packaged at room temperature by wafer-bonding.
Abstract

This thesis describes the development of wafer-level fabrication and packaging methods for micro-electromechanical (MEMS) devices, based on wafer-bonding.

The first part of the thesis is addressing the development of a wafer-level technology that allows the use of high performance materials, such as monocrystalline silicon, for MEMS devices that are closely integrated on top of sensitive integrated circuits substrates. Monocrystalline silicon has excellent mechanical properties that are hard to achieve otherwise, and therefore it fits well in devices for adaptive optics and maskwriting applications where nanometer precision deflection requirements call for mechanically stable materials. However, the temperature sensitivity of the integrated circuits prohibits the use of monocrystalline silicon with conventional deposition and surface micromachining techniques. Here, heterogeneous 3-D integration by adhesive wafer-bonding is used to fabricate three different types of spatial light modulators, based on micromirror arrays made of monocrystalline silicon; micromirror arrays with vertically moving “piston-type” mirrors and with tilting mirrors made of one functional monocrystalline silicon layer, and vertically moving hidden-hinge micromirror arrays made of two functional monocrystalline silicon layers.

The second part of the thesis addresses the need for room-temperature packaging methods that allow the packaging of liquids or in general heat sensitive devices on wafer-level. A packaging method was developed that is based on a hybrid wafer-bonding approach, combining the compression bonding of gold gaskets with adhesive bonding. The packaging method is first demonstrated for the wafer-level encapsulation of liquids in reservoirs and then applied to packaging a dye-based photonic gas sensor.
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<th>Full Form</th>
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<tr>
<td>3-D</td>
<td>Three dimensional</td>
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<tr>
<td>AO</td>
<td>Adaptive optics</td>
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<tr>
<td>BCB</td>
<td>Benzocyclobutene</td>
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<tr>
<td>BEOL</td>
<td>Back-end-of-line</td>
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<tr>
<td>BHF</td>
<td>Buffered hydro-fluoric acid</td>
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<tr>
<td>CMOS</td>
<td>Complementary metal-oxide semiconductor</td>
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<td>CMP</td>
<td>Chemical-mechanical polishing</td>
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<td>CoB</td>
<td>Chip on Board</td>
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<tr>
<td>DMD</td>
<td>Digital mirror device</td>
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<tr>
<td>DRAM</td>
<td>Dynamic random access memory</td>
</tr>
<tr>
<td>DUV</td>
<td>Deep ultra-violet</td>
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<tr>
<td>FEM</td>
<td>Finite element method</td>
</tr>
<tr>
<td>FEOL</td>
<td>Front-end-of-line</td>
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<tr>
<td>IC</td>
<td>integrated circuits</td>
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<tr>
<td>ICP</td>
<td>Inductively coupled plasma etcher</td>
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<tr>
<td>LPCVD</td>
<td>Low pressure chemical vapor deposition</td>
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<tr>
<td>MCM</td>
<td>Multi-Chip-Module</td>
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<tr>
<td>MEMS</td>
<td>Micro-electromechanical systems</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed circuit board</td>
</tr>
<tr>
<td>PECVD</td>
<td>Plasma enhanced chemical vapor deposition</td>
</tr>
<tr>
<td>RIE</td>
<td>Reactive ion etching</td>
</tr>
<tr>
<td>RMS</td>
<td>Root-mean-squared</td>
</tr>
<tr>
<td>SiGe</td>
<td>Silicon-Germanium</td>
</tr>
<tr>
<td>SiP</td>
<td>System-in-Package</td>
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<tr>
<td>SLM</td>
<td>Spatial light modulator</td>
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### List of Abbreviations

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<th>Abbreviation</th>
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<tr>
<td>SoB</td>
<td>System-on-Board</td>
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<tr>
<td>SoC</td>
<td>System on Chip</td>
</tr>
<tr>
<td>SOI</td>
<td>Silicon on insulator</td>
</tr>
<tr>
<td>TSV</td>
<td>Through silicon via</td>
</tr>
<tr>
<td>UV</td>
<td>Ultra-violet</td>
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### Chemical formulas

<table>
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<th>Chemical formula</th>
<th>Description</th>
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<tr>
<td>Al-2%Si-0.5%Cu</td>
<td>Aluminum with 2% silicon and 0.5% copper content</td>
</tr>
<tr>
<td>SiO$_2$</td>
<td>Silicon dioxide</td>
</tr>
<tr>
<td>SF$_6$</td>
<td>Sulfur hexafluoride</td>
</tr>
<tr>
<td>Si$_3$N$_4$</td>
<td>Silicon nitride</td>
</tr>
<tr>
<td>Ni[H$_2$PO$_2$]$_2$</td>
<td>Nickel hypophosphite</td>
</tr>
<tr>
<td>NO$_2$</td>
<td>Nitrogen dioxide</td>
</tr>
<tr>
<td>O$_2$</td>
<td>Oxygen</td>
</tr>
<tr>
<td>HF</td>
<td>Hydrofluoric acid</td>
</tr>
<tr>
<td>HNO$_3$</td>
<td>Nitric acid</td>
</tr>
<tr>
<td>CF$_4$</td>
<td>Tetrafluoromethane</td>
</tr>
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List of Publications

The thesis is based on the following international journal publications:

1. “Wafer bonding with nano-imprint resists as sacrificial adhesive for fabrication of silicon-on-integrated-circuit (SOIC) wafers in 3-D integration of MEMS and ICs,”


3. “One-Megapixel Monocrystalline-Silicon Micromirror Array on CMOS Driving Electronics Manufactured With Very Large-Scale Heterogeneous Integration,”

4. “Heterogeneous 3-D Integration of Hidden Hinge Micromirror-Arrays Consisting of Two Layers of Monocrystalline Silicon,”

6. “Development of photonic systems on a chip based on dyes for sensing applications scalable at wafer fabrication,”

The contribution of Martin Lapisa to the different publications:

1. part of design, part of fabrication, part of experiments, part of writing
2. part of design, all fabrication, all experiments, major part of writing
3. part of experiments, major part of writing
4. part of design, all fabrication, all experiments, major part of writing
5. major part of design, major part of fabrication, major part of experiments, major part of writing
6. part of design, part of fabrication, part of experiments, part of writing
The following journal publication is not based on original research, and therefore it is not part of the thesis:


The work has also been presented at the following reviewed international conferences:


1 Introduction

This thesis presents research in the field of micro-electromechanical systems (MEMS), in particular the technology development of a wafer-level integration platform for integrating MEMS on top of integrated circuit (IC) substrates, and the development of a packaging method that is performed at ambient conditions.

The integration of MEMS with IC typically imposes various constrains on the allowed fabrication conditions, and limits thereby the design freedom and device performance. In application areas, in which MEMS are operated at the technological limit, such as in maskwriting or adaptive optics applications, these limitations have a direct influence on the achievable technical specifications. The proposed heterogeneous 3-D integration platform overcomes the fabrication constraints and enabled the successful fabrication of three different types of large-scale and very-large-scale micromirror arrays made of high performance monocrystalline silicon.

Mild processing conditions are also desirable in some packaging application, which is the focus of the second part of this thesis. It explores a novel packaging method that allows the packaging at ambient conditions. The packaging method is demonstrated for the encapsulation of liquids and for the packaging of a heat sensitive photonic gas and UV-sensor.
The thesis is divided into 7 chapters. The structure is as follows:

Chapter 2 introduces micromirror based spatial light modulators and describes requirements from a device perspective.

Chapter 3 motivates the integration of micro-electromechanical systems with integrated circuits and explains the potential and limitations of various chip-level and conventional wafer-level integration approaches.

Chapter 4 introduces heterogeneous integration and integration strategies.

Chapter 5 describes the improvement potential of MEMS spatial light modulators and presents the research done on large and very-large scale micromirror arrays made of monocrystalline silicon.

Chapter 6 introduces wafer-level packaging schemes and presents the work done on developing a wafer-level packaging method at ambient conditions.

Chapter 7 concludes the thesis.
2 Background on Spatial Light Modulators

2.1. Definition of a spatial light modulator

A spatial light modulator (SLM) is a device that modulates the amplitude or the phase of an incident light beam with spatial variation. Main application fields of spatial light modulators are imaging systems and adaptive optics applications. In imaging systems, the spatial light modulator is used to generate a pattern that is projected either magnified in cinema and video-projection systems or demagnified in maskwriting and maskless lithography applications. The goal in imaging systems is to achieve an amplitude modulation of the incident light, i.e. areas with varying brightness values between bright and dark. In adaptive optics applications the incident light has a wavefront aberration and the aim of the adaptive optics system is to correct this aberration to obtain a clearer, less aberrated signal. Main drivers of adaptive optics applications are astronomy where wavefront aberrations are induced by atmospheric turbulences or thermally induced drifts in the optical system, ophthalmology where aberrations are induced by inhomogeneity in the vitreous body and free-space optical communication where time-varying aberrations are caused by atmospheric turbulences [1,2].

Spatial modulations of a light beam can be obtained in many various ways such as electro-optically, magneto-optically, acousto-optically, with liquid-crystals, deformable mirrors, and mirror arrays [3–6]. This thesis concentrates on MEMS spatial light modulators based on micromirror arrays.
Different basic types of micromirror arrays exist. They show different performance and are therefore suited for different applications. An overview of possible implementations is shown in Figure 2.1. A classification into segmented micromirror arrays and deformable mirrors can be made. Segmented micromirror arrays have in common, that the micromirrors are individual elements that are controlled without influencing each other. The advantage lies in a relatively simple control algorithm and therefore potentially faster operation. This comes at the penalty of a reduced fill-factor, meaning that only a part of the total mirror array area is reflective. Hinges, anchoring posts and gaps between the mirror elements reduce the effective reflective area and thereby the optical performance.

A deformable mirror is strictly speaking not a micromirror array but a single mirror with an array of actuators below the mirror face sheet. The actuator array deforms the face.
Background on Spatial Light Modulators

sheet so that the reflected light is modulated. A natural drawback of this mirror-type is the complicated control algorithm because of cross-talk. When a single actuator is displaced, the deformation of the face sheet influences the surrounding actuators. A deformable mirror is therefore typically operated with a closed-loop control circuit, requiring 20-30 iterations to settle in the desired position. The important benefits are the optical properties; the discontinuities in segmented mirror arrays yield performance losses and induce failures in the reflected light due to phase-step errors that result in unwanted amplitude modulation [1]. This type of error is especially large for tilting and piston-type micromirrors where the height difference between neighboring mirror-edges can be large. A solution is an increased mirror density so that one large phase step is divided into many smaller phase-steps. Another possibility is the use of piston-tip/tilt mirrors that can additionally be tilted. Due to their ability to move vertically and at the same time tilt, the phase-steps in between the mirrors are minimized and the desired shape can be resembled with less mirror elements.

2.3. Amplitude modulation with micromirror arrays

Amplitude modulation is typically used in projection applications. The amplitude modulation with micromirror arrays can be achieved in two different ways. The commonly used method in cinema and video projection systems is depicted in Figure 2.2. To generate a bright pixel on the projection screen, a micromirror is tilted to its on-state, thereby steering the reflected light from its surface into the projection lens. A dark pixel is created on the screen by tilting the mirror into its off-state. The reflected light is then steered away from the projection lens into the aperture stop. The required tilt of the micromirrors is dependent on the dimensions of the optical projection system but typical values are in the range of $\pm 10^\circ$ to $\pm 12^\circ$ [7,8]. Gray-scaling, i.e. generating a light intensity between fully bright and fully dark, is achieved by time-multiplexing methods. The mirror vibrates between the on and off states during the exposure cycle to generate an intermediate intensity on the projection screen.
Another method, typically used in maskwriting and maskless lithography applications, creates bright and dark pixels by diffraction. Diffraction is wavelength dependent and based on interference between neighboring reflected beams. For that reason only monochromatic light that at least is partially coherent can be used with this method. To project a dark pixel, a destructive interference in the reflected light of neighboring mirrors is created [9]. This requires a differential deflection between the mirrors of only $\lambda/4$. For a mirror pixel of $16 \times 16 \, \mu\text{m}^2$ and UV illumination with a wavelength of 243 nm, this translates to a required tilt angle of less than 0.5 °, which is considerably less than with the previous method where deflection angles in the range of 10 ° are required. Gray scaling is achieved directly from the mirror tilt, by deflection to intermediate angles [10]. The amplitude modulated signal in projection is obtained by spatial filtering, as shown in Figure 2.3 [9]. The diffracted high spatial light frequencies are filtered in the Fourier plane and only the reflected light is projected. For this method of amplitude modulation only small tilting angles are required, which allows fast operation. However, this method is also less forgiving in terms of deflection precision.

Figure 2.2: Amplitude modulation of a projection system [1].
2.4. Phase modulation with micromirror arrays

Phase modulation in the reflected light of a micromirror array is achieved by deflecting the mirrors to different tilt or displacement levels. Thereby the distance that the light travelled is different for different micromirrors. Phase modulation is used in projection applications, as described in section 2.3, or in adaptive optics applications to correct...
Chapter 2

Wavefront aberrations of incident light beams. Dynamic wavefront aberrations, i.e. wavefront distortions that change over time, can have various sources. For the correction of these time-dependent errors in the wavefront, a dynamic correction system is required. The basic principle for the correction of an aberrated wavefront is shown in Figure 2.4. A plane, i.e. not aberrated wavefront is passing through turbulent medium, in which it is distorted. When the distorted wavefront reflects off a mirror surface that resembles the complementary shape of the incoming wavefront, the phase errors in the reflected light are corrected and a plane wave is reflected. Since the correction is performed in reflection mode, a mirror deflection of half the phase-error is sufficient.

2.5. Phase wrapping

For technological reasons, it is desired to keep the required mirror displacement low. In some phase modulation applications it is possible to reduce the required mirror displacement with phase wrapping. The technique is based on light being a periodically repeating electromagnetic wave with the wavelength $\lambda$. Therefore, it is sufficient to correct only the part of the wavefront distortion that does not fit into an integer number of wavelengths, i.e. the modulo $2\pi$ of the distortion. This is shown in Figure 2.5. The wavefront distortion exceeds the wavelength of the light, so the wavefront is divided into

Figure 2.4: Wavefront distortion and correction principle. The incoming wavefront reflects at the mirror surface resembling the complementary wavefront shape with half the amplitude. The reflected light is thereby corrected.
“wraps” containing each a wavefront part with aberrations between 0 and \( \lambda \). All parts that exceed \( \lambda \) or an integer multiple thereof are subtracted. This technique, however, can only be used with monochromatic light and with spatial light modulators that can generate abrupt phase steps such as segmented micromirror arrays. It must also be noted, that abrupt phase steps cause an amplitude modulation at the step, as described in section 2.2. This is not acceptable in some applications.

### 2.6. Requirements on spatial light modulators

The requirements on SLM’s are varying with the application. For the three main drivers of SLM development, maskless lithography, astronomy, and ophthalmology, the main requirements are briefly discussed, followed by an overview of typical figures of merit for micromirror SLMs.

In maskless lithography applications the throughput and positioning precision is of utmost importance. Throughput, in this context, includes optical efficiency aspects, mirror
response time, and the SLM array size. An open-loop operation without active feedback of the actual mirror position is favorable in this respect. However, an open-loop operation somewhat infringes with the requirement of positioning precision, which is achieved with grayscaling [10–15]. Grayscale is a technique that allows the shifting of lithographical patterns in a sub-pixel grid by tilting the mirrors to intermediate angles between zero and full deflection. The position of the pattern is strongly dependent on the exact mirror tilt. Combining these contradictory demands requires a reliable mirror deflection to the desired position over a long operation period.

In astronomy, SLMs are primarily used for the correction of atmospheric turbulences for ground-based optical telescopes. The atmospheric changes depend strongly on the temperature and wind speed at the observation site with a typical bandwidth of up to several hundred Hz [16]. The response time of the mirror array must be at least fast enough to follow these quickly occurring changes but typically a control loop is used that iteratively approaches the measured wavefront, so shorter response times are required. The number of the required iterations depends on the SLM and the efficiency of the control loop. Segmented SLM are easier to control and need fewer iterations than deformable mirrors because the mirrors do not influence each other upon deflection. As a rule of thumb the closed loop bandwidth for deformable mirrors should be at least ten times the bandwidth of the turbulences [17,18]. The required stroke in this application is dependent on the turbulence strength, the used optical system and the observed wavelength. For Kolmogorov turbulence the required stroke after tilt compensation can be approximately described by

$$s = 0.15 \left( \frac{D}{r_0} \right)^{0.6} \lambda$$

where \(D\) is the telescope aperture, \(r_0\) is the coherence length of the light, which is an indirect measure of the atmospheric turbulences, and \(\lambda\) is the observed wavelength. For an exemplary \(D/r_0 = 40\) condition, the required stroke of a micromirror SLM is approximately 3.2 times the wavelength. Ground-based optical telescopes observe wavelengths up to 14 µm [20], with a special interest in the wavelength band of 3 - 5 µm [21], so a stroke of > 10 µm is typically desired [22].

In ophthalmic applications, such as retinal imaging, the dynamic changes are much slower with a dynamic range of only 30 Hz [23]. The wavefront distortions are large though, with values of up to 53 µm [24,25], so a mirror SLM would require a stroke of > 25 µm for compensation.
2.6.1. Figures of merit

Typical figures of merit for a micromirror array with some explanations are listed in the following:

- **Low surface roughness of the reflective surface**
  The surface roughness contributes to the optical loss of the array. It causes local interference at the mirror surface and reduces thereby the optical performance. Therefore, many systems require a surface roughness of $\lambda/20$ ($\equiv 10\%$ optical loss) [1], astronomy applications have typically higher requirements.

- **High reflectivity**
  Similar to the surface roughness, the reflectivity contributes to the optical efficiency and a reflectivity of $> 90\%$ is required. Because mechanically favorable materials [26] are not typically good reflectors, reflective coatings on basis of gold, aluminum, or silver are employed [27–31].

- **Low mirror curvature**
  A curved mirror acts as a lens with focal length $f=R/2$, with $R$ being the radius of curvature. Curvature can be easier compensated by the optical system and degrades the optical performance less than surface roughness [1].

- **Short settling time / high operation frequency**
  Typically, the mirrors are used in a defined position, which is after they have settled. A large settling time reduces therefore the operation frequency.

- **Low drift & imprinting, high repeatability**
  Drift in the mirror operation can be acceptable to a certain extent in closed-loop SLM systems where the actual mirror position is monitored and accordingly corrected. However, mechanical drift effects the lifetime of the device and should therefore be minimized [7]. In open-loop systems that are used in maskwriting applications it is crucial to avoid mirror drift.

- **Low Hysteresis**
  Hysteresis complicates mirror control, as the position of the mirror depends not only on the actually applied addressing signal but also on the previous mirror state. Preferably the hysteresis should be zero.
• **High fill-factor**
  The fill-factor is the quotient of reflective SLM area vs. total SLM area. A high value is beneficial.

• **Large stroke/tilt**
  In adaptive optics applications large mirror stroke is desired because it widens the operational bandwidth. In projection applications large tilt angles are required to steer light away from the projection lens and thereby create a dark pixel on the screen.

• **Large array size, high mirror density**
  Projection applications benefit from large pixel count by achieving higher resolution and larger throughput (maskwriting applications). Adaptive optics applications benefit from large mirror count with lower residual wavefront error and the ability to correct higher order aberrations [24,25]. On the other hand, the optimal size of an SLM is about the same size as the exit pupil of the optical system to avoid the need for additional scaling optics. So with increasing mirror count the mirror density should be increased, too.

2.6.2. Meeting the large stroke requirements

Electrostatic MEMS micromirrors are in many applications the preferred choice because of their fast response times, their low power consumption, and their low hysteresis. Many micromirror designs have a parallel-plate actuator design, as illustrated in Figure 2.6. However, the electrostatic force of a parallel-plate actuator depends inversely quadratic on the electrode distance, while the spring has typically a linear restoring force dependency on the displacement. The voltage-displacement dependency of the actuator system is described by

\[ V = \sqrt{\frac{2kx}{\varepsilon_0 A}} (g - x)^2 \]

where \( V \) is the voltage, \( k \) is the spring constant of the restoring mechanical spring, \( x \) is the deflection, \( \varepsilon_0 \) is the dielectric constant, \( A \) is the electrode area, and \( g \) is the electrode distance. To achieve a large deflection at a fixed maximal voltage, the electrode area must either be increased or the spring must be made weaker. Neither is desirable because it negatively effects the response time. Further, only about one third of the initial electrode gap distance is usable for displacement before the electrostatic parallel-plate actuator goes into pull-in [32,33]. To address this limitation, a double reflection scheme has been proposed in which the incident light is reflected twice at the same SLM and thereby
doubling the phase correction abilities [34]. Another possibility is the use of a woofer-tweeter technique. This approach is based on the observation, that large mirror strokes are only required for low order aberrations, while high order aberrations have substantially smaller stroke requirements [35,36]. This makes it possible to implement a large stroke SLM with only few actuators for the correction of low order aberrations (the woofer) and a second SLM (the tweeter) for high order aberrations with smaller stroke but many actuators [37–39].

Figure 2.6: Schematic of an electrostatic parallel-plate actuator.
3 CMOS – MEMS Integration

This chapter gives a background on MEMS integration with control electronics, which is the setting of this thesis.

3.1. Motivation for MEMS-IC integration

Micro-electromechanical systems (MEMS) refers to the fabrication of devices with at least some of their dimensions in the micrometer range [40]. These devices can be transducers that transform one physical entity into another such as actuators or sensors. Often one of the physical entities is an electrical signal that can be further processed [41]. The processing of the electrical signal can be done externally, then the raw sensor signal is fed into a measurement computer and processed there. This strategy is however not always wanted. For example, in environments where many sensor signals are monitored at a time, it is beneficial to process the sensor signals decentralized by electronic circuits that are optimized for this specific task. The electronic circuits are often integrated circuits (IC), meaning that all circuit functions are integrated onto one chip. Typical tasks that are performed by the IC are sensor readout, signal conditioning, signal processing and interfacing [42]. The sensor and its IC are combined into a single module that outputs readily conditioned electric signals. An integration of MEMS and IC is however often not a matter of choice but a necessity. Capacitive sensing and actuation is widely used in MEMS for its low cost, low temperature dependence, low power consumption and large dynamic range. The small dimensions of MEMS sensors however allow for only small capacitance values in the range of pF ($10^{12}$) and sensing signals in the range of fF ($10^{15}$) [41]. For such small signals, parasitic capacitances and environmental noise severely influence the sensor function. To reduce these effects, the sensor must be closely
placed to the read-out electronics. Common examples are MEMS microphones [43–46], capacitive pressure sensors [47–49], capacitive inertial sensors [50–55], and resonators [56–59].

When sensors or actuators are used in large arrays, the necessity of integrating them very closely to a driving or read-out circuit arises from the amount of electrical connections that are required. This is typically the case for large-scale and dense bolometer arrays [60–62] and micromirror arrays [8,15,63–71]. Finally, it can be beneficial to use a close integration scheme in high-volume production for economic reasons [72] and many more reasons are thinkable that are not related to technical considerations such as product placement, firm strategy, production availability, etc. [73].

### 3.2. Limitations of MEMS-IC integration

Integrated circuits can be manufactured with different technologies. Widely used are complementary metal-oxide semiconductor (CMOS) based integrated circuits [42]. For an understanding of allowed and disallowed processing conditions in presence of a CMOS electronic circuit, a short and simplified background on the working principle is given. The basic building block of each CMOS integrated circuit is the CMOS inverter, shown in Figure 3.1. It consists of an N-MOS and a P-MOS transistor. The N-MOS transistor on the left side of the figure is thereby counteracted by the P-MOS transistor on the right, i.e. when the N-MOS transistor is conductive the P-MOS transistor blocks the current and

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**Figure 3.1:** Simplified scheme of a CMOS inverter. n+ and p+ regions indicate a high dopant concentration of n or p type dopant.
vice-versa. This complementary behavior is achieved by changing the local electrical properties of the silicon lattice by doping, i.e. the controlled adding of impurities into the silicon lattice such as boron, phosphor, or arsenic. Maintaining a precise doping concentration profile is hereby important, as it defines the electrical properties of the transistors [74]. In the configuration shown in Figure 3.1 this ultimately allows the control of conductivity in the regions between source and drain by applying a voltage $U_{in}$ to the electrically isolated gates. The semiconducting regions in the silicon are electrically interconnected, as indicated in Figure 3.1 to work in the described way. The interconnection is typically done with several layers of metal wires, such as aluminum-alloy, copper, or tungsten, in a backend-of-line (BEOL) process (as opposed to the front-end-of-line processing of the active regions in the silicon). These metal interconnect layers are embedded in dielectric layers from SiO$_2$ or Si$_3$N$_4$ for mechanical stabilization, electrical insulation, and passivation [75].

The most pressing constraint that arises from the architecture of a CMOS circuit is its temperature sensitivity. Thermal processes cause an accelerated diffusion of the doping atoms in the silicon lattice and can change the profile of the doping concentration. The electrical characteristics of the transistors are thereby altered and in the worst case rendered unusable. How much change in the characteristic of the transistors is acceptable defines ultimately the allowed processing conditions. Diffusion is a temperature and time dependent process, with the temperature dependent diffusion constant $D$ and the time dependent diffusion length $l$, defined by

$$D = D_0 e^{-\frac{E_A}{kT}}$$

$[75] 3.1$

$$l = \sqrt{Dt}$$

$[75] 3.2$

where $D_0$ is the extrapolated diffusion coefficient for infinite temperature, $E_A$ is the activation energy, $k$ is the Boltzmann constant (1.38 e$^{-23}$ J/K), $T$ is the temperature, and $t$ is the time. The allowed thermal impact on a CMOS integrated circuit is therefore often called the thermal budget, meaning, that a long exposure of the circuits at lower temperature has a comparable impact on their functionality as a short impact at higher temperature.

Before the passivation layers are applied to the CMOS substrates, the palette of allowed materials in presence of the transistors is very limited. The electric properties of the silicon were adjusted by the application of impurities into the silicon lattice and care must be taken not to change the properties unintentionally by contamination. Most problematic for silicon CMOS are thereby metals that have large diffusion coefficients in
silicon or silicon-dioxide or energy levels close to the center of the silicon band-gap such as Au, Pt, Cu, Li, K, and Na [75].

With the application of the BEOL metallization and passivation layers, the active transistor regions are encapsulated and a contamination is of less concern. The thermal budget, however, shrinks to lower values because the metallization layers are temperature sensitive and susceptible to a number of temperature enhanced degradation effects such as junction spiking, change in contact resistance due to the formation of different metal-phases, change in sheet-resistance, void formation, and hillock formation [74,76].

The maximum thermal budget for integrated CMOS circuits varies with the technology used. Smaller gate lengths and shallower junctions generally tolerate less diffusion. However, most CMOS-MEMS integration is done after the CMOS fabrication is completed, so the limiting factor is the BEOL metallization. The maximum allowed temperature depends on the particular core and barrier metals used. It is in the range of 400–500 °C [75–78] or up to 525 °C when parametric changes in the CMOS circuits can be tolerated [79]. To increase the thermal budget, tungsten has been used as interconnect metal [54,80] at the cost of an increased circuit resistance, which often is not acceptable.

Another constraint that applies to the allowed processing conditions is the exposure of the transistors to X-ray radiation or high-energy electron bombardment, which creates oxide-trapped charges that influence the threshold voltages [75].

From a MEMS perspective, the limitations arising from the sensitivity of the CMOS integrated circuits are significant. Many well-established MEMS processes rely on harsh processing conditions such as the use of high temperatures or X-ray generating machinery. A careful process selection and the development of new techniques to build MEMS within the limits set by CMOS integrated circuits are therefore necessary.

3.3. Integration techniques

The choice of the integration strategy depends on aspects such as system design, application requirements, physical necessities, cost, product strategy, and many others. Many different techniques for the integration of MEMS and integrated circuits have been developed and a short overview of the most common techniques is given in the following. Traditionally, the integration of MEMS and IC is performed after dicing the wafers, on chip-level with hybrid integration techniques. This is discussed in subsection 3.3.1. With decrease in size and increase in performance of MEMS devices, the integration earlier in the production line on wafer-level, i.e. before the wafers are diced into individual chips,
can be advantageous or enabling. Wafer-level integration techniques are discussed in subsection 3.3.2 and section 4.

3.3.1. Hybrid integration

Over the past decades, different integration technologies for MEMS and integrated circuits have been developed. Main development drivers are size, cost and performance considerations, i.e. the need to reduce parasitic influences. Some of the chip-scale integration concepts are picked in the following to give a general idea of the development direction in this field. The integration of separately packaged dies onto an interconnecting printed circuit board (PCB), as illustrated in Figure 3.2 a), is one of the simplest integration techniques, also called System-on-Board (SoB) [81]. A derivative of this technique is the Chip-on-Board (CoB) technology [82–84], in which the unpackaged dies are mounted on a PCB, as illustrated in Figure 3.2b). With both of these techniques, the components are placed relatively far apart from each other, so parasitic influences are of concern and the

Figure 3.2: Hybrid integration techniques. a) System-on-Board, b) Chip-on-Board, c) Multi-Chip-Module, d) System-in-Package.
amount of connections between the chips is limited. The integration of the separate dies into a single package in Multi-Chip-Modules (MCM), as illustrated in Figure 3.2c) yields many benefits [85,86]. It allows for shorter connections between the dies and therefore less parasitic influences, as well as a higher integration density and reduced volume. Here, the dies are placed side-by-side on a lead-frame or on an interposer substrate. Shorter connection lengths and a higher integration density are achieved by die-stacking in System-in-Packages (SiP) [87–89], as illustrated in Figure 3.2d). The connections between the dies are then achieved by wirebonding, with through-silicon-vias (TSV) and flip-chip bonding, or direct bonding techniques.

Many connection techniques can be used such as soldering (SoB, CoB), wire-bonding (MCM, SiP), tape-automated-bonding (SoB), flip-chip-bonding using solders, solid metals or conductive glue (SoB, CoB, MCM, SiP), and direct bonding (MCM, SiP). Further, for the stacking of chips edge metallization [90] or through-silicon-wires (TSV) can be used [91,92].

A general advantage of chip-level integration is the separate processing of the MEMS device and the CMOS IC. Changes in the MEMS part do not automatically require an adjustment of the CMOS processes and vise-versa. Chip-level integration also allows the economical use of dies with different sizes, which with other integration techniques is more problematic [93].

3.3.2. Wafer-level monolithic integration

A closer integration of IC and MEMS reduces the connection related parasitics, decreases the package sizes, and has the potential to lower the packaging and instrumentation cost [52]. Ultimately, this leads to the integration of different functions on the same chip, such as the integration of a MEMS device and its electronic circuits, which is why this approach is referred to as system-on-chip (SoC) [94–96].

When the MEMS device and the electronic circuit are fabricated on the same substrate, this is called a monolithic integration, referring to the single substrate that is used in the fabrication. Three fundamentally different integration approaches can be identified for monolithic integration; MEMS-first, MEMS-interleaved, and MEMS-last. They differ in the order of fabricating the MEMS part in relation to the IC part.

In the **MEMS-first** approach the MEMS part is fabricated first, followed by the fabrication of the IC [97]. This approach yields the benefit of having no restrictions on the processing conditions for the MEMS device. However, the created topography of the typically extruding MEMS structures makes a subsequent lithography of the fine CMOS structures impossible, unless extensive planarization is performed [80]. Further, advanced CMOS circuit processing cannot tolerate the risk of contamination that is involved with using preprocessed wafers containing readily fabricated MEMS devices.
In **MEMS-interleaved**, the MEMS part is fabricated on the CMOS substrate next to the transistor regions before the interconnecting metallization layers are applied [55,98]. This approach circumvents the thermal budget restriction arising from the BEOL metallization. However, the integration density is limited by the side-by-side processing of the MEMS and CMOS structures and on the non-passivated active CMOS regions bears risks of contamination, as described in section 3.2.

In **MEMS-last**, the MEMS part is fabricated after the CMOS circuits are finalized, containing the BEOL metallization and passivation layers[63,72,80,97]. This approach yields the benefit of processing the MEMS structures apart from the CMOS fabrication line, so the CMOS wafers can be fabricated in specialized foundries and the MEMS structures can then be fabricated in less restricted MEMS environments, which broadens the allowed material palette. Further, with this approach the MEMS can be fabricated on top of the CMOS integrated circuits, yielding the highest integration density and making this 3-D integration approach the most viable monolithic integration scheme. However, the thermal budget restrictions are tightest in MEMS-last monolithic integration and all processing must be performed at CMOS BEOL compatible low temperatures (typically below 450 °C).

This is a severe limitation for the fabrication of MEMS devices. The most widely used material for MEMS structures, polysilicon, requires deposition temperatures of > 580 °C using low pressure chemical vapor deposition (LPCVD) [99–101]. Depending on the deposition conditions, annealing is additionally required at temperatures > 900 °C to reduce the internal stresses of the as deposited polysilicon film or activate dopants [41]. A monolithic integration of polysilicon with standard CMOS integrated circuits is therefore only possible in MEMS-first or MEMS-interleaved schemes, which are problematic for the above described reasons.

The monolithic integration of MEMS with CMOS IC requires highly specialized processing schemes in which all processing steps are potentially influential to each other. Compared to chip-level integration schemes it is highly inflexible and changes in parts of the system bare the risk of influencing other functions. Furthermore, the error propagation of monolithic integration schemes with many processing steps requires a high yield of each individual processing step.
4 Heterogeneous Integration

The MEMS-IC integration with hybrid integration techniques, as described in section 3.3.1, allows the flexible modular optimization of the CMOS IC fabrication and the MEMS fabrication separately. Changes in either of the components can easily be realized without redesigning all other parts. Compared to that, monolithic wafer-level integration offers the highest degree of integration density with the accompanying benefits, but has stark restrictions on the material and processing conditions and is highly inflexible to changes. Heterogeneous integration combines the benefits of chip-level hybrid integration and wafer-level monolithic integration. It offers the same degree of integration density as monolithic integration but overcomes its stringent processing and material restrictions. With this technique, materials with highly desired or enabling characteristics can be used for highly integrated microsystems. This includes monocrystalline silicon or germanium, III-V materials, piezoelectric materials, shape-memory alloys, carbon nanotubes or nanowires.

Heterogeneous integration is based on the separation of fabrication processes that are not compatible with the sensitive CMOS circuits onto a dedicated handle substrate. The MEMS devices can be fully or partly fabricated on the dedicated handle substrate, with no restrictions on processing conditions or material selection. A transfer of the MEMS device to the wafer containing the CMOS integrated circuits is then performed by CMOS compatible wafer-bonding and removal of the handle substrate. Further processing of the MEMS on top of the CMOS electronic circuits is possible, but with the same restrictions that apply to monolithic MEMS-last integration schemes.
4.1. Wafer bonding techniques

Heterogeneous integration of MEMS with CMOS integrated circuits relies on wafer bonding in which the separately fabricated MEMS parts are transferred to the CMOS substrates. Beside the general compatibility with employed materials on the CMOS and MEMS wafers, the requirements on the wafer bonding technique can vary for different applications. Typical aspects to consider in the choice of the bonding technique for heterogeneous integration are required temperature/voltage/pressure for bonding, the potential annealing temperature, the surface preparation requirements, allowed wafer topography, the particle tolerance, the bond strength, the release ability, the throughput, the chemical resistivity, void formation, allowed processing conditions after bonding, and many more.

Today’s wafer bonding techniques can be divided into three general categories; direct bonding, anodic bonding, and intermediate layer bonding.

Direct bonding is based on intermolecular attraction forces that occur when two surfaces are brought into close proximity. Extremely clean and smooth (< 1 nm RMS) mating wafer surfaces are therefore required but it is fast, can have high bond strength [102–111], and in-situ electrical contact of CMOS and MEMS is possible [111–116].

In anodic bonding a large electric field dissociates alkali-oxide at increased temperatures and dislocates the ions in an alkali-doped glass substrate. The oxygen-ions diffuse to the bond interface and form an oxide with the mating wafer. The requirements on surface roughness are much lower as for direct-bonding, particles can create voids in the bond interface [106,117–120].

Intermediate layer bonding utilizes an additional material layer that bonds the wafers. Techniques that are based on this approach are eutectic bonding [102,103,108,120–124], solder bonding [120,125–133], thermo-compression bonding [106,116,120,134–138], low-temperature melting glass bonding [106,107,120,139,140], adhesive bonding [106,108,117,120,124,141–150]. The particle tolerance is high and wafer topographies can be compensated.

Hybrid bonding is the attempt to combine different bonding techniques and thereby eliminate the shortcomings of each individual technique [108,124,151,152]. The goal is to achieve highly reliable wafer bonds with electrical connection between MEMS and CMOS in the same process step. For example, the combination of direct metal bonding and adhesive bonding yields the electrical interconnection of the wafers in a particle tolerant wafer bonding process. Different combinations of wafer bonding techniques are thinkable in this category.
### Table 4.1: Wafer bonding techniques [26,106,120,124]

<table>
<thead>
<tr>
<th>Method</th>
<th>Conditions</th>
<th>Pros</th>
<th>Cons</th>
<th>Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Direct bonding</td>
<td>RT − 1200 °C No – low bond pressure</td>
<td>+ High bond strength (annealing) + Hermetic + High temperature compatibility + Fast + CMOS compatible (PA)</td>
<td>– Requires very low surface roughness – High bond strength after HT annealing or PA – CMOS incompatible with HT annealing – Low particle tolerance</td>
<td>SOI wafer fabrication, heterogeneous integration</td>
</tr>
<tr>
<td>Anodic bonding</td>
<td>150 – 500 °C 200 – 1500 V Electrostatic pressure, no mechanical bond pressure</td>
<td>+ High bond strength + Hermetic + Resistant to high temperature</td>
<td>– High electric field strength can damage integrated circuits – Sodium contamination problematic for CMOS integration</td>
<td>Sensor packaging and fabrication</td>
</tr>
<tr>
<td>Solder bonding</td>
<td>150 – 450 °C Low bond pressure</td>
<td>+ High bond strength + Hermetic + CMOS compatible</td>
<td>– Solder flux</td>
<td>Flip-chip bumping, hermetic sealing</td>
</tr>
<tr>
<td>Eutectic or transient liquid phase bonding</td>
<td>200 – 400 °C Low – moderate bond pressure</td>
<td>+ High bond strength + Hermetic + CMOS compatible</td>
<td>– Native oxide sensitivity</td>
<td>Hermetic sealing, heterogeneous integration</td>
</tr>
<tr>
<td>Thermo-compression bonding</td>
<td>350 – 600 °C High bond pressure</td>
<td>+ Hermetic + CMOS compatible</td>
<td>– High bonding pressure – High surface flatness (direct-bonding)</td>
<td>Hermetic sealing, wire bonding, flip-chip bumping, 3-D ICs</td>
</tr>
<tr>
<td>Metal–metal direct bonding</td>
<td>150 – 400 °C Low bond pressure</td>
<td>+ High bond strength + Hermetic + CMOS compatible</td>
<td>– High surface flatness (direct-bonding)</td>
<td>Hermetic sealing, 3-D ICs</td>
</tr>
<tr>
<td>Ultrasonic bonding</td>
<td>RT − 250 °C High bond pressure, ultrasound</td>
<td>+ CMOS compatible</td>
<td>– Only small bond area demonstrated</td>
<td>Wire bonding, flip-chip bonding</td>
</tr>
<tr>
<td>LT melting glass bonding</td>
<td>400 – 1100 °C Low – moderate bond pressure</td>
<td>+ High bond strength + Hermetic</td>
<td>– CMOS compatibility</td>
<td>Hermetic sealing</td>
</tr>
<tr>
<td>Adhesive bonding</td>
<td>RT − 400 °C</td>
<td>+ High bond strength + LT bond + Substrate material diversity + Particle tolerant + CMOS compatible</td>
<td>– Not hermetic – Temperature stability</td>
<td>3-D ICs, temporary bonding, MEMS packaging, heterogeneous integration</td>
</tr>
</tbody>
</table>

RT: Room-temperature, LT: Low-Temperature, HT: High-temperature, PA: Plasma activation
4.2. Integration strategies

Various heterogeneous integration strategies have been reported. They differ in three main aspects: the degree of MEMS structure pre-fabrication, the type of removal of the handle substrate, and the point in the processing scheme when a permanent electrical connection between MEMS and IC is established. The final choice of a heterogeneous integration scheme is application specific and can be a combination of the approaches described in the following.

4.2.1. Degree of pre-fabrication

The degree of MEMS pre-fabrication before heterogeneous integration varies between integrating an unstructured material layer, and a fully fabricated and capped MEMS structure. A minimal amount of pre-processing is done on the MEMS handle wafer when an unstructured material layer is transferred to the CMOS substrate [61,66–68,129,131,132,148,153–159]. This approach can be used when only the material deposition/growth is CMOS incompatible and all other fabrication processes can be done in presence of the CMOS integrated circuits. Because the MEMS handle wafer does not contain any patterning, the transfer bonding can be performed without prior bond alignment. The structural patterning of the MEMS devices is performed on the CMOS substrates, preferably with use of the CMOS fabrication alignment marks, which yields the highest alignment accuracy. The integration of partly or fully fabricated MEMS structures from the handle wafer requires wafer alignment, which offers only limited accuracy [50,51,151,160–164]. For further processing of partly fabricated MEMS structures on top of the CMOS wafer, the transfer of the alignment marks to the CMOS wafer is required if patterning steps follow. The pre-fabrication of the MEMS devices on the separate handle substrate is however advantageous, as is discussed in section 4.3.

4.2.2. Handle substrate

The Removal of the handle substrate after the transfer of the MEMS structures to the CMOS wafer can be destructively or non-destructively. Destructive removal uses chemical or mechanical etching to decompose the handle wafer with the use of protective etch-stop layers or selective etchants [60,61,68,141,147,148,153,155,165,166]. Non-destructive removal bears the benefit of potential reuse of the handle substrate. It can be done by bond interface decomposition with etchants [167,168] or light [169–175], thermal exfoliation of ion implanted layers (ion cutting) [113,115,176,177], mechanical cleaving on predefined breaking points [160,178], or a deliberately weak bond interface to the handle substrate [179–181].
4.2.3. Signal interfacing

The time of permanent signal interface connection between the MEMS and CMOS part is a well suited property for a general categorization [93].

Via-first describes hereby integration approaches in which the electrical connections are prepared on either the CMOS substrates or the MEMS handle substrate before the transfer bonding step. The electrical connection is then established during the transfer bonding step. Via-first integration has been shown with wafer-level bumping techniques and subsequent, flip-chip bonding [130,154,160,167,182–186] or flip-chip like wafer-bonding [96,187]. However, these bonding techniques typically have only a contact area of 5 – 20% between the MEMS and IC devices, which makes the compounds fragile for further processing. With hybrid bonding the mechanical stability is increased by increasing the contact area between the bonded wafers. The area that is not used for electrical contact is bonded using a complementary bonding technique such as low temperature fusion [159,162,163,188] or polymer adhesive bonding [151,152,159–161,169,170,173,189,190]. In principle any other bonding technique that suits the purpose could be used. The main advantage of via-first integration schemes is the reduction of processing steps and thereby potentially reducing fabrication costs or increasing the total yield. However, the required bond-alignment adds to the fabrication costs and influences the overall yield, so a reliable alignment technology is crucial. A potential limitation of via-first scalability is the achievable alignment precision, which is currently in the range of about 3 µm for adhesive wafer bonds and less than 500 nm for direct wafer bonds with automatic bond equipment [191].

In via-last, the signal interface is established after the transfer bonding step, with additional processing steps. The electrical connection can be established with surface-micromachining techniques that allow an extremely fine pitch [89,192], but also packaging techniques, such as wire bonding, are thinkable for devices with low interconnection count. When surface micromachining is used, typically via-holes are etched trough the MEMS device and the bond-interface down to the connection pads on the CMOS wafer. The via-holes are filled with metal, e.g. by sputter deposition [66–68,141,156–158,193], electroplating [60,61,194] or electroless plating [153,155,166,195]. A very high interconnect density is possible, especially for heterogeneous integration schemes that rely on unpatterned layer transfer with pattern alignment to the CMOS substrate alignment marks in subsequent processing steps. The via-last heterogeneous integration has been demonstrated with different bonding techniques, such as adhesive bonding [66,141,142,145,148,150,153,156,158,166,181,194,196–200], eutectic bonding [122,164,201], solder bonding [132,133], and direct bonding [159,193,202], but no commercial high volume products have been reported yet.
4.2.4. Wafer alignment

Wafer bond alignment precision is an important issue in many heterogeneous integration approaches. The bond equipment manufacturers honor these requirements with constantly improved alignment systems. However, if alignment beyond the machine capabilities is required, additional techniques must be employed. The typically larger misalignment in adhesive bonding is attributed to the bonding mechanism. The bond adhesive transfers into a viscous phase, such as a sol-gel or liquid, which allows a relative wafer sliding during bonding. Techniques that reduce the sliding include the pre-curing of the bond adhesive to increase the viscosity during bonding [147] and the incorporation of deformable anchors that increase the friction between the substrates [203]. For improvement of the wafer alignment beyond the machine capabilities, tapered interlocking structures are used that force the wafers into the correct alignment upon vertical load [204].

4.2.5. Die to wafer integration

Die to wafer integration transfers individual MEMS dies to the CMOS substrate or vise-versa with pick-and-place processes. The dies can have different degrees of pre-fabrication and a further processing on wafer level is possible after the transfer. Again, the alignment accuracy is a limiting factor but this approach bears a number of advantages. The overall yield can be substantially increased by transferring only known good dies to known good CMOS circuits on the CMOS substrate [152,205,206]. Further, with die to wafer integration it is economical to heterogeneously integrate dies of different sizes, as opposed to wafer-level heterogeneous integration. In wafer-level integration approaches the dies with the highest cost per area define the maximal economical chip size. If the lower cost per area component is oversized, it adds drastically to the final chip costs. By dicing the expensive but small components, this cost premium can be avoided. However, pick and place processes are serial and might not be economical with small die dimensions in large volumes. Techniques for parallel batch placement of dies have therefore been investigated such as matrix expansion [207,208], selective device transfer [169–173,175,209], and self-assembly [209–213].

4.3. Yield considerations

Error propagation in lengthy processes is a general problem because each processing step potentially decreases the overall yield. Although the fabrication of CMOS integrated circuits requires a large number of photolithography masks and hence consists of many processing steps, the overall yield is comparatively high. This is attributed to the highly
standardized planar processing technology that is employed for the fabrication of integrated circuits. The yield in MEMS fabrication is typically lower. A number of factors make MEMS fabrication less predictable such as out-of-plane fabrication, large variety of materials, thick material layers, long processing times, harsh processing conditions, and unusual or custom fabrication processes. The yield of the MEMS processes performed on top of a CMOS wafer has therefore a large impact [73]. An advantage of heterogeneous integration is in this respect that the MEMS processes can be performed on a separate substrate and the (pre-)fabricated MEMS devices on the handle wafer can be tested before transfer to the CMOS wafer. In that way low yield handle substrates can be rejected, saving the CMOS substrates and achieving overall a higher yield. With the transfer of only known-good dies in die-to-wafer integration approaches with selective transfer techniques [169–173,175,209] or pick-and-place approaches [152,206], the yield can be increased further.
5 Heterogeneous Integration of Spatial Light Modulators

This chapter presents the work done on heterogeneous 3-D integration of spatial light modulators on top of CMOS control circuits.

5.1. Spatial light modulators

Typical applications for micromirror based spatial light modulators are projection systems [8,63,64,214], optical cross-connects [201,215], laser-pulse shaping [216,217], retinal imaging [24,38,39,218–220], atmospheric turbulence correction [18,21,29], confocal microscopy, and maskwriting or maskless lithography applications [12–15,157,221–224]. This thesis concentrates on the wafer-level fabrication of large micromirror arrays driven by CMOS integrated circuits. In the following, three different micromirror designs are presented for wavefront aberration correction used in ophthalmic applications or atmospheric turbulence correction and for maskwriting applications.

5.2. Problem formulation

In some optical applications, it is desirable to use micromirror arrays with a large number of actuators on small space. In adaptive optics applications, a large number of actuators allows for more precise wavefront error approximation, as well as the correction of wavefront errors of higher order. Maskwriting applications benefit from a large mirror
count by an increased throughput. For economic reasons, the array dimensions are to be shrunked at the same time. Small micromirror arrays are typically built on fan-out substrates, on which the electrical connections are routed in the spaces between the address electrodes to the outer chip edges for further interfacing. For micromirror arrays with a high density and a large number of actuators, passive wiring on a fan-out substrate becomes unpractical because the spaces in between the address electrodes allow for only a limited number of connections [65,225]. A solution is to build the mirrors directly on top of the integrated driving circuits with vertical interconnections between the MEMS mirrors and the IC. A close monolithic integration with a driving circuit however limits the allowed processing conditions, as described in sections 3.2 and 3.3.2, which prohibits the use of mechanically very stable materials such as monocrystalline silicon.

The mechanical stability of the mirror springs is very important, though. When micromirrors are displaced from their initial position, the mechanical springs holding the mirrors in place are stressed. Micromirrors that are made from polycrystalline metal thin-films are known to undergo stress relaxation processes due to grain-boundary sliding [226,227]. The result are mirrors that drift over time from their target deflection and that do not return instantly to their initial position that they had before deflection [228]. A remnant deflection state, called imprinting [9] is observed with the mirrors. This same phenomenon is also known as hinge-memory effect [7,229].

Digital operating micromirrors, such as Texas Instruments tilting DMD [8,63,64,214], can avoid the influence of imprinting effects when the mirrors are tilted between two stable states that are defined by physical stoppers. However, the hinge-memory effect causes a pre-tilt of the mirrors in the non-actuated 0 V state. With growing pre-tilt, the gap length between one side of the mirror and the corresponding address electrode becomes smaller while on the opposing side of the mirror the gap length increases. If the gap on one side of the mirror becomes too large, a reliable switching between the off-state and the on-state cannot be guaranteed and the mirror element fails [7,229]. The hinge-memory effect has therefore an influence on the lifetime of the DMD but not on the optical performance within the lifetime.

Analog operating micromirrors are deflected to arbitrary displacement or tilt levels. Drift prevention with stoppers, such as for digital operating mirrors, is therefore not possible. In closed-loop operation, the drift and imprinting of the micromirrors is actively compensated but the imprinting narrows down the achievable stroke over time. With larger stress levels on the micromirror springs and a longer load time, the drift effects become more pronounced, which is a problem for adaptive optics applications that require fast operating micromirror arrays with large strokes. The stress level in the springs can be reduced by increasing their length, but this increases at the same time the mirror mass and has adverse effects on the mirror response time.
Micromirror arrays for maskwriting applications require only small strokes but at the same time fast operation is of utmost importance. A closed-loop actuation scheme in which the mirrors iteratively approximate their target position is therefore not possible. The mirrors are operated in open-loop mode, meaning that the actual position of the mirror is not sensed or corrected during operation. Because grayscaling, an essential technique for the precise placement of patterns (see section 2.6), is extremely sensitive to the mirror drift, it is vital that the mirror drift is minimized. In mask-writing applications, it is possible to reduce the drift by special actuation schemes that minimize the deflection time of the mirrors [9,11,222]. Drift-free micromirrors are however the preferred choice in this application because drifting mirrors must be calibrated in regular cycles, which adds to the maintenance cost and decreases the machine uptime.

5.3. Previous work addressing these problems

Silicon is a well understood material with outstanding mechanical properties and a wide toolbox of processing techniques for the fabrication of MEMS structures. Alternative materials with similar properties that allow the monolithic integration of micromirror arrays with CMOS IC are therefore difficult to find. Micromirror arrays from metal alloys, such as amorphous aluminum alloy [9,69,71,224,228,230,231] or platinum alloy [232–234], have been reported to reduce the micromirror drift and imprinting. Metal alloys can be deposited and processed at CMOS compatible processing conditions and allow the fabrication of MEMS micromirrors on top of CMOS backplanes. Mirrors from amorphous aluminum alloy show a much better mechanical stability, as compared to polycrystalline aluminum alloy but they are not entirely drift-free. Silicon-germanium (SiGe) has been proposed as a possible polysilicon replacement [15,52,78] but has not yet been used widely. A possible reason might be that the deposited SiGe films exhibit internal stresses that are compensated with tailored stress compensation layers. A tight process control is therefore required with large effects on the layer properties upon process variations [235].

The heterogeneous integration of micromirror arrays from monocrystalline silicon has been shown with flip-chip integration techniques [130,154,167,182–186]. As described in sections 3.3.1 and 4.2.5, this approach bears potential benefits but it requires per chip alignment and the down-scaling in size as well as the up-scaling in connection count are limited [71]. Heterogeneous wafer-level integration of monocrystalline silicon has been demonstrated on small scale for the fabrication of micromirror arrays for adaptive optics applications or not CMOS integrated for maskwriting applications [66,193,210,236–239].
5.4. Large-scale SLMs made of monocrystalline silicon for adaptive optics applications

In this section the wafer-level heterogeneous 3-D integration of large-scale micromirror arrays from monocrystalline silicon for adaptive optics applications is presented. The integration with passive CMOS dummy substrates, i.e. substrates that only resemble the surface properties of CMOS wafers but do not contain any integrated circuits, is shown.

5.4.1. Design

The micromirror design, illustrated in Figure 5.1, has been previously used for SLMs in vision science applications [240] and has been monolithically integrated with CMOS control electronics by aluminum surface micromachining. The mirror element consists of a bottom address electrode that is placed on the CMOS dummy substrate and a mirror plate above it that is attached with four flexures (springs) to via-posts. The mirror plate and flexures are made from the same monocrystalline silicon material layer. The via-posts hold the mirror plate at a defined gap distance to the address electrode and provide electrical connection. When a voltage is applied to the address electrode, the grounded mirror-plate is attracted by electrostatic forces toward the bottom electrode. The electrostatic force is counteracted by the symmetrically placed flexures, so a parallel, piston-type motion results.
The micromirror elements are arranged in a two-dimensional array that forms the SLM. The bottom electrodes of the SLM are interconnected to sub-arrays that are actuated simultaneously, as illustrated in Figure 5.2. This division into sub-arrays is required because the array is too large for individual mirror addressing with passive wiring, as touched upon in section 5.2. Table 5.1 gives an overview over the properties of the fabricated micromirror arrays.

Figure 5.2: Interconnection of the address electrodes to sub-arrays. All micromirrors within a sub-array are actuated simultaneously.
Table 5.1: Specifications of SLMs for adaptive optics applications made of one monocrystalline silicon layer.

<table>
<thead>
<tr>
<th></th>
<th>SLM 1</th>
<th>SLM 2</th>
<th>SLM 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLM type</td>
<td>Vertical movable micromirrors (piston-type) with mirror plate and flexures in same plane</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mirror material</td>
<td>Monocrystalline silicon</td>
<td>Monocrystalline silicon</td>
<td></td>
</tr>
<tr>
<td>Flexure material</td>
<td>Monocrystalline silicon</td>
<td>Monocrystalline silicon</td>
<td></td>
</tr>
<tr>
<td>Crystal type (Si)</td>
<td>Diamond-cubic (100)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Young’s modulus (Si)</td>
<td>160 GPa</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Plastic deformation (Si)</td>
<td>None (fully elastic material)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mirror material resistivity</td>
<td>14 - 22 Ωcm, p-type / boron</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Si roughness (RMS)</td>
<td>&lt; 1 nm (for area of 1 µm²)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Array size</td>
<td>96 × 96</td>
<td>96 × 96</td>
<td>48 × 48</td>
</tr>
<tr>
<td>Mirror dimensions</td>
<td>35 × 35 µm²</td>
<td>35 × 35 µm²</td>
<td>74 × 74 µm²</td>
</tr>
<tr>
<td>Mirror pitch</td>
<td>40 µm</td>
<td>40 µm</td>
<td>80 µm</td>
</tr>
<tr>
<td>Fill factor</td>
<td>74.8 %</td>
<td>74.8 %</td>
<td>78.0 %</td>
</tr>
<tr>
<td>Smallest dimension of micromirror features (flexure-width)</td>
<td>1.4 µm</td>
<td>1.4 µm</td>
<td>3 µm</td>
</tr>
<tr>
<td>Flexure length</td>
<td>15 µm</td>
<td>15 µm</td>
<td>34 µm</td>
</tr>
<tr>
<td>Mirror air gap to electrode</td>
<td>2.2 µm</td>
<td>5.1 µm</td>
<td>5.1 µm</td>
</tr>
<tr>
<td>Mirror-layer thickness</td>
<td>340 nm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Buried oxide thickness (SOI wafer)</td>
<td></td>
<td>400 nm</td>
<td></td>
</tr>
</tbody>
</table>
5.4.2. Heterogeneous integration scheme

Based on the categorizations in section 4.2, we propose the fabrication of SLMs on top of CMOS backplanes by heterogeneous 3-D integration of monocrystalline silicon by unstructured layer transfer using adhesive bonding with an intermediate polymer spacer layer in a via-last processing scheme. The 340 nm thick monocrystalline silicon layer originates from commercially available silicon-on-insulator substrates. Two different fabrication approaches were investigated, differing in the gap between address electrodes and mirror plates and the fabrication of the vias that establish the permanent electrical and mechanical connection of the silicon mirror layer to the dummy CMOS wafer. Fabrication scheme 1 was used for the fabrication of SLM 1 (see Table 5.1) and is illustrated in Figure 5.3. Fabrication scheme 2, illustrated in Figure 5.4, was used for SLM 2 and SLM 3.

CMOS dummy wafer

The fabrication starts with the electrical interconnections and electrodes on the CMOS dummy wafer. A 2 µm thick thermal oxide is grown on a 100 nm silicon wafer and subsequently 150 nm thick aluminum-alloy (Al-2%Si-0.5%Cu) is sputter-deposited and patterned together with a thin Ti-W adhesion layer on one side of the oxidized silicon wafer (Figure 5.3a). For the chemical growth of nickel in a later processing step a 150 nm thick nickel layer is deposited and patterned using a lift-off process (Figure 5.3b).
**Sacrificial polymer spacer**

A negative tone, high-temperature stable photoresist (AZ nLOF 2070) is used as sacrificial spacer to define the gap distance between the address electrode and the mirror plate. As the surface of the CMOS dummy wafer exhibits a topography that originates from the patterned metallization layers, the trenches in between electrodes and electrical interconnections on the substrate cause surface topography in the spin-coated sacrificial polymer. To reduce this topography, the polymer coating is performed in two passes. In the first pass diluted polymer with a low viscosity is used to provide a layer thickness of 200 nm. The polymer is spun onto the fan-out wafer for 5 s at 3000 rpm. This short coating period distributes the polymer over the wafer while keeping it still very mobile and allowing it to fill the trenches. Thereby, the surface topography is smoothened (Figure 5.3c). The polymer is soft-baked after 2 minutes of reflow time, to drive out most of the remaining solvent. Then a second polymer layer with higher viscosity is applied, to obtain a layer thickness of 1.8 µm (Figure 5.3d). The remaining surface topography of the sacrificial layer has been measured to be 150 nm peak-to-valleys, which is a reduction by 40 % compared to standard single pass spin coating of high viscous polymer. Although this topography seems still very high for an application, in which the aim is to achieve a micromirror surface planarity in the low nm regime, it is sufficiently low in combination with the adhesive bond process in which a 300 nm thick bonding polymer is used. The adhesive bond process offers excellent planarization properties due to the reflow of the bonding polymer if the underlying surface topography is lower than the thickness of the bonding polymer. As the sacrificial polymer spacer is a negative photoresist, it can be photo-lithographically patterned. This feature is used to create via-holes in the polymer at the positions of the nickel plating bases (Figure 5.3e). The holes act as plating molds that are filled with nickel at a later stage in the process. Finally, the polymer is fully cross-linked by flood exposure in a mask aligner and baking in an oven for 120 minutes at 205 °C in a N₂ atmosphere.

**Transfer of the monocrystalline silicon layer**

The 340 nm thick monocrystalline silicon layer that is used for the micromirrors and flexures originates from a silicon-on-insulator (SOI) donor wafer (Soitec Unibond). The monocrystalline silicon layer transfer from the SOI wafer to the sacrificial polymer on the fan-out wafer is done with adhesive wafer-bonding, using a nano-imprint polymer (MRI-9030, Microresist GmbH, Germany) as the bond adhesive. This thermosetting polymer can be etched residueless in oxygen plasma. The bond-polymer is spin-coated onto the sacrificial polymer and onto the monocrystalline silicon device layer of the SOI wafer (Figure 5.3f). A total layer thickness of 2.2 µm of the sacrificial polymer and the bond-polymer defines the total spacer thickness and the air-gap distance between the
micromirrors and the underlying electrodes on the substrate. The wafers are baked on a hot-plate for 2 minutes at 120 °C to evaporate the solvents from the bond-polymer. Subsequently, the wafers are loaded into a commercial wafer bonder where the surface of the SOI device layer faces the surface of the fan-out wafer. Since the SOI wafer is not patterned, bond alignment is not needed for the assembly. The wafers are bonded by first evacuating the bond chamber to $5 \times 10^{-5}$ mbar, then bringing the wafers into contact and applying a pressure of 4500 mbar on the bond chuck, while heating the bottom and top bonding plate of the bond chuck to 200 °C within 30 minutes. After one hour at bonding temperature, a cooling ramp of 30 minutes is applied to reach 50 °C while maintaining the bond tool pressure. The bond process is finalized by removing the bond tool pressure from the wafer stack and purging the chamber (Figure 5.3g). After bonding, the SOI handle substrate is etched away in SF$_6$ plasma using an inductively coupled plasma etcher (ICP). The 400 nm thick buried oxide of the SOI wafer acts as an etch-stop layer protecting the monocrystalline silicon device layer of the SOI wafer from being attacked during the etch. The transfer of the monocrystalline silicon device layer is finished by stripping the buried-oxide layer in buffered hydro-fluoric acid (BHF) (Figure 5.3h).

Although the monocrystalline silicon membrane has been transferred to the sacrificial polymer layer with a surface topography of 150 nm peak-to-valley, we measured the topography of the transferred monocrystalline silicon membrane to have a root-mean-squared (RMS) height deviation of $R_q < 1$ nm on an area of $316 \times 237 \mu m^2$. This excellent result is due to the planarizing capabilities of the adhesive bonding process, in which the bond polymer refows and evens out the topography of the underlying substrate.

**Clamping and electrical connection**

In the remaining fabrication steps, alignment of the lithography masks to the embedded metal layers on the fan-out substrate is necessary. Because the wafer alignment marks on the fan-out substrate are visible through the thin transferred monocrystalline silicon layer they can be used in subsequent lithography steps.

At this point the monocrystalline silicon membrane is resting on the sacrificial layer but is not connected to the bottom substrate. It needs a permanent mechanical and electrical connection. Therefore, holes are etched into the monocrystalline silicon layer by RIE to reveal the plating molds (Figure 5.3i). The plating molds are filled with bonding polymer originating from the bond procedure, i.e. from the coating of the wafer with the bond polymer and the subsequent reflow during wafer-bonding. To clear the plating molds from the bonding polymer and to make the underlying nickel plating base accessible, anisotropic RIE with oxygen plasma is used. During this etch the bond polymer is etched three times faster than the highly cross-linked spacer polymer (negative photoresist). In addition, the spacer polymer is masked by the monocrystalline silicon layer during the directional RIE, resulting in a negligible etching of the spacer polymer (Figure 5.3j).
The nickel plating base on the bottom of the via-molds is exposed after the bonding polymer has been removed from the molds and in the subsequent electroless plating process the molds are filled with nickel. When the wafer is immersed into the nickel electrolyte, the nickel growth starts spontaneously as the nickel plating base gets in contact with the nickel hypophosphite plating solution (Ni[H₂PO₂]₂ DNC 571, AHC Oberflächentechnik Holding GmbH, Germany) at a temperature of 90 °C. During this timed process, the nickel is plated slightly above the edge of the monocrystalline silicon layer resulting in clamping of the silicon membrane (Figure 5.3k).

**Mirror patterning and SLM release**

In a last lithography step, the mirror and flexure pattern is etched with RIE into the monocrystalline silicon membrane (Figure 5.3l). A thick photoresist cladding is applied to the wafer surface for protection of the micromirrors during wafer dicing (see Figure 5.3m) and is stripped afterwards with solvent that also washes away the dicing debris. The micromirror release etching is done using isotropic oxygen plasma in a standard barrel reactor. In this final step the bond polymer and the sacrificial spacer polymer are selectively removed from the microstructures (Figure 5.3n).
The second fabrication scheme was used for the micromirror arrays SLM 2 and SLM 3 (see Table 5.1) with larger gap distance between mirror plate and address electrode. It differs from the first fabrication scheme in that the via-posts are prefabricated before the monocrystalline silicon layer is bonded to the sacrificial polymer spacer. Figure 5.4 illustrates the processing steps that are different from the processing scheme illustrated in Figure 5.3. The via-molds are filled with electroless plated nickel right after the photolithographic patterning of the sacrificial polymer and before wafer bonding (Figure 5.4f). The plating process is stopped when the metal growths close to the mold edge, as shown in Figure 5.6. Subsequently the monocrystalline silicon layer is transferred as described previously (Figure 5.3f-i). Because the vias are already filled with nickel, the bond polymer resides only on top of the pre-plated posts (Figure 5.4i) and can easily be removed in oxygen plasma. The exposed pre-plated nickel posts are very close to the transferred monocrystalline silicon membrane (Figure 5.4j) and the additional electroless nickel plating to contact and clamp the monocrystalline silicon membrane can be very
short (Figure 5.4k). From here on the further fabrication is identical with the previously described fabrication process.

**Figure 5.6:** Patterned sacrificial polymer spacer with preplated nickel via-posts before wafer bonding.

**Figure 5.5:** SLM 2 after release.
5.4.3. Results

A readily fabricated and released micromirror array (SLM 2) is shown in Figure 5.5. The main purpose of using monocrystalline silicon for micromirror arrays is its mechanical stability. The long-term stability of deflected mirrors made of monocrystalline silicon and possible imprinting are of major importance for phase aberration correction in adaptive optics applications. Preferably, an actuated micromirror should reach its maximum deflection instantly when switching on the actuation voltage and remain in this position without drifting. Upon switching off the actuation voltage, the mirror should return instantly to its initial position. The stability measurement of the fabricated micromirrors made of monocrystalline silicon is illustrated in Figure 5.7. The mirrors follow the ideal actuation scheme with an instant maximum deflection and a stable deflection over time with no measurable drift. When switching off the actuation voltage, the mirrors return instantly to their initial position and no imprinting is observed, as can be seen in the inset of Figure 5.7.

The use of monocrystalline silicon allows for a much thinner mirror membrane, as compared to for example polycrystalline silicon. The result is a small mirror mass which allows fast actuation speeds because the natural frequency of a mass-spring system is defined by
where $k$ is the spring constant and $m$ is the mass (in this simplified equation electrostatic spring effects are neglected). This is illustrated in Figure 5.8 where the mechanical response to a square wave actuation is shown at atmospheric pressure conditions. The mirrors have a rise and fall time of only about 2 µs and are slightly under-damped, resulting in a small over-shooting of the mirror and settling after another 2 µs. This leads to a possible operation frequency of about 125 kHz.

The optical properties of the fabricated micromirrors lagged behind the expectations, though. Especially the micromirrors with larger electrode gap distance showed larger deviations. It was found, that the monocrystalline silicon layer on the SOI wafer is compressively stressed. The initial compressive stress of the monocrystalline silicon is relieved to a large extent to the relatively soft polymer spacer. A further stress relief has been observed by patterning of the membrane with via holes, which caused a different curvature radius for the 40 µm and 80 µm pitch mirrors with identical electrode gap distance. This leads to the conclusion that the stress level can be further reduced by rearranging the fabrication process to pattern the complete micromirror features into the monocrystalline silicon membrane before the silicon membrane is clamped by the plated posts. It was also found to be beneficial not to prefabricate the via-posts, as those micromirrors showed in general worse pre-deflection and pre-tilt properties.

$$f_0 = \frac{1}{2\pi} \sqrt{\frac{k}{m}} \quad (5.1)$$
5.5. **CMOS integrated, very-large-scale SLM made of monocrystalline silicon for maskwriting applications**

In this section the wafer-level heterogeneous 3-D integration of a one megapixel spatial light modulator from monocrystalline silicon for maskwriting applications is presented. The integration with functional CMOS integrated circuits is shown. This is the first demonstration of wafer-level heterogeneous 3-D integration with functional CMOS driving circuits for very large scale actuator or sensor devices.

5.5.1. **Design**

The design of the mirrors and the CMOS integrated circuits that are used in this work have also been used for metal SLMs [13] for maskwriting applications previously [9,11,12,224]. A schematic illustration of the torsional micromirrors used for the fabrication of the one megapixel SLM is given in Figure 5.9 [13]. The spatial light modulator consists of an array of $2048 \times 512$ micromirrors with individual mirror dimensions of $16 \mu m \times 16 \mu m$. To each mirror two torsional hinges are attached at the center of the mirror plate on opposing sides that allow mirror tilting around one axis. The hinges are attached to via-posts (not shown in the figure) that hold the mirror free hanging above the bottom CMOS substrate and provide electrical ground potential. The mirror plates and torsional springs are fabricated...
from the same monocrystalline silicon material layer. Address electrodes on the CMOS substrate underneath the mirror plates deflect the mirrors by electrostatic force to arbitrary analog deflection angles within the operation range. The address electrodes are connected to an analog DRAM structure, i.e. a storage capacitor that is charged over a transistor with a defined address voltage. To feed the address signal to the storage capacitors, the SLM is partitioned into blocks of 32 columns that are connected to one analog signal multiplexer each, which is illustrated in Figure 5.10. Horizontally the SLM is partitioned in two parts with a row-select driver, each. With this setup the data is loaded into the SLM row by row. Detailed specifications of the SLM are listed in Table 5.2
Table 5.2: Specifications of one megapixel SLM for maskwriting applications made of one monocrystalline silicon layer.

<table>
<thead>
<tr>
<th>Property</th>
<th>Nominal value</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLM type</td>
<td>Tilting micromirrors with mirror plate and hinges in same plane (1-level)</td>
</tr>
<tr>
<td>Mirror material</td>
<td>Monocrystalline silicon</td>
</tr>
<tr>
<td>Flexure material</td>
<td>Mono-crystalline silicon</td>
</tr>
<tr>
<td>Crystal type (Si)</td>
<td>Diamond-cubic (100)</td>
</tr>
<tr>
<td>Young’s modulus</td>
<td>160 GPa</td>
</tr>
<tr>
<td>Plastic deformation (Si)</td>
<td>None (fully elastic material)</td>
</tr>
<tr>
<td>Si roughness (RMS)</td>
<td>&lt; 1 nm (for area of 1 µm²)</td>
</tr>
<tr>
<td>Array size</td>
<td>1 megapixel (2048×512)</td>
</tr>
<tr>
<td>Mirror dimensions</td>
<td>16 µm × 16 µm</td>
</tr>
<tr>
<td>Fill factor</td>
<td>85 %</td>
</tr>
<tr>
<td>Smallest dimension of micromirror features</td>
<td>600 nm</td>
</tr>
<tr>
<td>Mirror air gap to electrode</td>
<td>700 nm</td>
</tr>
<tr>
<td>Mirror-layer thickness</td>
<td>340 nm</td>
</tr>
<tr>
<td>Buried oxide thickness (SOI wafer)</td>
<td>400 nm</td>
</tr>
<tr>
<td>CMOS address voltage</td>
<td>~ 25 V</td>
</tr>
<tr>
<td>Max. edge deflection (tilt)</td>
<td>~ 160 nm</td>
</tr>
</tbody>
</table>

Figure 5.11: Heterogeneous integration scheme for the fabrication of a one megapixel micromirror array for maskwriting applications.
5.5.2. Heterogeneous integration scheme

A similar 3-D heterogeneous integration strategy as for the adaptive optics applications SLMs has also been used for the one megapixel SLM, meaning an unstructured layer transfer by adhesive wafer bonding with intermediate spacer in a via-last approach. The employed fabrication technologies and materials are however different and described in the following.

*Sacrificial dielectric spacer*

The wafers, containing the high-voltage CMOS integrated circuits and the mirror electrodes in the top BEOL metal layer, are fabricated in a dedicated proprietary CMOS fabrication line. A sacrificial spacer layer of silicon-dioxide (SiO$_2$) is deposited by plasma-enhanced chemical vapor deposition (PECVD) onto the 150 mm CMOS wafer, followed by chemical-mechanical polishing (CMP) to obtain a smooth and homogeneous layer of SiO$_2$ with 550 nm thickness (Figure 5.11a).

*Transfer of the monocrystalline silicon layer*

The adhesive layer, a thermosetting polymer (Benzocyclobutene – BCB), is spin-coated onto the sacrificial layer and pre-cured at 120 °C for 2 minutes (Figure 5.11b). The resulting BCB layer thickness has been measured with a spectroscopic reflectometer to be very uniform over the wafer with nominal values of 133 nm and a minimum to maximum deviation of only 1 nm within a wafer and 2 nm from wafer to wafer.

A SOI wafer with a 340 nm thick monocrystalline silicon device layer is doped by boron-ion implantation with a dose of 2*10$^{15}$ cm$^{-2}$ at 50 keV and dopant activation at 960 °C for 60 minutes in nitrogen atmosphere. The SOI wafer is cleaned and loaded together with the CMOS substrate into a commercial wafer bonder. The monocrystalline silicon device layer of the SOI wafer faces thereby the surface of the adhesive layer on the CMOS wafer (Figure 5.11c). The wafer pair is bonded with a pressure of 5600 mbar at a temperature of 250 °C for 1 hour in high vacuum (Figure 5.11d). After bonding, the back side of the SOI wafer is removed by mechanical grinding and chemical spin-etching with HF + HNO$_3$. The chemical ablation stops at the buried SiO$_2$ layer of the SOI wafer. The buried SiO$_2$ is removed in buffered hydrofluoric acid (BHF), leaving only the monocrystalline silicon device layer on the CMOS wafer behind (Figure 5.11e). As the silicon layer is only 340 nm thick, it remains partly transparent for visible light, so that an alignment in subsequent lithography steps to the alignment marks on the underlying CMOS substrate is possible.
Clamping and electrical connection

Of particular importance in the heterogeneous integration of MEMS with CMOS IC is the electrical interconnection. To obtain a reliable contact between the monocrystalline MEMS mirrors and the CMOS circuits, a via-hole etch process was employed that provides tapered sidewalls and an increased contact area of the via-post to the monocrystalline silicon layer, which is illustrated in Figure 5.12. The via-holes for permanent electrical and mechanical interconnection of the transferred monocrystalline silicon layer with the CMOS wafer are etched down to the upper metallization layer of the CMOS wafer with reactive ion etching (RIE) using a photoresist mask. This same photoresist is exposed to oxygen plasma after the RIE etch to broaden the via-pattern in the photoresist by some tens of nanometers. This step ensures a sufficient contact area between the via-metal and the silicon layer (Figure 5.11f). Subsequently, aluminum is sputter-deposited onto the wafer to fill the via-holes (Figure 5.11g). The via-post patterning is finalized by spin-coating and photo-lithographical pattern of a second photoresist layer onto the wafer to dry-etch the excess metal with RIE. Both photoresist layers are stripped in oxygen plasma (Figure 5.11h).
Mirror patterning and SLM release

A final photolithography is performed to define the mirror pattern in the monocrystalline silicon layer with RIE (Figure 5.11i). To release the micromirrors, the bond-polymer is decomposed in oxygen plasma and subsequently the sacrificial SiO$_2$ is removed in vaporized hydrofluoric acid (Figure 5.11j). When BCB is etched in oxygen plasma, a SiO$_2$ residue is formed that eventually stalls the etching of thicker BCB layers. To prevent this, typically a certain percentage of CF$_4$ is added to the oxygen plasma, which also etches silicon. However, because the BCB layer is very thin, a CF$_4$ additive is not required and the residues are removed together with the sacrificial SiO$_2$ spacer in the vapor HF release step. To protect the BEOL dielectric layers on the CMOS wafer from being etched during the micromirror release, an etch stop layer has been integrated underneath the top metal-layer containing the mirror electrodes [241].
Figure 5.13: One megapixel SLM from monocrystalline silicon on CMOS driving electronics in ceramic pin grid array package.

Figure 5.14: Close-up SEM picture of the SLM. The micromirrors were individually deflected to different tilt angles by the underlying high-voltage CMOS circuits.
5.5.3. Results

The packaged one megapixel SLM made of monocrystalline silicon is shown in Figure 5.13 and a close-up view on individually actuated micromirrors in Figure 5.14. Long-term deflection measurements to determine drift and imprinting of the micromirrors are conducted by actuating a micromirror with a constant driving voltage to its maximum deflection and observing the deviation over time. A micromirror should reach its maximum deflection instantly when the actuation voltage is turned on, and it should return instantly to its initial position after it is turned off. As for the AO micromirrors from monocrystalline silicon in the previous section, also the CMOS integrated micromirrors for maskwriting applications are drift-free and show no imprinting, as illustrated in Figure 5.15.

![Figure 5.15: Long-term deflection profile of monocrystalline silicon micromirrors (red dots) in comparison to micromirrors from polycrystalline aluminum (black squares).](image)
Although the mechanical properties of the mirrors fulfill the high expectations, the optical quality of the monocrystalline silicon mirrors turned out to be insufficient. All mirrors showed a concave curvature (cupping) of about 40 nm peak-to-valley, as illustrated in Figure 5.16. The root cause of this unwanted curvature was found in the ion implantation process of the monocrystalline silicon device layer on the SOI wafer. An inhomogeneous implantation profile causes a stress gradient in the silicon layer, which results in cupping micromirrors after the release etch. With changes in the doping process or the use of pre-doped silicon layers for the fabrication of micromirrors, it is expected that very flat micromirror arrays on CMOS that meet the requirements of maskwriting applications with 193 nm DUV laser light can be achieved.

Figure 5.16: Evaluation of static mechanical micromirror array properties. The graph shows the average bow (blue dots), height deviation $\sigma_z$ (red triangles), and tilt (green squares) of the micromirrors at nine measurement positions distributed over the entire array. Averaging is done over 35 micromirrors within each measurement field. The standard deviation for each measurement is given with error bars.
5.7. Large-scale, hidden-hinge SLMs made of monocrystalline silicon for adaptive optics applications

In this section, the wafer-level heterogeneous 3-D integration of large scale monocrystalline silicon micromirror arrays made of two monocrystalline silicon layers is described. The integration with passive CMOS dummy substrates, i.e. substrates that only resemble the surface properties of CMOS wafers but do not contain any integrated circuits, is shown. This is the first demonstration of heterogeneous wafer-level integration that has been reported for two functional material layers.

5.7.1. Design

Heterogeneous 3D integration has previously only been demonstrated with the transfer of one material layer. For micromirror arrays this means that flexures (also called hinges) and mirror surfaces have to be designed from this same functional layer. This results in a low fill-factor of the array and a compromise between soft flexures on the one hand and a stiff mirror plate, which does not bend under load, on the other hand. The separation of mirror plates and flexures onto different material layers with the flexures underneath the mirror plates yields the benefit of a high fill factor of the array together with a separate optimization of flexure layer and mirror plate layer, resulting in a stiffer mirror plate and more design flexibility for the flexures. In principle, the mirror plate could be fabricated from a different material, but the monocrystalline silicon material originating from SOI wafers offers a very flat surface, which is difficult to achieve otherwise.

The design of the three different mirror elements used in this work is illustrated in Figure 5.17. The address electrodes and electrical interconnect lines (not shown in the figure) are on the bottom dummy CMOS substrate. The flexure layer is placed free hanging on the first level above the substrate and is anchored by four posts per mirror element. The mirror plate layer is built on the second level at a defined distance to the flexure layer and anchored by one post in the center of the mirror plate. Electrostatic force attracts the mirrors in a piston-type, parallel motion toward the address electrode on the bottom substrate. Each monocrystalline silicon layer adds a 5 µm gap distance to the bottom address electrode, resulting in a total of 10 µm gap distance between mirror plate and address electrode.
Three different spring designs are used. A parallel-plate design (Figure 5.17a) that is based on the micromirror design discussed in section 5.4, a cross-bars design (Figure 5.17b) that consists of two orthogonally crossing beams that are attached to an outer frame, and a diagonal-beam design (Figure 5.17c) that, with larger deflection, behaves less like a linear spring but increasingly like a string with a nonlinear increasing restoring force [242]. This non-linear behavior is in particular interesting for parallel-plate electrostatic actuators, which are limited in their stroke to a third of the electrode gap distance before being pulled-in, as discussed in section 2.6.2. A range extension is thinkable with a non-linear spring design, together with a partly linearized voltage response curve. However, this type of actuator can only be used with perfectly elastic materials because the nonlinear effect is achieved by a stark material strain, which otherwise results in enhanced plastic deformation and speeds up the unwanted drift and imprinting effect.

The micromirror elements are arranged in two-dimensional arrays that form the SLMs. As for the single layer SLMs in section 5.4.1, the bottom electrodes of the SLM are interconnected to sub-arrays that are actuated simultaneously. This division into sub-arrays is required because the arrays are too large for individual mirror addressing with passive wiring, as touched upon in section 5.2. Table 5.1 gives an overview over the fabricated micromirror arrays.
Table 5.3: Specifications of hidden-hinge SLMs for adaptive optics applications made of two monocrystalline silicon layers.

<table>
<thead>
<tr>
<th>Property</th>
<th>Nominal value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
<td>Vertical movable micromirrors (piston-type) with flexures underneath the mirror plates</td>
</tr>
<tr>
<td>Array size</td>
<td>$48 \times 48$ micromirrors</td>
</tr>
<tr>
<td>Flexure material</td>
<td>Monocrystalline silicon</td>
</tr>
<tr>
<td>Mirror material</td>
<td>Monocrystalline silicon</td>
</tr>
<tr>
<td>Crystal type (Si)</td>
<td>Diamond-cubic (100)</td>
</tr>
<tr>
<td>Plastic deformation (Si)</td>
<td>None (fully elastic material)</td>
</tr>
<tr>
<td>Young’s modulus</td>
<td>160 GPa</td>
</tr>
<tr>
<td>Si roughness (RMS) (measured)</td>
<td>$&lt; 1$ nm (for area of 1 $\mu$m²)</td>
</tr>
<tr>
<td>Mirror dimensions</td>
<td>$78.4 \times 78.4$ $\mu$m²</td>
</tr>
<tr>
<td>Mirror pitch</td>
<td>80 $\mu$m</td>
</tr>
<tr>
<td>Fill factor</td>
<td>96 %</td>
</tr>
<tr>
<td>Flexure type</td>
<td>Parallel plate / cross-bar / diagonal beam</td>
</tr>
<tr>
<td>Flexure thickness</td>
<td>340 nm</td>
</tr>
<tr>
<td>Mirror plate thickness</td>
<td>1.5 $\mu$m</td>
</tr>
<tr>
<td>Buried oxide thickness (flexure SOI wafer)</td>
<td>400 nm</td>
</tr>
<tr>
<td>Buried oxide thickness (mirror plate SOI wafer)</td>
<td>1000 nm</td>
</tr>
<tr>
<td>Flexure air gap to address electrode</td>
<td>5 $\mu$m</td>
</tr>
<tr>
<td>Mirror air gap to address electrode</td>
<td>10 $\mu$m</td>
</tr>
</tbody>
</table>
5.7.2. Heterogeneous integration scheme

The heterogeneous integration scheme used for the fabrication of the hidden-hinge micromirror arrays is partly similar to the previously reported fabrication scheme in section 5.7.2, which is why here only the differences are discussed, while similar processing steps are only briefly mentioned.

**CMOS dummy wafer**

The fabrication of the CMOS dummy wafer, illustrated in Figure 5.18 is similar to that described in section 5.4.2 with the difference of additional SiO$_2$ stoppers and different material thicknesses. A 1 µm thick SiO$_2$ layer (previously 2 µm thick) and thicker metal layers with 350 nm Al-2%Si-0.5%Cu (previously 150 nm) and 200 nm nickel (previously 150 nm) are used. The thickness of the oxide layer was chosen upon availability while probing the fabricated micromirror devices is found to be easier with thicker metal layers (Figure 5.18a). The increased thickness of the nickel layer (Figure 5.18b) is beneficial in the via-hole etching process described in the next fabrication section. The SiO$_2$ stopper layer is plasma deposited in a PECVD reactor onto the metal layers and patterned with RIE to create 500 nm high bumps on the address electrodes that prevent short circuiting of the mirrors in case of a pull-in (Figure 5.18c).
First heterogeneous 3-D integration sequence

The same sacrificial polymer spacer (negative photoresist AZ nLof 2000) is used in this fabrication as for the one-level micromirrors but the application is performed differently. First a layer of highly diluted photoresist is coated on the wafer and allowed to reflow to fill the trenches in between the metal interconnect lines on the fan-out wafer. This layer is now highly cross-linked by flood exposure with UV light in a mask aligner and extensive baking at high temperatures. This treatment of the photoresist ensures that with the following polymer coating step no previously deposited polymer is dissolved, which would cause an inhomogeneous coating result. Then, in multiple cycles always 1 µm of sacrificial spacer polymer is added and highly cross linked before the next layer is added, until
A 4 µm thick sacrificial spacer is achieved (Figure 5.19). This seemingly complicated coating strategy yields a sacrificial layer with a surface flatness of 10 nm RMS, as illustrated in Figure 5.20, although it is coated on a substrate with underlying 850 nm peak-to-valley topography. However, the level of cross-linking prohibits a lithographical patterning of the sacrificial polymer.

The monocrystalline silicon layer for the flexures is transfer bonded with adhesive wafer bonding (Figure 5.19b-c), as described in section 5.4.2, and then the handle substrate is removed by isotropic plasma etching, followed by removal of the buried oxide layer of the SOI wafer. The surface flatness of the transferred monocrystalline silicon flexure layer,
illustrated in Figure 5.21, is below 1 nm RMS. This additional flattening is attributed to the adhesive bonding process in which the bond adhesive undergoes a viscous state and thereby levels out remaining topographies [243–246].

For the later clamping of the monocrystalline mirror plate layer above the flexures, nickel via landing pads are deposited and patterned on the monocrystalline silicon flexure layer (Figure 5.19d). The nickel layer is covered with a low temperature PECVD deposited SiO$_2$ layer (Figure 5.19e) that prevents chemical reactions during the plating of the via-posts that connect the hinge layer with the CMOS dummy wafer. At the same time the low temperature oxide serves as a hard-mask for etching the via-holes down to the CMOS dummy wafer and ensures that possible unwanted spontaneous nickel depositions on the wafer surface, illustrated in Figure 5.22, can be easily removed together with the oxide layer. The via-holes are etched though the monocrystalline silicon layer and the sacrificial resist layer using RIE (Figure 5.19f). The low temperature silicon oxide masking layer is then retracted a few tens of nm from the via-holes in the silicon layer, so that a larger contact area between the nickel posts and silicon layer is achieved (Figure 5.19g). The nickel via-posts are thereafter electroless plated, which clamps the flexure silicon layer (Figure 5.19h). The first heterogeneous integration sequence is finalized with RIE etching the flexure pattern into the silicon layer (Figure 5.19i). Then the low temperature oxide is removed to reveal the clamped monocrystalline silicon flexure layer and the previously covered nickel landing pads for clamping of the second monocrystalline silicon layer (Figure 5.19j).
The second heterogeneous 3-D integration sequence to transfer a 1500 nm thick monocrystalline silicon layer for the mirror plates is to a large extent a repetition of the first heterogeneous 3-D integration step. Again, the surface of the wafer has a large topographical variance caused by the 340 nm thick flexures, the slightly protruding via-posts and the nickel plating base at the center of the flexures. The multiple-cycle polymer spin-coating process is used to apply the sacrificial polymer spacer (AZ nLof 2000) (Figure 5.19k). Then, the SOI wafer is bonded with adhesive bonding to the sacrificial polymer spacer (Figure 5.19l), and the handle substrate is etched away with SF$_6$ plasma in the ICP etcher using the buried oxide of the SOI as etch stop layer (Figure 5.19m). Now the buried oxide layer is used as a hard mask for RIE etching the via-holes into the monocrystalline silicon layer and through the sacrificial polymer spacer down to the nickel via-landing pads on the flexure layer (Figure 5.19n). The buried oxide layer is again retracted a few tens of nm from the via-holes in the silicon mirror plate layer in buffered oxide etch to increase the contact area of the silicon with the via-posts (Figure 5.19n). The via-holes are filled with nickel (Figure 5.19o) and the silicon layer is clamped by slightly plating over the silicon edges. The mirror pattern is etched with RIE in a standard lithography process into the buried oxide and silicon layers (Figure 5.19p) with subsequent removal of the buried oxide layer in BHF. Finally, the micromirrors are diced and the sacrificial layers and bond polymers are removed by oxygen plasma etching to release the free hanging micromirror structures (Figure 5.19q).
5.7.3. Results

The fabricated and released micromirror arrays are shown in Figure 5.23. Given the similar structural built-up as for the one-level micromirror arrays presented in section Figure 5.6, the hidden-hinge micromirror arrays are expected to also be drift-free and to show no imprinting. However, the diagonal beam flexure has a strong nonlinear restoring force that is caused by the string-like spring mechanism. Here, the material strain is larger than for linear springs and although monocrystalline silicon is a perfectly elastic material, plastic deformation could in principle occur in the metal posts at which the flexures are anchored. Long-term deflection measurements of the diagonal beam flexure design,
illustrated in Figure 5.24, revealed that the micromirrors return instantly to their initial position, which confirms that no deformations occur in the nickel posts that might have a negative influence on the mirror performance.

The mechanical response of the micromirrors with parallel-plate and cross-bar flexures at atmospheric pressure is illustrated in Figure 5.25. The parallel-plate flexure design shows a slightly over-damped behavior. The rise-time to 90% of the maximum deflection is 44 µs. The cross-bar flexure design is under-damped with four oscillations before settling at the final displacement. The rise time is 7.1 µs. The micromirrors have to settle at their final deflection to be used for wavefront correction. An operation frequency of 3 kHz for the parallel-plate flexures and 3.2 kHz for the cross-bars design is therefore achievable. This considerably lower value compared to that of the one-level mirrors is a result of the larger size of the mirrors and the additional mirror plate layer made of thick and therefore ‘heavy’ monocrystalline silicon. The operating frequency nevertheless is sufficiently high and approximately three times higher than the operation frequency of the intended CMOS driving circuits (1 kHz) [240].

The static optical parameters of the SLMs were governed by large predeflections and pretilts of the micromirrors with the tendency to a larger value spread for SLMs with softer flexures, illustrated in Figure 5.26. Further, the mirror plates have a cone-shaped profile with a mean topography of about 14 nm RMS for all mirror designs. The mirror plates straighten out though when forcefully removed from their clamping post, which is illustrated in Figure 5.27. The cone-shaped mirror profile is therefore not a result of an intrinsic stress gradient in the monocrystalline silicon layer, as observed for the ion-doped micromirrors in section 5.5, but an otherwise induced stress. It was found, that the monocrystalline silicon layer bends upward in the region around the via-holes when exposed to elevated temperature. Because the nickel posts are electroless plated at 92 °C, the silicon is in a bended state when clamped and this bending is preserved by the nickel post. This induced bending effect, together with the compressively stressed flexure silicon layer from the SOI wafer that was found in section 5.4 can cause unexpected deformations in the flexure layer that manifest themself in the measurements of Figure 5.26.
Figure 5.26: Out of plane pre-deflection for the different SLMs.
A heterogeneous 3-D integration platform based on unstructured layer transfer by adhesive wafer bonding in a via-last concept was investigated. The CMOS compatible integration scheme was successfully applied to the fabrication of a number of large scale and very large scale micromirror arrays from monocrystalline silicon for adaptive optics and maskwriting applications. Although, this technology has not yet demonstrated its full potential in terms of optical properties of the fabricated micromirrors, the reasons for it were for every SLM isolated and none of which was found to be inevitable.

The multiple coating spacer technology used in the fabrication of the SLMs for adaptive optics application proved very viable and extremely flat monocrystalline silicon layers could be transferred to very uneven base substrates with no additional polishing steps. This technique is especially well suited for the fabrication of thick and flat polymer spacers.

The flattening capability of the adhesive wafer bonding technology is especially in this application beneficial where extremely flat functional layers are required. The relative large chip sizes of SLMs, especially for very large scale arrays, make void-free wafer bonding increasingly important. The particle tolerance of the adhesive wafer bonding technology is in this respect an important feature, as it allows void-free wafer bond

**Figure 5.27:** Line scan of clamped and unclamped mirror plates. The unclamped mirror plates were removed with manual force from their anchoring post. Note that the center post of the clamped mirror plate has been excluded from the measurement for scaling reasons.
interfaces. Drawbacks that arise from less accurate wafer bond alignment are for the presented unstructured layer transfer approaches irrelevant, and the patterning of the MEMS structures with alignment toward the CMOS alignment marks yields the placement accuracy of the lithographical tool, which is typically in the range of a few tens of nanometers.
6 Room-temperature, Wafer-level Packaging of Liquids & Sensitive Devices

In this chapter an overview of wafer-level packaging techniques and techniques developed for the packaging of sensitive media, such as liquids, is given. Then a novel wafer-level encapsulation method is presented that allows the wafer-level encapsulation of liquids or in general heat sensitive materials, as it is performed at room temperature and ambient pressure. The room-temperature encapsulation has, beside its mild processing conditions, also the benefit that no thermal stress is induced when dissimilar materials are involved. The basic principle of the packaging method is first demonstrated for the encapsulation of liquids, and it is then applied to package an optical gas sensor. A novel, bubble-free application method of epoxy underfill is also presented that allows the epoxy distribution between wafers with small gap distances, by using microfluidic distribution channels.

6.1. Wafer-level packaging schemes

When readily fabricated devices are encapsulated before the wafer is diced into separate dies, this is called wafer-level packaging or 0-level packaging. Wafer-level packaging has several advantages compared to techniques that are performed on chip-level, which were briefly discussed in section 3.3.1. Foremost, when the dies are processed
on the wafer, then packaging processes can be applied to all dies in parallel at the same time. This can result in a large cost benefit, especially for small sized dies with a large number of dies per wafer or when individual chip handling becomes difficult, due to small dimensions. Wafer-level packaging can potentially result in higher yield because handling steps on unpackaged sensitive devices are omitted and dirty processes, such as wafer dicing, take place only after the devices are protected. Additionally, the packages can be made smaller than with chip-level packaging, and no dedicated packaging equipment is required because the same fabrication equipment tools as in MEMS fabrication are used. However, these potential benefits are opposed by the fact that process variations during the wafer-level packaging impact all devices on the wafer, and that known bad devices cannot be excluded from the packaging process. They are packaged with no regard to their functionality, which in turn increases the packaging costs [247].

Wafer-level packaging is typically performed by deposition sealing or wafer-bonding techniques, illustrated in Figure 6.1. With deposition sealing, illustrated in Figure 6.1a), a cavity is formed around the MEMS structure by embedding it in a sacrificial layer and then covering the sacrificial layer with the enclosing cavity material. Access holes are etched into the cavity, through which the sacrificial material is stripped from the cavity,
leaving the package shell around the released device behind. The final sealing of the cavity is done by a second deposition that closes the access holes. The cavity can also be fabricated from a second wafer that is bonded toward the device wafer, followed by a deposition sealing, as illustrated in Figure 6.1b).

Wafer-bonding has the advantage to minimize the amount of processing steps on the device wafer that contains the potentially sensitive MEMS structures. Similar to some heterogeneous integration approaches, discussed in section 4.2, the aim is to decouple fabrication steps from the device wafer and perform them on the separate packaging substrate. Preferably, no additional processing steps are required after wafer bonding, as illustrated in Figure 6.1c).

In principle, any of the wafer bonding techniques discussed in section 4.1 can be used for wafer-level packaging, but not all wafer bonding techniques are suited for each task. Especially when hermetic seals are required, some materials are less suited to be used due to their permeability to gas molecules. The permeability of some material classes to water
molecules is illustrated in Figure 6.2 [248]. Tendentially, solid materials with higher densities are more hermetic, which favors direct wafer bonding techniques (fusion bonding, metal-metal direct bonding, and anodic bonding) and intermediate layer bond techniques using metals and low-temperature melting glasses. Most widely used for commercial wafer-level packaging is glass-frit bonding [107,139,140] and anodic bonding [107,119,247], for their simple application and high bond strength.

For vacuum packaging, beside the diffusion of molecules through the package materials, also molecule desorption from the cavity surfaces and leaks are of concern. This concerns basically all wafer-bonding technologies that involve a phase change during bonding, such as solder bonding, eutectic bonding, and glass-frit bonding, but also anodic bonding where oxygen gas is created at the bond interface [247,249]. To preserve a high vacuum, molecular getters are implemented in the packages, with the aim to capture free gas molecules within the package and thereby maintain or even increase the vacuum level [250,251].

However, a hermetic or even vacuum package is not always required. MEMS sensors often have to interact with the environment. Especially the sensing of gases requires the direct environmental contact to the sensing structure, while a protection from dust and damage must be ensured. This makes the packaging of MEMS sensors much more complex than for example the packaging of integrated circuits that do not contain any moving structures and do not require environmental interfaces.

### 6.2. Packaging schemes for liquids

The encapsulation of liquids for the use in microsystems has a number of applications such as variable focus micro-lenses [252–254], switches and devices based on switches [255–261], drug-delivery devices [262–269], microfluidic electronics [270], tactile displays [271–274], and others [275].

The wafer-level encapsulation of liquids is however a technological challenge. Traditional wafer-level packaging techniques discussed in sections 6.1 and 4.1 are performed at elevated temperatures and / or at vacuum atmosphere, both of which accelerate the evaporation of liquids, which is why these methods are not suitable for the encapsulation of liquids. Some exceptions have been reported, such as the encapsulation of a low vapor pressure liquid under vacuum conditions by parylene deposition [254] or the encapsulation of water by parylene bonding [276] at 220 °C where the bond-tool pressure was maintained higher than the water vapor pressure to confine the water in the cavities. However, these techniques can only be used in exceptional cases when the liquid can tolerate these harsh process conditions. Another possibility to integrate liquids is the needle injection of the liquid into the reservoirs after their fabrication [271]. Processing
restrictions for the reservoirs are thereby circumvented, but this method requires serial filling, and it is only possible to it when the reservoirs can be pierced without creating a leak.

From the wafer-bond techniques presented in section 4.1 only adhesive bonding can be performed at room-temperature and atmospheric pressure, while providing a reliable bond. A common polymer-based liquid encapsulation technique is based on the use of UV curable epoxy [255,261,271–273,277–280]. The use of a Teflon gasket to confine a liquid in combination with the application of an epoxy underfill for stabilization has been reported in [277]. Another polymer-based liquid encapsulation utilizes stiction valves made from parylene [274,276,281,282]. However, as illustrated in Figure 6.2, pure polymer-based encapsulation approaches cannot be hermetic. The confinement period of polymer encapsulated liquids is limited, and molecule diffusion between the liquid and the polymer takes place. Metals on the other hand show the lowest permeability and even thin layers are sufficient to achieve good hermeticity. In particular gold is a well suited metal for sealing applications because it is chemically inert, so it does not react with what is encapsulated, it is ductile and deformable, so it can be processed at low pressure levels, and it has a high density, so even thin layers of gold in the range of only a few micrometers result in high hermeticity values.

Recently, a method to encapsulate liquids at ambient conditions by plugging of the reservoir access ports with gold stud-bumps [283] was reported. This is an elegant and fast solution for applications that allow the cavity filling thru small inlet ports and protruding stud-bumps. A hermetic sealing method at room-temperature that is based on cold welding of corresponding and partly overlapping gold rings has been presented in [284]. However, in this method shear forces occur that can break off the sealing rings, or induce micro-cracks underneath the gold rings on surfaces with a lower modulus of rupture such as glass.

### 6.3. A novel room-temperature packaging method

We propose a method of encapsulation that allows the packaging of liquids and other heat sensitive materials at ambient conditions. Similar to the hybrid wafer bonding techniques discussed in section 4.1, it combines gold compression bonding with adhesive bonding. This combination of bond technologies yields a room-temperature wafer-level packaging method with increased hermeticity compared to pure polymer encapsulation. The method is based on gold gaskets that pose the inner cavity walls, and the application of epoxy underfill for mechanical stabilization. The gold gaskets on the lid wafer are fabricated by any suitable technique such as sputter deposition, evaporation, or electroplating. The gaskets are very small compared to the package dimensions, so when the lid wafer is pressed against the device/reservoir wafer at a sufficiently large bond force,
plastic deformation of the gold gaskets occurs. As a result, the gold adapts to the surface roughness of the mating surface and seals thereby the leaks, as illustrated in Figure 6.3a. When the mating surface is also made from gold, illustrated in Figure 6.3b, the gold structures can be cold welded, which results in a seal with improved hermeticity [128,188,284–286]. The mechanical stability of the wafer bond is achieved by epoxy underfill that is applied to the gap between the wafers. Epoxy underfill shrinks typically by several percent [144,287,288] upon curing. This results in permanent tensile layer stress on the order of a several MPa to a few tens of MPa [287–291], with only little relaxation over time [292–295]. A permanent vertical force on the gold gaskets keeps the surfaces therefore in close contact.
6.4. Wafer-level liquid sealing

For evaluation of the proposed packaging method, the sealing of liquids has been chosen. Figure 6.4 illustrates the reservoir concept. The reservoirs are defined by metal walls on the bottom silicon wafer, into which the liquid is dispensed. The lid wafer is equipped with the sealing gold gaskets, which hermetically seal the reservoirs after attaching the lid wafer to the reservoir wafer. A number of design variations of the gold gaskets on the lid wafer and the reservoir walls on the bottom wafer have been implemented, some of which are illustrated in the lower part of Figure 6.4. Circular reservoirs, square reservoirs with rounded edges, and rectangular reservoirs with rounded edges were implemented. Common for all reservoirs is the 50 µm wall width and 50 µm wall height that forms the cavity. The design variation for the gaskets includes different gasket widths, different amount of concentrically arranged gaskets per reservoir, and the use of cross connections between multiple, concentric gaskets. The gasket geometry
always matches the geometry of the reservoir wall and all geometries have rounded edges. Table 6.1 gives an overview of the design variations.

### 6.4.1. Fabrication of reservoirs and lid

To fabricate reservoirs and gaskets as illustrated in Figure 6.3b, a 500 µm thick 100 mm diameter glass wafer is used as substrate for the reservoirs and a silicon wafer of the same dimensions is used as lid wafer. A gold seed layer from 20/150 nm Ti/Au in combination with a patterned photoresist mold is used on both wafers for electroplating. Gold reservoir walls, 50 µm high, and 3 µm high gold gaskets are plated on the glass, respectively on the silicon wafer. The photoresist is removed in oxygen plasma, and the wafers are immersed in potassium iodide and subsequently in hydrogen peroxide, to etch away the seed layer.

Because the top surface of the fabricated reservoir walls is too rough for the sealing with the gold gaskets, having grooves in the order of the gasket height, the top surface of the reservoir walls is mechanically polished to obtain a smooth surface. This step might not be necessary with higher gold gaskets, but here the gasket height was only 3 µm.

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**Table 6.1: Design variations of reservoirs and gaskets.**

<table>
<thead>
<tr>
<th>Reservoirs</th>
<th>Geometries</th>
<th>Round, square, rectangular</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wall width</td>
<td>50 µm</td>
<td></td>
</tr>
<tr>
<td>Wall height</td>
<td>50 µm</td>
<td></td>
</tr>
<tr>
<td>Side lengths</td>
<td>2.5 mm – 7.5 mm (10 variations)</td>
<td></td>
</tr>
</tbody>
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<table>
<thead>
<tr>
<th>Gaskets</th>
<th>Geometries</th>
<th>Matches the geometry of reservoir</th>
</tr>
</thead>
<tbody>
<tr>
<td>Width</td>
<td>2 µm – 7 µm (14 variations)</td>
<td></td>
</tr>
<tr>
<td>Height</td>
<td>4 µm</td>
<td></td>
</tr>
<tr>
<td>Gaskets per reservoir</td>
<td>1 – 3</td>
<td></td>
</tr>
<tr>
<td>Cross connections between multiple gaskets</td>
<td>Only some structures</td>
<td></td>
</tr>
</tbody>
</table>
6.4.2. Encapsulation of liquids

Ethylene glycol is dispensed manually into the reservoirs on the wafer, as illustrated in Figure 6.5a. The lid wafer is then aligned with the bottom wafer under a microscope and subsequently loaded into a wafer bonder for compression, as illustrated in Figure 6.5b. The gold gaskets are in this way pressed against the flat top surface of the reservoir walls, resulting in embossing the walls and plastic deformation of the gaskets. Thereby, the mating surfaces seal off the reservoirs. A room-temperature curable epoxy underfill (Epotek 301) is applied to the side of the wafer, while the bond pressure is still applied. Due to capillary action, the epoxy penetrates the gap between the wafers and around the encapsulated reservoirs, as illustrated in Figure 6.5c. The bond pressure is released after the epoxy underfill is fully cured.
6.4.3. Results of liquid encapsulation

After encapsulating the liquids in the reservoirs, vacuum experiments were performed. The wafer stack containing the encapsulated liquids was placed in a vacuum chamber under high vacuum conditions ($10^{-5}$ mbar) for 24 hours. Liquid in leaking reservoirs would escape under these conditions and a subsequent inspection would reveal an empty reservoir. Two exemplary reservoirs after the vacuum experiment are illustrated in Figure 6.6. The fully embedded reservoir on the left was positioned close to the epoxy insertion point, while the partly embedded reservoir was positioned further away. The liquid remains in both reservoirs unchanged. It is remarkable, that even for the partly surrounded reservoir where the outer reservoir walls were directly exposed to the vacuum atmosphere with no epoxy underfill in between, the liquid did not evaporate. This indicates that the sealing is achieved by the gold gaskets and not by the epoxy underfill, in which the reservoirs are embedded. Further experiments were performed to confirm this. Liquid filled reservoirs were capped with the lid wafer but no epoxy underfill was applied. The chamber was evacuated to $10^{-5}$ mbar for 24 hours with applied tool pressure on the wafer stack. In both sealing tests, with and without epoxy, approximately the same sealing rate of about 85% of the present cavities on the wafer was achieved. Unsealed reservoirs were found to have insufficiently flat reservoir walls, so that the gold gaskets could not seal properly.

Figure 6.6: Reservoirs with encapsulated liquid, surrounded by epoxy underfill (left) and only partly surrounded by epoxy underfill (right). The reservoirs were exposed to vacuum ($10^{-5}$ mbar) for 24 hours with the liquid remaining in both reservoirs.
Also, indications were found that the gold gaskets at least partly create a strong bond with the reservoir walls. After detaching the wafers used in the vacuum experiments without epoxy underfill, parts of the reservoir wall were broken out and remained attached to the gold gaskets, as illustrated in Figure 6.7.

The epoxy was found to cause tensile stresses that result in a permanent vertical pressure on the gold gaskets, which keeps them in close contact with the reservoir walls. However, the underfill did not distribute over the full wafer and many air-pockets were trapped in the epoxy. Nevertheless, from the sealed reservoirs only 32% leaked their liquid after five years of shelf storage.

6.5. Gas sensor package

The packaging of gas sensors is in general a complicated matter. For one, the gas exchange cannot be impeded in a way that would affect the gas sensor performance. This requires sufficient exposure of the sensing structure toward the environment. At the same time, the sensing structure must be protected from the environment, which requires the exact opposite than exposure to it. In the case of the dye-based photonic gas sensor discussed here, the packaging requirements are extremely restrictive because the dye
material was still in development, and only little information on its characteristics was available.

6.5.1. Description of the gas sensor

The gas sensor is based on the interaction of dye molecules with NO\textsubscript{2} gas molecules that causes a detectable change in the dye fluorescence. The novelties of this sensor are the sensing dye thin-films that can now be plasma deposited, and thereby integrated and homogeneously distributed in a cross-linked polymer matrix without agglomeration of the dyes. In the following only the NO\textsubscript{2} detection is discussed although these polymer thin-films were also used for the detection of UV radiation within the project and can even be used for temperature detection [296–299].

The sensor layout is illustrated in Figure 6.8. A vertical resonant cavity consisting of alternating SiO\textsubscript{2}/Si\textsubscript{3}N\textsubscript{4} layers is used to filter the sensor signal. Perylene dye thin-films for NO\textsubscript{2} sensing are deposited by remote plasma deposition of Perylene dye and Adamantane precursor molecules on the 100 mm diameter glass wafer, containing the vertical resonant cavities. Upon UV light excitation, the dye thin-film emits fluorescent light, which is filtered by the vertical resonant cavities and guided through the glass substrate to the outer chip edges. The dye thin-films allow for detection of NO\textsubscript{2} concentrations as low as 0.5 ppm in air, at room temperature, within a few minutes [300].
6.5.2. Package requirements

The requirements on the package for this sensor are manifold. The photonic structures need to be protected from mechanical impact and from dust particles in the air, with the goal to filter all particles that are larger than 500 nm in diameter. At the same time, the package must not infringe the gas exchange at the sensor surface, such that the sensor performance is not altered. A for visible light transparent package is required to allow external excitation of the sensor. The sensing dyes are heat-sensitive and it has been observed that polymers and plastics in proximity to the gas sensor tend to deplete the gas analyte and disturb the measurement [301]. A mild packaging method close to room-temperature and with minimal interaction with the dyes is therefore required.

6.5.3. Package design

Based on the results of the experiments with packaging liquids, discussed in section 6.4, a wafer-level package for the dye-cladded, photonic NO\textsubscript{2} gas sensors was designed, as illustrated in Figure 6.9. The gas sensing dye-cladded photonic structures are situated on the bottom wafer, indicated by the red circular area. The package is designed in such a way that all machining is done on the lid wafer, to avoid influencing the dyes on the sensing wafer. The lid is a glass wafer with through-holes, which serve as gas inlets. Each die contains a circular gold gasket and concentrically arranged inner pillars. The gold gasket is used as a barrier and prevents the epoxy underfill from penetrating into the sensing cavity. The pillars are part of the filter mechanism which is described in the next paragraph. This gas sensor application does not require fully hermetic sealing; it is sufficient to restrict the diffusion of gas from the cavity toward the epoxy underfill to avoid gas analyte depletion within the sensing cavity. A mating gold structure on the sensing wafer as for the sealing of liquids is therefore not required. The gaskets and the pillars define the gap distance between the bottom and the top wafer after assembly and thereby the cavity height around the sensing structures.

The wafer-level package features a three stage air filter mechanism that allows gas diffusion toward the sensing structures, while filtering out particles down to a size of about 500 nm. The first filter stage is realized by the gas inlets in the lid wafer, having dimensions of 500 × 1000 µm\textsuperscript{2}. The second filter stage is realized by the gap length of 2 µm between the bottom and top wafer, which is about 2 µm after assembly. The third filter stage is formed by the closely spaced pillars that are radially arranged around the sensing surface with 8 µm pitches and 4 µm diameter before assembly. After assembly, the space in between these pillars is about 500 nm, as illustrated in Figure 6.10. This small distance between the sensing wafer and the lid wafer after assembly ensures a small cavity volume and therefore good gas exchange performance. FEM simulations, illustrated in Figure 6.11, showed a package gas exchange response time of only a few seconds, which is more than an order of magnitude faster than the response of the dye thin-films.
Figure 6.9: Exploded view of the gas sensor package (upper) and the assembled package with applied epoxy underfill (lower).

Figure 6.10: Filter pillars before and after plastic deformation.
6.5.4. Bubble-free epoxy underfill application

A novel bubble-free epoxy underfill application method is performed at atmospheric pressure, using microfluidic channels for epoxy distribution and capillary filling. The epoxy distribution channels solve two major challenges. The first challenge is the distribution of underfill over the full 100 mm diameter wafer pair by capillary forces. The capillary action of a viscous flow in between two parallel-plate surfaces is described by

\[ t = \frac{3\mu L^2}{h \gamma \cos \theta} \]  \hspace{1cm} [6.1]

where \( t \) is the time, \( \mu \) is the absolute viscosity of the fluid, \( L \) is the traveling distance, \( h \) is the gap between the wafers, \( \gamma \) is the surface tension, and \( \theta \) is the contact angle of the epoxy. The available time for filling the wafer gap is limited by the progressive polymerization level of the epoxy. To achieve a faster filling, the wafer gap should therefore be increased, but at the same time, the wafer gap must be small to obtain a small volume of the sensing cavity for good gas exchange performance. Another possibility to decrease the filling time is to use low viscous epoxy underfill. An epoxy with the required viscosity to fill the gap over the whole 100 mm wafer length, without microfluidic channels, is not available. The microfluidic channels, with their larger geometric dimensions, transport the epoxy
underfill across the 100 mm wafer, from where it penetrates into the 2 µm wafer gap. Now, only a relatively small length (half the distance between two neighboring channels) needs to be filled with epoxy in the constrained 2 µm gap region. This allows the use of epoxy underfill with higher viscosity. The second challenge is to prevent bubble formation during the epoxy filling. This is solved by the active routing of the epoxy underfill in the microfluidic channels, as illustrated in Figure 6.12. It allows pushing the air in between the wafers away from the sensing cavities and toward the space in the center between neighboring cavities where a venting hole allows the escape of the air.

6.5.5. Fabrication of the gas sensor package

The fabrication of the glass lid wafer starts with etching through holes for the gas inlets and venting holes using sandblasting. The microfluidic channels are then etched on the same side of the glass wafer, which holds the gold gaskets that are subsequently fabricated, using gold electroplating with the fabrication sequence described in section 6.4.1.
Figure 6.13: Schematic drawing of the lid wafer with open microfluidic channels for the distribution of the epoxy across the wafer.

Figure 6.14: Packaged and diced photonic gas sensor.
6.5.6. Assembly

Figure 6.13 illustrates the lid wafer, including the microfluidic channels, the epoxy distribution reservoir, into which the epoxy underfill is dispensed, and the venting holes that allow the escape of air during the epoxy filling. The lid wafer is aligned to the sensing wafer and then loaded into a wafer bonder. By applying a tool pressure, the gold gaskets and filter pillars are plastically deformed and get thereby into close contact with the sensing wafer surface. Epoxy underfill is dispensed into the distribution reservoir. The epoxy fills the microfluidic channels and penetrates from there into the narrow gap between the wafers. The wafer stack is left in the bond chamber with applied pressure, until the epoxy underfill is fully cured, and a strong joint between the wafers is achieved. The diced and packaged gas sensor chip is shown in Figure 6.14. It has been successfully implemented into a measurement system that was used for the monitoring of NO₂ concentrations in a car traffic tunnel, which is detailed in Paper 6.

6.6. Discussion

A novel room-temperature wafer-level packaging method based on a hybrid wafer-bonding scheme, using a combination of metal compression bonding and adhesive bonding, was developed. The packaging method was successfully applied for the wafer-level encapsulation of liquids and for the packaging of a photonic gas sensor.

In the case of liquid sealing the major failure mode was identified as insufficient lapping of the gold reservoir walls. The lapping was necessary because the plated gold structures used for the reservoirs had a rough surface. If the reservoirs are instead etched into the wafer, the deposited gold film on the reservoir wafer can be considerably thinner. Gold sputter deposition or evaporation in combination with a lift-off process can then be considered, making the lapping process unnecessary. Also, the use of higher gold gaskets might solve the problem.

With the designs presented in this work, the resulting wafer gap after assembly depends on the surface area of the gold gaskets and the bond pressure that is applied to the wafer stack. A more defined wafer gap can be achieved by utilizing stand-off structures on the lid wafer.

We have used room-temperature curable epoxy underfill in both examples of this method. The epoxy underfill is a central component of the package, as it provides the mechanical stability to the package together with a permanent compressive stress on the gold gaskets. However, curing of the epoxy at room-temperature is a lengthy process in which the wafers occupy the wafer bonder. To accelerate this process, several possibilities are feasible. The temperature during curing can be increased if the application allows this. As the curing rate of an epoxy shows an Arrhenius dependence on the temperature, a small
temperature increase already shortens the required curing time drastically [303]. Another possibility that may be viable is the early unloading of the wafer stack from the wafer bonder, i.e. before a high curing level has been reached. The solidification of the epoxy is a gradual process and a degree of polymerization that allows the unloading of the wafer bonder is likely reached before full curing. A considerable process speed-up can also be achieved with UV-curable epoxy in applications that allow this type of energetic radiation.
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7 Conclusion

In this thesis the fabrication of micro-electromechanical system devices under restrictive processing conditions was investigated.

The first part of the thesis investigated heterogeneous 3-D integration based on adhesive wafer bonding. This technology allows the use of high performance materials, such as monocrystalline silicon, on top of substrates containing CMOS driving electronics, which was shown for the fabrication of three different types of MEMS spatial light modulators made of perfectly elastic monocrystalline silicon.

In particular, a large scale micromirror array consisting of segmented, piston-type micromirrors with a large electrode gap for adaptive optics applications was shown. This spatial light modulator was built on CMOS dummy wafers in a CMOS compatible low temperature processing scheme, employing a polymer spacer and electroless nickel plating.

For the first time, a very large scale micromirror array from monocrystalline silicon with one million tilting micromirrors was integrated on fully functional CMOS driving electronics for maskwriting applications.

The first heterogeneous integration of two functional monocrystalline silicon material layers has been presented for the fabrication of large-scale, hidden-hinge micromirror arrays for adaptive optics applications.

In the second part of this thesis, a novel packaging method based on a hybrid bonding scheme was developed. It allows the room-temperature wafer-level packaging of heat sensitive devices. The method was demonstrated for the wafer-level hermetic sealing of liquids and for packaging an optical gas sensor.
Summary of Appended Papers

**Paper 1:** Wafer bonding with nano-imprint resists as sacrificial adhesive for fabrication of silicon-on-integrated-circuit (SOIC) wafers in 3-D integration of MEMS and ICs

In this paper, we present the use of thermosetting nano-imprint resists in adhesive wafer bonding. The presented wafer bonding process is suitable for heterogeneous three-dimensional (3-D) integration of microelectromechanical systems (MEMS) and integrated circuits (ICs). Detailed adhesive bonding process parameters are presented to achieve void-free, well-defined and uniform wafer bonding interfaces. Experiments have been performed to optimize the thickness control and uniformity of the nano-imprint resist layer in between the bonded wafers. In contrast to established polymer adhesives, such as BCB, nano-imprint resists as adhesives for wafer-to-wafer bonding are specifically suitable if the adhesive is intended as sacrificial material. This is often the case, e.g., in fabrication of silicon-on-integrated-circuit (SOIC) wafers for 3-D integration of MEMS membrane structures on top of IC wafers. Such IC integrated MEMS includes, e.g., micro-mirror arrays, infrared bolometer arrays, resonators, capacitive inertial sensors, pressure sensors and microphones.
**Paper 2: Drift-Free Micromirror Arrays Made of Monocrystalline Silicon for Adaptive Optics Applications**

In this paper, we report on the heterogeneous integration of monocrystalline silicon membranes for the fabrication of large segmented micromirror arrays for adaptive optics applications. The design relies on a one-level architecture with mirrors and suspension formed within the same material, employing a large actuator gap height of up to 5.1 μm to allow for a piston-type mirror deflection of up to 1600 nm. Choosing monocrystalline silicon as actuator and mirror material, we demonstrate a completely drift-free operation capability. Furthermore, we investigate stress effects that degrade the mirror topography, and we show that the stress originates from the donor silicon-on-insulator wafer. The novel heterogeneous integration strategy used in this work is capable of reducing this stress to a large extent.

**Paper 3: One-Megapixel Monocrystalline-Silicon Micromirror Array on CMOS Driving Electronics Manufactured With Very Large-Scale Heterogeneous Integration**

In this paper, we demonstrate the first high-resolution spatial-light-modulator chip with one million tilting micromirrors made of monocrystalline silicon on analog high-voltage complementary metal-oxide-semiconductor driving electronics. This device, as result of a feasibility study, shows good optical and excellent mechanical properties. The micromirrors exhibit excellent surface properties, with a surface roughness below 1 nm root mean square. Actuated micromirrors show no imprinting behavior and operate drift free. Very large-scale heterogeneous integration was used to fabricate the micromirror arrays. The detailed fabrication process is presented in this paper, together with a characterization of the SLM devices. Large arrays of individually controllable micromirrors are the enabling component in high-performance mask-writing systems and promising for high throughput deep-ultraviolet maskless lithography systems. The adoption of new materials with enhanced characteristics is critical in meeting the challenging demands with regard to surface quality and operation stability in the future. Very large-scale heterogeneous integration may enable virtually any solid-state material to be integrated together with CMOS electronics.
Paper 4: Heterogeneous 3-D Integration of Hidden-Hinge Micromirror-Arrays Consisting of Two Layers of Monocrystalline Silicon

We present a CMOS compatible heterogeneous 3-D integration process that allows the integration of two monocrystalline silicon layers on top of CMOS control electronics. With this process we demonstrate the fabrication of hidden hinge micromirror arrays from monocrystalline silicon for adaptive optics applications. The piston type micromirror arrays have the flexures underneath the mirror plates on separate silicon layers. Arrays of $48 \times 48$ mirror elements with an air-gap between mirror and address electrode of $10 \, \mu m$ were fabricated. The mirrors were found to be drift-free and showed no imprinting. A maximum electrostatic mirror displacement of $3 \, \mu m$ is demonstrated.


This paper reports on a novel wafer-level packaging method employing gold gaskets and an epoxy underfill. The packaging is done at room-temperature and atmospheric pressure. The mild packaging conditions allow the encapsulation of sensitive devices. The method is demonstrated for two applications; the wafer-level encapsulation of a liquid and the wafer-level packaging of a photonic gas sensor containing heat sensitive dye-films.

Paper 6: A Wafer-scale, Dye-based, Photonic Sensing System

We report on dye-based photonic sensing chips that are fabricated and packaged at wafer-scale. The demonstrated dye-based photonic sensor chips include an environmental NO$_2$ sensor and a sunlight ultraviolet light (UV) A+B sensor. These systems integrate for the first time luminescent organic nanocomposite thin-films deposited by plasma technology as active sensing elements. The luminescent signal of the thin-films responds to the changes in the environment and is selectively filtered by a photonic structure consisting of a Fabry-Perot cavity that also supports the thin-films. Thus, the photonic sensor system integrates all the structures required for detection, including a sensing element and a photonic transducer selectively tuning the signal that is bearing the information. The sensor system is manufactured at wafer-scale, which makes the technology viable for industrial up-scaling. Several prototype photonic sensor systems have been fabricated and tested in real scenarios.
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