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A Passive UHF-RFID Tag with Inkjet-Printed Electrochromic Paper Display

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Abstract—**In this paper, an inkjet-printed electrochromic (EC) paper display integrated with passive UHF-RFID tag is introduced as a solution for passive electronic shelf labels (ESL). To address the system challenges of the limited power budget of passive UHF-RFID tags and the material aging of EC display, a feedback comparator integrated digital display driver is proposed based on the study of electrochromic, bi-stable and aging features of the EC display. Modularized baseband with different enable conditions and clock domains is implemented in the system design level. Moreover, to maintain the system functions when the input power is lower than the display refresh power, a duty-cycled power management unit (PMU) is activated to reduce the load current during energy scavenging and drive the display in short intervals, enabling the fast charging of the voltage rectifier and the correct output of the regulated supply for the core circuit. The design is fabricated in a 0.18-um CMOS process with an area of 2.25 mm^2. Fed with EPC C1G2 protocol write command, experiments demonstrate correct refresh of EC display with 4 cm^2 effective area. System sensitivity at the antenna reference point is basically immune to the display load. Further improvements can be achieved after careful chip-to-antenna impedance matching and PMU efficiency optimization.**

Keywords—*electrochromic display, bi-stability, aging, passive UHF-RFID, feedback comparator, duty-cycled power management*

I. INTRODUCTION

By substituting a paper label with an easy-integrated wireless display tag, an electronic shelf label (ESL) enables automatic information update via radio frequency (RF) communications. One of the challenges impeding its market blooming is the cost limitation due to complex display driver and battery maintenance.

Most current ESLs operate in 2.4-GHz industrial, scientific and medical (ISM) radio band for RF communication due to smaller antenna size and higher data rate [1-5]. In comparison, smaller path loss and higher tag receivable power in UHF band can be more attractive for ESLs. Additionally, RFID transceiver can benefit from simpler structure and less power consumption by non-coherent detection and half-duplexed backscattering. Moreover, RFID rectifiers can harvest energy from input RF power and spare the battery integration for simple display tags. Data rate of UHF band is lower than that of the 2.4-GHz band but still acceptable for the ESL applications which require only a few display updates per day.

A few existing ESLs integrate newly-developed electronic paper display (EPD) of electro-phoretic (EP) or cholesteric-LCD (Ch-LCD) technology [1-4, 7]. EPD is the technology that resembles ordinary ink on paper by characteristics of ambient-light reflectivity, substrate flexibility, material printability and bi-stability. However, EP and Ch-LCD technologies demand driving voltages higher than 30 V [8-16], complicating the driving circuits by analog charge pumps.

In this paper, an inkjet-printed electrochromic (EC) display integrated 900-MHz passive UHF RFID tag is designed. Developed by Acreo Paper Display, EC display consists of an active electrode (pixel) and a counter electrode, both covered by a solid electrolyte as shown in Fig. 1. The electrodes which serve as the electrochromic material are made from PEDOT:PSS. The active voltage can be as low as 1.5V [11], enabling direct application of digital display driver. However, material aging of EC display is far more severe than that of EP and Ch-LCD displays, thus a feedback comparator is designed to control the timing of the digital driver. A modularized baseband is also designed in the system. Although the average display updating power has been low, the transient power over hundreds of microwatt per square centimeter surpasses the driving ability of conventional passive UHF-RFID tags when operating over applicable distance, resulting in the inevitable integration of batteries in the existing ESLs. Therefore, a duty-cycled power management unit is implemented to maintain enough power for the system when display starts refreshing.

This paper is organized by starting with the analysis of EC display. Following that is the system architecture with the
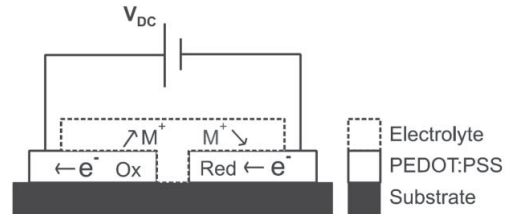

Fig. 1. The architecture of a lateral EC display cell. In the positive electrode PEDOT becomes oxidized, while in the negative electrode PEDOT is switched to the dark blue colored reduced state [11]

digital workflow. Block implementations of display driver and duty-cycled PMU, as well as experimental results are discussed subsequently.

II. INKJET-PRINTED ELETROCHROMIC DISPLAY

EC display parameters of switching energy, transient switching power and threshold voltage (Vth) during retention period are extracted as references for the system design. Switching energy is the charging energy that switches the display to full color gradient. Threshold voltage is the discharging voltage when the display returns to the default transparent color after disconnecting from supplies for a certain retention period. Measurement values of the parameters are listed in table 1.

A. Switching Energy and Trasient Power

Referring to the equivalent circuit structure of EC display extracted in [17], it is energy that switches display from the transparent oxidized state to the blue-colored reduced state, and vice versa. The switching energy demanded from external supplies is in proportional to display area and can be obtained by integrating the time-variant charging currents before the switching time as shown in Fig. 2. The display is supplied by a 1.8V DC source, and the current samples are recorded by Labview-controlled Keithley 2400.

For display cells with 10mm^2 effective area, the switching energy is around 112uJ. The switching energy can be converted to the commonly-mentioned driving voltage by $C*V^2$, where C is the equivalent capacitor in proportional to area. From the viewpoint of display driver design, the energy can also be represented by the switching time in counter-proportional to the circuit driving ability. The transient

TABLE I. ELECTROCHROMIC PARAMETERS OF EC DISPLAY

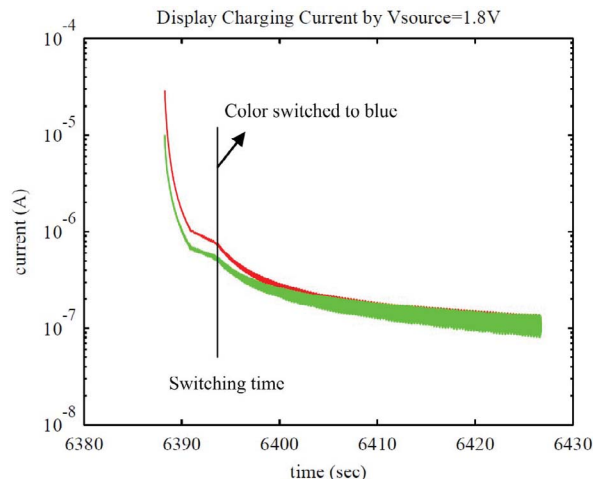| Switching energy	500uJ/cm²
Peak switching power	400uW/cm²
Threshold voltage	100mV~200mV

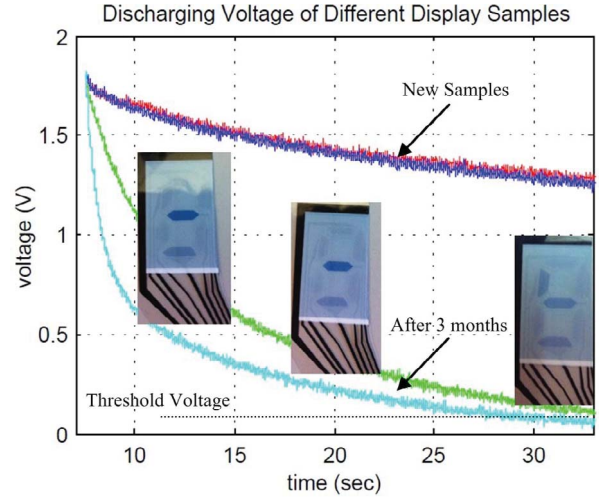Fig. 2. Measured charging currents of two 10mm^2 samples

Fig. 3. The variation of discharging speed of 2 samples over 3 months, and color gradient (of the middle segment) VS voltage (of the green curve).

switching powers are also obtained by the sampled currents with a peak value around 40uW for 10mm^2 samples.

B. Threshold Voltage and Material Aging

Fig. 3 shows the display color versus discharging voltage (referred to the green curve voltage), and discharging voltage versus retention time of two display samples over 3 months. A 10-Mohm resistor has been connected in serial with the oscilloscope probe to reduce the extra discharging. The discharging speed varies significantly yet the threshold voltage at which the color completely fades out does not, indicating that the threshold voltage instead of the retention time can be utilized in the driver design to solve the aging problem. From the viewpoint of the equivalent circuit [17], the equivalent resistors vary more than the capacitor. Although the charging time also varies a lot as illustrated in Fig. 2, it can be defined by the maximal experiment value because there is hardly any current drawn from the driver once the display is fully charged.

III. SYSTEM ARCHITECTURE AND WORKFLOW

A. System Architecture

Fig. 4 shows the system architecture of the display tag. The power management unit (PMU) implements a duty-cycled structure based on the design in [18] to improve the system sensitivity when the display is refreshed. Two voltage sensors (Vsen) switch on and off two low-drop-out (LDO) regulators according to the rectified voltage over a storage capacitor. The regulators generate 1.2 V supply for the core circuit and 1.8 V for display output buffers when the chip is switched on. To avoid the transient responses of regulators and Vsen as well as to provide a reset signal for the baseband logics, a Power-on-reset (PoRST) block is implemented to generate a delayed pulse compared to the Vsen switch of the 1.2 V supply.

The display driver is interfaced with a passive-matrix display. When refreshing images, the addressed row is supplied
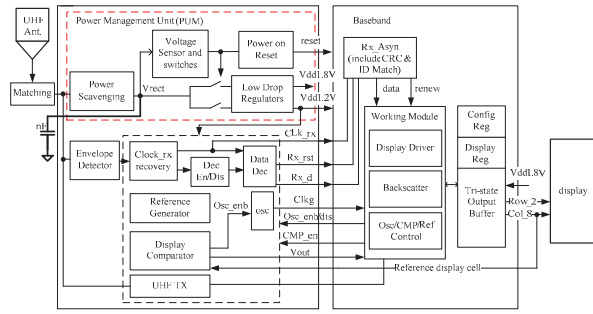
Fig. 4. Simplified system architecture

with ground and the other unaddressed rows in high-z state by disconnecting them with the tri-state buffers. Distinguished from those for conventional displays, it drives the display for a certain switching time, either accumulated during the duty-cycled mode in PMU or not, to represent the switching energy as discussed in section II, and stops driving when the time is reached. A feedback comparator monitors the discharging voltage over a reference display cell and restarts the driver when it drops below the threshold voltage which is measured around 100-200mV in section II.

The UHF reader broadcasts to the tag the configuration and display data conforming to the write command of EPC protocol by Amplitude-Shift Keying (ASK) modulation with pulse-interval encoding (PIE), and the tag backscatters its ID and display data by FM0-encoding when commanded. Both the data decoder and the decoder enable blocks utilize clock-free analog integrators which linearly charge capacitors when the RF envelope is high [19].

B. System Workflow

The system targets to constantly show data on EC display according to received data unless display disable command is transmitted from UHF reader. Thus the control logic and FSM differ from conventional RFID tag.

A modularized baseband is adopted and Fig. 5 illustrates the basic workflow. A controller monitors the working modules and the local oscillator. The controller consists of the analog blocks and the asynchronous digital receiving block (Rx_Asyn). The working modules comprise of the functional blocks as shown in the system architecture. The digital blocks
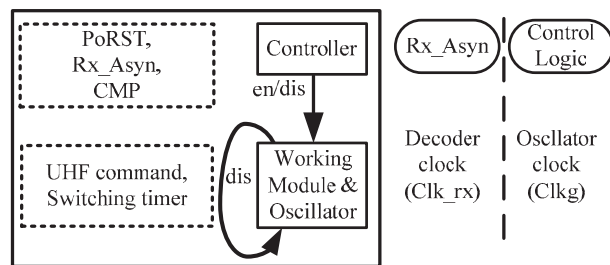

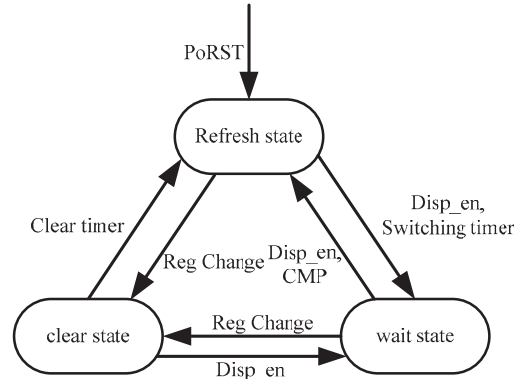Fig. 5. System workflow and clock domain division

Fig. 6. FSM of display driver

are divided into two clock domains with Rx_Asyn block triggered by the decoder clock and the working module by the oscillator clock. The working modules and the oscillator are enabled by three conditions: PoRST, the display feedback comparator (CMP) and the renew signal from Rx_Asyn block. They are disabled by two conditions: timer for the display switching time and the UHF command to idle the system. The Rx_Asyn block checks CRC-ID while shifting in the serially-decoded data, it also generates a renew signal once the check is correct and triggers the data to the baseband registers in this decoder clock period.

Responding to the transition conditions from the controller and the timers, the digital display driver operates in three different states: refresh, clear and wait. In refresh state, the driver operates similar to a conventional matrix-driver. In clear state, it connects all the rows with 1.8V buffer supply and columns with ground to remove the remained image originated from the bi-stability and the long retention time of EC display. In wait state, the driver disconnects from the display and the working modules go into idle mode until enabled by output from the CMP. A majority of power is saved by operating in wait state, taking advantage of the display bi-stability.

The finite state machine (FSM) is shown in Fig. 6. When the system is powered on, PoRST triggers the driver into refresh state. It keeps in this state when the UHF receiving starts because the enable signal for the display (Disp_en) has not been changed. If the received display data differs from that stored in the registers, it goes into clear state. The time for clearing the display is similar to the switching time, so the driver goes into refresh state once the clear time is accomplished. Similarly, it then goes into wait state when the switching time is reached. The output from the CMP triggers the transition from wait state to refresh state.

IV. BLOCK IMPLEMENTATION

A. Feedback Display Driver

The driving voltage of the inkjet-printed EC display can be 1.8V, therefore a digital driver is selected, saving not only the complexity and power from the otherwise required analog circuits but also the signal integrity problem when integrating

by the printed conductors with limited conductance in the future. FSM of the driver has been described in section III.

Since the inkjet-printed EC display suffers significant aging in retention time as illustrated in section II, a feedback display driver is implemented as shown in Fig.7. The voltage of a reference display cell whose correspondent register value is always one is compared by a Schmitt trigger with a low-to-high threshold voltage determined by the measurement described in section II. When the voltage drops below the threshold value, it outputs high to enable the digital driver. The reference column voltage will toggle to high immediately in ideal case, causing the holding time problem for the basic Schmitt trigger since its high-to-low threshold voltage is core supply voltage. In real case, however, it is delayed by the digital control links including the stabilizing time for the oscillator to restart. Fig. 8 shows the Monte-Carlo simulation results for 100 iterations of process variations and mismatches.

B. Duty-cycled Power Management Unit

Average power is reduced by the display driver discussed above; the transient power in the display refresh state, though, still challenges the power budget of a passive UHF-RFID tag.

For an example display with 1cm² effective area, the initial charging power is around -4dBm (400uW) according to Fig. 2, surpassing the driving ability of a passive tag over 3-meter distance according to Friis Equation. For conventional passive UHF-RFID tags with low-drop-out regulators (LDO), the charging time of the voltage rectifier (Vrect) becomes much longer, resulting in significant delays of the correct supply voltage for the core circuit before the display is fully charged,
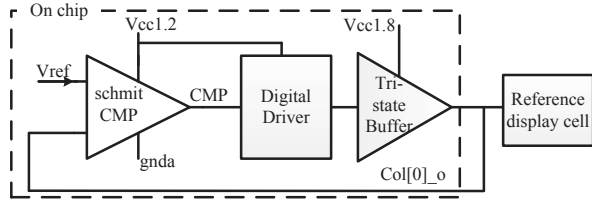
impairing the normal chip functions as illustrated in Fig. 9 (a).
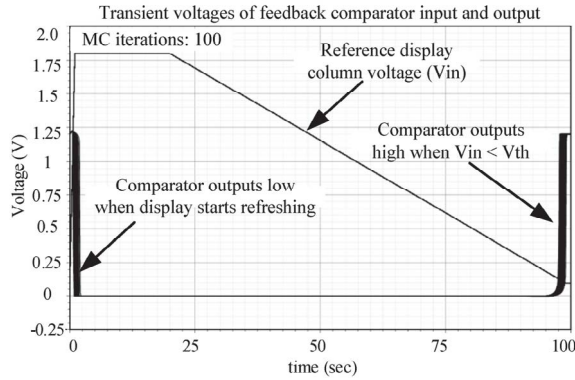
In order to power on the core circuit in parallel with display refreshing, a duty-cycled PMU based on the design in [18] is implemented. A Vsen for the 1.8 V LDO activates the display driving only when the rectified voltage in the storage capacitor surpasses a certain value (2.8 V in this system) and stops it when the voltage drops below another value (1.9 V). It reduces the load current during scavenging, enabling a fast charging of the Vrect and keeping its output above 1.9V when the input power surpasses that consumed by the Vrect and Vsen. Together with the PoRST block, a similar Vsen with different threshold rectified values of 1.8V and 1.3V is designed for the 1.2 V LDO to generate the reset signal for the digital control logics. Since the output of Vrect is kept higher than its threshold values, a stable 1.2 V supply voltage for the core circuit is maintained throughout the display refreshing. In the duty-cycled mode, the 1.8 V buffer supply voltage is powered on in short intervals and the total display switching energy is accumulated by the multiple charging cycles due to the low leakage current during display retention period. Transient simulation results of the display energy together with the voltage rectifier and two regulators are illustrated in Fig. 9 (b).

Fig. 9. (a) Simulation results with no voltage sensors
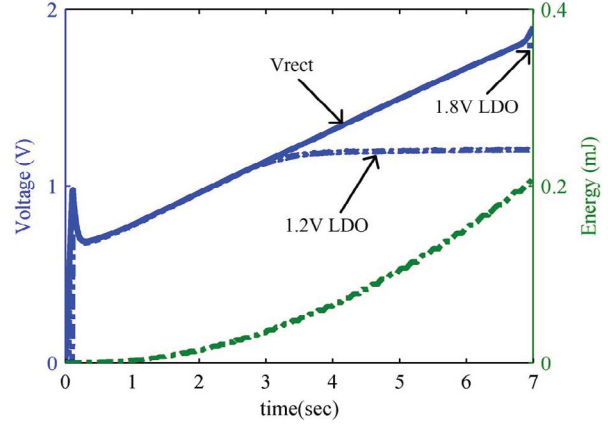

Fig. 7. Block diagram of display driver

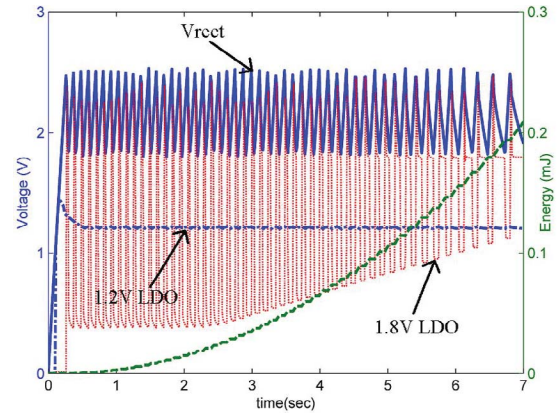Fig. 8. Monte-Carlo simulation results of display comparator

Fig. 9. (b) Simulation results with voltage sensors

Fig. 9. Voltages of the power management unit and energy of the display

The 1.8 V LDO does not drop to zero during the switching-off periods because of the effective voltage over the equivalent capacitor of the EC display. This voltage keeps increasing as the display energy accumulates and it stabilizes at 1.8 V when the display is fully charged.

V. EXPERIEMENT RESULTS AND DISCUSSION

The experiments are carried out with two seven-segment display samples with a total effective area around 4cm^2 (each segment is around 28mm^2). They are connected in a way to resemble the matrix structure of 7 columns and 2 rows.

Fig. 10 demonstrates the outputs of the 1.8 V and the 1.2 V LDO regulators during the display refresh state. In this experiment, the RF power less than the transient display refreshing power is fed into the system. In such cases, the Vsen switches on and off the output buffer supply in a duty-cycled mode, resulting in the periodic charging and discharging of the 1.8 V LDO. Meanwhile, since the Vsen stops the buffer supply when the rectified voltage drops to the pre-defined 1.9V, output of the Vrect is kept higher than the threshold values of the Vsen for the 1.2 V core supply. This results in a stable output of the 1.2 V and therefore the unimpaired chip functions throughout the display refreshing as shown in Fig. 10 (a) and (b). The voltages do not drop to zero during the chip charging when the Vsen is switched off because the display has an equivalent capacitor in serial with a resistor, and the LDO voltage indicates the effective voltage over the capacitor converted from the accumulated display energy. As the display energy increases, the effective voltage increases and so does the LDO voltages during the switching-off periods of the Vsen.

As demonstrated in Fig. 10 (b) and (d), the display switching time is less than the time to fully charge the display because the display switching energy is smaller than the total display charging energy. These results conform to the measured display charging energy shown in Fig. 2.

Since the 1.2 V core supply stays correct throughout the refresh state, the timer for the switching time keeps operating. However, the display energy is not charged continuously as discussed above. As a result, the timer must be programmed with a value more than that in the power-sufficient case. In this system, it is defined by $E_{disp}*\eta/P_{in}$. E_{disp} is the display switching energy, P_{in} is the input power and η is the PMU efficiency defined by the energy conversion efficiency of Vrect and the duty-cycle of Vsen.

Fig. 11 illustrates display state transitions after receiving the write command of EPC C1G2 protocol by the measured voltages of columns, row and decoder outputs. The RF-related experiments are measured by WareMaster 16G oscilloscope from Teledyne LeCroy. Since the display takes tens of seconds to tens of minutes to discharge from 1.8V according to Fig. 3, small capacitors of 4.7nF are instead connected at the outputs for a clearer illustration. Since the received display data as zoomed in Fig. 12 is different from the default all one values, the display goes into clear state first to remove the old image. When the clear time is achieved, it goes into refresh state, addressing one row after another, and in turn wait state after the switching time reaches. The oscillator stops working in wait state and the display is disconnected from the chip by
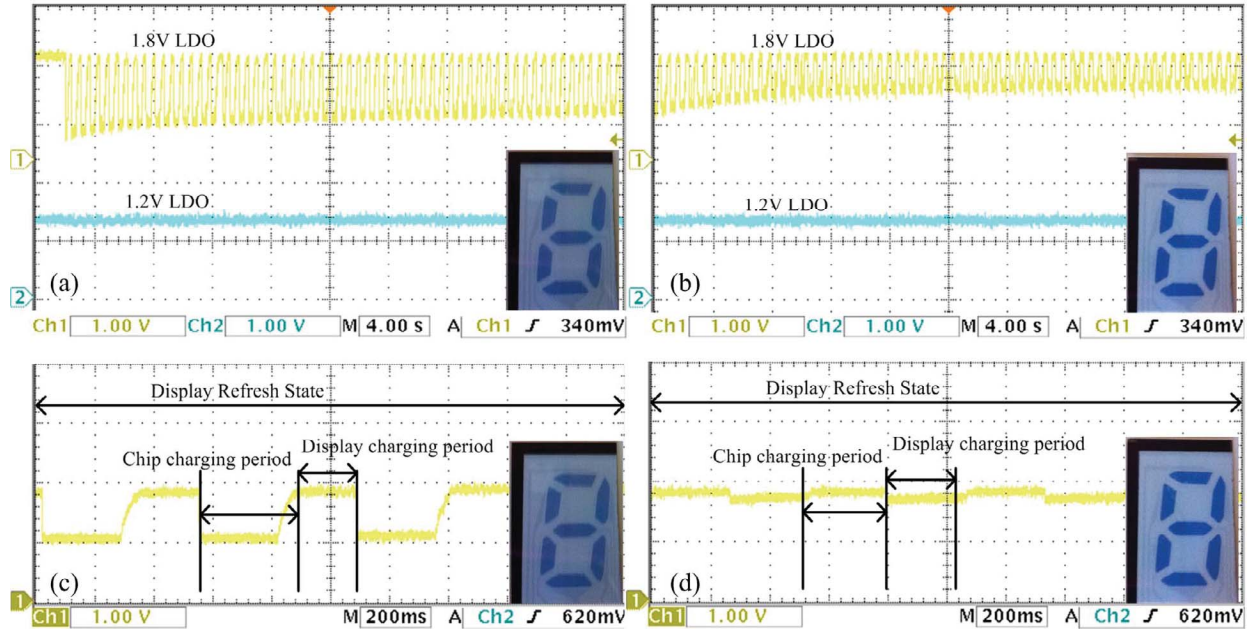

Fig. 10. Voltages of LDO1.2 and LDO1.8 during the display refresh state when input power is less than transient display refreshing power

(a) LDO voltages when the display starts to refresh (b) LDO voltages when the display is refreshed over 40 seconds and the display switching energy is approached (c) Zoomed-in 1.8 V LDO voltages during the chip and the display charging periods when display charging energy is not full (d) Zoomed-in 1.8 V LDO voltages during the chip and the display charging periods when display charging energy is approached full
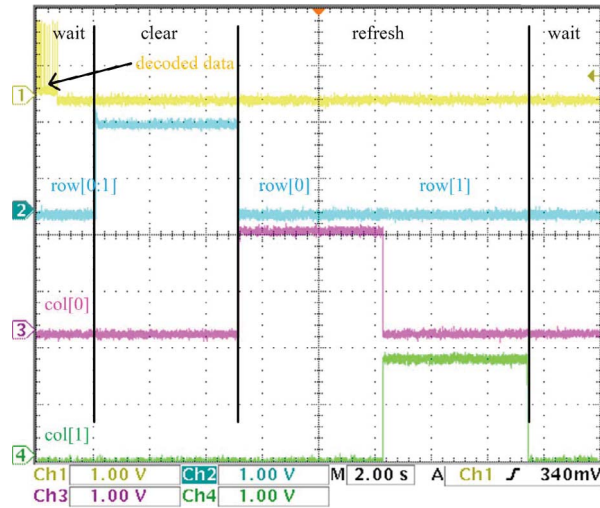
Fig. 11. Display state transitions after receiving a UHF command

high-z buffers, resulting in the column voltage drop. Input RF power in this test is more than that of the system consumption, so the clear and refresh operations are continuous rather than duty-cycled, and the time for both of them are four seconds.

VI. CONCLUSION

A passive UHF-RFID tag integrated with an inkjet-printed EC display is proposed in this paper for ESL applications. UHF-RFID radio band is adopted due to its less path loss and simpler transceiver structure. Low-voltage EC display is selected to reduce system power and analog design complexity. Electrochromic, bi-stable and aging performance of the display is studied. As a result, a feedback comparator integrated digital display driver is designed to take the advantages as well as to solve the material aging of EC display. A modularized baseband is designed to incorporate the display driver. Experimental results verify correct system state transitions and display driver outputs. To increase the system sensitivity, a duty-cycled PMU with voltage sensor switches on and off the supply for display buffers according to the rectified energy. Therefore, the display is charged with PMU driving ability and discharged with display retention current in a duty-cycled mode. Experimental results verify successful display color change when feeding the system with RF power less than the display refresh power. Further improvements of the input power level should be achieved after careful chip-to-antenna impedance matching and circuit level optimization of the PMU.

In conclusion, the passive UHF-RFID EC display tag offers a competitive system solution to the low-cost easy-integrated electronic shelf label. Future progress demands careful impedance matching and PMU efficiency optimization.
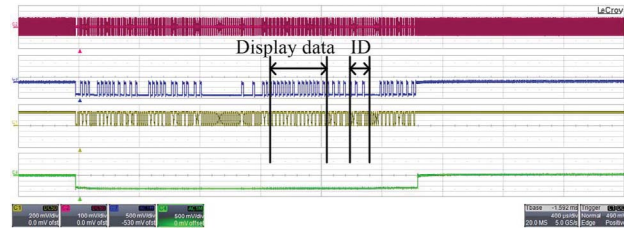

Fig. 12. The zoomed-in UHF command with ASK-PIE modulation and outputs of demodulator, decoder and decoder-enable

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