A Simple Controller for Displaying Restricted Patterns in RMS Responding LCDs

Vijaya P.Y, Reddappa D.J, T.N.Ruckmongathan.
Raman Research Institute, Bangalore. India

Abstract

A controller for displaying restricted patterns in passive matrix LCDs will be presented. Hardware complexity and the computational time for generating column signals are reduced considerably by using serial arithmetic directly from digitised samples and hence eliminating the frame buffer in multi-line addressing techniques.

Objective and Background

Liquid crystal displays are used in low cost portable instruments like Oscilloscopes and Logic Analysers. While active matrix LCDs could be used in such displays, passive matrix LCDs are an attractive option for reducing the cost of the display. A high contrast can be achieved in such devices by using restricted pattern addressing techniques [1,2]. Simple twisted nematic LCDs could be used in these applications since a high selection ratio and low supply voltage, which are independent of matrix size can be achieved by using a flicker free addressing technique proposed in SID'96 [2]. This technique is based on selecting all the rows in the matrix display simultaneously as in the case of active addressing [3]. However the hardware complexity of the column drivers is considerably lower than that of active addressing, since column waveforms have just few voltage levels.

Our objective was to reduce the computation required for generating the column waveforms and to avoid frame buffers that are necessary in multi-line addressing. This will result in a simple controller with minimal hardware complexity. The column signals are generated using a counter (as a serial adder). Number of clock cycles necessary for generating the column signal can be reduced to *w* clock cycles instead of *N* clock cycles. Wherein *w* is the number of waveforms that are displayed and *N* is the number of rows in the matrix display. The time required for generating the column signal is small since $w<<N$ in a display. This is feasible since the data for the background pixels is assigned to be zero in the techniques for displaying restricted patterns. The frame buffer usually present in the controllers based on multi-line addressing technique is eliminated by using the digitised samples of the waveform to be displayed directly for the generation of column signals.

PRBS –NC Technique

In Pseudo Random Binary Sequence - Negative Contrast (PRBS-NC) technique all the rows are simultaneously driven by waveforms which are *orthogonal* to each other. The column signals are the orthogonal transform of the data to be displayed. The column signal corresponding to each column is the dot product of data vector d_j and the row select pattern g_i This can be mathematically represented as $c_j = g_i.d_j$ Where d_j is the data vector (column in the bit-mapped image), with zeroes for background pixels. The data for the selected pixel which are points on the waveform is +1 and –1 for PRBS-NC and PRBS-PC respectively. g_i is the row select pattern (i^{th}column in the orthogonal matrix). c_j is the column signal for j^{th} column in the matrix LCD. Row select pattern g_i can take any one of the two values, +1 or –1, Hence c_j can take any one of the *(w+1)* possible values from *+w* to *-w*, resulting in *(w+1)* voltage levels.

The technique is best explained by taking a *7X8* matrix LCD, for displaying two waveforms, hence there are two selected pixels in each column.

i. Choose an orthogonal matrix, having number of rows greater than the number of rows in the matrix LCD. Since the matrix LCD shown in *figure 1* has seven rows, an orthogonal matrix of *8X8* is chosen. This orthogonal matrix derived from PRBS sequence is shown in *figure 2.*
ii. From the *figure 2* we can see that the first row of the orthogonal matrix has all +'s and the corresponding waveform is DC. Using rest of the seven waveforms result in a DC free operation of the display. The eight row select patterns corresponding to seven waveforms are also shown in the brackets in *figure 2.*
iii. Compute the column data for the all the columns in the display using the first row select pattern. It is given by: $c_j = g_1.d_j$. For example

$$c_1 = (0101000).(+++++++) = +2$$

Similarly the column data for remaining 7columns are (+2, +2, +2, +2, +2, +2, +2). A voltage of $+2v_c$ is applied to all the columns (since the column data for all the columns is +2). A voltage

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of $+v_r$ is applied to all the rows (since the row select pattern g_1 has all +'s).

iv. The step *iii* is repeated with rest of the seven row select patterns. Voltage $+v_r$ or $-v_r$ is applied to rows corresponding to + or – values in the row select pattern. Voltages of $+2v_c, 0v_c$ and $-2v_c$ are applied for the column data of $+2,0$ and -2 respectively. This will complete one frame. For example, the column data for the first column during a frame is given by $(+2,0,+2,-2,0,-2,0,0)$. Suitable frame rate has to be maintained to eliminate flicker.

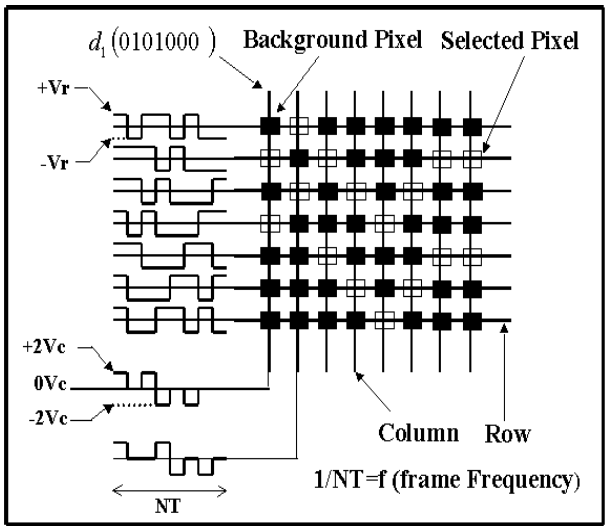

Figure 1: Row and Column Waveforms for driving 7X8 Matrix LCD having two selected pixels in each column *(w=2)*.

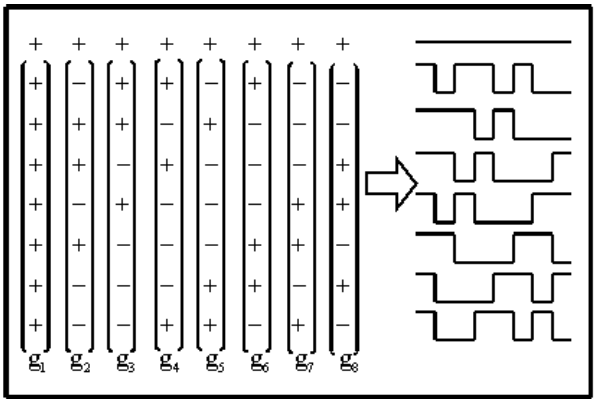

Figure 2: *8X8* Orthogonal matrix with its equivalent waveforms.

To have the maximum selection ratio the ratio of v_r by v_c should be made equal to $\sqrt{2}$ (since there are two selected pixels in each column) and the selection ratio is 1.8477[2].

Design And Implementation

Hardware complexity of the drive electronics depends considerably on the choice of the orthogonal functions. Simple orthogonal functions such as one derived from the Hadamard matrices, pseudo random binary sequences are preferred than those derived from sine and cosine functions. These orthogonal functions have just two values +1 or –1. Hence generation of row and column signals is simpler as compared to those derived from sine and cosine functions. Row and column waveforms get distorted due to the resistance of the indium tin oxide electrode and capacitance of the pixels. Error in the RMS voltage across the pixels due to this distortion in the waveform is same for all the pixels if the numbers of transitions in the addressing waveforms are equal. Hence brightness uniformity of pixels will be better if PRBS waveforms are used

The general block diagram for displaying waveforms on the LCD matrix display using PRBS-NC technique is shown in the *figure 3*.

In Orthogonal Matrix Memory one may store:

i. Only one sequence of the row select pattern. The successive row select patterns can be generated by shifting this row select pattern or by using a index counter while addressing.

ii. Entire orthogonal matrix, since the cost, size or availability of the memory is not a constraint. The controller is simpler when the entire orthogonal matrix is stored.

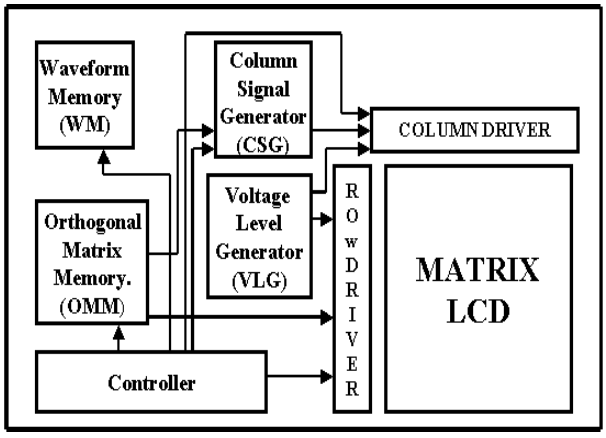

Figure 3: The General Block Diagram for Displaying waveforms on the LCD Matrix using PRBS-NC Technique

Since elements of the orthogonal matrix have only two values, they can be stored in the memory in the form of 0 and 1 instead of +1 and –1.

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The column signal generation is the most critical operation in the controller. One approach is to store the bit-mapped image in the memory. The row select pattern bits and data bits from the bit mapped memory may be serially fed to the AND gate for multiplication (since data is 0 or 1) and a serial adder may be used to sum these values. However to achieve a refresh rate of f in $(N \times M)$ matrix, the elements in the memory have to be accessed at a rate of $N^2 \times M \times f$, Which means the access time of the memory should be less than

$$t_{acc} < \frac{1}{N^2 \times M \times f} \qquad \textbf{Eqn 1}$$

In a matrix display of size *256X512* with refresh rate of 40Hz, we see that the elements in the memory have to be addressed at rate of 1342.10MHz. This results in access time of the memory to be less than 0.74 ns. Which is practically not feasible and also this is not preferable since a frame buffer is used to store the bit mapped image.

Alternatively one can store the waveform samples in the waveform memory. These samples can be used to address the corresponding bits in the row select pattern (for which data is 1), by adding these *w* values the column data can be generated. By this approach the memory has to be accessed at the rate of $N \times w \times M \times f$ (w is the number of selected pixels in each column), which means the access time should be less than

$$t_{acc} < \frac{1}{N \times w \times M \times f} \qquad \textbf{Eqn 2}$$

From equation 2 and 3 we can see that there is an increase of $\frac{N}{w}$ in access time of the memory, since w is very small as compared to N, this gain in the access time is substantial. This approach is used in the controller design. For example in a matrix of size *256X512* with *w=4* and refreshed at 40Hz the access time required is 47nsec.

The Row driver card and the column driver card were designed to apply necessary voltage levels to the LCD display. The Row driver card will apply $+v_r$ and $-v_r$ voltage levels for the row data of 0 and 1 respectively. The row drivers are realized using standard driver IC's such as HD44100.

The column driver card is designed to apply multiple voltage levels to the display. The column driver card shown in the *figure 4* take three bit column data and can apply 8 voltage levels to the display.

The following steps are employed in realising the addressing technique.

i. Generate the column data for a column and shift the column data to the column driver.
ii. Pick out the a bit from the row select pattern and shift it to row driver.
iii. Repeat the process until all the row select pattern is shifted to the row driver and all the column data is shifted to column driver.
iv. Apply the latch pulse, so that the necessary voltage levels are applied to the LCD matrix for duration T.
v. This process is repeated using all the row select pattern to complete one frame.
vi. A frame rate of 40 Hz is used in order to have a flicker free display.

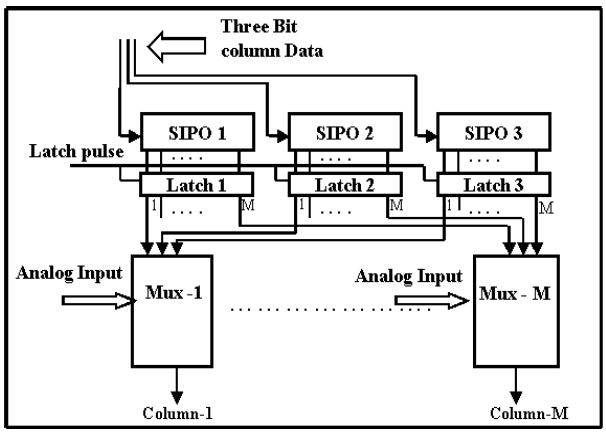

Figure 4: Schematic of a Column Driver Card

The Block Diagram of the controller is as shown in the *figure 5*. Each segment of the waveform memory contains scaled samples of a waveform. The orthogonal memory section consists of a EPROM and a multiplexer to have a memory organization of $N \times N \times 1$. The row select pattern counter is used to sequentially select different columns of the orthogonal matrix. Since the same orthogonal memory is used for row and column data an address multiplexer is used.

The *w* samples from waveform memory along with row select pattern counter is directly used to sequentially access *w* bits from the orthogonal memory. A 4-bit counter is used to generate column data. After computing each column data the address multiplexer is switched so that the address counter along with row select pattern counter can be used to access the row select pattern element from orthogonal memory. This row select pattern element and the column data in column counter are shifted to row and column driver cards respectively. It should be noted that 4 -bit counter is reset after shifting row and column data. A latch pulse is applied once all elements of row select pattern and

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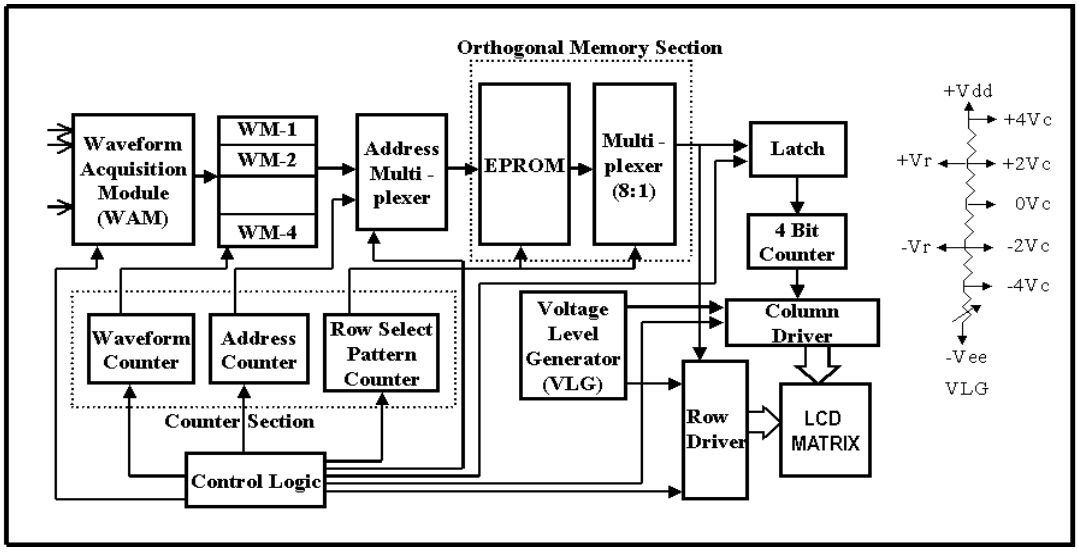

Figure 5: The detailed Block Diagram for displaying waveforms on screen.

column data for all columns are loaded to the row and column drivers respectively. The row select pattern counter is incremented so that the above process can be repeated for next row select pattern. All the row select patterns addressed once to form a frame. A frame rate of 40Hz is maintained to avoid flicker.

Results and Conclusion

The technique has been demonstrated by driving 64X64 displaying 4 waveforms. The RMS voltage across ON and OFF pixel Vs the supply voltage is shown in *figure 6*. For any given supply voltage the ratio of RMS voltage across on and off pixel is 1.414 Which is nearly equal to the theoretical value of $\sqrt{2}$. A good contrast can be achieved for a supply voltage as low as 7 volts. This supply voltage is independent of the matrix size.

The above approach results in a simple controller for displaying single valued function and is useful in instruments like Oscilloscopes, ECGs, and Logic analysers. The entire logic can be implemented in EPLD to reduce bulkiness.

Impact

While active matrix LCDs could be used in the Oscilloscopes and logic analyser, the use of passive matrix LCD, results in considerable reduction in the cost of the display. The high selection ratio achieved by the PRBS-NC technique[2] allows the use of TN LCDs rather than STN-LCDs. Use of TN LCDs in these applications has an added advantage of low response time as compared to STN-LCDs. Legends may also be displayed on the LCDs by adding dummy rows to the matrix as discussed in the reference 1. Passive matrix colour displays may also be driven using the same technique with out any compromise on the selection ratio. The very low supply voltage (independent of the matrix size) and flicker free operation are some of the additional advantages of using the PRBS-NC technique for driving the display.

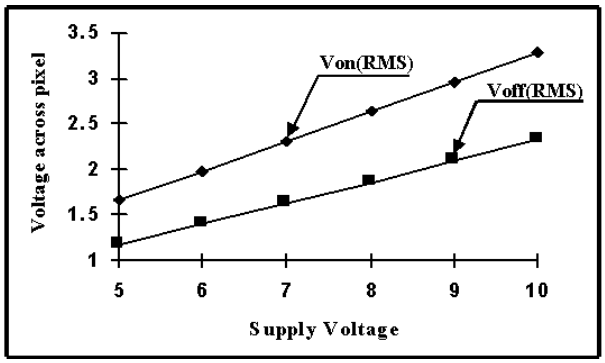

Figure 6: RMS voltage variation across the ON and OFF pixels with supply voltage.

References

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[2] Ruckmongathan T.N, "Flicker free Restricted - Pattern Addressing Technique with Low Supply Voltage", SID'96, 562-565.

[3] T.J.Scheffer and B.Clifton "Active addressing method for high video rate STN displays", SID'92, 228-231.

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