An Extended-Range Incremental CT ΣΔ ADC with Optimized Digital Filter

Julian Garcia$^1$ and Ana Rusu  
School of Information and Communication Technology (ICT)  
Royal Institute of Technology (KTH)  
SE-164 40 Kista, Sweden  
$^1$E-mail: julianmg@kth.se

Abstract

Extended range approach has been employed in discrete-time incremental sigma-delta analog-to-digital converters to reduce the number of cycles per conversion and therefore the power dissipation. In this work, extended range is combined with continuous-time filter implementation so as to reduce the integrators gain-bandwidth product requirement. The proposed architecture and mathematical analysis are presented using a 3rd order single-loop single-bit sigma-delta modulator as proof-of-concept. In order to overcome the analog-digital transfer function mismatches, an appropriate digital filter is designed using optimization tools. Behavioral simulations show that the proposed architecture with an optimized filter achieves 13.8 bits resolution with a 4 kSamples/sec sampling rate to comply with a high-resolution biomedical application.

Keywords

A/D conversion, extended-range sigma-delta ADC, continuous-time.

1. Introduction

Today analog-to-digital converters (ADCs) are increasingly being integrated into time-multiplexed low-power high-resolution biosensor applications, such as wearable and implantable biomedical systems [1–3]. While the required bandwidth is generally relaxed, the required resolution is, on the other hand, more stringent and varies from 12 to 16 bits, depending on each specific application. These requirements have been successfully covered by incremental sigma-delta (ΣΔ) [1, 4–6] and extended-range (ER) ΣΔ ADCs [7]. From a power consumption perspective, single-loop (SL) high-order ER-ΣΔ ADCs are especially attractive as they reduce the required number of cycles per conversion when compared to incremental counterparts. So far, discrete-time (DT) implementations have been the main focus in ER-ΣΔ ADCs while little attention has been paid to continuous-time (CT) counterparts. Continuous time implementation has been used, on the other hand, in traditional ΣΔ ADCs for low bandwidth applications [8], resulting in a power dissipation reduction. Such power reduction originates mainly from the relaxed slew rate and bandwidth requirements of the active blocks when compared to switch-capacitor counterparts. Moreover, even though a CT implementation has the potential of reducing the integrators gain-bandwidth product (GBW) requirement, its non-idealities also introduce new challenges. Particularly important for ER architectures is the degradation of the matching required between analog and digital transfer functions, which directly affects the ADC performance.

This work explores the challenges and opportunities of CT ER-ΣΔ ADCs by means of a test-case targeting a high-resolution (≥ 13 bits) clinical electro-encephalogram (EEG) recording system. Section 2 begins by analyzing the proposed test-case operation along with its theoretical performance. Section 3 investigates the sensitivity to critical non-idealities, such as excess loop delay (ELD), clock jitter, integrator’s coefficients deviation and finite’s amplifier GBW product, and discusses their effect on the analog and digital transfer function mismatch. Taken this into account, Section 4 proposes the design of an appropriate digital filter by using optimization tools so as to minimize such mismatches. A final test case, when both critical non-idealities and the novel filter are included, is presented in Section 5. Finally, Section 6 concludes the paper.

2. Proposed ER-ΣΔ ADC

ΣΔ ADCs differ from traditional ΣΔ ADCs in that their memory elements are reset every time a new conversion takes place. This provides a one-to-one mapping between input and output and makes the ΣΔ ADC suitable for conversion of time-multiplexed signals [1]. As shown on the shaded area of Figure 1, a new conversion begins by sampling the input signal $U(s)$ and resetting the states of both the ΣΔ modulator and the digital filter $H_{DF}(z)$. The input signal is then held for a period of $N/f_s$, while the ADC performs the conversion at $f_s$ frequency, where $N$ is the number of cycles per conversion and $f_s$ is the modulator’s sampling frequency. After $N$ cycles have passed, a valid result is obtained from the output of the digi-
Figure 2: Block diagram of the proposed SL CT ER-$I\Sigma\Delta$ ADC.

Figure 3: Simulated SNDR of ER-$I\Sigma\Delta$ (+) and $I\Sigma\Delta$ (□) ADC against theoretical SNDR derived from (5) of ER-$I\Sigma\Delta$ (+) and $I\Sigma\Delta$ (△) ADC vs. number of cycles ($N$). Input signal power: $P_{\text{sig}} = -6$ dBFS.

ADC at instant $N$, $x_3(N)$ is the sampled value of the 3rd integrator’s output at instant $N$, and $c_1$, $c_2$ and $c_3$ are also loop filter coefficients. As the extended range approach refines the quantization noise of the incremental ADC, $AD_{CER}$, its least-significant-bit (LSB) quantization error can be expressed as:

$$V_{\text{LSB,ER}} = \frac{V_{\text{LSB,1}}}{2^{M_{\text{EN}}}N^3}$$

where $B_{ER}$ is the number of bits in the extended range ADC, $AD_{CER}$, and $V_{\text{LSB,1}}$ is the LSB quantization error of the incremental ADC. $V_{\text{LSB,1}}$ is obtained assuming the maximum range for the output of the 3rd integrator equal to the maximum input full-scale value $[4]$, $\pm U_{FS}$, given by:

$$V_{\text{LSB,1}} = 2U_{FS}G_{X_3} = \frac{12U_{FS}}{b_1c_1c_2c_3N^3}$$

The effective number of bits (ENOB) for the ER-$I\Sigma\Delta$ ADC, $AD_{CER}$, when a differential input signal with amplitude

$$H_{DF}(z) = \left(\frac{1}{2} \left( 8\tau^2 \left( 1 - \frac{1}{z^{-2}} \right) - 4\tau + 1 \right) + \frac{1}{2} \left( 2\tau \left( 1 - \frac{1}{z^{-2}} \right) - 2 + \frac{1}{z^{-2}} \right) - \left( 1 - \frac{1}{z^{-2}} \right) \right) \frac{6a_1}{N^3b_1}$$

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±U_{\text{max}} \text{ is considered, can then be expressed as:}

\[ \text{ENOB}_{\text{ERI}} = \log_2 \left( \frac{2U_{\text{max}}}{V_{\text{LSB,ER}}} \right) \]

\[ = \log_2 \left( \frac{2U_{\text{max}}}{V_{\text{LSB,I}} \cdot 2^{B_{\text{ER}}}} \right) \]

(5)

where ENOB_{\text{I}} is the ENOB of the ADC_{\text{I}} and ENOB_{\text{ER}} is the ENOB of the ADC_{\text{ER}}. According to (5), the ENOB of the ADC_{\text{I}} is improved by B_{\text{ER}} bits when extended range is applied. In theory, this can be a significant improvement, depending on the resolution of the ADC_{\text{ER}}. In practice however, two factors will contribute to the degradation of such theoretical performance. The first factor originates from the assumption that the output of the third integrator is equal to the maximum input full-scale value while in reality it might be less than such value. As this assumption is considered when calculating the V_{\text{LSB,I}} value in (4) and the input range of the ADC_{\text{ER}}, it will affect both the performance of the IΣΔ and ER-IΣΔ ADC. With respect to IΣΔ ADC, its performance will be underestimated as the quantization noise is less than the one accounted by (4). On the other hand, the performance of the ER-IΣΔ ADC will be overestimated as the ADC_{\text{ER}} is not benefiting from its full dynamic range. These effects can be appreciated in Figure 3, where the signal-to-noise-plus-distortion-ratio (SNDR) performance of both the IΣΔ and the ER-IΣΔ ADCs were simulated while sweeping the number cycles N and compared against their theoretical SNDR derived from (5). The second factor that will affect the theoretical performance is the degradation due to non-idealities. This is critical for the optimum performance of the ADC and will be analyzed in detail in the following sections.

3. Nonideal behavior

As it can be seen from (1) and (2), the quantization error refinement depends on the matching between a digital and an analog transfer function. This type of requirement is also found in cascaded ΣΔ ADCs [12] and special attention has to be paid to the mismatch caused by CT non-idealities as it would cause a leakage of the modulator’s quantization noise to the output. In order to quantify the ADC performance degradation, MATLAB transient simulations have been performed while computing the SNDR of both the output of the ER-IΣΔ and the IΣΔ ADC, ADC_{\text{ER}} and ADC_{\text{I}} respectively, under different non-ideal conditions. The ADC was run for 40 cycles while using an 8-bit ADC_{\text{ER}} and a digital filter as described by (1). A mean lifetime value \( \tau = 1/25T_s \) was used in the feedback SCR-DAC when analyzing the sensitivity to process variations and to finite integrators GBW product. While simulations with \( \tau = 1/10T_s \) were added to the ELD and jitter analysis.

When considering the sensitivity to process variations, it has been assumed that the RC product would suffer the same spread [13]. As shown in Figure 4, the extended range implementation is, as expected, highly sensitive to coefficients variations and a tuning circuitry should be added in order keep the degradation between acceptable limits. It is also worth to notice the different sensitivity of incremental and extended range implementations.

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product as its performance would approach the incremental one. This reveals a severe drawback as it would directly impact the power consumption of the ER-ΣΔ ADC.

Similarly to half-return-to zero (HRZ) coding scheme, the SCR scheme is active during the 2nd half of the clock cycle. Therefore, as long as the quantizer delay is less than 0.5 $T_s$, the ELD will be generated by the DAC delay only. As it can be seen from Figure 6, although the extended range architecture is more sensitive to ELD than the incremental counterpart, by choosing an appropriate mean lifetime value it is possible to counteract the error injected by the DAC delay. As in the previous case, the degradation due to clock jitter can also be counteracted by using an appropriate mean lifetime value, as can be seen in Figure 7.

The results of this section show an increase in the sensitivity to critical non-idealities of the extended range approach when compared to the incremental counterpart. This was expected as the extended range implementation performance is highly dependent on the matching between analog and digital transfer functions and therefore highlights the need of careful filter design to counteract such mismatches.

4. Digital filter optimization

Although several optimal filters have been derived for DT IΣΔ ADCs [5, 15, 16], to the authors’ knowledge, the digital filter optimization for CT ER-ΣΔ ADCs has not been treated yet. In this section, optimization tools are employed as an alternative approach to design such filter so as to counteract analog-digital mismatches.

As the transfer function mismatches stem from different non-idealities affecting the modulator, it would be possible, in principle, to mathematically derive a digital filter to account for such divergences. The main drawback of this approach is that it becomes too complicated when going from system level to more refined abstraction levels such as block level or circuit level implementation. The following approach, on the other hand, could be directly applied by just running the optimization algorithm in each of the design steps.

The digital filter matching the ideal analog transfer function given in (1) is a sum of cascade of integrators which process $N$ samples coming from the ΣΔ modulator. This filter, when operates in transient mode, can instead be treated as an N-length finite impulse response (FIR) filter with the appropriate coefficients [17]. These coefficients can be obtained by computing
the N-length impulse response of the transfer function in (1) and, in a system-level model with no non-idealities included, they allow a maximum quantization error refinement. Put it in another way, if one would assume an “infinite” resolution ADC\textsubscript{ER} in such model (\(e_{QER}(n) = 0\)), this filter would allow a complete cancellation of the \(\Sigma\Delta\) ADC quantization error, thus obtaining, an “infinite” resolution at the output of the ER-\(\Sigma\Delta\) ADC. Once non-idealities are inserted into the system, either by adding them at system-level or by advancing to a more refined level of abstraction, the transfer function in (1) becomes less effective, degrading the quantization error refinement and, as a consequence, the performance of the ER-\(\Sigma\Delta\) ADC. So as to maximize the \(\Sigma\Delta\) ADC’s quantization error cancellation, this approach uses as objective the SNDR, assuming that a maximum SNDR will correspond to a maximum error refinement. Accordingly, the proposed filter uses the MATLAB optimization algorithm \textit{fmincon} [18] to find the optimum N coefficients of the FIR filter so as to minimize the \(1/\text{SNDR}\) value. Such algorithm attempts to find a constrained minimum of a scalar function, called the objective function, of several variables starting at an initial estimate. The coefficients obtained from the filter in (1) are then set as the initial estimate while the objective function calculates the SNDR of the filtered modulator’s stream and returns the \(1/\text{SNDR}\) value.

To validate the proposed filter, similar simulations as in Section 3 were performed to evaluate the ADC\textsubscript{ERI} output, with the exception of the sensitivity to clock jitter due to the random nature of this non-ideality. Moreover, the SNDR performance of the ADC\textsubscript{ERI} when the unoptimized filter derived from (1) is used has also been included for comparison.

As shown in Figure 8, the proposed filter can successfully counteract most of the degradation induced from the coefficients variations, obtaining up to 29 dB of SNDR improvement at \(\Delta_{C} = -30\%\). Although one can expect large deviations after physical implementation, the previous simulation highlights the possibility to compensate and even cancel the influence of such variations in the digital domain, as done in cascaded \(\Sigma\Delta\) modulators. Alternatively, this method can also be used in the circuit and physical level implementation to optimize the digital filter in order to account for discrepancies between different abstraction levels.

The effect of the optimized filter when considering the finite amplifier GBW product is presented in Figure 9. Contrary to the respective simulation shown in Section 3, now it is enough to use an amplifier GBW product close to \(f_s\) without suffering significant degradation. This represents a key feature for this architecture when compared to DT counterparts.

With respect to the ELD degradation, the proposed filter could only obtain marginal improvement, as depicted in Figure 10. The choice of the SCR-DAC mean lifetime value \(\tau\) therefore represents a key design parameter to fully benefit from the extended range approach, not only due to its sensitivity to ELD but also due to clock jitter. Although not treated in this paper, it may also be possible to counteract jitter and ELD degradations by using multibit feed-back DAC. This approach, however, would increase the complexity of the digital filter and may require an extra calibration circuitry to reduce the DAC mismatches.

5. Case study

To validate the proposed architecture, a test case for an EEG digital recording system in accordance with the International Federation of Clinical Neurophysiology (IFCN) standard [19] is presented. The proposed case uses the architecture proposed in Section 2 and targets 13-bits resolution and 4 kSamples/sec so as to process 8 channels at 500Hz. Practical values for all previous non-idealities have been included and the digital filter described in Section 4 has been used to counteract their impact. The SCR-DAC uses a mean lifetime value \(\tau = 1/25 T_s\) and a 5\% of \(T_s\) (312.5 ns) delay was considered for the ELD. Moreover, a finite GBW product equal to 3 \(f_s\) and a coefficient deviation of -10\% was assumed for the integrators. Finally, a clock having a jitter standard deviation of 0.1\% of \(T_s\) (6.25 ns) has also been included.

When the \(\Sigma\Delta\) modulator is running continuously, it achieves an SNDR of 63.5 dB @ -6 dBFS as shown in Figure 11. Similarly, Figure 12 depicts the power spectral density (PSD) of the ER-\(\Sigma\Delta\) ADC with the optimized and unoptimized digital filter. The proposed ADC can achieve 83 dB SNDR (13.8 bits) when running for 40 cycles and using an 8-bit ADC\textsubscript{ER}. A 13
dB increment with respect to the unoptimized filter case is obtained. For comparison, the same architecture would require around 80 cycles in incremental mode to achieve similar performance. By using the extended range approach, it is therefore possible to reduce the number of cycles by 50% which would also reduce the GBW product of the integrators by 50% when compared to the CT $\Sigma\Delta$ ADC. It is worth to notice that the 8-bit SAR ADC_{EE} would consume very little power with respect to the ADC_{I} as it runs at the decimated frequency $f_s/N$.

6. Conclusion

The extended range approach in high-order SL CT $\Sigma\Delta$ ADCs has been analyzed with the aid of a 3rd order $\Sigma\Delta$ modulator as example. Behavioral simulations showed the high sensitivity of this topology to critical non-idealities when compared to CT $\Sigma\Delta$ counterparts. As this sensitivity is mostly due to mismatches between the analog and digital transfer functions, a digital filter using optimization tools has been proposed to counteract their effect. This filter can effectively minimize the mismatches introduced by finite amplifier's GBW product as well as process variations. Simulation results show that the optimized digital filter can improve the ADC performance up to 13 dB when compared to the unoptimized filter case, further reducing the ADC's required number of cycles per conversion with respect to incremental counterparts.

7. References


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