Implementation of a Filter and Multiplier for Next Generation Transceivers

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Abstract

A new sub-sampling technology is presented to greatly lower the sampling frequency of the transceivers with wideband inputs. The innovation of the theory is the flexible selection and conversion of any single band out of a multiband spectrum. According to the theoretical work on a sub-sampling wideband receiver, such a technology enables demodulation of wideband inputs with a sampling frequency much lower than the carrier frequencies, and converts the band of interest to a low frequency band simultaneously. The purpose is to make it easier for the subsequent ADC to process a single band when applying a low-pass filter after the demodulation. The technology is also fit for the transmitter, which inversely converts wideband inputs to a high frequency band and make the band of interest located on the carrier frequency point.

Compared with traditional demodulation, we generate a waveform containing a multiple set of sinusoids instead of using a single local oscillator, and pass them through a carefully designed band-pass filter. The filter eliminates all the harmonics except the one located at the band of our interest. Then both the multiband inputs and the output of the filter are mixed by an analog multiplier. After such a process, the band we want is now converted to a low frequency.

The objective of this master thesis is verification and implementation of the principle in order to evaluate which best performance can be reached. The whole architecture is simulated and finally validated in circuit level using 90nm CMOS technology.
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1. Introduction

1.1. Nyquist sampling

The Shannon-Nyquist theorem [1], [2] which was originally stated by Harry Nyquist in 1928 and formulated by Claude E. Shannon in 1949 [3], has been the foundation of most architectures of ADC designs during the past six decades. The theorem [2] states that a signal $x(t)$ with the limited bandwidth $B$ can be perfectly reconstructed from uniform samples $x(nT)$ by a sinc function called Whittaker–Shannon interpolation formula [4], if the sampling rate is not less than $2B$. The bandwidth, called sampling rate of the Nyquist rate, is a lower bound for the sample rate for alias-free signal sampling. If no aliasing occurs after sampling, the sinc function represented by:

$$f(t) = \sum_{n=-\infty}^{\infty} x[n] \frac{\sin\pi(2Bt - n)}{\pi(2Bt - n)}$$

(1)

and a rectangle lowpass filter (LPF) in the frequency domain can be used to recover the original signal as well as eliminate higher repeated components caused by sampling. The sampled-data signal is usually further quantized by an Analog-to-Discrete-time (A/D) converter in the receiver to obtain a pure discrete-time signal (a binary signal consisting of bit ‘1’ or ‘0’) or a Discrete-time-to-Analog (D/A) converter in the transmitter to transform the signal back to the analog domain for transmission. Although a lot of different kinds of ADC/DAC designs are available by now, most of them still abide by the Shannon-Nyquist theorem, where sampling rate is at least twice the highest frequency of the input signal.

However, in practical communication, the information is modulated on a high carrier frequency in order to be transmitted for a long distance and for many channels. For example, GSM-900 uses 890–915 MHz for the uplink and 935–960 MHz for the downlink; WCDMA(UMTS) use 1920 -1980 MHz for the uplink and 2110 -2170 MHz for the downlink. The state-of-the-art transmission technology even enables signals modulated on a carrier frequency around tens of GHz [5]. Hence, when processing the signal, especially in receivers, such a high frequency of the input signal brings many difficulties on the design of ADC devices for sampling. Actually, none of the existing ADC device is able to reach such a high Nyquist rate due to technology limitations.

1.2. Conversional Receiver Architectures
Fig. 1. Three conventional receiver architectures: (a) Conventional dual-IF superheterodyne receiver architecture with two stages of down-conversion, (b) Homodyne receiver architecture, (c) Low-IF receiver architecture
The traditional solution in engineering to lower the required sampling rate is demodulation, namely multiplying the input by a local oscillator (LO) signal $f_{LO}$ that is lower or higher than or equal to the center frequency $f_c$ of the input signal, so that the band would be converted from the high frequency to a lower or zero frequency [6]. Fig. 1 shows three most used conventional receiver architectures [7]: a superheterodyne receiver architecture, a homodyne receiver architecture and an IF receiver architecture. The superheterodyne receiver mixes two frequencies and produce a beat frequency defined by the difference of the two. It translates the radio frequency signal to a low frequency band by two stages of down-conversion (dual-IF, IF stands for intermediate frequency) mixing. The homodyne receiver converts the signal to the baseband due to the absence of an IF stage between RF and baseband. Therefore, it is simpler than the superheterodyne receiver and prevented from the image, DC problems, etc. The IF receiver combines the advantages of both superheterodyne and homodyne receivers. The received RF signal is down-converted to IF by a LO, where the IF could be either one or two times the information bandwidth (in low-IF receivers) or arbitrary (in wideband-IF receivers) depending on the system specifications in terms of sensitivity and selectivity.

1.3. Bandpass Sampling (BPS)

Fig. 2. BPS receiver architecture

The common ground of these conventional receivers is that they need a LO which is a little higher/lower than or equal to the center frequency of the input band so as to obtain a low IF or a zero one. Otherwise, multiple stages of down-conversion have to be employed if the LO is lower. That means that the designers still have to generate a sinusoid with a frequency almost as high as the input radio frequency, or several sinusoids with lower frequencies for the usage of multiple stages. Therefore, in order to lower the frequency of the oscillator to be designed, a sampling
technology named Bandpass Sampling (BPS) [8] has been introduced. As Fig. 2 shows, compared with the down-conversion mixing, the input RF is now sampled at a low rate that is only slightly larger than twice the information bandwidth [9]. Since the information is band-limited at a rather high frequency, BPS can realize down-conversion through the intentional signal spectral folding. Thus, the whole band now can be obtained by using a LPF after sampling. BPS brings a great advantage in lowering the sampling rate, which results in easier real implementations and less power consumption.

However, in most cases, the received RF is a multiband signal. Therefore, different orders of Nyquist bands have to be selected and filtered out with a specific bandpass filter (BPF) after BPS in consideration of different users [10, 11]. If we want to further convert each band down to zero frequency so as to make the lowest sampling rate, that is twice the single bandwidth, available in the subsequent ADC devices, every band should be demodulated respectively with a corresponding IF. It results in much more extra cost in real implementations.

1.4. Motivations of the thesis

In this paper, we present a circuit-level prototype of a new sub-sampling system, which provides a good solution to the shortcoming of the traditional BPS. The theorem initially derives from an Xsampling system [12, 13], which is similar to BPS mentioned above, but brings a great improvement compared to BPS. Neither generating different LOs for each band for demodulation nor directly bandpass sampling the whole received wideband, the sub-sampling technology creates one multiple set of sinusoids for common use. The common series of sinusoids should be carefully adjusted so that for each of the input bands (assuming they are all Double-SideBand (DSB) signals), there is a sinusoid equal to the center frequency. Hence, in order to get the band of interest, we only need to eliminate all the other sinusoids except the one belonging to the target band. The elimination can be realized by a BPF. After mixing the new set of sinusoids with the input wideband signal, the band we want will be shifted to zero frequency. A LPF followed can filter out the remaining narrowbands and the standard low-rate ADCs can process the single band with the Nyquist rate. Since the BPF can be implemented as a discrete-time filter (DTF), its sampling rate can be designed much lower than the input carrier frequencies and we utilize a repeated passband to get the target sinusoid. The sinusoids after filtering will achieve “sub-sampling” for the input wideband information and no aliasing occurs.

The sub-sampling theorem has been verified by Matlab code [14]. This thesis presents the process and the results of the evaluation by Simulink and verification on 90nm CMOS technology. The simulation by Simulink further proves the principle by implementing the BPF and creating a signal flow graph in block-level. The implementation on circuit-level by Cadence is to test how good the performance of
the filter would reach, because the passband of a DTF suffers from an attenuation from harmonics due to the pulse shape of the output signal. The practical users should choose the appropriate passband depending on the gain they need. Our experiment is a demonstration of this sub-sampling technology and the result is limited by the bandwidths of the multiplier and the OTA in the filter. By using more advanced multipliers and OTAs, it can be scaled up to more interesting center frequencies.
2. Theoretical background

2.1. Sub-sampling principle

The sub-sampling strategy is aimed at sampling wideband sparse signals at sub-Nyquist rates with a multiband model. The proposed wideband receiver is shown by Fig. 3 [14], with an carrier-modulated bandpass signal which is represented as a DSB signal $x(t)$. We assume its Fourier transform $X(f)$, the number of the bands $N$ and the width of each band $B=1/T$. The carrier frequencies for each bands are $f_i$, $i = 1,2,3 \ldots N$. The periodic pulses

$$p(t) = \sum_n \delta(t - nT) \quad (2)$$

has a period of $T = 1/f_0$ and $\delta(t)$ is the Dirac delta function. The impulse response of the BPS is $h(t)$.

Then the theory of the whole sub-sampling can be done:

$$s(t) = p(t) \ast h(t) = \int h(t - \tau)p(\tau)d\tau$$

$$= \int h(t - \tau) \sum_{n} \delta(t - nT) \, d\tau = \sum_{n} h(t - nT) \quad (3)$$

After multiplying (2) with the input signal $x(t)$, we get the result of sub-sampling:

$$y(t) = x(t) \cdot s(t) = x(t) \sum_n h(t - nT). \quad (4)$$

The spectrum is given by the Fourier transform of $y(t)$.
\[ Y(f) = \int y(t)e^{-j2\pi ft}dt = \int \sum_n x(t)h(t-nT)e^{-j2\pi ft}dt. \quad (5) \]

According to the inverse Fourier transform

\[ h(t) = \int H(\nu)e^{+j2\pi \nu t}d\nu, \quad (6) \]

(5) can be rewritten as

\[ Y(f) = \int \sum_n x(t)H(\nu)e^{+j2\pi \nu(t-nT)}e^{-j2\pi ft}dt \ d\nu \]
\[ = \int \sum_n x(t)H(\nu)e^{-j2\pi nT}e^{-j2\pi (f-\nu)t}dt \ d\nu. \quad (7) \]

According to the Poisson summation formula

\[ \sum_{n=-\infty}^{+\infty} e^{-j2\pi n\nu T} = \frac{1}{T} \sum_{k=-\infty}^{+\infty} \delta(\nu - \frac{k}{T}), \quad (8) \]

(7) can be transferred to

\[ Y(f) = \frac{1}{T} \int x(t)H(\nu)e^{-j2\pi (f-\nu)t} \sum_n \delta(\nu - \frac{n}{T}) dt \ d\nu \]
\[ = f_s \sum_n x(t)H(nf_s) e^{-j2\pi (f-nf_s)t}dt \]
\[ = f_s \sum_n H(nf_s) \int x(t) e^{-j2\pi (f-nf_s)t}dt \]
\[ = f_s \sum_n H(nf_s)X(f-nf_s). \quad (9) \]

As we can see from (9), the received signal \( x(t) \) is sampled and its spectrum is now folded to be \( \sum_n X(f-nf_s) \). The coefficient for each term \( X(f-nf_s) \) is given by the transfer function of the BPF \( H(nf_s) \) at an integer multiple of \( f_s \). Since the width for each band of \( x(t) \) is \( B=1/T=f_s \), \( \sum_n X(f-nf_s) \) will suffer from aliasing of the \( N \) bands over the whole frequency domain. Therefore, in order to make the Kth band \((K\nu_i)\) available at zero frequency all the other \( N-1 \) neighbor bands, the BPF should be designed so that when \( n = N_0 = f_k/f_s \), \( H(N_0 f_s) = 1 \) and the other coefficients \( H(nf_s) \) for the other neighbor bands are 0. Then, after sub-sampling, only the Kth band which we want is located at zero frequency.

Fig. 4 shows an example with \( N=3 \) and \( K=2 \). \( f_1, f_2, f_3 \) respectively represent the three carrier frequencies with the values \( (N_0-1)B + B/2, \ N_0B + B/2, \ (N_0 + 1)B + B/2 \). B is the maximum width for each channel and B/2 represents an offset which ensures the carriers in the center of the channel. In this case, we generate a set of pulses \( p(t) \) with the period \( T = 1/B \), that is \( f_s = B \).
Fig. 4. Spectrum slices of \( x(t), p(t), h(t), s(t) \) and \( y(t) \) through the whole sub-sampling.

Since the whole width of the input signal is \( 3B \), the discrete-time filter \( h(t) \) has to use a sampling frequency \( FS = 2 \times 3B = 6B \). As the spectrum shown in Fig. 4(c), its passband is represented by the real rectangle, which only pass one pulse for the 2\(^{nd}\) Band and attenuate the others for the 1\(^{st}\) and the 3\(^{rd}\) band. If the target band is the 3\(^{rd}\) band, then the passband is shown by the dashed one.

By using an analog multiplier, \( x(t) \) and \( s(t) \) are mixed. Based on the characteristic of convolution, the multiplication in time domain results in the convolution in frequency domain. Hence, the whole band is then sub-sampled and the second band is shifted to zero frequency by the impulse. Then, a following ADC device can further process the information at a sampling rate as low as \( B \) if a LPF is used before to attenuate the high frequencies.

### 2.2. Discrete-time filter

One key point for the sub-sampling is the design of the filter. As we can see from Fig. 4, the only affect of the BPF is eliminating the certain pulses while for the other frequency range, there has not to be a large attenuation. Therefore, we only need to find a BPF which transfer function can generate zeros at all unwanted frequencies. The cascaded integrator-comb (CIC) filter [15] right has this characteristic.

The transfer function of a CIC interpolator can be written as

\[
H(z) = \left( \frac{1 - z^{-L}}{1 - z^{-1}} \right)^M.
\]  

(10)

\( L \) is the interpolation factor which represents the number of zeros that can be generated. \( M \) is the number of cascaded sections. The more sections there are, the larger attenuation the sidelobes of the filter will have. However, in our design, we don’t have to consider the attenuation other than the zeros, so that only one stage is
needed. Fig. 5 is the frequency response of a CIC filter with L=12 and M=1. As the figure shows, the CIC is a lowpass filter and it has L/2=6 zeros within half of the sampling frequency Fs. All the zeros are distributed uniformly, so that they can be directly used in Fig. 3 to attenuate the impulses. If we think of $H(z)$ as two filters in cascade, $H(z) = H_1(z)H_2(z)$, with the comb section $H_1(z) = 1 - z^{-L}$ (the "comb" due to its magnitude response) and the integrator section $H_2(z) = 1/(1 - z^{-L})$, we can derive the actual implementation in Fig. 6 by using Noble identities [15]. The input data is sampled at a low rate $Fs/L$, which is the sampling frequency of $p(t)$. The rate is increased by the upsampler and finally the output signal is sampled at $Fs$.

![Fig. 5. Frequency response of a CIC interpolator with the interpolation factor L=12](image)

![Fig. 6. An actual CIC interpolator in block-level](image)

However, since the CIC is a lowpass filter, it should be changed to realize a bandpass one. Actually, the CIC filters belong to a larger class of systems called frequency-sampling filters (FSFs) [16]. Frequency-sampling filters can be used to decompose the information spectrum into a set of discrete sub-bands, such as those found in multiuser communication systems. A classic FSF consists of a comb filter cascaded with a bank of frequency-selective resonators [17, 18]. The resonators independently produce a collection of poles that cancel selected zeros generated by the comb pre-filter. An FSF can also be created by all-zero filter (comb) sections with all-pole filter sections, as suggested in Fig. 7. The coefficients in the allpole filter are carefully chosen so that its poles cancel selected zeros of the comb section as shown in Fig. 8.

According to the principle of the FSF, the integrator section of the CIC filter should be revised in order to generate the poles we want. Thus, the whole transfer function $H(z)$ would be rewritten as
The numerator $1 - z^{-L}$ creates $L$ zeros, which start from $0^\circ$ and have the same angle $360^\circ/L$ apart from each other on the unit circle. The polynomial in the denominator generates two poles with the same angle but the opposite signs. The coefficient $-2\cos(2\pi n/L)$ controls the locations of the poles so as to cancel the corresponding zeros and realize a bandpass filter. The parameter $n$ ranges from 0 to $L-1$.

In the example of Fig. 4, $L$ is given by 12. In order to respectively pass the impulses
at $f_1$, $f_2$ and $f_3$, $n$ in (11) should be chosen as 1, 3 and 5. Fig. 9 shows the frequency responses of the bandpass filter on these three cases. As shown in the figure, (a), (b) and (c) are separately used to shift Band 1, 2 and 3 to zero frequency, and the poles should be located at the frequencies $1/16=0.0834$, $1/4=0.25$ and $5/12=0.4167$ (normalized to $2\pi f_1$s). However, since the precision of $\pi$ and the function $\cos(x)$ are limited by Matlab, as we can see in (a) and (c), the peak of the passband has a little difference from the value in theory. This error can be corrected in a practical implementation.

Fig. 9. Frequency responses of the FSF with $L=12$ when (a) $n=1$, (b) $n=3$ and (c) $n=5$
3. Simulation of the system

3.1. Generation of the periodic pulses

In this paper, we work on the model of the system shown in Fig. 4. The periodic series of pulses \( p(t) \) is generated by sampling a dc voltage at a rate of \( B = f_s = 20 \). Therefore, the sampling rate \( F_s \) for the subsequent BPF should be \( 6 \times B = 120 \). The Simulink of Matlab makes all the sampling done by sample and hold, so that in time domain the waveform is still a dc voltage and the following FSF gets samples every \( T_s = 1/f_s \). Such a pulse source is shown in Fig. 10 with an intrinsic sampling rate.

![Fig. 10. Pulse generator achieved by a sampled dc voltage](image)

3.2. FSF

The FSF model is shown in Fig. 11. The interpolation factor \( L \) is 12 and only one section is used. The coefficient \( c \) in the integrator section is \( -2 \cos(2\pi n/12) \), which decides the locations of the two poles. By setting \( n=1, 3 \) and 5, the poles are placed at angles \( \pm 30^\circ, \pm 90^\circ \) and \( \pm 150^\circ \) on the unit circle so as to cancel the zeros. Then the passband is shifted and passes the three impulses equal to the carrier frequencies \( f_1, f_2, f_3 \) respectively. The different spectrums of the output \( y(t) \) are given in Fig. 12. Since the frequency is normalized by \( F_s \), the three impulses should be at \( 1/12=0.08333, 3/12=0.25 \) and \( 5/12=0.41667 \). During simulation, \( F_s \) has not been specified and it can be applied for any value during practical implementation. The amplitude is also normalized to 0dB.

![Fig. 11. Model of the FSF with the pulse generator](image)
Fig. 12. Spectrum of $y(t)$ with the normalized frequency. (a) $n=1$. (b) $n=3$. (c) $n=5$. 
Fig. 13 shows the waveforms in the time domain for $x[n]$, $w[n]$, $w'[n]$ and $y[n]$ in three cases. The generation of the pulses $x[n]$ is realized by sample-and-hold, so that its waveform is still shown as a dc voltage in (a). (b) and (c) are the waveforms before and after the interpolator. One thing we can notice is that $w[n]$ and $w'[n]$ are same except for the sampling frequency. The reason is that the interpolation is done by inserting $L-1$ zeros between two samples. Thus, we can remove the interpolator while increasing the sampling frequency of the pulse generator by $L$ times. The new model is shown in Fig. 14 and its transfer function is now

$$H(z) = \frac{1 - z^{-1}}{1 - 2 \cos \left( \frac{2\pi n}{L} \right) z^{-1} + z^{-2}}.$$  (12)

Fig. 14. Model of the FSF without the interpolator
3.3. Receiver system

The whole receiver system is given by Fig. 15. In this case, the input is a three-band modulated signal

\[ x(t) = x_1(t) + x_2(t) + x_3(t). \]  \hspace{1cm} (13)

\[ x_1 = 100 \sin(2\pi t(f_1 + f_0)) + 100 \sin(2\pi t(f_1 - f_0)), \]  \hspace{1cm} (14)

\[ x_2 = 10 \sin(2\pi t(f_2 + f_0)) + 10 \sin(2\pi t(f_2 - f_0)), \]  \hspace{1cm} (15)

\[ x_3 = \sin(2\pi t(f_3 + f_0)) + \sin(2\pi t(f_3 - f_0)). \]  \hspace{1cm} (16)

The carrier frequencies are \( f_1 = 1210, f_2 = 1230, \) and \( f_3 = 1250. \) The whole width of the double-side band is \( B = 20 \) and the maximum frequency of each original signal is \( f_0 = 5. \)

![Fig. 15. Model of receiver system](image)

Taking the sub-sampling of \( x_3 \) for an example, its spectrum can derive from the Fourier transform and rearranged as:

\[ X_3(f) = \frac{1}{2j} \left( \delta(f - f_3 - f_0) + \delta(f - f_3 + f_0) \right) \]

\[ - \frac{1}{2j} \left( \delta(f + f_3 + f_0) + \delta(f + f_3 - f_0) \right). \]  \hspace{1cm} (17)

\( y(t) \) equals \( s(t) \) given in (3) and \( T = 1/f_s = 1/20. \) However, one thing to be noticed is that \( x_1, x_2 \) and \( x_3 \) are all DSB signals, which means their carrier frequencies are not integer times of \( T \) but has an offset of \( T/2. \) Therefore, the pulse source has to have an offset of \( T/2 \) as well. Thus, (2),(3) should be rewritten as

\[ p(t) = \sum_n \delta(t - T/2 - nT) \]  \hspace{1cm} (18)

\[ y(t) = \sum_n h(t - T/2 - nT) \]  \hspace{1cm} (19)

According to the convolution theorem in mathematics, point-wise multiplication in time domain equals convolution in the frequency domain, which is

\[ x_3(t) \cdot y(t) \xrightarrow{\text{Fourier}} X_3(f) \otimes Y(f) \]  \hspace{1cm} (20)
The whole calculation has been done in Section 2 and we can directly put $X_3(f)$ into (9). Then, considering the offset in $y(t)$, (9) can be rewritten as

$$= f_s \sum_n H(nf_s + f_s/2)X(f - nf_s - f_s/2)$$

$$= \frac{f_s}{2\pi} \sum_n H \left( nf_s + \frac{f_s}{2} \right) \left( \delta \left( f - nf_s - \frac{f_s}{2} - f_3 - f_0 \right) + \delta \left( f - nf_s - \frac{f_s}{2} - f_3 + f_0 \right) \right)$$

$$- \frac{f_s}{2\pi} \sum_n H \left( nf_s + \frac{f_s}{2} \right) \left( \delta \left( f - nf_s - \frac{f_s}{2} + f_3 + f_0 \right) + \delta \left( f - nf_s - \frac{f_s}{2} + f_3 - f_0 \right) \right).$$ (22)

If there is a $N_0 \in \mathbb{n}$ which makes $N_0 f_s + f_s/2 = f_3$, then (22) would be changed to

$$= \frac{f_s}{2\pi} \sum_n H \left( nf_s + \frac{f_s}{2} \right) \left( \delta(f - 2f_3 - f_0) + \delta(f - 2f_3 + f_0) \right)$$

$$- \frac{f_s}{2\pi} \sum_n H \left( nf_s + \frac{f_s}{2} \right) \left( \delta(f + f_0) + \delta(f - f_0) \right).$$ (23)

In our case, $f_s = 20, f_3 = 1250$, so that $N_0 = (1250 - 10)/20 = 62$. As we can see from (23), the first term is shifted to a much higher frequency and never effects the low band. In the second term, if the coefficient $H(nf_s + f_s/2)$ is always kept zero except for $n=N_0$, we get the final function

$$\frac{jf_s}{2\pi} H \left( N_0 f_s + \frac{f_s}{2} \right) \left( \delta(f + f_0) + \delta(f - f_0) \right)$$ (24)

which shows the signal $f_0$ is shifted to the baseband with a non-zero coefficient

$$\frac{jf_s}{2\pi} H \left( N_0 f_s + \frac{f_s}{2} \right).$$ (25)

Fig. 16 shows the spectrum of the signals before and after the sub-sampling. $x_3$ is marked by the red circle in (a). $y(t)$ is shown in (b), which is only one pulse at the carrier frequency $f_3$ passed by the BPF from a multiple set. By multiplying $x(t)$ and $y(t)$, a new discrete-time signal $z(t)$ is produced. The whole wideband at 1200-1260 is repeated and $x_3$ is shifted to zero frequency. The sideband of our interest is now at $f_0=5$. A LPF can be added later so as to eliminate the higher bands.
Fig. 16. Spectrum of (a) the input modulated signal, (b) the pulse coming out of the filter and (c) the output signal after the sub-sampling
4. Circuit implementation

The whole system is also implemented on 90nm CMOS technology in order to verify performance on practice.

4.1. Multiplier

We choose a linear four quadrant analog multiplier [19] for the implementation. This multiplier has a great advantage on the simplicity and the bandwidth. In addition, it has a low power consumption which is fit for our CMOS technology.

The principle of the proposed multiplier is based on the quarter-square algebraic identity [19]:

\[(V_1 + V_2)^2 - (V_1 - V_2)^2 = 4V_1V_2.\]  \hspace{1cm} (26)

Fig. 17 shows the relation. As it shows, the circuit needs summing, squarer circuits and a subtracter.

4.1.1. The squaring circuit

Considering the circuit in Fig. 18, where both transistors work in the saturation region.

\[\text{Fig. 17. Diagram of proposed circuit} \]

\[\text{Fig. 18. Squaring circuit} \]
The currents through the transistors can be expressed as:

\[ I_{DA} = 0.5\mu_{n1}C_{OX1} W/L_1 (V_{GS1} - V_{Th1})^2 \]  
\[ I_{DB} = 0.5\mu_{n2}C_{OX2} W/L_2 (V_{GS2} - V_{Th2})^2 \]  
\[ K = \mu_n C_{OX} W/L \]  
\[ V_{GS} > V_{Th}, V_{DS} \geq V_{GS} - V_{Th} \]  

Suppose all transistors are identical, then \( K_1 = K_2 = K \) and \( V_{Th1} = V_{Th2} = V_{Th} \) and:

\[ I_{SUMMATION} = I_{DA} + I_{DB} \]  
\[ = \frac{K}{2} \left[ (+V_{in} - V_x - V_{Th})^2 + (-V_{in} - V_x - V_{Th})^2 \right] \]  
\[ = K[V_{in}^2 + (V_{ss} + 2V_{Th})^2] \]  

The voltage at \( V_x \) can be derived from:

\[ V_x = V_{ss} + V_{Th} \]  

4.1.2. **Subtraction circuit**

The relationship of the drain current of transistors \( M_1 - M_2, M_3 - M_4 \) in Fig.19 (a) is:

\[ I_{D1} = I_{D2} \]  
\[ I_{D3} = I_{D4} \]  
\[ K(V_1 - V_{out1} - V_{Th})^2 = K(V_2 - V_{ss} - V_{Th})^2 \]  
\[ K(-V_1 - V_{out2} - V_{Th})^2 = K(-V_2 - V_{ss} - V_{Th})^2 \]  

Then the output voltage of signal subtraction circuit is:

\[ V_{out1} = V_1 - V_2 + V_{ss} \]  
\[ V_{out2} = -(V_1 - V_2) + V_{ss} \]  
\[ V_{out(SUB)} = V_{out1} - V_{out2} = 2(V_1 - V_2) \]  

4.1.3. **Summation circuit**

The summation circuit is just realized by switching the signs of \( V_2 \) as Fig. 19 (b) shows. Thus, the output voltages are:

\[ V_{out1} = V_1 + V_2 + V_{ss} \]  
\[ V_{out2} = -(V_1 + V_2) + V_{ss} \]  
\[ V_{out(SUB)} = V_{out1} - V_{out2} = 2(V_1 + V_2) \]  

4.1.4. **Multiplier circuit**

Employing the squaring circuit of Fig. 19 (a) and the summation-subtraction circuit of Fig. 19 (b), the analog multiplier can be realized as shown in Fig 20. The outputs from the subtraction and summation stages are apart applied to two squarer circuits. Then the differential output of squarer summing and squarer difference gives the result of multiplier in voltage mode.
\[ V_{\text{out}} = K(V_{\text{outsum}}^2 - V_{\text{outsub}}^2) = K(V_{\text{outp}}^2 - V_{\text{outn}}^2) \]  \hfill (45)

\[ V_{\text{out}} = K((V_1 + V_2)^2 - (V_1 - V_2)^2) \]  \hfill (46)

\[ V_{\text{out}} = \beta V_1 V_2 \]  \hfill (47)

\[ \beta = 4K \]  \hfill (48)

The performance of the proposed analog multiplier circuit is simulated by Cadence using 90nm CMOS with L/W=1/200. The supply voltage is VDD=0.6V and VSS=-0.6V.

Fig. 19. (a) Subtraction circuit. (b) Summation circuit

Fig. 20. Circuit of the analog multiplier in Cadence

Fig. 21 is the frequency and phase response of the multiplier. The -3dB bandwidth is about 25MHz. However, the gain of the multiplier is a little low. The output suffers from a loss of -10dB, which means a LNA followed might be needed for compensating the loss.
Fig. 21. Frequency and phase response of the multiplier

Fig. 22. DC transfer characteristic

Fig. 22 shows the DC transfer characteristics. The output voltage swings between -28.4mV and +28.4mV for the input voltage range of ±100mV. Comparing the different curves with different input voltages, we conclude that the linearity improves when the input voltages become smaller.

In order to quantify the gain error and the nonlinearity, we keep one input the largest voltage of 100mV and sweep the other input from -100mV to 100mV for analysis. Fig. 23 shows the input/output characteristic. In (a), we plot a straight line to represent the ideal one and obtain the maximum deviation, $\Delta V_1$, and normalize it to the maximum input swing, $V_{\text{in,max}}$. Then the gain error is $\Delta V_1/V_{\text{in,max}} = 0.003 = -15.15$ dB. In (b), we connect the origin and the end point of the actual characteristic and find the maximum difference, $\Delta V_2$, and normalize it to the maximum output swing, $V_{\text{out,max}}$. Then we can see that the multiplier exhibits a nonlinearity of $\Delta V_2/V_{\text{out,max}} = 1.17975/28.4031 = 0.0415 = -13.82$ dB.
We also multiply two sinusoids of 10MHz and 9MHz so as to analyze the harmonic distortion of the whole circuit. Both sinusoids’ amplitude is 100mV. Fig. 24 shows the spectrum of result. According to the demodulation, the fundamental component is at 1MHz. Since the differential multiplier cancels the even order harmonics, we only consider the 3\textsuperscript{rd} and 5\textsuperscript{th} harmonics which are located at 3MHz and 5MHz. For a five-order nonlinearity, the “total harmonic distortion” (THD) is:

\[
\text{THD} = \frac{\text{power of the fundamental}}{\text{power of all the harmonics}} = -13.4689\text{dBm} + (-21.9686\text{dBm}) \quad \frac{1}{11.756\text{dBm}} = -24.65\text{dB} \quad (49)
\]

Fig. 24. Spectrum after multiplying two sinusoids of 10MHz and 9MHz.
4.2. Frequency Sampling Filter (FSF)

![Fig. 25. A low-Q switched-capacitor filter (without switch sharing).](image)

![Fig. 26. A signal flow graph describing the switched-capacitor circuit in Fig.24.](image)

The transfer function of the filter is given in (12), which can be considered as an IIR filter. It can be realized by a switched-capacitor low-Q biquad filter [20]. A general implementation of such a biquad filter is illustrated in Fig. 25, which derives from the signal graph shown in Fig. 26. The input capacitor $K_1C_1$ is the major signal path when realizing low-pass filter; $K_2C_2$ is the major signal path when realizing band-pass filter; whereas, $K_3C_2$ is the major signal path when realizing high-pass filter. $K_4C_1$ and $K_6C_2$ are the feedback from the output which decide the poles of the filter. $K_5C_2$ is the input capacitor for the second amplifier generating one delay between the two stages.

The transfer function of this general biquad circuit is found to be given by:

$$H(z) = -\frac{(K_2 + K_3) + (K_4K_5 - K_2 - 2K_3)z^{-1} + K_3z^{-2}}{(1 + K_6) + (K_4K_5 - K_6 - 2)z^{-1} + z^{-2}}$$  \quad (50)
Comparing (50) with (12), we can obtain the values of the coefficients:

\[
K_1 = K_3 = K_6 = 0, \quad K_2 = -1, \quad K_4 K_5 = 2 - 2 \cos \left( \frac{2n\pi}{12} \right) = 4 \sin^2 \left( \frac{n\pi}{12} \right). \tag{53}
\]

The negative coefficient can be represented by replacing the non-inverting switch with an inverting one. We also make

\[
K_4 = K_5 = \sqrt{4 \sin^2 \left( \frac{n\pi}{12} \right)} = |2 \sin \left( \frac{n\pi}{12} \right)| \tag{54}
\]

for the purpose of optimizing the result.

The practical circuit of the filter is illustrated in Fig. 27. We modify the prototype in order to improve the performance. Firstly, we replace the NMOS switches with transmission gates (TG) due to its high output swing and the lower impedance when conducting. This change reduces the transmission time of the charges through the switches.

Secondly, since the loads are capacitive, we use an OTA [21] instead of amplifier. It also offers a high output impedance. The OTA, as given in Fig. 28, is composed of a folded cascade topology of a CS input stage and a CG stage with a common mode feedback. The common feedback is needed because in high-gain amplifiers, the output common-mode (CM) level is quite sensitive to device properties and mismatches, such as the mismatch in the PMOS and NMOS current mirrors, and it cannot be stabilized by means of differential feedback. As the circuit shown on the right side in Fig. 28, the common-mode feedback senses the output CM level and compares it with an external reference. The error will be returned to the amplifier’s bias network. The whole OTA has a gain of 48dB and a gain-bandwidth product of 22MHz. The characteristic of the OTA will limit the highest sampling frequency we can choose for the filter.
Finally, instead of the single-ended circuit, we implement a fully differential one. Although this differential circuit costs more switches and wires resulting in a larger area, it has a great advantage of rejecting more common-mode noise signals as well as having better distortion performance. The analysis of the filter will be shown in the simulation of the whole system in next section.

4.3. Sub-sampling system

The whole sub-sampling system is shown in Fig.29. The power supply is 1.2V and the sampling frequency is set to 960kHz due to the bandwidth limitation of the OTA. The input DC voltage of the filter is 100mV. The signal to be processed is a three-band double-side-band (DSB) modulated signal:

\[ x(t) = x_1(t) + x_2(t) + x_3(t) \]  \hspace{1cm} (55)

\[ x_1 = 5 \sin(2\pi t(f_1 + f_0)) + 5 \sin(2\pi t(f_1 - f_0)) \text{ mV} \]  \hspace{1cm} (56)

\[ x_2 = 50 \sin(2\pi t(f_2 + f_0)) + 50 \sin(2\pi t(f_2 - f_0)) \text{ mV} \]  \hspace{1cm} (57)
\[ x_3 = 5\sin(2\pi f_3 + f_0) + 5\sin(2\pi f_3 - f_0)\text{ mV} \quad (58) \]

The carrier frequencies, \( f_1, f_2, f_3 \), are respectively 2480kHz, 2640kHz and 2800kHz, which are chosen in the range of 2400kHz-3360kHz within the fourth lower sideband of the filter. The width of each DSB is 160kHz and the intermediate frequency of each signal from the carrier is \( f_0 = 40\text{kHz} \).

4.3.1. **Sub-sampling of Band 2**

In order to sub-sample \( x_2 \), \( n \) in (12) should be 3 and then we get the coefficients from (53)

\[ K_4 = K_5 = |2\sin\left(\frac{3\pi}{12}\right)| = \sqrt{2} = 1.414. \quad (59) \]

*Fig. 30. Waveforms of \( x(t) \), \( h(nT) \) and \( y(nT) \) when sub-sampling Band 2.*

*Fig. 31. Spectrums of \( X(f) \), \( H(f) \) and \( Y(f) \) when sub-sampling Band 2.*
One important thing to be mentioned is that the capacitors \( C_1 \) and \( C_2 \) in Fig. 25 and Fig. 27, which cannot be shown in the transfer function (50), do not have to be the same. Actually, each of them should be carefully tuned so as to realize a stable oscillation on the output of the filter. In our simulation, \( C_1=1.243\text{pF} \) and \( C_2=350\text{fF} \). Thus, after simulation, the waveforms of \( x(t) \), the pulses \( h(nT) \) and the sub-sampled signal \( y(nT) \) are shown in Fig. 30, and the spectrums are given by Fig. 31.

Compared to \( h(nT) \) in Fig. 30 with Fig. 13(e), the waveforms are matched and \( x(t) \) is then sub-sampled to \( y(nT) \). In the spectrums shown in Fig. 31, the second modulated band is shifted to zero frequency and its magnitude is attenuated by 34dB. In this condition, it seems that this sub-sampling technology will bring a quite large loss to the signal. However, according to the gain of the multiplier given by Fig. 21, the loss from the multiplier is only -15.15dB. Since the signal is multiplied by a set of pulses with the amplitude of 100mV and then demodulated by one component with the magnitude of 8.881dBm, we can do the calculation below:

\[
8.881\text{dBm} = -21.189\text{dB} = 0.0872
\]
\[
-21.189 + (-15.15) = -36.339\text{dB} = 0.01524
\]

Therefore, the output baseband suffers from an attenuation of 0.01524. The small difference of -34dB to -36dB is caused by noise aliasing from \( x(t) \), which can be eliminated by employing a BPF before processing \( x(t) \).

We also discover that the components in \( H(f) \) will be attenuated as they repeat in frequency. The first one has a magnitude of 19.4dBm\(\approx\)100m while the one used for demodulation has a magnitude of 8.811dBm\(\approx\)7.6m. This is caused by the width of the pulses in \( h(nT) \). In practice, it is impossible to realize ideal discrete-time signals while all the discrete values must have a hold time. In our design, the values are held for the whole sampling interval. Such a rectangular waveform will result in the attenuation of the repeated passbands of the filter. Hence, the use of this sub-sampling technology is based on how much attenuation the users can tolerate. If the sampling rate is kept, then the higher carrier frequency the signal has, the more attenuation the sub-sampled signal will receive.

### 4.3.2. Sub-sampling of Band 1

We also give the case of sub-sampling Band 1. For the sake of highlighting, the target band always has a larger magnitude than the other two bands. The waveforms of sub-sampling of Band 1 is shown in Fig. 32, in which \( h(nT) \) is matched with the simulation in Fig. 13(d).

Fig. 33 shows the spectrums of each signal. In this case, \( n \) in (12) is chosen as 5 and the coefficients should be changed to

\[
K_4 = K_5 = |2\sin \left( \frac{5\pi}{12} \right)| = 1.931851653.
\]

The signal suffers from an attenuation of -29dB during the sub-sampling. This result is a little different from that of sub-sampling Band 2, because the component used to shift the band has a larger magnitude which is 13dBm. The calculation can be done as:
Sub-sampling of Band 3

In sub-sampling of Band 3, the waves are shown in Fig. 34 and the spectrums are given by Fig. 34. In this case, n in (12) is 1 and the coefficients are given by:

\[ K_4 = K_5 = |2\sin\left(\frac{\pi}{12}\right)| = 0.5176. \]  \[ (65) \]

The waveform of h(nT) in Fig. 35 is matched with that in Fig. 13(d) as well. The total loss of Band 3 after the sub-sampling is -33.8dB, which derives from the calculation with the value in Fig. 34:

\[ 13\text{dBm} = -20.56676\text{dB} \]
\[ -20.57 + (-15.15) = -35.72\text{dB} \approx -33.8\text{dB}. \]  \[ (66) \]  \[ (67) \]
Fig. 34. Waveforms of $x(t)$, $h(nT)$ and $y(nT)$ when sub-sampling Band 3.

Fig. 35. Spectrums of $X(f)$, $H(f)$ and $Y(f)$ when sub-sampling Band 3.
5. Conclusion

This thesis presents a new sub-sampling technology for receiver architectures. It directly sub-samples a modulated wideband signal and simultaneously shifts the band of interest to zero frequency. Compared to traditional demodulation and BPS technology, this sub-sampling not only prevents from generating different high-frequency LOs for different bands, but also realizes a sampling rate much lower than the Nyquist rate. For multi-channel communication, only one DC voltage is used as the common source to generate pulses for sampling, and discrete-time BPFs with different capacitors are employed for selecting the channel. All the output signals of the sub-sampling can be processed by the ADC devices with a same Nyquist rate which can be lowered to twice the bandwidth of a channel.

One shortcoming of the sub-sampling is that the sampled signal suffers from attenuation. When the sampling rate of FSF has been chosen, the higher frequency the information has, the higher passband of FSF has to be used and the more attenuation will exist. In practical use, the designer should make a trade-off between the sampling rate and the gain of the sub-sampling, based on how much loss can be tolerated. Otherwise, a LNA before or after the multiplier might be needed to compensate for the loss.

Till now, we have proved that this sub-sampling works well in a receiver system with a lower sampling rate and less circuit cost. On the other hand, this technology also works for the transmitter. As we mentioned in the chapter of Introduction, the information has to be modulated on a quite high carrier frequency for transmission. The conventional way is opposite of what a receiver does, that is mixing the baseband with a high LO, or multiple stages of low LOs. However, if we replace the input signal x(t) with a baseband signal x’(t) in the sub-sampling system, it then will be changed to a “up-sampling” system. The spectrum of the sampled baseband signal is also periodically repeated and shifted to the high frequency for transmission. There is no change on the multiplier and the filter, but the attenuation of the sampling still has to be considered. Thus, we can also modulate a baseband to a high frequency with a sampling rate as low as the Nyquist rate.
6. Future work

In this paper, we propose a prototype of the sub-sampling system. We verifies the technology on both behavioral level and circuit-level. However, in order to make the whole design practically used, some future work still need to be done.

6.1. Designing a LPF

A LPF is needed after the sub-sampling. As Fig. 29, 31, 33 shows, the neighbor bands are also sub-sampled along with the band of interest, and the harmonics are produced as well after sampling. The elimination of all these unwanted components can be done by adding a LPF. In order to achieve a good performance so that ADC devices followed can process the target band with less noise, the LPF can be divided into an analog LPF as the anti-imaging filter cascaded by a switched-capacitor (SC) LPF as a channel-selection filter. The former LPF is aimed at removing the other channels while the latter one, which can utilize the same or lower clock frequency of the FSF as we used, is designed to attenuate the harmonics. The second LPF followed is aimed at removing the neighbor bands.

6.2. Optimizing FSF

The biquad filter we used for FSF still has to be further optimized. Due to the small feature of CMOS technology we used, the stability of the output signal of the FSF is so sensitive to $C_1$ and $C_2$ shown in Fig. 23 and 25 that $C_1$ and $C_2$ have to be tuned quite carefully, which brings more difficulty on the practical fabrication. Therefore, the trial of new filters is needed in order to find one with a more stable performance. Otherwise, a start-up/tuning circuit is probably needed. In addition, the sampling rate of the FSF is limited by OTAs inside. If the sub-sampling system needs to be applied in industry, the bandwidth of OTAs should be extended much higher.

6.3. Optimizing the multiplier

Although the multiplier we used in this paper has a simple circuit, it suffers from a loss of -15dB, which results in an additional LNA for compensating needed. Furthermore, it has a nonlinearity of $-13.82$dB and its THD is $-24.65$dB, which are too high to be applied in industry. Therefore, new multipliers should be further studied in order to increase the gain while keeping the simplicity of the design, and
lower the nonlinearity as well as THD. In addition, for practical use, the bandwidth of the multiplier should be increased as well as OTAs’.
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