Design and Optimization of an Analog Front-End for Biomedical Applications

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Abstract

The state-of-the-art analog front-end of implantable biosensors is the class of current-mirror-based circuits. Despite their superior noise performance, power consumption and area, they suffer from systematic and random errors causing offset, gain and linearity error in reading out the sensor data. In the first part of this thesis, a new analog front-end is proposed to eliminate the systematic error. The proposed topology is able to accurately copy the sensor current which will be converted into the proportional voltage for further processing. Additionally, a theoretical discussion regarding the functionality of the proposed topology is given and a thorough study on the effect of random error sources is carried out.

In the second part of this thesis, in order to optimize the design of the proposed analog front-end, an optimization algorithm is proposed. The proposed optimization algorithm takes advantage of a modified Imperialist Competitive Algorithm. The original imperialist competitive algorithm shows a low search ability in high-dimensional search spaces which is the case in optimization of analog circuits. A thorough comparison between the original imperialist competitive algorithm, the proposed algorithm and genetic algorithm as a reference is carried out. It will be revealed that the proposed algorithm is capable of exploring the cost space more efficiently than the other two algorithms, thereby resulting in better trade-offs between design objectives to reach higher cost values. Furthermore, according to the mathematical benchmarks, the proposed algorithm is more than 1.5 times faster than the other algorithms in finding the global minimum, which is essential in simulation-based optimization procedures.

The proposed optimization algorithm is used to design the proposed analog front-end. The results show an average of 25.8 times higher FoM when designed with the optimization algorithm as opposed to traditional design. The design and simulation is carried out in a commercial 150nm CMOS process. The optimally-designed analog front-end shows a highly-linear highly-accurate performance in a low-noise condition, while consuming only 32 µW.
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Finally, I acknowledge the Swedish Research Council (VR) for funding this research.
List of Acronyms

RF  Radio Frequency
WE  Working Electrode
CE  Counter Electrode
RE  Reference Electrode
CMRR Common-Mode Rejection Ratio
CMOS Complementary Metal-Oxide Semiconductor
OP  Opamp
TIA  Transimpedance Amplifier
OTA  Operational Transconductance Amplifier
MOS  Metal-Oxide Semiconductor
ICMR Input Common-Mode Range
UGBW Unity-Gain Bandwidth
AMS Analog, Mixed-Signal
EDA  Electronic Design Automation
EA  Evolutionary Algorithm
GA  Genetic Algorithm
EP  Evolutionary Programming
GP  Genetic Programming
DE  Differential Evolution
ICA  Imperialist Competitive Algorithm
CCA  Colonial Competitive Algorithm
SA   Simulated Annealing
MIMO Multiple-Input and Multiple-Output
PID  Proportional-Integral-Derivative
PSO  Particle Swarm Optimization
MICAO Modified Imperialist Competitive Algorithm for Analog Circuit Optimization
RHP  Right-Half Plane
LHP  Left-Half Plane
FoM  Figure-of-Merit
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Chapter 1

Introduction

In recent years, there has been major developments in different areas of biomedical industry including medical diagnostics and monitoring, cardiology, audiology, and neurology. In medical diagnostic and monitoring, there has been many advances in approaches to develop implantable biomedical devices. As opposed to external non-invasive devices, implantable biomedical devices are always carried by the patients eliminating pain, skin damages, and side effects. These devices are used to monitor biological compounds such as glucose, cholesterol, etc. [1, 2]. In such monitoring, one of the most popular approaches involves using amperometric biosensors [3, 4]. Basically, an amperometric biosensor generates a current proportional to the concentration of the under-measurement compound. By means of an implanted analog front-end, the current is measured and converted into a desired signal depending on the application. The signal will be applied to an implanted radio frequency (RF) front-end sending the data out to an external RF reader.

The state-of-the-art approach in extracting an amperometric biosensor data is to mirror the sensor current into another circuitry and process the mirrored current instead of the sensor current directly [5]. This approach is superior to conventional approaches in noise performance, power consumption, and area. However, due to existing sources of error in copying the sensor current, there is still room to enhance the accuracy and linearity in reading out the sensor current.

In the first part of this thesis, a new analog front-end is proposed to maximize the accuracy and linearity in reading out the sensor current. The proposed topology consumes less power and shows better noise performance compared with the state-of-the-art approach. Additionally, a thorough study on random sources of error is carried out. This study is important since these error sources cannot be calibrated out reducing the accuracy and degrading the linearity.
In the second part of this thesis, an optimization algorithm for automated design of analog circuits is proposed. The performance of the proposed algorithm is tested against conventional algorithms. The proposed algorithm is used to design the analog front-end that is introduced in the first part of the thesis. The results show that the figure-of-merit of the circuit designed by using the proposed algorithm is in average 25.8 times higher than that of the traditional design.

The thesis is organized as follows: chapter 2 describes different types of electrochemical sensors; chapter 3 introduces potentiostats for biosensors and reviews the state-of-the-art. The proposed potentiostat topology is presented in chapter 4; chapter 5 presents the critical simulation results; chapter 6 explains the proposed optimization algorithm; chapter 7 gives the optimization results and comparisons for two case studies, including the potentiostat as well as the mathematical benchmarks; chapter 8 concludes the thesis.
Part I

Design of an Analog Front-end for Biomedical Applications
Chapter 2

Electrochemical Sensors

The fundamental functionality of an electrochemical sensor is the following: while one or some variables of the sensor (e.g. current, potential, etc.) are held constant, a controlled variable changes by variations of a chemical species; therefore, the target chemical species can be measured via measuring the controlled variable. Basically, electrochemical sensors can be classified into three categories, based on their controlled variables [6]:

- **Voltammetric**: The target chemical species is measured via applying a potential over the sensor electrodes and reading the output current. An amperometric-type sensor is a type of voltammetric sensor in which the potential between certain electrodes is kept constant and the output current (as the controlled variable) is measured. The major benefit of such a sensor is the linear relation between the controlled variable and the target chemical species.

- **Potentiometric**: In this type, the controlled variable is the sensor potential which has a logarithmic relation with the target chemical species. Since the sensor operates in an open-circuit situation, no current passes through it.

- **Conductometric**: This type is used when measuring the resistance of the chemical species of interest. While the frequency is kept fixed at a certain value, the conductance between certain sensor electrodes is measured.

The amperometric-type sensor is used for the proposed analog front-end in this thesis. Generally, a two- or three-electrode version of the sensor can be used. However, a three-electrode sensor is preferred because of its
highly-controllable interfacial potential difference of the main sensor electrodes [6]. As it is shown in Fig. 2.1, the sensor is composed of three electrodes, namely, working electrode (WE), counter electrode (CE) and reference electrode (RE) [7]. The main chemical reaction takes place at the WE in a certain cell potential $V_{cell}$. The RE is used to generate a potential reference for measurement. Thus, no chemical polarization should occur on the surface of this electrode and no current should pass through this electrode. The CE is merely an auxiliary electrode used to counterbalance the current, $I_F$, which sinks from (sources into) the WE.

![Figure 2.1. A three-electrode amperometric sensor.](image)

Fig. 2.2 depicts a generic lumped equivalent circuit of an electrochemical sensor. $R_{WE}$, $R_{CE}$ and $R_{RE}$ represent the resistance of the working, counter and reference electrode, respectively. $C_{WE}$ and $C_{CE}$ denote the capacitance of the working and counter electrode, respectively. $R_{S1}$ and $R_{S2}$ are the chemical solution resistances. Note that the equivalent circuit of an electrochemical sensor is usually more detailed than that shown in Fig. 2.2. However, this circuit can be used to simplify hand calculations, simulations and the optimization process. If enough margin is considered in satisfying the design constraints, it will be guaranteed that the specifications do not change considerably in presence of a real electrochemical cell.

![Figure 2.2. A generic lumped equivalent circuit of an electrochemical sensor.](image)

In this thesis, the electrochemical biosensor for measuring blood glucose concentration reported in [3] is employed. The equivalent circuit of the biosensor is shown in Fig. 2.3.
Figure 2.3. Equivalent circuit of the blood glucose monitoring biosensor.

The sensor operates at a $V_{cell}$ of 0.6V, while the sensor current changes from 10nA to 1µA, $R_{WE}$ varies from 60MΩ to 600kΩ.
Chapter 3

Potentiostat for Biosensors

3.1 Introduction

Fig. 3.1 illustrates a generic block diagram of an analog front-end for an amperometric biosensor. As seen in the figure, the main block is the potentiostat which is responsible for two main functions [7]: First, to ensure that the sensor is biased at the required potential which can vary for different sensors. Second, to extract the sensor output current for subsequent processing.

The challenges in designing a potentiostat are as follows [8]: 1) stability has to be guaranteed when a negative feedback configuration is used; this is a quite challenging task since biosensors have highly variable internal impedances causing the dominant poles and zeros of the system to change considerably; 2) the potentiostat has to consume the minimum possible power if connected to an implantable biosensor; to achieve such a goal, working in
the sub-threshold region is a potential solution; 3) the potentiostat has to guarantee that the sensor cell potential ($V_{cell}$) tracks a reference DC voltage ($V_{ref}$) which enables the required electrochemical reaction; 4) low noise operation is needed in order to process weak signals with large enough resolution; 5) the accuracy as well as the linearity of the potentiostat response has to be maximized.

### 3.2 State-of-the-art Review

To measure an amperometric sensor current, several current-measurement-based potentiostats have been proposed in the literature. The most popular approach is to use a transimpedance amplifier as shown in Fig. 3.2. The advantages of employing such an approach are as follows: 1) the circuit realization is relatively simple; 2) very small currents can be measured via increasing the $R_M$ value; 3) current is measured with reference to ground. The shortcomings of this approach are: 1) since the working electrode is not connected to a true ground, environmental noise can be easily picked up via this electrode; 2) the input resistance behaves inductively which resonances with the sensor capacitor at a certain frequency; 3) for the specific sensor that is shown in Fig. 3.2, the input DC voltage has to be negative if a positive output voltage is desired; this needs a double-supply power which is not suitable for implantable applications.

![Figure 3.2. A current-measurement-based potentiostat using a transimpedance amplifier.](image)

The second approach is to use a resistor in the main current path connected to the working electrode and measure the voltage drop over that resistor. The circuit schematic is depicted in Fig. 3.3. The circuit is capable of measuring
very small currents via increasing the $R_M$ value, working with a single-supply power, and measuring the sensor current with reference to ground. However, there are few disadvantages to this approach as follows: 1) compared to the previous approach, since more active and passive components are used, it is potentially noisier and more sensitive to mismatch between the components; 2) since the working electrode is not connected to a true ground, environmental noise is picked up via this electrode; 3) when the voltage drop over $R_M$ increases with increasing the sensor current, the headroom for voltage swing at the counter electrode decreases.

![Figure 3.3. A current-measurement-based potentiostat using a resistor in the main current path connected to the working electrode.](image)

Fig. 3.4 shows the third approach where a resistor is connected to the counter electrode and the voltage drop over that resistor is measured via an instrumentation amplifier. Similar to the previous approach, this approach is vulnerable to mismatch between components and potentially noisier. Also, it suffers from the headroom issue with the counter electrode that was explained for the previous approach. However, it has several advantages as follows: 1) since the working electrode is connected to a true ground, no environmental noise and interference are picked up via this electrode; 2) since no extra active component except the control amplifier is used in the negative feedback loop, the stability is potentially better; 3) the output voltage and current are measured with reference to ground.
Figure 3.4. A current-measurement-based potentiostat using a resistor connected to the counter electrode and an instrumentation amplifier.

The fourth approach proposes a fully differential potentiostat which has been reported in [4]. This approach enables the potentiostat to work with the sensors having a cell potential near to \( VDD \). As it can be seen in Fig. 3.5, since the voltage of working and counter electrodes are dynamically controlled by the potentiostat, the voltage swing over the sensor is almost doubled. Better common-mode rejection ratio (CMRR) as well as almost 6dB extra dynamic range are obtained using this approach. However, the large power consumption of this topology makes it unsuitable for implantable applications. Also, the output voltage is not measured with reference to ground. The picked-up noise via the working electrode is another disadvantage of this approach.

All the reviewed approaches make use of more than one opamp. This potentially leads to high power consumption and large area [6]. Recently, a current-mirror-based approach has been reported [5], which is shown in Fig. 3.6. Since the number of opamps (especially in the negative feedback loop) is decreased, this topology is potentially more stable, low-power, and low-noise. It is also well-suited for CMOS integration since the area is reduced to the minimum possible level.

Considering Fig. 3.6, the main idea is to mirror the sensor current into another circuitry and process the mirrored current instead of the sensor current directly. The sources of error of this configuration can be classified into systematic and random errors. The systematic error is caused by channel-length modulation in \( M_1 \) and \( M_2 \), and can be calibrated out from the potentiostat response. However, a calibration error which degrades the accuracy of reading out the sensor data is still present. Also, random errors such as device mismatch and temperature variations cannot be calibrated which reduce the accuracy and degrade the linearity. In the next chapter, based on the topology
of Fig. 3.6, a new potentiostat is introduced eliminating the systematic error problem of current-mirror-based potentiostats.
Chapter 4

Proposed Potentiostat Topology

4.1 Circuit Description

The proposed potentiostat topology is shown in Fig. 4.1 [9]. It is composed of two main sub-circuits. First, the conventional potential-control loop through which the potential of RE is stabilized at $V_{\text{ref}}$. Second, an introduced error-cancellation loop to maximize the accuracy of current-copying operation from $I_F$ to $I_{F1}$.

The potential-control loop consists of OP1 followed by a common-source stage $M_1$, and the sensor cell itself as the feedback network. This loop ensures that $V_{RE}$ tracks the reference DC voltage, $V_{\text{ref}}$, for the entire range of sensor current (so, $V_{\text{cell}} = V_{DD} - V_{\text{ref}}$). To study the accuracy of tracking, the small-signal transfer function from $V_{\text{ref}}$ to $V_{\text{cell}}$ is extracted and can be expressed as

![Figure 4.1. The proposed potentiostat topology.](image)
\[ \frac{V_{cell}}{V_{ref}} \approx \frac{1}{1 + \frac{1}{A_1 g_{m1} (R_{WE} || r_{ds1})}} \] (4.1)

where \( A_1 \) is the open-loop gain of OP1, \( g_{m1} \) and \( r_{ds1} \) are the transconductance and output resistance of transistor \( M_1 \), respectively. Also, since the CE is designed to be much larger than WE [3] (i.e., \( R_{CE} \ll R_{WE} \)), it is assumed that \( R_{CE} \ll R_{WE} r_{ds1} A_1 g_{m1} \). Considering (4.1), the term \( A_1 g_{m1} (R_{WE} || r_{ds1}) \) determines the deviation of (4.1) from the ideal value of 1. Since the sensor current along with \( R_{WE} \) varies several decades, and \( M_1 \) is biased merely with this current, \( g_{m1} \) and \( r_{ds1} \) change considerably. Therefore, a sufficiently large \( A_1 \) should be designed to guarantee that (4.1) is set close to the ideal value of 1 for the whole range of sensor current.

Transistor \( M_1 \) is biased with the sensor output current, \( I_F \), and mirrors the current to \( M_2 \). In order to increase the accuracy of current-copying, \( M_1 \) and \( M_2 \) can be realized as cascode topologies. However, the channel-length modulation effect still causes current mismatch. In order to overcome this problem an error-cancellation loop is introduced. The loop is formed by an error-tracking amplifier OP2, and a transimpedance amplifier (TIA) consisting of OP3 and \( R_f \) with an adjustable input common-mode voltage. It is worth mentioning that OP2 could have conventionally been connected to the gate of \( M_{1,2} \) to control the current mismatch. However, this node is already under the control of the potential-control loop and cannot be re-used. Instead, OP2 is connected to the common-mode terminal of the TIA. This configuration introduces a global feedback and thus enhances the loop gain of the error-cancellation loop considerably. Therefore, the TIA biases \( M_2 \) via \( R_f \) to match the current of \( M_1 \) eliminating the \( V_{DS} \) mismatch. The TIA also provides a current-to-voltage conversion such that,

\[ V_{out} = R_f I_{F1} \] (4.2)

where in ideal case \( I_{F1} = I_F \).

To evaluate the contribution of OP2 and OP3 in eliminating the channel-length modulation effect, (4.2) is re-calculated in presence of \( V_{DS} \) mismatch between \( M_1 \) and \( M_2 \) as

\[ V_{out} = R_f I_{F1} - \Delta V_{DS(\text{feedback})} \] (4.3)

where

\[ \Delta V_{DS(\text{feedback})} = \Delta V_{DS} \left( \frac{1}{1 + A_2 A_3 \beta_3} \right), \] (4.4)
4.2. DEVICE MISMATCH ANALYSIS

$\Delta V_{DS(feedback)}$, as noticed in Fig. 4.1, represents $\Delta V_{DS}(= V_{DS1} - V_{DS2})$ after adding the error-cancellation loop, the feedback factor $\beta_3 = r_{ds1}/(r_{ds1} + R_f)$, and $A_x$ is the open-loop gain of $OP_x$.

As noticed in (4.3), $\Delta V_{DS(feedback)}$ causes offset error in the transfer function. However, following (4.4), a sufficiently large $A_2$ and $A_3$ can almost set this error to zero increasing the accuracy in reading out the sensor current.

4.2 Device Mismatch Analysis

If it is designed carefully, the proposed topology eliminates the channel-length modulation effect maximizing the accuracy of copying the sensor current. However, random errors such as device mismatch still remain which are investigated in this section.

The output voltage in presence of device mismatch between $M_1$ and $M_2$ can be expressed as

$$V_{out} \simeq R_f I_{F1} \left( 1 + \frac{\Delta \beta}{\beta_1} \right) - R_f \Delta V_T \sqrt{2I_{F1}\beta_1}$$

(4.5)

where $\Delta V_T = V_{T2} - V_{T1}$, $\Delta \beta = \beta_2 - \beta_1$, and $\beta_{1,2}$ is the current gain factor of $M_{1,2}$. To simplify the calculations, it is assumed that there is no $V_{DS}$ mismatch between $M_1$ and $M_2$ due to the high enough loop-gain of the error-cancellation loop. Also, the following assumptions introduced in [10] validated for 150nm technology have been used, $\Delta \beta \ll \beta_1$, $\Delta V_T \ll \sqrt{2\lambda/\beta_1}$, and $\lambda_1 V_{DS1}$, $\lambda_2 V_{DS2} \ll 1$.

As it can be noticed in (4.5), $\Delta \beta$ and $\Delta V_T$ cause gain (first term) and linearity (second term) error, respectively. Note that, these errors cannot be eliminated by OP2 and OP3.

4.3 Design Considerations

The potentiostat was designed and simulated using the Cadence environment in a commercial 150nm CMOS process. In order to provide large signal swing and high gain to maintain the potential-control loop, OP1 is realized as a folded cascode operational transconductance amplifier (OTA) shown in Fig. 4.2. As it will be shown in the next chapter, a loop-gain of 70 dB and a phase margin of 90 degree for the potential-control loop was achieved. Therefore, following (4.1), we have $V_{cell}/V_{ref} = 0.99971$ for the worst case condition. This guarantees that $V_{cell}$ tracks $V_{ref}$ for the whole range of sensor operation. OP1 consumes only 11.7 $\mu$W from a $V_{DD}$ of 1.8V.
In order to find the major contributors to the noise level, the input referred noise can be calculated with the following approach [11]:

1. A voltage source, \( e_n \), representing the MOS input voltage noise is placed in series with the gate terminal of each MOS transistor. In this case, the transistor itself is assumed noise-free. Note that in low-frequency applications, the MOS current noise which is correlated with the voltage noise can be neglected.

2. The total power of output voltage noise, \( e_{n_{out}}^2 \), is calculated for the entire circuit using the super-position technique.

3. \( e_{n_{out}}^2 \) is referred to the input to obtain the total equivalent input noise, \( e_{n_{eq}}^2 \).

The noise calculation is only carried out for OP1 as the input stage. The noise of the second stage (the common-source stage \( M_1 \)) is divided by the gain of the entire circuit and is negligible. The total power of output voltage noise of OP1 can be expressed as

\[
e_{n_{out}}^2 = i_{n_{out}}^2 R_{out}^2
\]  

(4.6)

where

\[
R_{out}^2 = (g_{m10}r_{ds10}r_{ds12}) \parallel g_{m8}r_{ds8} (r_{ds6} \parallel r_{ds3})^2,
\]  

(4.7)

![Figure 4.2. Schematic of the folded-cascode OTA.](image)
and

\[ i_{nout}^2 = g_{m3}^2 e_n^2 \left( \frac{r_{ds3} + \frac{1}{g_{m3}} \frac{r_{ds3}}{1 + 2g_{m10}r_{ds10}r_{ds12}r_{ds8}}}{r_{ds3}} \right)^2 \]

\[ + g_{m3}^2 e_{ns}^2 \left( \frac{r_{ds3}}{r_{ds3}} + \frac{1}{g_{m3}} \frac{r_{ds3}}{1 + 2g_{m10}r_{ds10}r_{ds12}r_{ds8}} \right)^2 \]

\[ + g_{m4}^2 e_{n4}^2 \left( \frac{r_{ds4}}{r_{ds4}} + \frac{1}{g_{m4}} \frac{r_{ds4}}{1 + 2g_{m11}r_{ds11}r_{ds13}r_{ds9}} \right)^2 \]

\[ + g_{m7}^2 e_{n7}^2 \left( \frac{r_{ds7}}{r_{ds7}} + \frac{1}{g_{m7}} \frac{r_{ds7}}{1 + 2g_{m12}r_{ds12}r_{ds15}r_{ds9}} \right)^2 \]

\[ + g_{m6}^2 e_{n6}^2 \left( \frac{r_{ds6}}{r_{ds6}} + \frac{1}{g_{m6}} \frac{r_{ds6}}{1 + 2g_{m10}r_{ds10}r_{ds12}r_{ds8}} \right)^2 \]

\[ + g_{m12}^2 e_{n12}^2 \left( \frac{r_{ds12}}{r_{ds12}} + \frac{1}{g_{m12}} \frac{r_{ds12}}{1 + 2g_{m11}r_{ds11}r_{ds15}r_{ds9}} \right)^2 \]

\[ + g_{m13}^2 e_{n13}^2 \left( \frac{r_{ds13}}{r_{ds13}} + \frac{1}{g_{m13}} \frac{r_{ds13}}{1 + 2g_{m9}r_{ds9}r_{ds11}r_{ds15}r_{ds9}} \right)^2 \]

\[ \left( \frac{g_{m8}}{1 + g_{m8}(r_{ds6}r_{ds3})} \right)^2 e_{n8}^2 + \left( \frac{g_{m9}}{1 + g_{m9}(r_{ds7}r_{ds4})} \right)^2 e_{n9}^2 \]

\[ \left( \frac{g_{m10}}{1 + g_{m10}r_{ds12}} \right)^2 e_{n10}^2 + \left( \frac{g_{m11}}{1 + g_{m11}r_{ds13}} \right)^2 e_{n11}^2 \]

The input referred noise can be calculated as

\[ e_{n_{eq}}^2 = \frac{e_{n_{out}}^2}{A_v^2} \] (4.9)

where \( e_{n_{out}} \) is already given in (4.6), and \( A_v \) is the voltage gain of the amplifier and can be formulated as

\[ A_v = g_{m3}R_{out} \]. (4.10)

As it can be seen in (4.8), the major noise contributors are the input transistors \( M_{3,4} \), transistors \( M_{6,7} \), and \( M_{12,13} \). The noise from \( M_5 \) was neglected since it is not in the signal path.

Generally in low-frequency applications, the flicker noise is the dominant source of noise for a MOS transistor. The flicker noise power of a MOS transistor can be expressed as \[12\]:

\[ 4.3. \text{DESIGN CONSIDERATIONS} \]
As noticed, the flicker noise is inversely proportional to the length and width of a MOS transistor. To minimize the noise level, the maximum noise contributor, i.e. the input transistors $M_{3,4}$, is considered. There are several trade-offs in sizing these transistors. On one hand, increasing the widths reduces the flicker noise but increases the power consumption. On the other hand, increasing the lengths reduces the flicker noise but also reduces the open loop gain by decreasing the transconductance. However, the reduced open loop gain can be compensated by the second stage, i.e. transistor $M_1$. Another important trade-off is between noise and bandwidth. Although increasing the transistors size will reduce the noise level, it increases the area, and thus, the parasitic capacitances which will reduce the bandwidth. As mentioned earlier, transistors $M_{6,7}$ and $M_{12,13}$ are also major contributors to the noise level. The lengths of these transistors are increased to reduce the noise level. This will reduce the power consumption by decreasing their bias currents in a fixed $V_{GS}$. The widths of $M_{6,7}$ and $M_{12,13}$ could have been also increased to reduce the noise level. However, it will increase the power consumption which is not desirable. By taking all the mentioned trade-offs into account, the sizes of $M_{3,4}$, $M_{6,7}$ and $M_{12,13}$ are chosen to meet the noise requirement.

As mentioned earlier, the open loop gain of OP1 contributes to the accuracy of voltage tracking in the potential control loop. In order to increase the open loop gain, apart from the input transistors, transistors $M_{8,9}$ and $M_{10,11}$ are suitable candidates. The output impedance can be increased by increasing their lengths. However, since they are directly connected to the output node, increase in length reduces the bandwidth by enhancing the parasitic capacitances.

A detailed pole/zero analysis of the potential-control loop can be found in [5]. The dominant poles of the proposed potentiostat topology can be formulated as follows:

\[ P_1 \simeq -\frac{1}{C_{WE}(R_{WE} \parallel (R_{CE} + r_{ds1}))} \]  
(4.12)

\[ P_2 \simeq -\frac{1}{C_{CE}(R_{CE} \parallel r_{ds1})} \]  
(4.13)

\[ P_3 \simeq -\frac{1}{(C_{gd8} + C_{gd10} + C_{gs1} + C_{gd1}(1 + g_{m1}r_{ds1})) R_{out_{OP1}}} \]  
(4.14)
where $R_{out,OP1}$ is the output resistance of OP1 already given in (4.7). The first and second dominant poles are generated by the working and counter electrode, respectively. The third dominant pole is caused by the output node of OP1. The fourth pole has a very high frequency since $R_{s1,2}$ are very small.

As it can be seen in (4.12), $P_1$ is dependent on the variations of $R_{WE}$ and $r_{ds1}$. For the entire range of sensor operation, $M_1$ is designed in such a way that $r_{ds1} \gg R_{WE}, R_{CE}$. Therefore, it holds $(R_{WE} \parallel (R_{CE} + r_{ds1})) \simeq R_{WE}$, and thus, the variations of $R_{CE}$ can be neglected and the stability must be guaranteed only for the variations of $R_{WE}$. From the same analysis, it can be concluded that $P_2$ is only dependent on $R_{CE}$. This resistance does not change considerably during the sensor operation, and thus, the $P_2$ frequency remains almost constant.

The output voltage swing of OP1 is critical and has to be analyzed due to the following reason: according to (4.16), $V_{DS1}$ is approximately determined by $V_{ref}$, and thus, it is a constant value;

$$V_{DS1} = V_{ref} \left( \frac{R_{CE} + R_{WE}}{R_{WE}} \right) \simeq V_{ref}$$

(4.16)

on the other hand, $I_{DS1}$ is directly determined by the sensor output current; so, in the worst case, $V_{GS1}$ will decrease considerably if the sensor operates at its minimum output current (note that $V_{GS1}$ and $I_{DS1}$ are proportional); this decrease in $V_{GS1}$ should be covered by the minimum output voltage swing of OP1 in order to maintain the negative feedback loop.

The output voltage swing of OP1 can be expressed as

$$V_{b4} - V_{T10} \leq V_{out} \leq V_{b3} + |V_{T3}|$$

(4.17)

where $V_{T,x}$ is the threshold voltage of transistor $M_x$. According to the earlier discussion, it must hold

$$V_{GS1(\text{min})} \geq V_{b4} - V_{T10}.$$  

(4.18)

Also, the input common-mode range (ICMR) of OP1 can be formulated as

$$V_{DS5_{\text{sat.}}} + V_{G3} \leq V_{CM_{\text{in}}} \leq V_{DD} - |V_{DS6_{\text{sat.}}}| + V_{T3}$$

(4.19)
where $V_{DSx_{sat}}$ is the minimum $V_{DS}$ needed for transistor $M_x$ to operate in the saturation region. The larger the range of $V_{CM_{in}}$, the more types of sensors with different $V_{cell}$ values can be supported by the proposed potentiostat.

A single-stage differential amplifier was used for OP2 and OP3 which is shown in Fig. 4.3. A loop-gain of 50 dB with 60 degree of phase margin was obtained for the error-cancellation loop. Resulted from power consumption versus gain optimization, OP2 and OP3 consume only 9.25 $\mu$W and 10.8 $\mu$W, respectively. Resistor $R_f$ was set to 400 k$\Omega$ providing adequate signal swing under the maximum sensor current, and 112 dB gain from the sensor current to the output voltage. The transistors sizes, DC operating points and capacitances can be found in Appendix A.

4.4 Design Flow

The design of the proposed potentiostat is divided into two parts: 1) design of the potential-control loop, 2) design of the error-cancellation loop. This division makes it easy to evaluate the contribution of each loop and debug any possible design mistakes. However, the loading effect of each loop on the other one must be considered. Regarding the loading effect of the second loop on the first one, the input capacitances of OP2 does not have any effect on stability of the first loop since the drain of $M_1$ (where OP2 is connected to)
The loading effect of $M_2$ on the output pole of OP1 must be considered since this node causes one of the dominant poles.

To start designing each loop, first, the AC signal path must be designed to guarantee the target specifications (the PI model for transistors is used). In this design stage, the target specifications include achieving enough loop gain for each loop to obtain enough accuracy, enough bandwidth, and enough phase margin to guarantee the stability. Also, the effect of negative feedback on changing the mentioned specifications must be studied. To do so, the asymptotic gain approach can be used. To apply this approach to the potential control loop, a test current source is placed between the drain and source of $M_1$. Then, $g_{m1}$ is swept between 0 and its actual value while the closed loop pole/zero response is observed. This method gives all the frequency changes of poles/zeros from the loop response to the closed-loop situation. Stability is guaranteed if there is an acceptable margin between the dominant poles and the right-half plane.

After designing the AC signal path, PI models are replaced with self-biased transistors. As it is shown in Fig. 4.4, a self-biased transistor determines its own $V_{GS}$ through a negative feedback loop to meet the required $I_{DS}$ and $V_{DS}$. The capacitors in the figure are only decoupling capacitors and have large values. In this design stage, the noise performance can be optimized and all the target specifications from the previous step must be double-checked.

In the next step, the negative feedback loop of the self-biased model must be removed and all the transistors must be nullified. Fig. 4.5 shows a nullified transistor model. Considering the figure, if the source is connected to ground,
the voltages at the gate and drain terminals (labeled with Gate and Drain in the figure) will be zero. This is because of the polarity of the voltage sources $V_{GS}$ and $V_{DS}$. Also, no current will pass through $R_D$ because of the current source $I_D$. Using this model, each transistor stays at its operating point under any circumstances.

Finally, all the voltage and current sources that are added to the circuit in the previous step for nullification must be moved and merged to minimize the amount of voltage and current sources.
Chapter 5

Simulation Results and Discussions

In this chapter, the simulation results of all the critical AC and transient analyses on the proposed potentiostat are presented. Except for Section 5.5, the results are given for the worst case where the sensor current is at its minimum value of 10nA (i.e. $R_{WE}=60\text{M}\Omega$). In Section 5.5, the results are presented for the case in which the sensor current is at its maximum value of $1\mu\text{A}$ (i.e. $R_{WE}=600\text{k}\Omega$). The notations of the previous chapter is used for transistors, currents and voltages.

5.1 Accuracy, Loop gain and Closed-loop gain

As explained in the previous chapter, the potential-control loop has to guarantee that $V_{\text{cell}}$ accurately tracks $V_{\text{ref}}$. This can be tested by checking the loop gain, closed-loop gain, and transfer function of $V_{\text{cell}}/V_{\text{ref}}$, which are plotted in Fig. 5.1–5.3, respectively. As seen in Fig. 5.1, a unity-gain bandwidth (UGBW) of 11.2 Hz with 90 degree phase margin is achieved. Note that in order to obtain Fig. 5.1, a test current source is located between drain and source of transistor $M_1$ while $g_{m1}$ was set to zero, and the multiplication of the gate voltage of $M_1$ and the actual $g_{m1}$ value is considered as the output. For Fig. 5.2 and Fig. 5.3, a test voltage source is applied to the input of OP1, and $I_F$ and $V_{\text{cell}}/V_{\text{ref}}$ are considered as the output, respectively.

Since the valuable data exists in the output current of the sensor, it is worthwhile to study the case where a test current source is located in the sensor and $I_F$ is the output. Fig. 5.4 depicts the result. As expected, $I_F$ is equal to the sensor current for frequencies less than UGBW. Using the same
setup, Fig. 5.5 is obtained showing the output current of the entire circuit. The phase margin can be calculated as 135 degree.

![Simulation Results and Discussions](image)

**Figure 5.1.** Loop gain frequency response of the potential-control loop.

![Simulation Results and Discussions](image)

**Figure 5.2.** Closed-loop frequency response of the potential-control loop.
5.1. ACCURACY, LOOP GAIN AND CLOSED-LOOP GAIN

Figure 5.3. Frequency response of the transfer function $V_{\text{cell}}/V_{\text{ref}}$.

Figure 5.4. Closed-loop frequency response of the potential-control loop where a test current source is located inside the sensor.
5.2 Pole and Zero Analysis

The pole and zero characteristics are studied in this section. First, the potential-control loop is analyzed by applying a test voltage source to the input of OP1 while $I_F$ is considered as the output. The critical loop poles and zeros (not closed-loop) can be found in Table 5.1. The first dominant pole and zero are generated by the working electrode. The second pole and zero are coming from the counter electrode which are so close in frequency. Finally, the third pole is caused by the output node of OP1.

<table>
<thead>
<tr>
<th>Poles (Hz)</th>
<th>Zeros (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-2.77 m</td>
<td>-15.9 k</td>
</tr>
<tr>
<td>-159.1 k</td>
<td>-158.2 k</td>
</tr>
<tr>
<td>-259.1 k</td>
<td></td>
</tr>
</tbody>
</table>

The same analysis is carried out for the closed-loop case and the result can be seen in Table 5.2. The dominant loop pole is moved to higher frequencies
increasing the stability. However, the dominant loop zero is moved toward lower frequencies causing the noise to be amplified at low frequencies. The noise analysis results that will be given later shows that the circuit meets the noise requirements.

<table>
<thead>
<tr>
<th>Table 5.2. Critical closed-loop poles and zeros of the potential-control loop: test source at the input</th>
</tr>
</thead>
<tbody>
<tr>
<td>Poles (Hz)</td>
</tr>
<tr>
<td>-11.4</td>
</tr>
<tr>
<td>-259.3 k</td>
</tr>
<tr>
<td>-5.6 +/- 0.82i M</td>
</tr>
</tbody>
</table>

Table 5.3 gives the closed-loop result where a test current source is located inside the sensor while $I_F$ is considered as the output. Since the test source has to be placed in parallel with the working electrode impedance, the dominant zero coming from this electrode can not be seen. As seen in the table, the dominant pole is still far from the right-half plane guaranteeing the stability.

<table>
<thead>
<tr>
<th>Table 5.3. Critical closed-loop poles and zeros of the potential-control loop: test source in the sensor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Poles (Hz)</td>
</tr>
<tr>
<td>-11.4</td>
</tr>
<tr>
<td>-259.3 k</td>
</tr>
<tr>
<td>-5.6 +/- 0.82i M</td>
</tr>
</tbody>
</table>

Finally, Table 5.4 summarizes all the poles and zeros of the entire circuit where a test current source is applied to the sensor while the output current is considered as the output.

<table>
<thead>
<tr>
<th>Table 5.4. All the poles and zeros of the entire circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Poles (Hz)</td>
</tr>
<tr>
<td>-11.4</td>
</tr>
<tr>
<td>-159.0 k</td>
</tr>
<tr>
<td>-160.5 k</td>
</tr>
<tr>
<td>-6.99 +/- 363.5i k</td>
</tr>
<tr>
<td>-391.4 +/- 977.0i k</td>
</tr>
<tr>
<td>-1.28 M</td>
</tr>
<tr>
<td>-1.2 +/- 0.69i M</td>
</tr>
<tr>
<td>-5.6 +/- 0.36i M</td>
</tr>
</tbody>
</table>
5.3 Transient Response

A time domain analysis is performed in this section. While $I_F$ is 10nA, a pulse-shape test signal with 1nA amplitude is applied to the sensor. The critical node voltages and branch currents that are shown in Fig. 5.6 (i.e., $I_F$, $I_{OUT}$, $V_{CELL}$, and $V_{CONTROL}$) are plotted which can be found in Fig. 5.7–5.10, respectively. As expected, there is a one-to-one relation between the sensor current (Fig. 5.7) and the output current (Fig. 5.8). Fig. 5.9 shows the accuracy in biasing the sensor with $V_{ref}=1.2$. Finally, Fig. 5.10 shows the proper functionality of the error-tracking amplifier OP2.

![Figure 5.6](image)

**Figure 5.6.** Critical node voltages and branch currents that are simulated in this section.

![Figure 5.7](image)

**Figure 5.7.** Transient Response of $I_F$. 
5.3. TRANSIENT RESPONSE

Figure 5.8. Transient Response of $I_{OUT}$.

Figure 5.9. Transient Response of $V_{CELL}$.

Figure 5.10. Transient Response of $V_{CONTROL}$.
5.4 Noise Analysis

A noise analysis is carried out in this section to find the major noise contributors. For the first case, a test voltage source is applied to the input of OP1 and $I_F$ is considered as the output. The results can be found in Table 5.5. The contribution values less than 1pV are not listed in the table. As expected, the most contribution comes from the flicker noise of input transistors $M_{3,4}$ and $M_{6,7}$. The total input referred noise calculated from 10mHz to 100Hz is 26.6µV. In the second case, the output current is analyzed while a test current source is located in the sensor. Table 5.6 summarizes the results. For this case, the total input referred noise calculated from 10mHz to 100Hz is 27nV.

### Table 5.5. Noise analysis result of the potential-control loop

<table>
<thead>
<tr>
<th>Device</th>
<th>Noise Type</th>
<th>Contribution (V)</th>
<th>% of Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>M3,4</td>
<td>flicker</td>
<td>1.5 n</td>
<td>30.6</td>
</tr>
<tr>
<td>M6,7</td>
<td>flicker</td>
<td>1.07 n</td>
<td>15.5</td>
</tr>
<tr>
<td>M12,13</td>
<td>flicker</td>
<td>0.37 n</td>
<td>1.93</td>
</tr>
<tr>
<td>M10,11</td>
<td>flicker</td>
<td>0.29 n</td>
<td>1.17</td>
</tr>
<tr>
<td>M5</td>
<td>flicker</td>
<td>0.25 n</td>
<td>0.89</td>
</tr>
<tr>
<td>M8,9</td>
<td>flicker</td>
<td>0.23 n</td>
<td>0.75</td>
</tr>
<tr>
<td>$R_{RE}$</td>
<td>termal</td>
<td>36.5 p</td>
<td>0.02</td>
</tr>
<tr>
<td>$R_{SOURCE}$</td>
<td>termal</td>
<td>3.25 p</td>
<td>0</td>
</tr>
<tr>
<td>$R_{WE}$</td>
<td>termal</td>
<td>1.64 p</td>
<td>0</td>
</tr>
<tr>
<td>$R_{S1}$</td>
<td>termal</td>
<td>1.45 p</td>
<td>0</td>
</tr>
</tbody>
</table>

### Table 5.6. Noise analysis result of the entire circuit

<table>
<thead>
<tr>
<th>Device</th>
<th>Noise Type</th>
<th>Contribution (V)</th>
<th>% of Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>M3,4</td>
<td>flicker</td>
<td>1.44 n</td>
<td>31.3</td>
</tr>
<tr>
<td>M6,7</td>
<td>flicker</td>
<td>0.98 n</td>
<td>14.6</td>
</tr>
<tr>
<td>M12,13</td>
<td>flicker</td>
<td>0.37 n</td>
<td>2.15</td>
</tr>
<tr>
<td>M10,11</td>
<td>flicker</td>
<td>0.26 n</td>
<td>1.03</td>
</tr>
<tr>
<td>M8,9</td>
<td>flicker</td>
<td>0.21 n</td>
<td>0.68</td>
</tr>
<tr>
<td>M5</td>
<td>flicker</td>
<td>0.14 n</td>
<td>0.33</td>
</tr>
<tr>
<td>M1,2</td>
<td>flicker</td>
<td>0.12 n</td>
<td>0.25</td>
</tr>
<tr>
<td>$R_{RE}$</td>
<td>termal</td>
<td>35 p</td>
<td>0.02</td>
</tr>
<tr>
<td>$R_{SOURCE}$</td>
<td>termal</td>
<td>3.11 p</td>
<td>0</td>
</tr>
<tr>
<td>$R_f$</td>
<td>termal</td>
<td>2.02 p</td>
<td>0</td>
</tr>
<tr>
<td>$R_{WE}$</td>
<td>termal</td>
<td>1.56 p</td>
<td>0</td>
</tr>
<tr>
<td>$R_{S1}$</td>
<td>termal</td>
<td>1.39 p</td>
<td>0</td>
</tr>
</tbody>
</table>
5.5 Sensor Current Variation

In this section, all the critical AC and transient analyses are carried out for the case in which the sensor operates at its maximum current of 1 µA (i.e. $R_{WE}=600 \, \text{k}\Omega$).

5.5.1 Accuracy, Loop gain and Closed-loop gain

Similar to Section 5.1, the loop gain, closed-loop gain, and transfer function of $V_{cell}/V_{ref}$, which are plotted in Fig. 5.11–5.13, respectively. As it can be seen in Fig. 5.11, UGBW is increased to 794.3 Hz compared with Section 5.1, and a phase margin of 92 degree is achieved. The enhancement of UGBW is due to the increase in the frequency of the dominant pole.

Fig. 5.14 depicts the result for the case where a test current source is located in the sensor and $I_F$ is the output. Finally, Fig. 5.15 shows the output current of the entire circuit. As seen in the figure, stability is guaranteed with 134 degree phase margin.

Figure 5.11. Loop gain frequency response of the potential-control loop.
Figure 5.12. Closed-loop frequency response of the potential-control loop.

Figure 5.13. Frequency response of the transfer function $V_{cell}/V_{ref}$. 
5.5. SENSOR CURRENT VARIATION

Figure 5.14. Closed-loop frequency response of the potential-control loop where a test current source is located inside the sensor.

Figure 5.15. Closed-loop frequency response of the entire circuit where a test current source is located inside the sensor.
5.5.2 Pole and Zero Analysis

Table 5.7 gives the loop poles and zeros of the potential control loop. As noticed, the dominant pole is moved to a frequency 100 times higher than that previously given in section 5.2. This is due to the 100 times decrease in $R_{WE}$. Also, the output pole of OP1 has moved to lower frequencies and determines the second dominant pole (note that this pole was the third dominant pole in section 5.2). The reason is that the output current of the sensor which directly biases $M_1$ has increased 100 times. Thus, $C_{gs1}$ which contributes to the output pole of OP1 has increased accordingly. The third dominant pole is coming from the counter electrode for which the frequency has not changed. The first and second dominant zeros are caused by the working and counter electrode, respectively.

Table 5.8 gives the critical closed-loop poles and zeros of the potential-control loop. Table 5.9 gives the closed-loop result where a test current source is located inside the sensor and $I_F$ is considered as the output. Finally, Table 5.10 summarizes all the poles and zeros of the entire circuit. As seen in the table, the frequency of the dominant pole has increased almost 70 times compared with section 5.2. Therefore, the stability is this case is much better.

### Table 5.7. Critical loop poles and zeros of the potential-control loop

<table>
<thead>
<tr>
<th>Poles (Hz)</th>
<th>Zeros (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-0.27</td>
<td>-15.9 k</td>
</tr>
<tr>
<td>-56.9 k</td>
<td>-158.1 k</td>
</tr>
<tr>
<td>-159.1 k</td>
<td></td>
</tr>
</tbody>
</table>

### Table 5.8. Critical closed-loop poles and zeros of the potential-control loop: test source at the input

<table>
<thead>
<tr>
<th>Poles (Hz)</th>
<th>Zeros (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-796.6</td>
<td>-0.26</td>
</tr>
<tr>
<td>-59.0 k</td>
<td>-6.9 +/- 6.0i M</td>
</tr>
<tr>
<td>-4.9 M</td>
<td></td>
</tr>
</tbody>
</table>

### Table 5.9. Critical closed-loop poles and zeros of the potential-control loop: test source in the sensor

<table>
<thead>
<tr>
<th>Poles (Hz)</th>
<th>Zeros (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-796.6</td>
<td>3.1 +/- 6.8i M</td>
</tr>
<tr>
<td>-59.0 k</td>
<td>-9.0 +/- 2.7i M</td>
</tr>
<tr>
<td>-4.9 M</td>
<td></td>
</tr>
</tbody>
</table>
5.5. SENSOR CURRENT VARIATION

Table 5.10. All the poles and zeros of the entire circuit

<table>
<thead>
<tr>
<th>Poles (Hz)</th>
<th>Zeros (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-806.8</td>
<td>-0.12 +/- 1.41i M</td>
</tr>
<tr>
<td>-30.4 k</td>
<td>-1.36 +/- 0.55i M</td>
</tr>
<tr>
<td>-5.99 +/- 363.1i k</td>
<td>-1.49 M</td>
</tr>
<tr>
<td>-392.8 +/- 969.2i k</td>
<td>1.6 M</td>
</tr>
<tr>
<td>-1.28 M</td>
<td>-2.43</td>
</tr>
<tr>
<td>-1.2 +/- 0.69i M</td>
<td>-2.43 +/- 2.81i M</td>
</tr>
<tr>
<td>-4.84 M</td>
<td>-6.14 +/- 0.89i M</td>
</tr>
<tr>
<td>-6.45 M</td>
<td></td>
</tr>
</tbody>
</table>

5.5.3 Transient Response

Similar to section 5.3, transient analyses are carried out for the critical nodes and branches. The results are plotted in Fig. 5.16–5.23. According to Appendix A, as the sensor current increases, the capacitance values of transistors $M_{1,2}$ increase. As seen in the figures, increase of capacitance values slows down the transient responses due to the increase in charging time of the capacitances.

![Figure 5.16. Rise time transient Response of $I_F$.](image-url)

![Figure 5.17. Fall time transient Response of $I_F$.](image-url)
Figure 5.18. Rise time transient Response of $I_{OUT}$.

Figure 5.19. Fall time transient Response of $I_{OUT}$.

Figure 5.20. Rise time transient Response of $V_{CELL}$. 
Figure 5.21. Fall time transient Response of $V_{CELL}$.

Figure 5.22. Rise time transient Response of $V_{CONTROL}$.

Figure 5.23. Fall time transient Response of $V_{CONTROL}$. 
5.6 Linearity and Mismatch Analysis

The calibration curve of the potentiostat is shown in Fig. 5.24. In this figure, a regression line is fitted over the simulation results in order to examine the accuracy and linearity. The figure reveals an overall accuracy of 0.02% with high linearity in reading out the sensor current. The accuracy can also be illustrated using the histogram shown in Fig. 5.25.

Mismatch parameters for the current-mirror transistors $M_1$ and $M_2$ were extracted from the statistical data of the process. The threshold voltage mismatch $\sigma_{V_T}=0.4\,\text{mV}$, and the beta mismatch $\sigma_{\beta}/\beta=0.2\%$. Fig. 5.26 demonstrates the validity of (4.5) under the worst case condition where a $3\sigma$ mismatch for both $V_T$ (=1.2mV) and $\beta$ (=0.6%) were applied to $M_1$ and $M_2$. The result indicates that (4.5) can estimate the simulation results with an accuracy better than 0.1%.

![Figure 5.24. Simulated calibration curve of the proposed potentiostat.](image)

![Figure 5.25. Histogram analysis.](image)
Fig. 5.27 demonstrates the linearity versus $V_T$-mismatch (Fig. 5.27 (a)), β-mismatch (Fig. 5.27 (b)) and temperature (Fig. 5.27 (c)). As it was expected from (4.5), this figure reveals that the linearity degrades mostly by increasing $\Delta V_T$ instead of $\Delta \beta$. Also, it can be noticed that temperature variations have the least influence on the linearity compared to $\Delta V_T$ and $\Delta \beta$. Accuracy in reading out the sensor current was also analyzed under the same mismatch condition and the result is summarized in Table 5.11. The worst case situation is considered where the minimum resolvable current is measured. As it can be seen in the table, the worst accuracy value belongs to the maximum $\Delta V_T$. Also, unlike the case for linearity, temperature has more effect on accuracy.
compared to $\Delta \beta$. As a final conclusion, among all the random sources of error, $\Delta V_T$ is the major source degrading both the linearity and accuracy.

Finally, Table 5.12 shows a result comparison with recent published potentiostats. As it can be seen in the table, although the proposed potentiostat employs more opamps compared to [5], it achieves higher linearity and accuracy at lower power consumption. In comparison with [4], the magnitude of $V_{cell}/V_{ref}$ and also the linearity are improved considerably. Finally, compared to [13] with equal bandwidth, the proposed topology shows better noise performance and less power consumption. Although this work is mostly compared to other works’ measurement results, enough margin is considered, that if it is fabricated, the performance will not degrade significantly.
Part II

Optimization
Chapter 6

Proposed Optimization Algorithm

6.1 Introduction

Due to significant advances in semiconductor technology, the process of designing analog, mixed-signal and RF (AMS/RF) circuits is facing new complicated challenges. Analog design teams are currently facing increasing difficulties to satisfy design constraints in a short time-to-market, degrading the productivity of AMS/RF design. The solution is in the hands of electronic design automation (EDA) tools, which unfortunately, are not developed at same speed as nanometer technology.

Generally, the nature of optimization search space for AMS/RF circuits is multi-dimensional and highly non-linear. Hence, the EDA tools should be equipped with an efficient, and thus, fast optimization algorithm in order to properly explore the entire search space. A powerful candidate for such an optimization algorithm is the class of evolutionary algorithms (EAs) that has been already adopted for AMS/RF circuit design [14]. As instances of EAs, genetic algorithm (GA) was used for design of a direct-conversion receiver front-end [15], an inverter-based amplifier [16], a switched capacitor integrator and an RF low-noise amplifier [17]. Evolutionary programming (EP) was used for design of an RF diplexer [18], and genetic programming (GP) was employed for synthesis of various analog blocks [19] and opamp design [20]. Differential evolution (DE) was introduced in [21], used for parasitic-aware power amplifier design [22], synthesis of RF integrated passive components [23], and combined with GA for design of complex analog blocks [24]. Several modified EAs were also proposed in [25–27].

Basically, EAs are population-based global optimization algorithms that
are mostly inspired by nature. The basic procedure of these algorithms can be divided into three main steps: evaluation, selection and reproduction. In the evaluation step, all the members of the population are evaluated using a so-called fitness function. In AMS/RF design, the fitness function is composed of design objectives that have to be minimized (or maximized if the sign is changed), subject to some design constraints. This can be expressed as

\[
\begin{align*}
\text{Minimize } & f(\vec{x}) \\
\text{subject to : } & \\
& \vec{g}_i(\vec{x}) \leq 0, \quad i \in [1, n] \\
& \vec{h}_j(\vec{x}) = 0, \quad j \in [1, m] \\
& \text{and } \vec{x}_L \leq \vec{x} \leq \vec{x}_U
\end{align*}
\]  

where \( f(\vec{x}) \) is the fitness function, the vector \( \vec{g}_i(\vec{x}) \) represents \( n \) design constraints, \( \vec{h}_j(\vec{x}) \) is the vector of \( m \) equality constraints, \( \vec{x} \) is the design variables vector that is bounded between \( \vec{x}_L \) and \( \vec{x}_U \), as the lower and upper limits, respectively. Next, in the selection step, the population members are selected in proportion to their fitness values previously obtained. In the final step, the selected members produce a new population based on the reproduction scheme. This process is repeated until the convergence condition is satisfied.

In AMS/RF design, EAs can be used in the form of simulation-based or equation-based tools [28]. For evaluating the circuit performance, the former employs a circuit simulator while the latter uses the equations extracted from the circuit topology. Due to high precision performance evaluation and low setup time for new problems, simulation-based EAs have attracted more interest [28]. Nevertheless, since a circuit simulator has to be invoked several hundred times, a typical optimization process becomes computationally intensive and extremely time-consuming. This opens a research challenge to develop more efficient optimization algorithms speeding up the optimization process by decreasing the number of required simulations.

The Imperialist Competitive Algorithm (ICA) (also called Colonial Competitive Algorithm (CCA)) is a recently proposed global optimization algorithm, inspired by the socio-political phenomenon of imperialism [29]. Unlike other optimization algorithms that are inspired by nature and biology (e.g., GA [30], simulated annealing (SA) [31], ant colony [32], etc.), ICA is inspired by human social evolution. The ICA can be classified as an EA since it is governed by the mentioned main steps of EAs (i.e. evaluation, selection and reproduction), as it will be explained later.

Recently, ICA has been successfully applied to diverse engineering problems such as, mobile robot global localization [33], template matching in pattern recognition [34,35], data clustering [36], artificial neural network weights
optimization [37, 38], game theory [39], production management and scheduling problems [40–46], optimum design of skeletal structures [47] and urban traffic optimization [48]. Also, it has been employed for optimization in communication systems [49], design of a linear induction motor [50], a MIMO PID controller [51], and a fuzzy controller [52]. Several hybrid solutions have also been proposed such as CCA-GA [53], recursive ICA-GA [54], and ICA with chaos theory [55]. All these works that have been reported so far reveal that ICA is superior to conventional algorithms such as GA and particle swarm optimization (PSO). However, this superiority does not hold when dealing with multi-variable multi-objective optimization problems, and the algorithm presented in [56] is the first time this problem is addressed.

The MICAO (Modified Imperialist Competitive Algorithm for Analog Circuit Optimization) [57] presented in this chapter adapts the original ICA for high-dimensional optimization problems and proves its performance for analog circuit optimization. Since MICAO does not follow the socio-political phenomenon of imperialism, the terminology is changed accordingly.

### 6.2 Imperialist Competitive Algorithm

This section briefly introduces ICA and its implementation [29]. The flow diagram of ICA is presented in Fig. 6.1.

Like other EAs, it starts with an initial randomly-generated population. Each member of the population is called *country* defined by

$$
country_{(1 \times N)} = [p_1, p_2, \ldots, p_N]
$$

(6.2)

where $N$ is the number of optimization variables and $p_i$ is the $i$th variable. After generating the initial population, a *power* value will be calculated for each country using the cost function. Note that, the term *power* that is used in this section is a value inversely proportional to the cost value. After calculating the power, two groups are formed with user-defined sizes, namely *imperialists* and *colonies*. Imperialists are the most powerful countries of the initial population and the rest are the colonies. In order to form *empires*, all the colonies will be assigned to the imperialists in proportion to the power of each imperialist. In other words, the most powerful imperialist possesses the largest number of colonies. Fig. 6.2 illustrates the initial population and empires in ICA. Note that this is just a conceptual figure and in reality the empires’ territories have overlaps covering the whole search space.
Generating initial population

Generating empires

Assimilation

Is there any colony more powerful than its imperialist?

Yes

Replace the imperialist with that colony

Imperialistic competition

Collapse of empires with no colony

Convergence check?

Yes

Output

No

No

Generating initial population

Figure 6.1. Flow diagram of the original ICA.

Figure 6.2. Initial population in ICA: the more powerful an imperialist is, the more colonies it will possess.
6.2. IMPERIALIST COMPETITIVE ALGORITHM

In a real-world model, after creation of empires, colonies tend to follow their imperialists in different aspects (e.g., language, culture, politics, etc.) which is referred to as assimilation. This socio-political phenomenon is modeled by a process in which all the colonies in every empire start moving toward their imperialist (one step in each generation of the algorithm). Fig. 6.3 depicts the movement process in which the movement magnitude is defined as

\[ \| \vec{M} \| \sim U \left( 0, \beta \cdot \| \vec{D} \| \right) \]  \hspace{1cm} (6.3)

where

\[ \vec{M} = C'_{(1 \times N)} - C_{(1 \times N)} \]  \hspace{1cm} (6.4)

\[ \vec{D} = I_{(1 \times N)} - C_{(1 \times N)} \]  \hspace{1cm} (6.5)

\( C'_{(1 \times N)} \) and \( C_{(1 \times N)} \) are the new and old position of a colony, respectively, \( I_{(1 \times N)} \) is the position of imperialist, \( U \left( a, b \right) \) generates a random number with uniform distribution in the interval of \( [a, b] \), and \( \beta \) is a number greater than 1 to control the upper limit of movement magnitude. As it can be noticed in the figure, a random deviation is also incorporated in the direction of movement by \( \theta \sim U(-\theta_0, \theta_0) \) which improves the search ability of the algorithm.

After assimilation, it may happen that a colony becomes more powerful than its imperialist. If so, that colony will become the new imperialist of that empire, and from that generation on, the colonies of the empire will move toward their new imperialist.

Another real-world phenomenon that is realized in ICA corresponds to imperialistic competition between empires. Generally, empires tend to take control of other empires’ colonies in order to expand their territories. The competition starts with defining the total power of each empire as

\[ \text{Position of imperialist} \]
\[ \circ \text{New position of colony} \]
\[ \bullet \text{Old position of colony} \]

Figure 6.3. Assimilation in ICA.
\[ TC_i = f(I_i) + \alpha \cdot \left( \frac{1}{N_i} \sum_{j=1}^{N_i} f(C^i_j) \right) \]  

(6.6)

where for \( i \)th empire, \( TC_i \) represents the total power, \( I_i \) is the imperialist, \( C^i_j \) is the \( j \)th colony, and \( N_i \) is the number of colonies; \( f() \) is the cost function, and \( \alpha \) is a user-defined factor in an interval of \([0, 1]\) to control the impact of colonies’ power versus imperialist’s power on total power of an empire. After calculating the total power of all empires, a procedure similar to cost weighting roulette wheel technique [58] is utilized. As a result, the empire with the highest power has the greatest chance to be selected, and thus, possesses some of the weakest colonies of the weakest empires.

Due to the imperialistic competition, gradually, weak empires become weaker, and eventually, they collapse when all their colonies are possessed by other empires. Finally, there will be only one empire in which the imperialist and all the colonies have the same power. This is the convergence criterion to stop the algorithm.

6.3 The Proposed MICAO Algorithm

Although ICA is efficient and effective, when it comes to high-dimensional optimization problems such as sizing analog circuits, it cannot show an acceptable performance as it will be demonstrated in chapter 7. This shortcoming is addressed in the MICAO tool by proposing a modified ICA as shown in Fig. 6.4.

6.3.1 Generating Initial Groups of Countries

Fig. 6.5 illustrates the initial population, where two groups of countries are introduced, namely developed countries and developing countries. As opposed to “imperialist” and “colony” in ICA, this terminology is inspired by the modern-history where no specific territories (empires) are assumed. To create the initial groups, first, an initial population with \( N_{pop} \) countries (each a \( 1 \times N \) vector) is generated and evaluated using the cost function. Then, \( N_i \) number of the most powerful countries form the developed countries’ group whereas the rest form the developing countries’ group with a size of \( N_j \) (so it holds \( N_{pop} = N_i + N_j \)).

A major benefit of having countries’ groups is that the developing countries take advantage of several developed countries as opposed to the only imperialist of the empire in ICA. As a result, assume that there are several
6.3. THE PROPOSED MICAO ALGORITHM

Generating initial population

Generating groups of countries

Selection

Reform

Revolution

Are any developing countries qualified to enter the developed countries’ group?

No

Yes

Exchange the qualified developing and weak developed countries

Convergence check?

Yes

No

Output

Figure 6.4. Flow diagram of MICAO.

Developing countries’ group

Developed countries’ group

Most powerful

Weakest

Figure 6.5. Initial population in MICAO.
weak developed countries which satisfy different sets of constraints. It may occur that by reforming a developing country with reference to those weak developed countries, a powerful solution will be found that satisfies all those sets of constraints.

6.3.2 Selection

The selection operator models the following assumption: one of the key factors of development for developing countries is to learn from the experiences of country role models (developed countries); developing countries have the right to select their country role models. To start the selection process after generating the initial groups of countries, some candidates from the developed countries’ group are selected using the cost-weighting roulette-wheel technique \cite{58}. Since selecting two candidates has shown a good result in our case studies, it will be assumed the case for all the calculations in this chapter. For the first candidate, as it is shown in Figure 6.6, the more powerful a developed country is, the more chance it has to be selected (this candidate is named the powerful candidate). On the other hand, for the second candidate, the weakest developed country has the greatest chance to be selected (this candidate is named the weak candidate).

\begin{figure}[h]
\centering
\includegraphics[width=0.5\textwidth]{figure6.6.png}
\caption{Selecting two candidates from developed countries’ group.}
\end{figure}
6.3.3 Reform

One major issue with the assimilation policy in the original ICA is that a weak imperialist can mislead all the colonies of the empire into a weak region of the search space. Accordingly, a lot of colonies as potential solutions are wasted degrading the search efficiency of the algorithm. This issue becomes even worse in high-dimensional search spaces for which powerful imperialists may not be found in several consecutive generations. The mentioned shortcoming is addressed here by detecting weak developed countries (as well as the powerful ones) using the selection operator complemented with a proposed modified assimilation policy called reform. The reform operator is implemented based on the assumption that, in modern-history, developing countries improve their social, economic and etc. conditions by following or avoiding the policies of developed countries. This phenomenon is translated into two principal rules taking advantage of the candidates that were selected in the previous subsection: 1) moving toward the powerful candidate, 2) moving away from the weak candidate. The latter fits especially analog circuit design where the search space does not contain sharp peaks and valleys, and thus, a weak point can be an indicator of a weak region surrounding it.

As it is shown in Fig. 6.7, first, a developing country is randomly selected from the developing countries’ group. Then, it moves one step either toward the powerful candidate (see Fig. 6.7 (a)), or away from the weak candidate (see Fig. 6.7 (b)). As seen in the figures, this is decided by the random selector \( S \), as it will be explained later. This process is repeated for a certain percentage of developing countries in the group. The new position of a developing country can be formulated as

\[
C'_{(1 \times N)} = C_{(1 \times N)} + K_{(1 \times N)} \otimes \vec{D}_S \quad (6.7)
\]

where \( C'_{(1 \times N)} \) and \( C_{(1 \times N)} \) are the new and old position of a developing country, respectively, the operator “\( \otimes \)” indicates an element-by-element multiplication, and \( K_{(1 \times N)} \) is a vector of random elements each with a uniform distribution of \( U (0, \lambda) \). \( \lambda \) is a user-defined factor to control the upper limit of the developing country’s new position. The vector \( \vec{D}_S \) in (6.7) can be expressed as

\[
\vec{D}_S = (-1)^S \cdot \left(I_{S_{(1 \times N)}} - C_{(1 \times N)} \right) \quad (6.8)
\]

where \( S \) is the random selector which is either 0 or 1 with equal chances; so, if \( S = 0 \), \( I_{0_{(1 \times N)}} \) denotes the powerful candidate, otherwise if \( S = 1 \), \( I_{1_{(1 \times N)}} \) is the weak candidate.
Movement Angle

In ICA, a random angle is added to the direction of movement in order to increase the search efficiency. However, it is computationally expensive (almost unfeasible) to take each step with a pre-specified angle in high-dimensional search spaces. To cope with this issue, a random perturbation is proposed to be added to the new position of some selected colonies [59]. However, it is not guaranteed that the colony will not violate the principal goal of assimilation (i.e. getting near to the imperialist in each step) after adding the random perturbation. Another approach addressing the mentioned problem is proposed in this work.

Considering Fig. 6.7, the angle between $\vec{M}$ and $\vec{D}_S$ can be expressed by

$$\theta = \cos^{-1} \left( \frac{(\vec{D}_S \cdot \vec{M})}{\|\vec{D}_S\| \cdot \|\vec{M}\|} \right). \quad (6.9)$$

Note that this angle is inherently random because of the random behavior of $\vec{M}$ (see (6.7)). The idea is to calculate $\theta$ after a step is taken and to reject the new developing countries that have a $\theta$ beyond a user-defined range $(-\theta_0, \theta_0)$. In our case studies, a $\theta_0$ of 45 degree showed an acceptable result. Employing this approach, no violation from the principal rules of the reform operator will occur.
6.3.4 Revolution

The idea of revolution operator has been introduced in [40] for another application. However, the mathematical formulation required for implementation of the operator is not presented. Therefore, the original ICA will be used for comparisons in our case studies. Basically, the revolution operator is employed to overcome a substantial shortcoming of ICA in introducing information that does not exist in the current population (similar to the mutation operator in GA). To further elaborate this issue in ICA, assume that the imperialist is located in a local minimum leading all its colonies in that direction; to escape from the local minimum, there is hope that the colonies will find a more powerful point than the local minimum in the vicinity; if so, the successful colony will become the new imperialist saving the empire from converging to the local minimum; however, the disadvantage of this strategy is that the search is only limited to the vicinity of the local minimum and not to the entire search space.

In MICAO, revolution causes a sudden change in the position of a developing country with the hope of becoming a more powerful country. By using this operator in the proposed algorithm, a premature convergence to the position of developed countries is prevented before sampling the entire search space. To start the revolution, in each generation, some developing countries are selected based on the revolution rate. Note that these countries will not be considered for the reform operator. The revolution rate is the fraction of the total number of design variables (i.e. $N_j \times N$) that are randomly selected to be revolutionized. During this process, some variables may exceed the design variable boundaries causing more computational effort to fix them again. To solve this problem, the revolutionized variable of a developing country can be formulated as

$$c'_i = v \cdot (c_i + m_i) + (1 - v) \cdot (c_i - l_i) \quad (6.10)$$

where $c'_i$ and $c_i$ are the $i$th variable of the revolutionized and main developing country, respectively, and $v$ is randomly 1 or 0 with equal chances, in order to select either the first or the second term. The variables $m_i$ and $l_i$ in (6.10) are given by

$$m_i \sim U (0, u_i - c_i) \quad (6.11)$$
$$l_i \sim U (0, c_i - l_i) \quad (6.12)$$

where $u_i$ and $l_i$ denote upper and lower boundary for the $i$th variable of the developing country, respectively. It can be concluded from (6.10) that the revolutionized variable is always within the design boundaries.
6.3.5 Exchanging Qualified Developing and Weak Developed Countries

After reform and revolution, the power of all developing countries must be re-calculated. This is to see whether there is any new developing country that has more power than the weakest member of the developed countries’ group, and if so, they will be exchanged.

6.3.6 Convergence

Finally, the algorithm is checked for convergence. The following conditions can be set to stop the algorithm: 1) after a certain number of generations; 2) if the mean power of the developed countries’ group does not change considerably after a certain number of generations.

6.3.7 Comparison with ICA and GA

The functionalities and differences between the main operators in the candidate algorithms can be summarized as follows:

- **Initial population:** It is composed by a population of chromosomes in GA, and by countries that after evaluation will be divided into imperialists and colonies in ICA. In MICAO, the countries will be initially divided into two groups of developed and developing countries.

- **Evaluation:** The same cost function is used to calculate the cost value in GA and the power value in ICA and MICAO, which will be given in section 7.1. Also, the combination of MATLAB, as the optimization engine, and HSPICE, as the circuit simulator, is used.

- **Selection:** In GA, based on the cost value, chromosomes are selected from the mating pool to produce offspring. In ICA, an empire is selected based on its total power and win the weakest colony of the weakest empire. In MICAO, however, a developed country is selected per each movement of a developing country.

- **Reproduction:** In GA, two operators of crossover and mutation are used to produce offspring from parent chromosomes. In ICA, new countries are produced by the assimilation process (counterpart of crossover in GA). The reform and revolution (counterparts of crossover and mutation in GA, respectively) are the sources of reproduction in MICAO.
Chapter 7
Optimization Results and Comparisons

In this chapter, MICAO, ICA and GA are used for sizing a two-stage telescopic OTA (case study 1) and the proposed potentiostat (case study 2). Additionally, optimization results of two mathematical benchmarks are presented. The purpose is to evaluate the capability of the under-study algorithms in constraint satisfaction and execution time. To determine each algorithm parameters, several simulations with different sets of parameters are performed and the best set is selected. Due to the partially-random nature of the candidate algorithms, three simulations are carried out for each algorithm in each case study and the average is considered (the total run time of the three simulations are reported).

For the first case study, for ICA, a total number of 100 countries divided into 20 imperialists and 80 colonies is used; but for the second case study, 200 countries divided into 40 imperialists and 160 colonies are chosen; $\alpha$ is set to 0.1, $\beta$ is 2, and $\theta_0$ is 45 degree.

For MICAO in the first case study, $N_{\text{pop}}$ is 100 which is composed of an $N_i$ of 10 and an $N_j$ of 90; for the second case study however, an $N_{\text{pop}}$ of 200 divided into an $N_i$ of 20 and an $N_j$ of 180 is used; $\lambda$ is 2 and $\theta_0$ is 45 degree; the developing countries’ group is treated such that 50% is considered for reform while revolution is applied to the other 50%; the revolution rate is 80%.

As mentioned earlier, GA is employed as a reference to which the other two algorithms are compared. For the first case study, the population size of GA is 100 including 10 elites which was increased to a population size of 200 with 20 elites for the second case study; the crossover operator is applied to 50% of the population whereas the other 50% is purely mutated with mutation rate of 80%.

All the test circuits are designed on a 2.66 GHz dual core PC with 4 GB
RAM. Reported run times are the sum of HSPICE simulation time, MATLAB processing time and the communication time between them. In order to speed up the HSPICE simulations, the batch mode simulation is used. Hence, instead of simulating the population members separately, they are simulated all at once in each generation. The total run time of the batch mode versus the normal mode are reported.

7.1 Cost function

The global optimization process carried out in this paper relies on minimizing the cost function $C(X)$ given by

$$C(X) = \frac{1}{n} \cdot \sum_{i=1}^{n} F(w_i \cdot \hat{f}_i(X))^2 + \sum_{j=1}^{k} w_j \cdot P_j(X)$$  \hspace{1cm} (7.1)

where

$$F(Y) = 1 - \frac{1}{e^Y}$$  \hspace{1cm} (7.2)

$$\hat{f}_i(X) = \frac{f_i(X) - \text{desired}_i}{\text{acceptable}_i - \text{desired}_i}$$  \hspace{1cm} (7.3)

$n$: number of objectives
$k$: number of constraints
$\hat{f}_i()$: normalized deviation error of $i$th objective from the desired value ($\text{desired}_i$)
$P_j()$: a set of user-defined penalty factors
$w_i$: weight coefficient for objective functions
$w_j$: weight coefficient for constraint functions.

Considering (7.1), the cost function $C(X)$ is composed of two parts; the first part, $\frac{1}{n} \cdot \sum_{i=1}^{n} F \left( w_i \cdot \hat{f}_i(X)^2 \right)$, is used to optimize the objectives (e.g. power consumption, area, etc.) as well as some of the constraints (e.g. DC gain $\geq 70$ dB) that are treated as extra objectives; the second part, $\sum_{j=1}^{k} w_j \cdot P_j(X)$, is a weighted summation of user-defined penalty factors to handle another type of constraints such as biasing, pole/zero placement, etc. For objective optimization, the combination of an exponential-type function and a normalized error function is utilized. First, by means of (7.3), the normalized deviation of the $i$th objective from the desired value is calculated using the user-defined
desired, and acceptable values. Then, (7.2) is utilized to smooth (7.3) near the desired value. This is to avoid introducing highly steep regions near desired values and thus keep the algorithm from converging too fast to the early constraint-satisfying regions. Fig. 7.1 compares the cases with and without the exponential-type function when \( f_i(x) = x, \) desired\(_i\)=0 and acceptable\(_i\)=0. As it is clear in the figure, the exponential-type curve converges to the minimum value of 0 smoother than the other function. The user can also control the relative importance of competing objectives and constraints by adjusting the scalar weights \( w_i \) and \( w_j \), respectively.

### 7.2 Case Study 1: Two-Stage Telescopic OTA

The two-stage telescopic operational transconductance amplifier (OTA) shown in Fig. 7.2 is designed in a 0.18 \( \mu \)m CMOS process. The design variables for this problem are given in Table 7.1. Along with the typical symmetric matching constraint, the following expression must be satisfied to avoid systematic offset:

\[
y = \frac{1}{1 + e^{-x^2}}
\]

Figure 7.1. Exponential-type versus normal cost function.

<table>
<thead>
<tr>
<th>Design variables</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>( W_{2,4,5,8,9} )</td>
<td>[0.5-90]-( \mu )m</td>
</tr>
<tr>
<td>( L_{2,4,5} )</td>
<td>[0.5-20]-( \mu )m</td>
</tr>
<tr>
<td>( V_{b_{1,2}}, V_{cm} )</td>
<td>[0-3.3]-V</td>
</tr>
<tr>
<td>( C_c )</td>
<td>[1f-100p]-F</td>
</tr>
</tbody>
</table>
In order to reduce the computational tasks to satisfy (7.4), \( L_{9,12,7,11} \) are fixed at 0.5 \( \mu \)m, and also the following relations are set \( W_{12} = 2 \times W_7 \), and \( W_9 = W_{11} \). Moreover, length and width of \( M_{10} \) are fixed at 0.5 \( \mu \)m and 0.75 \( \mu \)m, respectively, allowing \( W_9 \) to set the bias current for the first stage individually. Finally, \( VDD \) is set to 3.3 V, \( I_{\text{ref}} \) is 5 \( \mu \)A and \( C_L \) is 10 pF.

Here, 12 parameters are used as design variables which along with the advanced frequency compensation technique place a great challenge on the candidate algorithms. Moreover, the following specifications dealing with pole/zero placement are added targeting a single-pole frequency response: 1) the dominant pole has to be greater than a certain frequency while all other non-dominant poles are placed beyond UGBW; 2) all the right- and left-half plane (RHP and LHP) zeros have to be transferred beyond UGBW. This pole/zero placement results in a single-pole frequency compensated OTA.

Due to several typical trade-offs between constraints (e.g. between DC gain and UGBW, or power dissipation and UGBW), a linear Figure-of-Merit (FoM) is defined for a proper comparison between different algorithms:

\[
(W/L)_9 \cdot (W/L)_{12} = 2 \cdot (W/L)_7 \cdot (W/L)_{11}.
\] (7.4)
7.2. CASE STUDY 1: TWO-STAGE TELESCOPIC OTA

\[
F_{oM} = k \cdot \frac{DC \text{ Gain} \cdot UGBW \cdot Swing}{Power \cdot Area}
\]  

(7.5)

where \( k \) is a normalization factor. The final simulation results are summarized in Table 7.2 after evaluation of 5000 individuals for each algorithm in each run. As it can be seen in the table, ICA slightly violates the phase margin constraint and cannot meet the desired UGBW, and so, its FoM is not considered. These violations reveal the shortcoming of ICA mentioned in Sections 6.3.3, 6.3.4. Given the equal time as ICA, GA and the proposed algorithm cope with all the constraints properly. However, the proposed algorithm achieves lower power consumption, larger signal swing and UGBW, and thus the best FoM. It is worthwhile to see in Fig. 7.3 the frequency response of the circuit designed with the proposed algorithm showing its capability to handle the new added constraints for pole/zero placement.

---

**Figure 7.3.** Frequency response for case study 1 designed by the proposed algorithm.
Table 7.2. Simulation Results for Case Study 1

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Constraints</th>
<th>ICA</th>
<th>GA</th>
<th>MICAO</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC gain (dB)</td>
<td>≥70</td>
<td>87.8</td>
<td>124.83</td>
<td>109.3</td>
</tr>
<tr>
<td>UGBW (MHz)</td>
<td>≥2</td>
<td>0.92</td>
<td>2.32</td>
<td>5.13</td>
</tr>
<tr>
<td>Phase margin (deg.)</td>
<td>[50-80]</td>
<td>95.5</td>
<td>70.57</td>
<td>52.4</td>
</tr>
<tr>
<td>Signal swing (V)</td>
<td>≥2.8</td>
<td>2.87</td>
<td>2.85</td>
<td>2.87</td>
</tr>
<tr>
<td>CMRR (dB)</td>
<td>≥100</td>
<td>113.8</td>
<td></td>
<td>124.90</td>
</tr>
<tr>
<td>Dominant pole (Hz)</td>
<td>≥1</td>
<td>37.2</td>
<td>1.12</td>
<td>24.10</td>
</tr>
<tr>
<td>All non-dominant poles (MHz)</td>
<td>≥UGBW</td>
<td>5.41</td>
<td>4.052</td>
<td>5.296</td>
</tr>
<tr>
<td>All LHP and RHP zeros (MHz)</td>
<td>≥UGBW</td>
<td>6.07</td>
<td>4.047</td>
<td>5.409</td>
</tr>
<tr>
<td>Area (µm²)</td>
<td>minimize</td>
<td>662</td>
<td>1403</td>
<td>435</td>
</tr>
<tr>
<td>Power consumption (µW)</td>
<td>minimize</td>
<td>306.0</td>
<td>760.0</td>
<td>397.9</td>
</tr>
<tr>
<td>FoM ((V/V).Hz.V/W.m²)</td>
<td>—</td>
<td>0.10</td>
<td>0.24</td>
<td></td>
</tr>
<tr>
<td>Run time (batch mode) (s)</td>
<td>1380</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\(^{a}\) Lowest frequency.
\(^{b}\) Run time (normal mode) = 4125 s.

7.3 Case Study 2: The Proposed Potentiostat

The proposed potentiostat in chapter 4 is designed in this section. A total number of 32 design parameters is considered and 80,000 individuals are evaluated in each run for each algorithm. Table 7.3 shows the final result where the FoM is defined as

\[
FoM = k \cdot \frac{DC\ Gain \cdot UGBW}{\text{Noise} \cdot VDS_{\text{mismatch}} \cdot \text{Power}}.
\] (7.6)

As it can be seen in the table, ICA failed to fully satisfy the biasing constraint and thus the corresponding AC responses are not reliable. Compared to GA, the proposed algorithm presents the best results in all the specification except for only the noise performance, and shows a remarkable FoM. In order to further evaluate the effectiveness of the proposed algorithm operators, their contributions were monitored for the last 100 generations and is illustrated in Fig. 7.4. As it can be concluded from the figure, since the optimization process is ending, the contribution of the revolution operator dominates.
Table 7.3. Simulation Results for Case Study 2

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Constraints</th>
<th>ICA</th>
<th>GA</th>
<th>MICAO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bias (^a)</td>
<td>all satisfied</td>
<td>—</td>
<td>done</td>
<td>done</td>
</tr>
<tr>
<td>DC gain (dB)</td>
<td>maximize</td>
<td>63.6</td>
<td>56.3</td>
<td>64.4</td>
</tr>
<tr>
<td>UGBW (kHz)</td>
<td>≥1</td>
<td>4.7</td>
<td>1.78</td>
<td>9.15</td>
</tr>
<tr>
<td>Noise (\mu V/\sqrt{Hz})</td>
<td>≤50</td>
<td>39.5</td>
<td>18</td>
<td>44.4</td>
</tr>
<tr>
<td>(V_{cell}/V_{ref})</td>
<td>maximize</td>
<td>0.9995</td>
<td>0.9998</td>
<td>0.99997</td>
</tr>
<tr>
<td>(I_{out}/I_{in})</td>
<td>maximize</td>
<td>0.975</td>
<td>0.966</td>
<td>0.976</td>
</tr>
<tr>
<td>(V_{DSmismatch}) (mV)</td>
<td>minimize</td>
<td>0.91</td>
<td>0.72</td>
<td>0.12</td>
</tr>
<tr>
<td>Power ((\mu W))</td>
<td>minimize</td>
<td>264.3</td>
<td>392.9</td>
<td>80.8</td>
</tr>
<tr>
<td>FoM (\left(\frac{V}{V/\sqrt{Hz}}\right)/V\cdot W)</td>
<td>—</td>
<td>0.002</td>
<td>0.35</td>
<td></td>
</tr>
</tbody>
</table>

Run time (batch mode) \(s\) 16560\(^b\)

\(^a\) \(V_{DS} > V_{GS} - |V_T|\)

\(^b\) Run time (normal mode) = 57600 s.

However, the selection/assimilation operator resulted in the notable decrease in cost value between generation 300 to 350.

Table 7.4 shows the result of designing the potentiostat using MICAO compared with the results of the traditional design already given in chapter 5. As it can be seen in the table, different target objectives are considered when designed with MICAO. This is done via increasing the corresponding coefficient of that target objective in the cost function. In the case that noise is the target objective, MICAO sacrifices the power consumption to minimize...
Table 7.4. Traditional design versus optimization algorithm

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Traditional Design (1)</th>
<th>MICAO (2)</th>
<th>MICAO (3)</th>
<th>MICAO (4)</th>
<th>MICAO (5)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Target objective</td>
<td>–</td>
<td>noise</td>
<td>power</td>
<td>noise,</td>
<td>accuracy</td>
</tr>
<tr>
<td>UGBW (kHz)</td>
<td>1</td>
<td>9.4</td>
<td>3.55</td>
<td>5.0</td>
<td>9.15</td>
</tr>
<tr>
<td>Noise ($\mu V/\sqrt{Hz}$)</td>
<td>26.6</td>
<td>20.0</td>
<td>94.4</td>
<td>20.2</td>
<td>44.4</td>
</tr>
<tr>
<td>$V_{cell}/V_{ref}$ (dB)</td>
<td>-2.5</td>
<td>-0.26</td>
<td>-0.78</td>
<td>-0.95</td>
<td>-0.26</td>
</tr>
<tr>
<td>$I_{out}/I_{in}$</td>
<td>0.94</td>
<td>0.90</td>
<td>0.92</td>
<td>0.93</td>
<td>0.97</td>
</tr>
<tr>
<td>$VDS_{mismatch}$ (mV)</td>
<td>0.15</td>
<td>0.08</td>
<td>0.19</td>
<td>0.33</td>
<td>0.12</td>
</tr>
<tr>
<td>Power ($\mu W$)</td>
<td>32</td>
<td>101</td>
<td>20</td>
<td>63</td>
<td>80</td>
</tr>
<tr>
<td>FoM</td>
<td>0.0029</td>
<td>0.20</td>
<td>0.011</td>
<td>0.011</td>
<td>0.08</td>
</tr>
</tbody>
</table>

the noise. The exact opposite situation occurs when power in the target. When noise and power are the targets, MICAO keeps the power between the two previous cases and minimizes the noise as low as the first case. In the final case where accuracy is the target, the best $V_{cell}/V_{ref}$ and $I_{out}/I_{in}$ are achieved. Note that in all the cases designed with MICAO, the UGBW is higher than that of the traditional design. For an overall comparison, the following FoM is defined

$$FoM = k \cdot \frac{UGBW \cdot (I_{out}/I_{in})}{Noise \cdot VDS_{mismatch} \cdot Power \cdot (V_{cell}/V_{ref})}.$$ (7.7)

The best FoM is 0.20 resulted by MICAO, which is considerably higher than that of the traditional design.

7.4 Mathematical Benchmark Functions

In this section, the speed factor is tested in terms of the number of generations required to reach an already-known global minimum. The under-study algorithms are compared using two mathematical benchmarks [58], namely:

$$f_1 = 0.5 + \frac{\sin^2 \sqrt{x^2 + y^2} - 0.5}{1 + 0.1(x^2 + y^2)}$$ (7.8)

$$f_2 = (x^2 + y^2)^{0.25} \sin \left(30 \left((x + 0.5)^2 + y^2\right)^{0.1}\right) + |x| + |y|$$ (7.9)
where $-\infty \leq x, y \leq \infty$ for both functions, and the global minimum for $f_1$ is -0.5231 and for $f_2$ is 0. The final result showing the minimization process is plotted for $f_1$ in Fig. 7.5 and for $f_2$ in Fig. 7.6. Considering GA and ICA in function $f_1$, it can be seen that GA finds the global minimum faster than ICA, but this occurs vice versa for function $f_2$. Nevertheless, the proposed algorithm reaches the global minimum faster than the other two algorithms in both $f_1$ and $f_2$. 
Part III

Conclusion and Future Work
Chapter 8

Conclusion

In order to overcome the systematic error problem in current-mirror-based potentiostats, a new topology was proposed. Due to the high-loop-gain error-cancellation loop, the potentiostat generates a precise copy of the sensor current eliminating the channel-length modulation effect. Analytical expressions verified by simulation in a 150nm CMOS process were presented to calculate the effect of systematic and random errors.

In order to optimize the design of the proposed topology, an optimization algorithm MICAO was proposed. The optimization algorithm took advantage of a modified imperialist competitive algorithm, which proved to be an effective approach for automated synthesis of analog circuits. The proposed algorithm exhibited a remarkable performance in searching the design space more efficiently than the original ICA and GA, and finding better solutions in the same run time as them. This was achieved by introducing the concepts of selection, reform, and adding the revolution operator. Due to the mentioned efficiency in search and according to the mathematical benchmarks, MICAO is more than 1.5 times faster than the other algorithms. This is essential for AMS/RF EDA tools, where the optimization engine has to repeatedly communicate with a circuit simulator.

Finally, the proposed optimization algorithm was applied for design of the proposed potentiostat topology. The results of the traditional design carried out in the first part of the thesis were compared with those of the optimization algorithm. The optimization algorithm resulted in an average of 25.8 times higher FoM compared to traditional design. The optimally-designed potentiostat shows high-accuracy, high-linearity, low-power, and low-noise features, which makes it a potential candidate for implantable biomedical devices.
8.1 Future Work

The proposed potentiostat is only one of the critical blocks in an implantable blood glucose monitoring system. To complete all the required circuit blocks of the system, the following approaches can be used: 1) connecting the potentiostat output to an RF front-end to send the sensor data out to an external RF reader; 2) connecting the potentiostat output to an implanted analog-to-digital converter which is connected to an RF front-end for sending the data out. Depending on which approach is used, the total power consumption and area will be affected, due to the different architecture for the RF front-end.

The system can be further improved by supplying the required power wirelessly. The power will be consumed to bias the electrochemical sensor, and the implanted circuitry (for glucose monitoring, the system is only needed to be switched on every 10min). Wireless power transfer will eliminate the need for changing the battery via surgery, which brings more comfort for patients.

Finally, this work can be completed by layout and fabrication. It is not expected to have major difference between the measurement and simulation results, due to enough margin from the specifications that is considered in the design process. If the actual electrochemical sensor is not available, the final chip can be also measured using chemical electrodes placed in a suitable electrolyte.
## Appendix A

### Transistors Sizes, DC Operating Points and Capacitances

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W/L</th>
<th>NF</th>
<th>VGS (V)</th>
<th>VT (V)</th>
<th>VDSsat (V)</th>
<th>Gm (Ω)</th>
<th>RDS (Ω)</th>
<th>Gain</th>
<th>CGS (F)</th>
<th>CGD (F)</th>
<th>CDS (F)</th>
<th>CDB (F)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1,2</td>
<td>3/8</td>
<td>4</td>
<td>0.24</td>
<td>0.062</td>
<td>0.22</td>
<td>0.27</td>
<td>0.002</td>
<td>61</td>
<td>0.021m</td>
<td>15.32M</td>
<td>318.5</td>
<td>336.8</td>
</tr>
<tr>
<td>M1,3,4</td>
<td>3/8</td>
<td>4</td>
<td>0.29</td>
<td>0.27</td>
<td>0.002</td>
<td>0.002</td>
<td>62</td>
<td>21.55</td>
<td>0.021m</td>
<td>37.4</td>
<td>37.5</td>
<td>1M</td>
</tr>
<tr>
<td>M5</td>
<td>3/8</td>
<td>4</td>
<td>0.29</td>
<td>0.27</td>
<td>0.002</td>
<td>0.002</td>
<td>62</td>
<td>21.55</td>
<td>0.021m</td>
<td>37.4</td>
<td>37.5</td>
<td>1M</td>
</tr>
<tr>
<td>M6</td>
<td>3/8</td>
<td>4</td>
<td>0.29</td>
<td>0.27</td>
<td>0.002</td>
<td>0.002</td>
<td>62</td>
<td>21.55</td>
<td>0.021m</td>
<td>37.4</td>
<td>37.5</td>
<td>1M</td>
</tr>
<tr>
<td>M7</td>
<td>3/8</td>
<td>4</td>
<td>0.29</td>
<td>0.27</td>
<td>0.002</td>
<td>0.002</td>
<td>62</td>
<td>21.55</td>
<td>0.021m</td>
<td>37.4</td>
<td>37.5</td>
<td>1M</td>
</tr>
<tr>
<td>M8</td>
<td>3/8</td>
<td>4</td>
<td>0.29</td>
<td>0.27</td>
<td>0.002</td>
<td>0.002</td>
<td>62</td>
<td>21.55</td>
<td>0.021m</td>
<td>37.4</td>
<td>37.5</td>
<td>1M</td>
</tr>
<tr>
<td>M9</td>
<td>3/8</td>
<td>4</td>
<td>0.29</td>
<td>0.27</td>
<td>0.002</td>
<td>0.002</td>
<td>62</td>
<td>21.55</td>
<td>0.021m</td>
<td>37.4</td>
<td>37.5</td>
<td>1M</td>
</tr>
<tr>
<td>M10</td>
<td>3/8</td>
<td>4</td>
<td>0.29</td>
<td>0.27</td>
<td>0.002</td>
<td>0.002</td>
<td>62</td>
<td>21.55</td>
<td>0.021m</td>
<td>37.4</td>
<td>37.5</td>
<td>1M</td>
</tr>
<tr>
<td>M11</td>
<td>3/8</td>
<td>4</td>
<td>0.29</td>
<td>0.27</td>
<td>0.002</td>
<td>0.002</td>
<td>62</td>
<td>21.55</td>
<td>0.021m</td>
<td>37.4</td>
<td>37.5</td>
<td>1M</td>
</tr>
<tr>
<td>M12</td>
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Bibliography


