Control Strategy of Cascaded H-Bridge Multilevel Inverter With PV system as Separate DC Source

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Degree project in Electrical Engineering
Master of Science
Stockholm, Sweden 2011

XR-EE-EME 2011:009
Control Strategy of Cascaded H-Bridge Multilevel Inverter with PV System as Separate DC Source

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Master of Science Thesis in Power Electronics
at the School of Electrical Engineering
Royal Institute of Technology
Stockholm, Sweden, June 2011
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XR-EE-EME 2011:009
Abstract

The integration of solar energy to the power grid is a challenging topic nowadays. Many topologies and control methods have already been proposed. In this thesis, the cascaded H-bridge (CHB) multilevel inverter is adopted for the photovoltaic (PV) energy integration. The purpose of this thesis is to develop a control strategy for the CHB multilevel inverter with PV array as separate DC source.

The thesis first gives a short review of the three commonly used multilevel inverter topologies. Then the PV array with maximum power point tracker (MPPT) is modeled. The selection mechanism with some improvements is chosen as the control and modulation method for the CHB inverter with PV system. Real and reactive power exchange between the inverter and grid are also discussed. Finally, the simulation results are presented to verify the control methods.

The software for the simulation is PSCAD/EMTDC and all the figures are plotted in MATLAB.

Keywords: Cascaded H-bridge multilevel inverter, Photovoltaic array, MPPT, Selection mechanism, PSCAD/EMTDC
Acknowledgment

This master thesis is one part of the degree requirements in Electric Power Engineering. The time length for this master thesis is five months from January 2011 to June 2011.

At first, I think I should express my highest gratitude to my supervisor Kalle Ilves and Antonios Antonopoulos, for their great guide and support throughout the whole work. They have also given me valuable feedback on my report. Without their efforts, the thesis would not reach the same level as it is today.

I also would like to thank Prof. Hans-Peter Nee for good input during the work and for proof reading the master thesis report.

I specially want to thank my colleagues Nima Madani and Roberto Bracco for providing a good research atmosphere in the Lab.

I also would like to say thanks to Ru Zhang, Tian Xia, Yiming Wu, Xiang Gao, Yalin Huang, Weiming Li, Zhengwu Zhang, Ruolan Liang, Miaomiao Zheng, Lin Zhu and all my friends in Stockholm for making my spare time more colorful every day.

Last but not least, a deeply appreciation is given to my family for their support during my education abroad.
List of Symbols

\( l \quad \) The number of output voltage levels of multilevel inverter
\( A \quad \) Effective radiation area of PV cell \( m^2 \)
\( I_{sc} \quad \) PV cell photo current \( A \)
\( I_d \quad \) PV cell diode current \( A \)
\( I_{sh} \quad \) PV cell shunt branch current \( A \)
\( I_o \quad \) PV cell dark current \( A \)
\( R_{sr} \quad \) Series resistance of PV cell \( \Omega \)
\( R_{sh} \quad \) Shunt resistance of PV cell \( \Omega \)
\( n \quad \) Diode ideality factor
\( e_g \quad \) PV cell band gap energy \( eV \)
\( T_c \quad \) PV cell temperature \( ^\circ C \)
\( R \quad \) Radiation level for PV cell \( kW/m^2 \)
\( \alpha_T \quad \) Temperature coefficient of photo current
\( v_{MPP} \quad \) Maximum power point voltage for PV cell \( kV \)
\( \hat{v}_g \quad \) Grid peak phase voltage \( kV \)
\( V_l \quad \) Grid RMS line to line voltage \( kV \)
\( v_{HT} \quad \) Output voltage of the inverter \( kV \)
\( i_g \quad \) Current injected into the grid from the inverter \( kA \)
\( v_{Cj} \quad \) DC link voltage for each module \( kV \)
\( f_{sw} \quad \) Multilevel inverter switching frequency \( Hz \)
\( m \quad \) Modulation ratio
\( N_{floor} \quad \) Floor level
\( N_{ceil} \quad \) Ceiling level
\( C_{level} \quad \) Comparison level
\( i'_g \quad \) The current injected to the inverter from the grid \( kA \)
\( r_j \quad \) Ratio between module DC link voltage \( v_{Cj} \) and its corresponding \( v_{MPP} \)
\( Q_{ca} \quad \) Calculated Reactive Power \( MVar \)
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Chapter 1

Introduction

1.1 Background

Due to the energy shortage, the integration of renewable energy sources to the electricity grid becomes an interesting research topic nowadays. The number of renewable energy sources and distributed generators is increasing very fast which also brings some threats to the power grid. In order to maintain or even to improve the power supply reliability and quality of the power system with distributed generation, it is necessary to have some new strategies for the operation and management of the electricity grid. Modern power electronic technology is an important part in distributed generation and the integration of the renewable energy to the power grid. It is widely used in the grid based system [1].

Since the output power of micro-sources (photovoltaic, wind energy etc.) is more or less dependent on the environment condition such as irradiance and wind, it is necessary to use some specific control strategies or to have some energy storage system (battery, super-capacitor etc.) in order to compensate for the fluctuations. One traditional way is to use different kind of converters to integrate the micro-sources, energy storage and different types of loads into a common DC bus [2], [3], the basic structure is shown in Figure 1.1.

![Figure 1.1. Connection of grid, micro-sources, energy storage systems and load](image-url)
CHAPTER 1. INTRODUCTION

Some problems with this kind of structure are as follows:

- There are lots of power electronics converters in the system so the harmonics components would be very high, which increases the cost and size of the harmonics filter.

- If the voltage level is very high, the switching stress of the power electronic device would increase.

- The efficiency would be low due to the power losses in different converters.

To overcome the above shortcomings, a modular power electronics technology named multilevel inverter, which is very appropriate for the integrating renewable energy source is proposed in [4], [5]. The core idea of the multilevel inverter is to achieve the desired ac voltage from several levels of dc voltages. Theoretically, the number of levels for the multilevel inverter can be chosen arbitrarily, so the output voltage of the inverter can reach high level even without the use of transformer. In addition, due to the step characteristic, the output voltage can be almost sinusoidal which, in turn, decrease the size of the filter.

There are three commonly used topologies for the multilevel inverter called diode-clamped inverter (neutral-point clamped), capacitor-clamped (flying capacitor), and cascaded multilevel inverter. Among these topologies, the cascaded H-bridges (CHB) multilevel inverter is seen as the most suitable topology for the integration of the renewable energy since the separate DC sources that it requires can be directly fed by PV arrays, wind turbine or fuel cells. In addition, in order to compensate the fluctuation of the output power of the PV arrays and wind turbines, several energy storage devices can also be incorporated into the system. Furthermore, since the number of DC sources can be chosen arbitrarily, it is convenient to increase the level of the output voltage and output power. One proposed topology for the cascaded H-bridge multilevel inverter with renewable energy sources is shown in Figure 1.2. Note that the number of inverters for each kind of renewable energy sources can be increased.

In [5], the following advantages for the cascaded H-bridge multilevel inverters are presented.

- They are appropriate in high voltage high power application.

- They are one of the best candidates for the interface between power grid and renewable energy sources.

- Due to the minimum switching frequency, the efficiency is very high.

- By using some control strategies of the cascaded H-bridge multilevel inverter, the power quality and dynamic stability of the power system can be improved.

- The switching stress and Electro Magnetic Interference (EMI) are very low

- The number of levels for the output voltage can be scaled up to unlimited number because of the modular structure.
1.2. OUTLINE OF THE THESIS

In this thesis, the cascaded H-bridge multilevel converter with PV arrays as separate DC sources is modeled and simulated. The possibility of integrating solar energy to the grid by using multilevel inverter is verified. A brief outline of the thesis is given below:

- Chapter 2 describes the three common topologies of multilevel inverter and presents the traditional modulation methods for cascaded multilevel inverter.
- Chapter 3 gives the detailed information about the PV array model and Maximum Power Point Tracking method.
- Chapter 4 demonstrates the control strategies for the grid-connected cascaded H-bridge multilevel inverter with PV systems.
- Chapter 5 gives the simulation results of the system.
- Chapter 6 presents the conclusions and future work.

Figure 1.2. The topology of cascaded H-bridge multilevel inverter with renewable energy sources
Chapter 2

Multilevel Inverter Topology

In this chapter, the three common multilevel inverter topologies as mentioned in Chapter 1 will be described. More details will be given to the cascaded H-bridge multilevel inverter and its modulation methods.

2.1 Diode-Clamped Multilevel Inverter

Figure 2.1(a) shows a three-level diode-clamped inverter. The output voltage is expressed as \(v_{an}\) where \(n\) is chosen as the neutral point. The series-connecting bulk capacitors \(C_1\) and \(C_2\) can split the DC bus voltage \(V_{dc}\) into three levels [6]. The switching state for different output is shown as follows:

- When the output voltage \(v_{an} = \frac{V_{dc}}{2}\), the upper two switch \(S_1\) and \(S_2\) are closed.
- When \(v_{an} = 0\), the switch \(S_2\) and \(S'_1\) are closed.
- When \(v_{an} = -\frac{V_{dc}}{2}\), the lower two switch \(S'_1\) and \(S'_2\) are closed.

The clamping diodes \(D_1\) and \(D'_1\) play as an important role in this kind of inverter which can clamp the switch voltage to half of the DC link voltage. The output voltage \(v_{an} = V_{dc}/2\) is served as an example. In this case, the switch \(S_1\) and \(S_2\) should be closed. \(D'_1\) is used to balance out the voltage sharing between the two switch \(S'_1\) and \(S'_2\). The voltage across \(C_1\) is blocked by \(S'_1\) and the voltage across \(C_2\) is blocked by \(S'_2\).

The five-level diode-clamped multilevel inverter is shown in Figure 2.1(b). The DC link voltage \(V_{dc}\) is evenly shared by four capacitors \(C_1, C_2, C_3\) and \(C_4\). The output voltage \(v_{an}\) and the corresponding switch state are shown in Table 2.1.

One disadvantage of this kind of inverter is the different reverse blocking voltage rating of the clamping diodes. The active switching device in the five-level diode-clamped multilevel inverter only need to block \(V_{dc}/4\). This is not the case for the clamping diodes. For example, when the upper switch \(S_1, S_2\) and \(S_3\) are closed, the clamping diode \(D_3\) is required to withstand a voltage level of \(3V_{dc}/4\); when the
CHAPTER 2. MULTILEVEL INVERTER TOPOLOGY

Figure 2.1. Diode-clamped multilevel inverter topologies. (a) Three-level. (b) Five-level

Table 2.1. Switching states for a 5 level Diode-Clamped Inverter

<table>
<thead>
<tr>
<th>Voltage $v_{an}$</th>
<th>$S_1$</th>
<th>$S_2$</th>
<th>$S_3$</th>
<th>$S_4$</th>
<th>$S'_1$</th>
<th>$S'_2$</th>
<th>$S'_3$</th>
<th>$S'_4$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$v_{an} = V_{dc}/2$</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$v_{an} = V_{dc}/4$</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$v_{an} = 0$</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$v_{an} = -V_{dc}/4$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>$v_{an} = -V_{dc}/2$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

switch $S_1$ and $S_2$ are closed, the clamping diode $D_2$ need to block $V_{dc}/2$; when the lower switch $S'_2$, $S'_3$ and $S'_4$ are closed, the clamping diode $D'_3$ is required to block $3V_{dc}/4$. If the level of the inverter is $l$ and the clamping diode has the same voltage rating as the active switching device ($V_{dc}/4$ in this five level diode-clamped multilevel inverter), then the number of clamping diode can be expressed by $(l - 1) \times (l - 2)$. It can be seen that the number of clamping diode would be quadratically increase with the level $l$. Therefore, when the level of the inverter is sufficiently high, the number of clamping diodes required in the circuit would be very high which make the whole system impractical to implement [6].
2.2 Capacitor-Clamped Multilevel Inverter

In Figure 2.2, the topologies of the three-level and five-level capacitor-clamped multilevel inverter are presented. They have similar structure as the diode-clamped multilevel inverter. The capacitors are used in the topology instead of diodes.

![Diagram of Capacitor-Clamped Multilevel Inverter](image)

Figure 2.2. Capacitor-clamped multilevel inverter circuit topologies. (a) Three-level. (b) Five-level

The three-level capacitor-clamped multilevel inverter is shown in Figure 2.2(a). One advantage of this kind of topology is that it can provide some redundancies for a certain output voltage. Taking the three-level Capacitor-Clamped Inverter as an example, for $v_{an} = 0$, either pair $(S_1, S'_1)$ or $(S_2, S'_2)$ needs to be turned on. The number of redundancies will increase as the output voltage level increases. The switch state and its corresponding output voltage for a five-level capacitor-clamped Inverters are shown in Table 2.2. With these redundancies, the capacitor voltages can be easily balanced with some control strategies and modulation methods since it is possible to choose which capacitor is to be charging and which one is to be discharging [7].
CHAPTER 2. MULTILEVEL INVERTER TOPOLOGY

Table 2.2. Switching states for a 5 level Capacitor-Clamped Inverter

<table>
<thead>
<tr>
<th>Voltage $v_{an}$</th>
<th>Switch State $S_1$</th>
<th>$S_2$</th>
<th>$S_3$</th>
<th>$S_4$</th>
<th>$S'_1$</th>
<th>$S'_2$</th>
<th>$S'_3$</th>
<th>$S'_4$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$v_{an} = V_{dc}/2$ (no redundancies)</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$v_{an} = V_{dc}/2 - V_{dc}/4$ (2 redundancies)</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$v_{an} = V_{dc}/4 - V_{dc}/2$</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>$v_{an} = V_{dc}/2 - 3V_{dc}/4 + V_{dc}/2$</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>$v_{an} = 0$ (5 redundancies)</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>$v_{an} = -V_{dc}/2$ (2 redundancies)</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>$v_{an} = -3V_{dc}/4$</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>$v_{an} = -V_{dc}/4 - V_{dc}/4$</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>$v_{an} = -V_{dc}/2$ (0 redundancies)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Considering the voltage rating of the devices in the circuit, it can be seen that the number of capacitor which is used to clamp voltage is very high. If it is assumed that the voltage rating for all the capacitors is the same as the main dc-bus capacitors ($V_{dc}/4$ in the five-level capacitor clamped inverter shown in Figure 2.2(b)), the number of additional capacitors besides the main dc-bus capacitor can be expressed as $(l - 1) \times (l - 2)/2$, where $l$ is the level of the inverter. Hence, the capacitor-clamped multilevel inverter has the same problem as diode-clamped multilevel inverter when the level of the inverter is high.

2.3 Cascaded H-Bridge Multilevel Inverter

2.3.1 Topology

The Cascaded H-Bridge (CHB) multilevel inverter is based on the series connection of single phase H-bridge inverters with separate DC sources. The topology is shown in Figure 2.3. The output phase voltage is synthesized by the addition of the voltages that are generated by different modules [6]. If the separate DC sources have the same voltage level ($V_{dc}$), the resulting phase voltage will be able to range from $-nV_{dc}$ to $nV_{dc}$ which would have $2n + 1$ levels. And $n$ is the number of the total modules or the the number of separate DC sources. As the number of DC
2.3. CASCADED H-BRIDGE MULTILEVEL INVERTER

sources increases, there would be more levels in the output voltage. So the output voltage waveform will be nearly sinusoidal, even without filtering.

![CHB multilevel inverter topology](image)

**Figure 2.3.** CHB multilevel inverter topology

The cascaded inverter topology has several advantages that have made it attractive in medium to high-power applications. The first one is its modularity. Each DC source is fed into an individual full bridge inverter so it is easy to plug into more separate DC sources without changing the dimension of the system. Moreover, the switching stress for each switch device would be less than the regular two level topology since the switch and diode need only withstand one separate DC voltage. If the Harmonic Selective Modulation method is used, the switching frequency will be at the fundamental frequency which decreases the switching loss [8]. Finally, as mentioned above, the output voltage waveform is nearly sinusoidal which decreases the cost of the filter.
CHAPTER 2. MULTILEVEL INVERTER TOPOLOGY

2.3.2 Modulation Methods

In this section, two commonly used modulation method for the CHB multilevel inverter will be presented.

Selective Harmonic Elimination

The basic idea of the selective harmonic elimination is to pre-determine the switching angle for each module to get the expected waveform of the output [8]. To explain its implementation in the cascaded H-bridge multilevel inverter, one example of five modules, eleven levels CHB multilevel inverter is shown in Figure 2.4.

By using Fourier Transform, the output voltage \( V(\omega t) \) can be expressed as

\[
V(\omega t) = \frac{4V_{dc}}{\pi} \sum_n \left[ \cos(n\theta_1) + \cos(n\theta_2) + \ldots + \cos(n\theta_5) \right] \frac{\sin(n\omega t)}{n} \tag{2.1}
\]

where \( n \) is the harmonic order. Since the waveform is both half wave symmetry and odd symmetry, \( n = 1, 3, 5, 7, \ldots \).

Usually, the normalized Fourier coefficients of the magnitude are used for further analysis. The normalized magnitude can be obtained by dividing \( V_{dc} \) on both sides of equation 2.1. Hence, the normalized Fourier coefficients for each harmonic order components are

\[
H(n) = \frac{4}{\pi n} \left[ \cos(n\theta_1) + \cos(n\theta_2) + \ldots + \cos(n\theta_5) \right] \tag{2.2}
\]

Figure 2.4. Output waveform of an 11-level cascade inverter
2.3. CASCADED H-BRIDGE MULTILEVEL INVERTER

where \( n = 1, 3, 5, \ldots \).

Then by choosing the conducting angle \( \theta_1 \rightarrow \theta_5 \) appropriately, it is possible to eliminate some target harmonic components [8]. Another point need to be mentioned is that the number of harmonic components which can be eliminated by this modulation method is one less than the number of the conducting angles since one degree of freedom should be given to the fundamental components of the waveform. In this case, the number of harmonics that can be eliminated is 4. Since the triple harmonic would not exist in the line to line voltage, the 5th, 7th, 11th and 13th order harmonics are chosen as the target harmonics that need to be eliminated in this case. The following equations can be obtained:

\[
\begin{align*}
\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cos(5\theta_4) + \cos(5\theta_5) &= 0 \\
\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \cos(7\theta_4) + \cos(7\theta_5) &= 0 \\
\cos(11\theta_1) + \cos(11\theta_2) + \cos(11\theta_3) + \cos(11\theta_4) + \cos(11\theta_5) &= 0 \\
\cos(13\theta_1) + \cos(13\theta_2) + \cos(13\theta_3) + \cos(13\theta_4) + \cos(13\theta_5) &= 0 \\
\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4) + \cos(\theta_5) &= 5m_i
\end{align*}
\]

where \( m_i \) is reference modulation index which is defined as \( m_i = \frac{V_{ref}}{V_{dc}} \).

One advantage of this modulation method is that the inverter are switching at the fundamental frequency which decreases the switching losses. However, the pre-calculation of the conducting angle requires the solution of non-linear equation. When the level of inverter increases, the number of the non-linear equations would also be very high. Then the solution for these equations would be inaccurate which may increase the distortion in the output voltage waveform [9].

Phase Shifted Pulse Width Modulation

Phase shifted PWM is one of the most commonly used modulation method in CHB multilevel inverter since it is very suitable for the modularity of the topology. For each module, the reference signal is the same. However, the carrier waveform (usually triangular waveform) for each module would have a phase shift to ensure the step characteristic of the output voltage. How many degrees are the phase shift between each module depends on the modulation method for the individual H-bridge inverter. If the unipolar modulation method is selected, the phase shift between each module should be \( 180^\circ/k \) to achieve the lowest output voltage distortion; if the bipolar modulation method is chosen, the phase shift between each module should be \( 360^\circ/k \) [10], where \( k \) is the number of modules. A three modules, seven level CHB multilevel inverter with unipolar modulation method is shown in Figure 2.5.
The output voltage of the inverter is as $k$ times as the output voltage of each module which is one advantage of this modulation method since the switching devices need only withstand the voltage of their modules. Moreover, the frequency of the output voltage has $k$ times as the switching frequency of each module which is beneficial in reducing the conducting losses of the inverter.

In this thesis, the selection mechanism presented in [11], [12] will be used as the modulation method for the Cascaded H-Bridge (CHB) Multilevel Inverter. The modulation and control method will be discussed later in Chapter 4.

Figure 2.5. Three cell PS-PWM waveform generation
Chapter 3

Grid-connected Photovoltaic System

Grid connected photovoltaic (PV) power conversion systems are getting more and more attention in the last decade, mainly due to cost reduction of PV modules and government incentives, which has made this energy source and technology competitive among other energy sources [13].

3.1 PV Array Model

The output of the PV system is largely dependent on the outside environment conditions. In order to make the correct analysis of the photovoltaic system, a suitable simulation model must be chosen initially.

3.1.1 Mathematical Model

PV arrays consists of series and parallel connected PV modules. For each PV module, there are series and parallel connected PV cells. The PV cell is usually described by the equivalent circuit shown in Figure 3.1. It can be seen that one current source antiparallel with a diode, a shunt and a series resistance are included in the equivalent circuit [14].

The basic equation for the PV cell can be derived by the Kirchhoff’s current law:

\[ I = I_{sc} - I_d - I_{sh} \]  \hspace{1cm} (3.1)

The diode current \( I_d \) and the shunt branch current \( I_{sh} \) can be expressed as

\[ I_d = I_o \left( \exp \left( \frac{V + IR_{sr}}{nkT_c/q} \right) - 1 \right) \]  \hspace{1cm} (3.2)

\[ I_{sh} = \frac{V + IR_{sr}}{R_{sh}} \]  \hspace{1cm} (3.3)

In (3.1), \( I_{sc} \) is defined as the photo current. The value of \( I_{sc} \) under reference conditions can be obtained by seeing the data sheet of the PV cell. The photocurrent
under arbitrary environment conditions can be expressed as:

\[ I_{sc} = I_{scR} \frac{R}{R_R} [1 + \alpha_T(T_c - T_{cR})] \]  

(3.4)

Where \( I_{scR} \) is the short circuit current at the reference solar radiation \( R_R \) and the reference cell temperature which are selected as 1\( kW/m^2 \) and 25\( ^\circ C \) respectively in this thesis. The parameter \( \alpha_T \) is the temperature coefficient of photo current [14]. And the current \( I_o \) is the dark current which is only the function of cell temperature:

\[ I_o = I_{oR} \left( \frac{T_c^3}{T_{cR}^3} \right) \exp \left[ \left( \frac{1}{T_{cR}} - \frac{1}{T_c} \right) \frac{q e_g}{k n} \right] \]  

(3.5)

In (3.5), \( I_{oR} \) is the reference dark current. The other parameters appeared from (3.2) to (3.5) are the electron charge \( q \), the Boltzmann constant \( k \), the band-gap energy of the PV cell \( e_g \), and the diode ideality factor \( n \) which is used to adjust the characteristic \( I - V \) curves. The constants in the above equations can be obtained from the data sheet provided by the manufacturer [14]. The parameter of the PV cell used in this thesis is shown in table 3.1.

<table>
<thead>
<tr>
<th>A [m^2]</th>
<th>( R_{sr} )[( \Omega )]</th>
<th>( R_{sh} )[( \Omega )]</th>
<th>n</th>
<th>( e_g )[eV]</th>
<th>( I_{oR} )[A]</th>
<th>( I_{scR} )[A]</th>
<th>( \alpha_T )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.01</td>
<td>0.02</td>
<td>1000</td>
<td>1.5</td>
<td>1.013</td>
<td>( 10^{-9} )</td>
<td>2.5</td>
<td>0.001</td>
</tr>
</tbody>
</table>

The output voltage and power for each PV cell is relatively small. In order to increase the voltage level and output power, the PV cells can be connected in series and parallel to form one PV module and the PV modules can be also connected in series and parallel to form one PV array.
3.1. PV ARRAY MODEL

3.1.2 Simulation of PV Array

The software used for the simulation is PSCAD/EMTDC which is a fixed time-step simulation software. Since the PV array was interfaced as a nonlinear current source, accurate implementation on the above equation requires iterative solution of (3.1) simultaneously with the network equations. However, due to the small steps used in typical emt simulations, voltage calculated from the last time step can be used to calculate the new current injection. In order to ensure the simulation stability under rapidly changing output voltages, feedback of the voltage at previous time step was provided through a first order filter [14].

The simulation results of the $I-V$ characteristic curves for the PV array under different environment conditions are shown in Figure 3.2. The PV array consists 20 PV modules in parallel and 20 PV modules in series, each PV module contains 108 PV cells in series and 4 PV cells in parallel.

![I-V curve for the PV array](image)

**Figure 3.2.** $I$-$V$ characteristic curve under different environment conditions

The maximum power that can be drawn from the PV array depends on the operation point of the $I-V$ curve. As it is shown in Figure 3.2, the maximum power output of one PV array usually occurs around the knee point of the curve [14]. When the radiation level or the cell temperature changes, the $I-V$ curve as well as the Maximum Power Point (MPP) would also change. The PV array simulated in this thesis can be served as one example, when the radiation level $R = 1\text{kW/m}^2$, cell temperature $T = 25^\circ\text{C}$, the output voltage for the MPP is around 1.5kV; when the radiation level $R = 1\text{kW/m}^2$, cell temperature $T = 50^\circ\text{C}$, the output voltage for the MPP is about 1.4kV. In order to always get the maximum output power from
CHAPTER 3. GRID-CONNECTED PHOTOVOLTAIC SYSTEM

PV array at the corresponding radiation level and cell temperature. A maximum power point tracker (MPPT) should be included in the PV system.

3.2 Maximum Power Point Tracking Method

The change of environment condition would affect the output power of the PV array. By installing the MPPT in the PV system, it is possible to always ensure the maximum output power under the corresponding environment condition. There are many MPPT algorithms proposed in the research publications. In this section, the Perturbation & Observation (P&O) method and Incremental Conductance method will be presented.

Figure 3.3 shows the characteristic power curve for a PV array. This characteristic curve would change for different environment conditions. Then the core idea of the MPPT technique is to automatically adjust its output voltage and current in terms of $V_{MPP}$ and $I_{MPP}$ under which the PV array can output the maximum power.

![Figure 3.3. Characteristic PV array power curve](image)

**P&O Method**

In Perturbation & Observation method, the operating voltage of the PV array is the value which is to be increased or decreased in the MPPT [15]. In Figure 3.3, it can be seen that when the operating points are on the left side of the MPP, increasing the operating voltage of the PV array would increase the output power and decreasing the operating voltage would decrease the output power. However, when the operating point are on the right side of MPP, increasing the operating voltage of the PV array would reduce the output power and decreasing the operating voltage of the PV array would increase the output power. Hence, the perturbation
would be kept the same if the output power is increased while the direction of the perturbation should be changed if the output power is decreased. The algorithm is shown in Table 3.2.

### Table 3.2. P&O algorithm

<table>
<thead>
<tr>
<th>Perturbation</th>
<th>Power</th>
<th>Next Perturbation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Increasing</td>
<td>Increasing</td>
<td>Increasing</td>
</tr>
<tr>
<td>Increasing</td>
<td>Decreasing</td>
<td>Decreasing</td>
</tr>
<tr>
<td>Decreasing</td>
<td>Increasing</td>
<td>Decreasing</td>
</tr>
<tr>
<td>Decreasing</td>
<td>Decreasing</td>
<td>Increasing</td>
</tr>
</tbody>
</table>

When the operating voltage reaches MPP, it will oscillate around the MPP. The selection of the perturbation size is just the trade off between this oscillation and the response time of the MPPT. By using small perturbation size, the oscillation around MPP would be very small but the response time of MPPT would be very long. Some solutions for this problem have already be proposed. For example, in [16], [17], the perturbation size can adjust automatically which ensure large perturbation size far way from MPP and relatively small perturbation size around MPP.

### Incremental Conductance

From the power curve shown in Figure 3.3, it can be seen that the slope of the curve which is defined as $\frac{dP}{dV}$ would be different at different operating point. When the operating point is on the left of MPP, $\frac{dP}{dV} > 0$; when the operating point is on the right of MPP, $\frac{dP}{dV} < 0$; when the operating point is at MPP, $\frac{dP}{dV} = 0$. The incremental Conductance algorithm is based on the above fact [18]. The expression for $\frac{dP}{dV}$ is given by

$$\frac{dP}{dV} = \frac{d(IV)}{dV} = I + V \frac{dI}{dV} = I + V \frac{\Delta I}{\Delta V}$$ \hspace{1cm} (3.6)

The instantaneous conductance is defined as $I/V$ and the incremental conductance is defined as $\Delta I/\Delta V$. Then the operating point of the PV array can be obtained by comparing the instantaneous conductance with the incremental conductance which is shown in equation (3.7)

$$\begin{cases} 
\Delta I/\Delta V = -I/V, \text{ at MPP} \\
\Delta I/\Delta V > -I/V, \text{ left of MPP} \\
\Delta I/\Delta V < -I/V, \text{ right of MPP}
\end{cases}$$ \hspace{1cm} (3.7)

When the operating point is achieved, it is possible to increase or decrease the operating voltage to make it get close to $V_{MPP}$. The control algorithm is shown in Figure 3.4.
CHAPTER 3. GRID-CONNECTED PHOTOVOLTAIC SYSTEM

Figure 3.4. Incremental Conductance algorithm

$V_{ref}$ is the reference voltage which is equal to $V_{MPP}$ at the maximum power point. When the MPP is achieved, $V_{ref}$ will maintained at this value unless the change $\Delta I$ due to the weather condition occurs. After that, the algorithm will increase or decrease the $V_{ref}$ to track for the new MPP.

In this thesis, the incremental conductance method is used for the maximum power point tracking since the output voltage can better follow the change weather condition and the oscillation around MPP is smaller when compared with P&O method. When implementing the algorithm in PSCAD, the sampling time for the MPPT should be selected appropriately. Large sampling time may decrease the accuracy of the MPP voltage while very small sampling time may lead to relatively large oscillation around the MPP voltage. In the simulation work, the sampling time for the MPPT is chosen as 0.01 s.

3.3 The Topologies of Single Phase Grid-Connected Inverters with Photovoltaic Array

The past and present topologies for the grid connected photovoltaic power conversion system are presented in [19]. There are four configurations for these kinds of systems which are shown in Figure 3.5.
3.3. THE TOPOLOGIES OF SINGLE PHASE GRID-CONNECTED INVERTERS WITH PHOTOVOLTAIC ARRAY

Centralized Inverters

This technology is the oldest topology for the grid connected PV system which is based on centralized inverters that interfaced a large number of PV modules to the grid [19]. Several PV modules are connected in series to form a string in order to reach higher voltage level without the transformer or DC-DC boost converter. The advantage of this technology is its simple structure and control. However, there are many limitations for this kind of topology. First of all, only one MPPT is installed in the central inverter which would reduce the power generation due to the module mismatch and partial shading. Moreover, the commutation of the inverter is usually line commutated by means of thyristors which would inject a lot of harmonics currents and reduce the power quality.

String Topology

The string inverter is a reduced version of the centralized inverter. In this topology, a single PV string is connected to the inverter. This improves the MPPT and the total generated power. Moreover, this technology also increases the modularity since additional strings can be added into the system without changing the inverter dimensions. However, depending on the size of the string, the MPPT is not optimal because of partial shading and module mismatch.
CHAPTER 3. GRID-CONNECTED PHOTOVOLTAIC SYSTEM

Multi-String Topology

In multi-string topology, each PV string has their own DC-DC converter and the output of the converter are connected to a common DC bus. The DC bus voltage will be fed into the DC/AC inverter. Since there is a dc-dc converter to boost the voltage, then the MPPT can be well implemented. Moreover, due to its modularity, a new string with dc-dc converter can be plugged into the system easily. But there is also a disadvantage of this topology. It is necessary to have long dc cables to connect each string to the common dc-dc converter which increases the losses.

AC Module Topology

The AC module topology is the most suitable one for the implement of MPPT since one converter is dedicated for one PV module. In addition, due to the modular structure, the system can be easily enlarged. However, this technology is only intended for smaller systems and domestic use. The main disadvantage is that a DC-DC boost stage or step-up transformer is a must which increase the cost.
Chapter 4

Grid-Conneted Cascaded H-Bridge Multilevel Inverter with PV System

The traditional topologies for grid-connected PV systems have certain kind of
disadvantages which have already been shown in Chapter 3. Recently, Cascaded H-
Bridge Multilevel Inverter is proposed as a possible interface for the grid connection
of PV systems.

The separate DC sources can be individual PV arrays, depending on the output
power level. It is very beneficial for the high voltage and high power application since
the output voltage level can be reached by interconnecting enough number of PV
arrays which also eliminate the use of step-up transformer or dc-dc boost converter.
In addition, the inherent improved power quality of multilevel converters reduces
filter size and switching frequency, improving the system efficiency. Furthermore,
each PV array is connected to a single DC-AC converter which improves the MPPT
algorithm. One of the drawbacks of this topology is its in need of a sophisticated
control method for the grid current, capacitor voltage, etc.

4.1 Grid Model

The target grid in this thesis has a line to line voltage of 10 kV. Then the peak
voltage for one phase can be calculated as follows:

\[ \hat{v}_g = \frac{V_{ll}}{\sqrt{3}} \sqrt{2} = \frac{10}{\sqrt{3}} \sqrt{2} = 8.165kV \]  \hspace{1cm} (4.1)

In addition, the grid can be modeled as a voltage source behind a impedance. The
corresponding grid data is shown in Table 4.1.
### 4.2 Mathematical Model for the Multilevel Inverter with PV System

From Chapter 3, it can be seen that the output voltage of the PV array at MPP is around 1.5 kV under the reference environment condition. The peak value of the phase voltage of the grid is 8.165 kV. Therefore, at least 6 modules should be included in the CHB multilevel inverter. As mentioned in Chapter 2, this would result in $2 \times 6 + 1 = 13$ levels of the output voltage. The topology is shown in Figure 4.1.

![Topology for the CHB multilevel inverter with PV arrays](image)

**Figure 4.1.** Topology for the CHB multilevel inverter with PV arrays

The output voltage for each cell is determined by

$$v_{Hj} = (T_{j1} - T_{j3}) \cdot v_{Cj}, \quad j = 1, \ldots, 6 \quad (4.2)$$

---

**Table 4.1. Grid Data**

<table>
<thead>
<tr>
<th>$V_u [kV]$</th>
<th>$V_g [kV]$</th>
<th>Inductance $L [H]$</th>
<th>Resistance $R [\Omega]$</th>
<th>Frequency $f [Hz]$</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>8.165</td>
<td>0.01</td>
<td>0.1</td>
<td>50</td>
</tr>
</tbody>
</table>

---

**CHAPTER 4. GRID-CONNECTED CASCADED H-BRIDGE MULTILEVEL INVERTER WITH PV SYSTEM**
4.3 CONTROL AND MODULATION STRATEGIES

where $T_{XX}$ represents the state of each switch according to Figure 13. $T_{XX}$ presents two discrete values: '1' when the switch is on and '0' when the switch is off. Therefore, the output voltage of the H-bridge is $-v_c, 0, v_c$, respectively. The switching action of the module will be discussed in section 4.4. The mathematical model of the system can be expressed by [20]

$$\frac{di_g}{dt} = \frac{1}{L} \left( \sum_{j=1}^{6} [(T_{j1} - T_{j3})v_{Cj}] - R_{ig} - v_g \right)$$

(4.3)

$$\frac{dv_{Cj}}{dt} = \frac{1}{C_j}(i_{PVj} - (T_{j1} - T_{j3})i_g), \ j = 1, 2, \ldots, 6.$$  

(4.4)

4.3 Control and Modulation Strategies

In this thesis, the modulation method is Pulse Width Modulation (PWM). However, it is different from normal PWM in which the state of each switch is determined by the comparison of a reference waveform with the carrier waveform. Instead, the firing signals of the switch are obtained by comparing the control signal from the proposed control law with the carrier waveform, as shown in Figure 4.2. The selection of the switching frequency of the carrier waveform is the trade off between switching losses in the inverter and the harmonic distortion of the current injected into the power grid. Moreover, in high power application, the switching frequency should be limited to a certain level due the switching stress imposed on the switch device. Here the switching frequency $f_{sw} = 600Hz$ is selected.

![Figure 4.2. Modulation strategy](image)

At each sampling time $t_k$, the desired modulation index can be obtained by comparing the value of reference waveform at this time (red dots in Figure 4.2)
with the sum of DC voltages (the sum of capacitor voltages in Figure 4.1),

\[ m(t_k) = \frac{v_{ref}(t_k)}{\sum_{j=1}^{6} v_{Cj}(t_k)} \]  

(4.5)

For each sampling time \( t_k \), the highest level that does not exceed the value of the reference waveform \( v_{ref}(t_k) \) at this time is called the floor level \( N_{floor}(t_k) \). Moreover, the lowest level which exceeds the \( v_{ref}(t_k) \) is called the ceil level \( N_{ceil}(t_k) \). In Figure 4.2, for \( t_1 \) and \( t_2 \), level 1 is the \( N_{floor} \) and level 2 is the \( N_{ceil} \); for \( t_3 \), \( t_4 \) and \( t_5 \), level 2 is the \( N_{floor} \) and level 3 is the \( N_{ceil} \); for \( t_6 \), level 1 is the \( N_{floor} \) and level 2 is the \( N_{ceil} \). For a certain modulation index \( m(t_k) \), \( N_{floor} \) and \( N_{ceil} \) can be determined by

\[ N_{floor} = \text{int}(6 \times (m(t_k) + 1)) - 6 \]  

(4.6)

\[ N_{ceil} = N_{floor} + 1 \]  

(4.7)

The triangular waveform has a positive slope during one sampling interval and a negative slope during the consecutive sampling interval as shown in Figure 4.2. The following definition for the modulation strategy is given

- Interval with the ascending triangular waveform → The modulated voltage is going to shift from the floor level to the ceil level (Insert a positive module or bypass a negative module)

- Interval with the descending triangular waveform → The modulated voltage is going to shift from the ceil level to the floor level (Insert a negative module or bypass a positive module)

The transition between the floor level and the ceil level takes place inside the interval at a certain time which is determined by comparing the Comparison Level \( (C_{level}) \) with the value of the triangular waveform. When the triangular wave coincides with the \( C_{level} \), one switching will occur. Actually, the value of the reference waveform at the sampling time, \( v_{ref}(t_k) \), indicate a desired average potential for the upcoming sampling interval. Therefore, the \( C_{level} \) can be determined by

\[ C_{level} = 1 - [6 \times (m(t_k) + 1) - N_{floor} - 6] \]  

(4.8)

There is another point need to be mentioned in the modulation strategy. If the sampled modulation level has moved to different floor-ceiling interval as compared with the preceding sampling point. One or more modules would be switched at the sampling time instantaneously. This can also be seen from Figure 4.2. At \( t_3 \), the previous interval has shifted the modulated voltage from level 2 to level 1. However, the transition process for the upcoming interval will happen between level 2 and level 3. Therefore, at the sampling time \( t_3 \), one positive module should be inserted (Or one negative module should be bypassed) in order to make the starting level to be level 2 for the upcoming interval. Similar process is happened for the sampling time \( t_6 \).
4.3. CONTROL AND MODULATION STRATEGIES

4.3.1 Switching Action of Each H-bridge Module

From the mathematical section, the switches in each module are controlled such that only two of the four switches are turned on at any time. The switch positions for four possible gate signals are given below. 1 and 0 represent on and off state of the switch respectively. In addition, $i_g'$ denotes the current from grid to the inverter.

When the control signal is 1, the inverter operates in the forward direction (from the grid to the inverter) as shown in Figure 4.3.

If $i_g'$ is positive and the module is inserted by the modulation method, then the capacitor will be charged in this case. If $i_g'$ is negative and this module is inserted by the modulation method, the capacitor $C$ will be discharged.

When the control signal is -1, the inverter operates in the reverse direction as shown in Figure 4.4.

If $i_g'$ is positive and this module is inserted by the modulation method, the capacitor will be discharged in this case. If $i_g'$ is negative and this module is inserted by the modulation method, the capacitor will be charged.

When the control signal is 0, the inverter operates in the bypass mode which are shown in Figure 4.5 and Figure 4.6.
4.3.2 Selection Mechanism for the Modules

From the previous section about the modulation strategy, it can be seen that the change of the number of the inserted modules occurs in the following two conditions:

- Insert or bypass one module within each sampling interval
- Possibly insert or bypass several modules at the sampling time $t_k$

Therefore, it is important to define a mechanism that can determine which individual module should be inserted or bypassed at the above switching events. In this thesis, the selection mechanism presented in [11], [12] is used. However, there is one change for for the mechanism due to different applications. For the normal case, each module has the same voltage rating and there is only a slight difference of the capacitor voltage during the operation due to the charging and discharging. Then the selection process is as follows: when the current is charging, the bypassed module with the lowest voltage is the candidate to be inserted and the inserted module having the highest voltage is the candidate to be bypassed; when the current is discharging, the bypassed module with the highest voltage is the candidate to be inserted and the inserted module with the lowest voltage is the candidate to be bypassed.
4.3. CONTROL AND MODULATION STRATEGIES

In this thesis, the capacitor voltage depends on the output voltage of the PV array which will change with different environment conditions. Moreover, as mentioned in Chapter 3, the Maximum Power Point Tracker (MPPT) would be installed in the system in order to always get maximum output power from the PV array. The output of the MPPT is the $v_{MPP}$ at which the maximum power is achieved. Therefore, if the capacitor voltages of all the modules are directly compared, the output voltage of the PV array will not be able to get close to its $v_{MPP}$. Instead of the actual capacitor voltage for each module, the ratios between the capacitor voltage and its corresponding $v_{MPP}$ are compared. The ratio $r_i$ is defined as

$$ r_j = \frac{v_{Cj}}{v_{MPPj}}, \quad j = 1, 2, \ldots, 6 $$ (4.9)

Assume that $N_{\text{insert}}$ modules will be inserted and $N_{\text{bypass}}$ modules will be bypassed. Then the selection mechanism is based on

- Instantaneous AC current $i'_g$ at the switching event
- The ratio $r_i$ for each module
- Control signal of H-bridge inverter module

The AC current $i'_g$ (from grid to the converter) is seen as the positive current. This means that

Control signal is 1

- Positive AC currents charges the capacitors in inserted modules.
- Negative AC currents discharges the capacitors in inserted modules.

Control signal is -1

- Positive AC currents discharges the capacitors in inserted modules.
- Negative AC currents charges the capacitors in inserted modules.

If the modulation method requires the modulated voltage to step up one or more levels, this can be done by inserting one or more positive output modules (control signal from 0 to 1) or bypassing one or more negative output modules (control signal from -1 to 0). If the modulation method requires the modulated voltage to step down one or more levels, this can be done by inserting one or more negative output modules (control signal from 0 to -1) or bypassing one or more positive output modules (control signal from 1 to 0). Either to insert or bypass modules depend on the number of positively connected modules or negatively connected modules and the value of reference waveform at switching time.

Therefore, the modules to be inserted or bypassed will be selected according to the following rules.

For the step up case, when the current is positive
• The presently bypassed modules with the lowest $r$ is to be positively inserted
• The presently negatively inserted modules with the lowest $r$ is to be bypassed
When the current is negative
• The presently bypassed module with the highest $r$ is to be positively inserted
• The presently negatively inserted modules with the highest $r$ is to be bypassed
For the step down case, when the current is positive
• The presently bypassed modules with the highest $r$ is to be negatively inserted
• The presently positively inserted modules with the highest $r$ is to be bypassed
When the current is negative
• The presently bypassed modules with the lowest $r$ is to be negatively inserted
• The presently positively inserted modules with the lowest $r$ is to be bypassed

4.4 Active Power Control

The control of the Cascaded H-Bridge (CHB) multilevel inverter mainly focuses on two parts: the capacitor voltage and the output power control. The capacitor voltages can be balanced by the selection mechanism and the output power is discussed in this section.

Normally, it is required that the converter only inject the active power to the grid. However, by using some control method, it is possible that the reactive power can be also injected to or extracted from the grid (see next section).

From the point of PV arrays, the reason that the output active power should be controlled lies in the fact that the output power from the PV arrays may change due to the environment conditions. Therefore, the output power should be controlled in such a way that the grid can always get the maximum power from the PV arrays. To control the output active power, the simplified equivalent circuit and phasor diagram as shown in Figure 4.7 can be first considered.
4.4. ACTIVE POWER CONTROL

The resistance is neglected since during the normal operation the reactance $X_L$ would be much larger than the resistance $R$. $V_{HT}$ is the output voltage from the inverter, $V_L$ is the voltage across the grid inductance and $V_{grid}$ is the grid voltage. Hence, the active output power can be calculated by using the following equation:

$$P = \frac{V_{HT}V_{grid}}{X_L} \sin \delta$$  \hspace{1cm} (4.10)

Then the output active power can be controlled by changing the phase difference between the output voltage and grid voltage. Usually the phase of the grid voltage is chosen as the reference which means that $\varphi_{grid} = 0$. In addition, the phase angle of the output voltage can be controlled by the phase angle of the modulation reference waveform. The proposed control strategy for the active power is shown in Figure 4.8.

From the MPPT, the sum of the capacitor voltage reference $\sum_{j=1}^{6} v_{MPPj}$ are obtained. The sum of the actual capacitor voltages $\sum_{j=1}^{6} v_{Cj}$ is also measured. The error of these two values will go through the proportional-integral (PI) controller, the output of the PI controller is the phase angle difference between the grid voltage and the reference voltage waveform. By adding the phase angle of the grid $\varphi_{grid}$, the phase angle of the modulation reference waveform is achieved.
4.5 Reactive Power control

As mentioned in the previous section, normally it is required that the inverter only provide active power to the grid. But in some special cases such as voltage support, the inverter should also have the ability to exchange reactive power with the grid. It is well known that the reactive power transmission is related to the voltage magnitude. Therefore, the reactive power control can be implemented by controlling the magnitude of the output voltage. Similar with the phase angle, the voltage magnitude of the modulation reference waveform is controlled instead of the real output voltage.

The proposed control strategy for the reactive power is shown in Figure 4.9. $Q_{ca}$ represents the reactive power from the calculation, the formula for this calculation is

$$Q_{ca} = \hat{v}_{grid} \frac{\hat{i}_g}{\sqrt{2}} \sqrt{2} \sin(\varphi_{grid} - \varphi_i)$$  \hspace{1cm} (4.11)

where, the grid voltage magnitude can be obtained from the grid data, that is $\hat{v}_{grid} = 8.165kV$, the grid voltage angle is chosen as the reference, meaning that $\varphi_{grid}$ is equal to zero. Hence, to get the calculated value of the reactive power, it is important that the grid current magnitude and phase angle are known. This can be achieved by using Recursive Least Square (RLS) estimation (given in appendix). Then the error between $Q_{ca}$ and $Q_{ref}$ will pass the PI controller. The output value of the PI controller plus $\hat{v}_{grid}$ will determine the voltage magnitude of the reference waveform.

![Figure 4.9. Proposed control strategy for the reactive power](image-url)
Chapter 5

Simulation Results

The simulation software for this thesis is PSCAD/EMTDC and all the simulation results are plotted in MATLAB.

5.1 Simulation of the System Under Different Environment Conditions

5.1.1 Reference Environment Condition

The reference environment condition corresponds to the condition under which radiation level for each PV array is $R = 1\text{kW/m}^2$ and cell temperature for each PV array is $T = 25^\circ C$. In addition, the reactive power is controlled to be zero which means the power factor is unity. The output voltage $v_{HT}$ and the modulation reference waveform are shown in Figure 5.1.

![Output voltage waveform of the CHB multilevel inverter](image)

**Figure 5.1.** Output voltage waveform of the CHB multilevel inverter

Every PV array works under the same environment condition in this case, they have similar output voltages. The output voltage for PV array 1 is plotted in Figure 5.2 and Figure 5.3.
From Figure 5.2, it can be seen that after 3 s from the beginning of the simulation, the output voltage of the PV array will go to the steady state. By using MPPT, the output voltage of the PV array can follow the trend of $v_{MPP}$, which can be seen in Figure 5.3. The maximum power point output voltage is around 1.48 kV. The actual output voltage of the PV array $v_C$ oscillates around 1.48 kV. In Figure 5.1, it is very clear that the output voltage of the inverter comprises 13 levels, $\pm 6v_C$, $\pm 5v_C$, $\pm 4v_C$, $\pm 3v_C$, $\pm 2v_C$, $\pm v_C$, and 0.

The output power for PV array 1 and the total of 6 PV arrays are shown in
5.1. SIMULATION OF THE SYSTEM UNDER DIFFERENT ENVIRONMENT CONDITIONS

Figure 5.4 and Figure 5.5.

From the above two Figures, it can be seen that the output power for one PV array is around 0.275 MW at steady state. Moreover, the output power of all the PV arrays is around 1.65 MW which means that the inverter can inject 1.65 MW active power to the grid if the conducting losses for the switch and the losses due to the grid resistance are neglected. The reactive power injected to the grid is controlled to be 0 which is shown in Figure 5.6.
CHAPTER 5. SIMULATION RESULTS

It can be seen that the reactive power oscillates around 0, the oscillation magnitude of the reactive power is around 0.02 MW. The zero injection of reactive power can also be verified by observing the grid current $i_g$ and grid voltage $v_g$, which is shown in Figure 5.7.

In Figure 5.7, it can be observed that the grid current is in phase with the grid voltage which also indicate the unitary power factor. In addition, the grid current is almost sinusoidal which reduces the filter size.

5.1.2 Step Change in Radiation Level

In order to specify the MPPT, a step change in radiation level is introduced. At first, the whole system operates under the reference environment conditions just as shown in the previous section. While at $t = 9.01s$, the radiation level for PV
5.1. SIMULATION OF THE SYSTEM UNDER DIFFERENT ENVIRONMENT CONDITIONS

array 1 is changed from $1kW/m^2$ to $0.6kW/m^2$. The DC link voltages for module 1, module 2 and module 3 are shown in Figure 5.8.

![Figure 5.8. DC link voltage of different modules](image)

It can be seen that after the change of radiation level, the MPPT of module 1 adjusts fast and locks into the new MPPT levels which are a little bit higher than the MPPT levels of module 2 and module 3. However, module 2 and module 3 have a similar trend. This can also be seen from Figure 3.2, the $v_{MPP}$ for the green line is a little bit higher than the $v_{MPP}$ of the red line.

The output power for the PV arrays are shown in Figure 5.9 and Figure 5.10.

![Figure 5.9. Output power for PV array 1 and PV array 2](image)
In Figure 5.9, due to the step change of the radiation level on the PV array 1, the output power for this PV array decrease to about 0.165 MW which is the maximum output power at $T = 25^\circ\text{C}$, $R = 0.6\text{kW/m}^2$, while the rest of the PV arrays still deliver 0.275 MW under the reference environment condition. The total output power will also decrease due to the lower radiation level on the PV array 1. The active power control can be seen from the phase angle of reference waveform which is shown in Figure 5.11.

It can be seen that after the step change of the radiation level for PV array 1, the phase angle of the reference waveform decreases from about 0.268 $\text{rad}$ to 0.255 $\text{rad}$. The reason for the change is as follows. The active power injected to the grid can be expressed by using equation 4.10. The grid voltage and inductance are constant all the time, so the amount of the active power depends on the magnitude and phase angle of the inverter output voltage which is controllable by changing the magnitude and phase angle of the reference waveform. In this case, the reactive power is controlled to be 0 so the magnitude will not change. When the radiation level
5.1. SIMULATION OF THE SYSTEM UNDER DIFFERENT ENVIRONMENT CONDITIONS

decrease, the maximum output power that can be injected into the grid from the PV arrays would also be reduced. Then the phase angle of the reference waveform will decrease.

The output voltage $v_{HT}$, grid current $i_g$ and grid voltage $v_g$ are shown in Figure 5.12 and Figure 5.13.

![Figure 5.12. The output voltage of the inverter](image)

![Figure 5.13. Grid current and grid voltage](image)

The grid voltage is still in phase with the grid current which ensure the unitary power factor. However, due to the decrease of the active power injected into the grid, the grid current decreases, which can be seen from Figure 5.13.

5.1.3 Step Change in PV Array Temperature

Temperature is another factor that can influence the operation of the PV array. In the following simulation, the whole system is at first operated under the reference
environment condition, at $t = 9.0\text{s}$, the temperature of array 1 is changed from $T = 25^\circ\text{C}$ to $T = 50^\circ\text{C}$. The capacitor voltages of module 1 and module 2 are shown in Figure 5.14.

From Figure 5.14, it can be seen that $v_{MPP}$ of module 1 decreases from 1.48 kV to 1.38 kV due to the increase of the array temperature. However, the other modules still work around the voltage of 1.48 kV. Figure 3.2 also shows that the $v_{MPP}$ of the PV array under $R = 1\text{KW/m}^2$, $T = 25^\circ\text{C}$ is larger than the $v_{MPP}$ of the PV array under $R = 1\text{KW/m}^2$, $T = 50^\circ\text{C}$. The output power of module 1 and module 2 are shown in Figure 5.15.
5.1. SIMULATION OF THE SYSTEM UNDER DIFFERENT ENVIRONMENT CONDITIONS

Figure 5.15 shows that the output power of PV array 1 decreases from 0.275 MW to 0.26 MW due to the temperature change. The other PV arrays can still provide 0.275 MW. The output voltage of the inverter $v_{HT}$, grid current $i_g$ and grid voltage $v_g$ are shown from Figure 5.16 to Figure 5.17.

![Output voltage of the inverter](image1)

Figure 5.16. Output voltage of the inverter

![Grid voltage and grid current](image2)

Figure 5.17. Grid voltage and grid current

Figure 5.17 shows that the grid current is in phase with the grid voltage which ensures the zero injection of the reactive power.

5.1.4 Step Change in Both the Radiation Level and Temperature

Both the radiation level and the temperature will change in this simulation to test the system reliability. Initially, the whole system operates at the reference condition, at $t = 9.0\,s$, the radiation level for PV array 1 changes from $1\,kW/m^2$ to $0.6\,kW/m^2$ and the temperature of PV array 2 shifts from $T = 25^\circ C$ to $T = 50^\circ C$. The reactive power is still controlled to be zero. The DC link voltage of module 1, module 2 and module 3 are shown in Figure 5.18.
The output power of all the PV arrays and the reactive power, the inverter output voltage $v_{HT}$, the grid current and grid voltage are shown from Figure 5.19 to Figure 5.21.
5.2. REACTIVE POWER EXCHANGE WITH THE GRID

The above figures show that the system can go through the rapidly change environment conditions and MPPT works during the simulation.

5.2 Reactive Power Exchange with the Grid

As mentioned before, sometimes it is required that the inverter can provide or consume reactive power. In the following simulation, the inverter works under the reference environment conditions.

5.2.1 Reactive Power Injection

Initially, the inverter injects zero reactive power to the grid, at \( t = 9.0 \text{s} \), the grid require the inverter to provide 0.5 MVar reactive power. The real and reactive power is shown in Figure 5.22.
CHAPTER 5. SIMULATION RESULTS

It can be seen that the real power keeps constant during the step while reactive power change from 0 to 0.5 MVar. The reason for the reactive power delivery can be seen from the magnitude of the reference waveform, which is shown in Figure 5.23.

The voltage magnitude for the reference waveform increases from 8.37 kV to 8.75 kV which makes more reactive power be transferred from the inverter to the grid.

5.2.2 Reactive Power Consumption

Reactive power consumption means inject negative reactive power to the grid. At first, the inverter injects zero reactive power to the grid, at \( t = 9.0 \) s, the inverter will inject -0.5 MVar reactive power to the grid. The real and reactive power is shown in Figure 5.24.
5.2. REACTIVE POWER EXCHANGE WITH THE GRID

![Graph of real and reactive power into the grid]

Figure 5.24. Real and reactive power into the grid

The voltage magnitude for the reference waveform is shown in Figure 5.25.

![Graph of voltage magnitude of reference waveform]

Figure 5.25. Voltage magnitude of the reference waveform $v_{ref}$
Chapter 6

Conclusions and Future Work

6.1 Conclusions

The task of this master thesis is to develop the control method for the cascaded multilevel inverter with PV arrays as separate DC sources. The software used in this thesis is PSCAD/EMTDC.

From the above section, it is found that PV arrays with MPPT works well under rapidly changing environment condition. This can always ensure that the maximum active power can be injected into the grid. In addition, by using the improved selection mechanism as the modulation method, the simulation results shows that the capacitor voltages can be balanced around their $v_{MPP}$. Moreover, the output voltage of the inverter has 13 levels which makes the shape almost sinusoidal. Finally, the reactive power control method realizes the exchange of reactive power between the inverter and the grid.

6.2 Future Work

There are still some improvements which can be added to the system. First of all, it would be very interesting that the energy storage system such as battery or super-capacitor can be integrated into the system. This will make the system more reliable. When there is no radiation at all, the system can still provide power from the energy storage system.

Secondly, other micro-sources such as wind turbine can also be used as the separate DC sources for each module. However, the output of the wind turbine should be connected to the AC/DC converter to realize this.
Appendix A

A Phasor Estimation Based on a Recursive Least Square Algorithm

This appendix is taken from paper [12].

Assume that a signal is composed of a constant and an oscillating component with a given frequency $\omega$, as in

$$i(t) = I_{ofs} + Re(\tilde{I}_{ph}e^{j\omega t}) \approx \tilde{I}_{ofs} + \tilde{I}_d \cos \omega t - \tilde{I}_q \sin \omega t$$  \hspace{1cm} (A.1)

When the phase reference $\omega t$ is given, a Recursive Least Square (RLS) estimation can be applied to a sequence of measurements of $i_V$ in order to extract the constants $\tilde{I}_{ofs}$, $\tilde{I}_d$, $\tilde{I}_q$, which determine the amplitude and phase of the current according to

$$|\tilde{I}| = \sqrt{\tilde{I}_d^2 + \tilde{I}_q^2}$$  \hspace{1cm} (A.2)

$$\tilde{\phi} = \angle (\tilde{I}_d + j \tilde{I}_q)$$  \hspace{1cm} (A.3)

The formulas based on the stationary solution to the RLS equations are updated with the relative bandwidth $\xi = \frac{\omega_{BW}}{\omega}$. A high bandwidth naturally means faster response, but also a larger sensitivity to noise. During every loop, the algorithm evaluates the error $\epsilon$ between the estimated offset and phasor derivatives, using some amplification factors ($\kappa_{ofs}$, $\kappa_{ph}$, $\mu$), which are calculated using the relative bandwidth $\xi$. The values mentioned are given in the following formulas,

$$\epsilon = i_V - \tilde{i}_V$$  \hspace{1cm} (A.4)

$$\frac{d\tilde{I}_{ofs}}{dt} = \omega \kappa_{ofs} \epsilon$$  \hspace{1cm} (A.5)

$$\frac{d\tilde{I}_{ph}}{dt} = 2\omega \kappa_{ph} \epsilon e^{-j(\omega t + \mu)}$$  \hspace{1cm} (A.6)

where

$$\kappa_{ofs} = \xi (1 + \xi^2)$$  \hspace{1cm} (A.7)
APPENDIX A. A PHASOR ESTIMATION BASED ON A RECURSIVE LEAST SQUARE ALGORITHM

\[ \kappa_{ph} = \xi \sqrt{1 + 1.25\xi^2 + 0.25\xi^4} \quad (A.8) \]

\[ \mu = \zeta \{ (2 - \xi^2) + j3\xi \} \quad (A.9) \]

In typical applications no offset component will exist and only the estimated phasor will be used.
Appendix B

Cascaded Multilevel Converter
Implement in PSCAD/EMTDC
Appendix C

H-bridge VSC with PV array Implement in PSCAD/EMTDC
Bibliography


