Analysis, implementation and experimental evaluation of a phase shifted PWM control system
for a modular multilevel converter

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ANALYSIS, IMPLEMENTATION AND EXPERIMENTAL EVALUATION OF A PHASE SHIFTED PWM CONTROL SYSTEM FOR A MODULAR MULTILEVEL CONVERTER

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ABSTRACT

Nowadays, it is problematic to connect only one power semiconductor switch directly to the grid due to the high voltage range. In order to solve this difficulty, a new type of power converter has been introduced as a solution in high power applications. Multilevel Converters use high speed switching components, avoiding the problem of linking them directly to the grid by connecting single devices among multiple DC levels. Different Multilevel topologies have been developed in the last few years. Multilevel Converters are more complex to modulate than the two-level traditional converters because of the number of switching alternatives that are available. The latest and most promising such topology for high power applications is the Modular Multilevel Converter (M2C). Several control and modulation methods have been suggested for this topology. The aim of this master thesis project is to deeply investigate and evaluate one of them, based on a carrier phase-shifted Pulse Width Modulation (PWM) technique.

Four different control topologies using phase shift PWM techniques on M2C are studied and explored in this work. These topologies include the following loops of control: Averaging Control based on the currents inside the converter, Individual Balancing Control based on the output current and capacitors voltages, and Arm Balancing Control based on the voltage difference between the arms of the converter. The operation principle of an M2C is presented. This project proposes a switching frequency that meets the two required criteria: low enough to maintain cost feasibility, and high enough to reach a harmonic performance target. Additionally, this work proposes an analytic expression for the output voltage spectrum of the converter, which enables prediction of harmonic performance.

Three distinct simulations were performed each one using different control topologies and switching frequencies. The first controller simulated took into account the Averaging Control topology, based on the circulating current. Within this topology both individual and arm balancing techniques are also explored. A second controller is also simulated using Averaging Control, based on the arms currents, as well as the other control loops. For the last case an Averaging Control, based on the arm currents, without the Arm Balancing is simulated. The results of each simulation are discussed and compared.

Finally, these topologies are implemented and verified experimentally on a 10-KVA M2C prototype. The experiments are performed using only one phase and 11-level modulation methods. The controller efficiency is studied and verified through step response analysis.

Keywords

Modular Multilevel Converter, Phased Shifted, Control Topologies, Modulation Techniques.
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INTRODUCTION

Large inverters have traditionally satisfied the ever-increasing demand of high power industrial applications, which currently extends from the tens to hundreds of megawatts. Some examples of this fact are the medium voltage range (2.3 to 13.8 KV) AC motor drives. Nowadays, it is problematic to connect only one power semiconductor switch directly to the grid due to the high voltage range. In order to solve this difficulty, a new type of power converter has been introduced as a solution in high power applications. Multilevel Converters use high speed switching components, avoiding the problem of linking them directly to the grid by connecting single devices among multiple DC levels [1].

Multilevel Converters are found in many applications; industrial motor drives, utility interfaces for renewable energy systems (photovoltaic, wind energy and fuel cells), flexible AC transmission systems (FACTS), high voltage direct current transmission (HVDC), and traction drives systems [2] [5].

The advantages of this type of converter over the conventional two level converter are:

1. They can operate through a lower switching frequency.
2. They draw input current with very low harmonic distortion.
3. They produce a smaller common mode voltage, reducing the stress in the motor bearings.
4. They generate a staircase waveform as an output with much lower harmonic distortion and dv/dt stresses.

These are some of the disadvantages when the number of levels in the converter is increased:

1. Unbalanced voltages are introduced.
2. A greater amount of switches are required.
3. A More complex controller is required due to the amount of capacitors, which need to be balanced.

Several Multilevel topologies have been developed in the last few years. They are more complex to modulate than the two level traditional converters because of the number of switching alternatives that are available [5]. In the last three decades, three main converter topologies have emerged from the many proposed:

• Diode Clamped (Neutral Clamped).
• Flying Capacitor (Capacitor Clamped).
• Cascade Voltage Source, Modular Multilevel Converter (M2C).

Furthermore, several modulation techniques have been developed for these converters. The modulation techniques include: sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE-PWM) and space vector modulation (SVM) [2].

The latest and most promising such topology for high power applications is the Modular Multilevel Converter (M2C). Various control and modulation methods have been suggested for this topology. The aim of this master thesis project is to deeply investigate and evaluate one of them, based on a carrier phase-shifted Pulse Width Modulation (PWM) technique.

Four different control topologies using Phase Shift PWM techniques on Modular Multilevel Converters are studied and explored in this work. These topologies could have three loops of control: Averaging Control based on the currents inside the converter, Individual Balancing Control based on the output current and capacitors voltages, and Arm Balancing Control based on the voltage difference between the arms of the converter. Moreover these topologies are easy to implement and do not demand high processing levels. This project proposes a switching frequency that meets the two required criteria: low enough to maintain cost feasibility, and high enough to reach a harmonic performance target. Additionally, this work proposes an analytic expression for the output voltage spectrum of the converter, which enables prediction of harmonic performance.
2 MULTILEVEL CONVERTER TOPOLOGIES

In the present chapter of the work there are briefly description of the most important topologies developed. In this regard, there will be mentioned their advantages and disadvantages while discussing the different configurations and their operation principles.

2.1 Diode Clamped Multilevel Converter

The first invention in multilevel converters was the so-called neutral point clamped inverter. It was initially proposed as a three level inverter. It has been shown that the principle of diode clamping can extended to any level. A diode clamped leg circuit is shown in Figure 2-1 [2] [3].

The main advantages and disadvantages of this topology are:

Advantages:

- High efficiency for the fundamental switching frequency.
- The capacitors can be pre-charged together at the desired voltage level.
- The capacitance requirement of the inverter is minimized due to all phases sharing a common DC link.

Disadvantages:

- Packaging for inverters with a high number of levels could be a problem due to the quadratically relation between the number of diodes and the numbers of levels.
- Intermediate DC levels tend to be uneven without the appropriate control making the real power transmission a problem.
- Uneven rating in the diodes needed for the converter.

Some of the applications using Multilevel Diode Clamped converters are:

- An interface between High voltage DC transmission line and AC transmission line.
- High power medium voltage variable speed drives.
- Static VAR compensation.
2.2 Flying Capacitor Multilevel Converter

As an alternative for the diode clamped inverter is the capacitor clamped inverter proposed by Meynard and Foch, which shared many of the advantages. The structure of the capacitor clamped inverter is similar to that of the diode clamped converter. The main difference is that the diodes used for the clamping are replaced by capacitors. A Flying capacitor Converter leg circuit is shown in Figure 2-2 [2] [3]. For this topology the most common application is static VAR generation.

The main advantages and disadvantages of this topology are:

Advantages:

• Control of the real and reactive power transmission.
• The large amounts of capacitors allow the inverter to handle voltages drops and spikes, and short outages.
• Redundancies in the switching states are available in order to balance the voltages in the capacitors.

Disadvantages:

• Efficiency is reduced for real power transmission.
• The large amount of capacitors is more expensive and bulky than the diodes in the neutral point clamped inverter. Also packaging is an issue in high number of level converters.
• Initialization of the system and pre charging the capacitor voltages is a complex procedure.

Figure 2-2. One phase 5-level structure of a Flying Capacitor Inverter
2.3 Cascade Voltage Source

The cascaded multilevel inverter is based on the series connection of single leg or double leg (H bridges) inverters with separate DC sources or capacitors. For each of these two types of configurations several states exist regarding to the switches states. Figure 2-3, the single leg unit, has 2 states for each of the two possible current(s) directions while the double unit has 4 states [2] [3].

![Figure 2-3. Left: Single Leg Unit. Right Double Leg Unit](image)

The series connection between the modules is represented in Figure 2-4; each module has a capacitor that is charged and discharged by a controlled DC current. The resultant voltage waveform is made by the addition of the voltage generated in each module that is connected.

![Figure 2-4. Left: Single leg unit connection. Right: Double leg unit connection](image)

The main advantages and disadvantages of this topology are:

**Advantages:**

- The modularized structure allows easy packaging and storage.
- The quantity of possible voltage levels is more than double the number of capacitors in the double leg unit (H bridge).

**Disadvantages:**

- Separated DC sources or capacitor are required for each module.
- A more complex controller is required due to the amount of capacitors, which need to be balanced.
2.3.1 Double Leg (H Bridge)

The double leg unit, as shown in Figure 2-3, consists of a full H-bridge. The series connection of this type of unit is made at the mid-point of each leg. By having two identical legs there is no rigorous way to connect them. This type of unit is characterized by many more states than a single leg unit. The connection of the capacitor to the system or direct connection of the input terminals is reached by selecting one of the 4 possible states for each of the two possible current flow directions.

The states for this type of unit are presented in Figure 2-5. In the figure, the commanded switches are marked with blue and the current path is marked with red. The states where the capacitor is connected to the system are: 01/10, where the current path crosses the capacitor in the other way discharging it, and 10/01. The opposite states the terminals of the modules are direct connected to the circuit [4].

![Figure 2-5. States of a double leg unit for positive current path](image)

For the reverse current path, the states are shown in Figure 2-6. In this table, the current path can cross the capacitor in the opposite way in only one state, 10/01. The states where the capacitor is connected to the system are: 01/10, and 10/01. The other 2 states are for the direct conduction [4].

![Figure 2-6. States of a double leg unit for negative current path](image)

There are the double of the number of semiconductors used in this unit type than the single unit configuration. The extra two switches allow control of power flow in both directions, allowing voltage balancing and control without an external circuit.
2.3.2 Single Leg

Two serial connected switches can characterize the single leg unit as shown in Figure 2-3. Special attention needs to be taken at the time to connect this unit type with the other units and the DC bus. The unit connections are made similar as shown Figure 2-8. The output of one leg is represented by the mid-point of the leg. Each phase-leg consists of two arms: the upper and the lower one connected in series, as shown in Figure 2-9.

The states for a single leg unit are presented in Figure 2-7. In the figure, the commanded switches are marked with blue and the current path is marked in red. The current direction is marked with an arrow on the positive line of the unit. In case of a direct current flow, in states 10, the capacitor is connected. This state is used for capacitor charging and usage. The opposite state for this is the state 01 where the unit works like a simple cable accordingly directly conducting the terminals. This state removes the unit capacitor from the circuit. For the reverse current path the states 01 have the same effect since they conduct the current towards the previous unit. This state have the capacitor removed from the circuit. The state 10 polarize the capacitor in the opposite way, thereby discharging it [4].

![Figure 2-7. States of a single leg unit](image)

The pros of this type of unit are that it is compact, has a low component count and reduced switching loses. The cons on the other hand are that the balancing and control of the voltages in the capacitors is achieved by using an external control.

**Operation Principle**

The series connection of a number of capacitors that can be connected or bypassed could be represented as a continuous, biased, AC voltage source. The sum of the voltages in these controllable voltage sources in one phase leg has to be equal the DC link voltage. Therefore, if the value of the upper voltage source increases, the voltage source value in the lower arm should decrease respectively and vice versa. Feeding active power from the leg in not necessary; it is favorable to transfer if from the DC side to the AC side and vice versa through temporary storage in capacitors. This brings along some problems due to the fact that capacitors do not assure a constant voltage while connected. The capacitor voltages will vary depending the direction of the current. One solution to this problem is to add an auxiliary control circuit for charging or discharging the capacitors while they are not connected. This brings more complication and cost to the whole system. The correct solution is to use the effect that charges and discharges the capacitors through the modulation in order to keep them balanced. However, the inconsistence of the capacitor voltages has to be also taken into account, for which there are employed inductances in each arm of the configuration. The final single-phase M2C circuit is shown in Figure 2-8 and the respective three-phase in Figure 2-9 [2].
Figure 2-8. Inverter’s Leg configuration

Figure 2-9. System Configuration
3 PULSE WIDTH MODULATION TECHNIQUES

In the present chapter of the work there are briefly description of the two modulation schemes using carrier based PWM. This modulation schemes are the phase-shifted and level-shifted. This type of modulation uses triangular carriers and two sinusoidal waves that have the same amplitude and frequency but which are 180° out of phase; one of them for the upper arm and the other for the lower arm. It is also presented the harmonic performance using Phase Shifted modulation schemes.

3.1 Phase Shifted

Phase-shifted multicarrier modulation is derived from unipolar modulation. The expression indicating the relation between the numbers of carriers and the number of voltage levels is shown in Eq. 3-1. All carriers must have the same frequency and peak-to-peak amplitude. The Eq. 3-2 gives the phase difference between two carriers. The frequency modulation index and amplitude modulation index are calculated as shown in Eq. 3-3.

\[ n_{\text{carriers}} = n_{\text{voltage level}} - 1 \]

Eq. 3-1

\[ \varphi_{\text{carriers}} = \frac{360^\circ}{n_{\text{voltage level}} - 1} \]

Eq. 3-2

\[ m_f = \frac{f_{cr}}{f_m} \quad \quad m_a = \frac{V_{ma}}{V_{cr}} \]

Eq. 3-3

It must be noted that in phase shifted modulation the device switching frequency coincides with the carrier frequency, \( f_{cr} = f_{sw} \). As result the line-to-neutral voltage is a \( n_{\text{voltage level}} \) waveform and the line-to-line voltage is \( 2 \times n_{\text{voltage level}} - 1 \), with an equivalent switching frequency of \( f_{eq} = n_{\text{carriers}} \times f_{cr} \) [4].

In Figure 3-1, the first plot illustrates all the carrier waveforms for an arm in one of the phases. The next 4 plots illustrate the pulses and control signals for the switches of an arm with 4 modules. Figure 3-2 represents an ideal output waveform for the arm voltage.

![Figure 3-1](image)

Figure 3-1. Carriers and modulation signal, \( m_f = 20, m_a = 0.9 \). Switch pulses
3.1.1 Harmonic Performance

Based on the derivation in [1], for the double edge natural sample of a half bridge leg, the complete harmonic solution can be expressed in terms of its harmonics components as:

$$V_{an}(t) = \frac{V_{DC}}{2} + \frac{V_{DC}}{2} M \cos(\omega_o t + \theta_0) + \frac{2V_{DC}}{\pi} \sum_{m=1}^{\infty} \frac{1}{m} f_0(m \frac{\pi}{2} M) \sin \left( m \frac{\pi}{2} \right) \cos(\omega_i t + \theta_i)$$

$$+ \frac{2V_{DC}}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{m} f_n(m \frac{\pi}{2} M) \sin \left( (m + n) \frac{\pi}{2} \right) \cos(m(\omega_i t + \theta_i) + n(\omega_d t + \theta_d))$$

Eq. 3-4

In this expression we can find the DC offset, the baseband, carriers' and sidebands' harmonics. Similar to before it is possible to define the harmonics components taking a reference at the midpoint of the DC link, in that case the first term which is defined as the DC offset is discarded [1].

Optimum harmonic cancellation is reached by phase shifting each carrier by $2\pi(i - 1)/N$, where $i$ is the $i$th converter and $N$ is the number of series connected half bridges per arm. In this regard, assuming natural sampling and equal DC voltages across each half bridge, the overall cascade inverter phase leg voltage to the DC link midpoint is given by Eq. 3-5, where $v_{an}^i(t)$ is the output voltage across each half bridge $i$.

$$v_{AN}(t) = \sum_{i=1}^{N} v_{an}^i(t)$$

Eq. 3-5

Substituting Eq. 3-4 into Eq. 3-5 gives:

$$V_{AN}(t) = \frac{V_{DC}N}{2} + \frac{V_{DC}N}{2} M \cos(\omega_o t + \theta_0)$$

$$+ \frac{2V_{DC}}{\pi} \sum_{i=1}^{N} \sum_{m=1}^{\infty} \frac{1}{m} f_0(m \frac{\pi}{2} M) \sin \left( m \frac{\pi}{2} \right) \cos \left( m \left( \omega_i t + \frac{2\pi(i - 1)}{N} \right) \right)$$
The expression for $V_{AN}(t)$ was verified by comparing its result with the one from the discrete Fourier transforms. The verification was performed in MATLAB by implementing an algorithm for a numerical estimation using Eq. 3-6 and the results of the FFT function. In order to use this "FFT" function there was needed the ideal voltage waveform as an input (Figure 3-3). This ideal output comes from the analysis of the control signals obtained by comparing the triangular waveforms with the sinusoidal reference.

Figure 3-3: Ideal leg Voltage Waveform for 5 modules per Arm, $m_f = 20, m_a = 0.9$.

Spectrum calculation from Fourier Transform and expression $V_{AN}(t)$, was found to be similar. Figure 3.4 shows the result from Fourier Transform. Likewise, results obtained from the use of expression $V_{AN}(t)$ are shown in Figure 3-5. Moreover it is even more clear the similitude between both methods when analyzing Figure 3-6.

Figure 3-4. Harmonic Components for 5 modules per Arm using FFT, $m_f = 20, m_a = 0.9$. 

\[ + \frac{2V_{DC}}{\pi} \sum_{i=1}^{N} \sum_{m=1}^{\infty} \sum_{n=0}^{\infty} \frac{1}{m} f_n(m \pi \frac{M}{2}) \sin \left( m + n \frac{\pi}{2} \right) \cos \left( m \left( \omega_c t + \frac{2\pi(i-1)}{N} \right) + n(\omega_0 t + \theta_0) \right) \]

Eq. 3-6
Figure 3-5. Harmonic Components for 5 modules per Arm using $V_{AB}(t), m_f = 20, m_a = 0.9$.

Figure 3-6. Harmonic Components around the first Carrier, $m_f = 20, m_a = 0.9$.

Once verified the Eq. 3-6 it is possible to predict analytically the spectrum of the converter’s output voltage and also calculate the WTHD0 (Weighted Total Harmonic Distortion), which, can be plotted against $m_f$, frequency modulation index, as show in Figure 3-7. A resonable trade off between the harmonic performance and the switching frequency comes when, a $m_f = 19$, in ther words, $f_{cr} = f_{sw} = 950$ Hz, has been chosen for use in the experiments and simulations. At this switching frequency, WTHD0=0.049%
3.2 Level Shifted

The level shifted modulation scheme is a modulation technique similar to the phase shifted PWM technique in relevant aspects such as the number of carrier calculation and the frequency modulation. Nonetheless, this technique differs from phase shifted PWM in the disposition of the triangular carriers, which in this case are vertically situated one after another. In this regard, the bands cover the whole interval and the amplitude modulation index is calculated as shown in Eq. 3-7.

\[ m_a = \frac{V_{ma}}{V_{cr} \left( n_{voltage\ level} - 1 \right)} \quad m_a \in [0,1] \]

Eq. 3-7

Based on the phase disposition of the carriers, level-shifted multicarrier modulations can be divided into the following three subcategories:

- In phase disposition (IPD).
- Alternative phase opposite disposition (APOD).
- Phase opposite disposition (POD)

All of these subcategories differ by the way the carriers are displaced. The displacement does not affect the amplitude or the frequency of the carriers [4].
3.2.1 Phase Disposition (PD)

The in phase disposition, or PD, is based on a single carrier that is multiplied across the entire voltage range. The difference between any two carriers is shown only in the voltage offset, which represents the actual step size of the modulation. In Figure 3-8 the first plot illustrates all the carrier waveforms for an arm in one of the phases. The next 4 plots illustrate the pulses and control signals for the switches. Figure 3-9 represents an ideal output waveform for the arm voltage.

Figure 3-8. Carriers and modulation signal, \( m_f = 20, m_a = 0.9 \). Switch pulses

Figure 3-9. Ideal Arm Voltage Waveform
### 3.2.2 Phase Opposition Disposition (POD)

The phase opposite disposition, or POD, uses two carriers, one for the positive voltage levels and one for the negative voltage levels. The negative voltage levels are shifted by 180 degrees with respect to the carrier for the positive voltage levels. The sign of their corresponding voltage levels in order to fill the entire voltage range then multiplies the carriers. In Figure 3-10, the first plot illustrates all the carrier waveforms for an arm in one of the phases. The next 4 plots illustrate the pulses and control signals for the switches. Figure 3-11 represents an ideal output waveform for the arm voltage.

![Figure 3-10](image1.png)

**Figure 3-10.** Carriers and modulation signal, $m_f = 20, m_d = 0.9$. Switch pulses

![Figure 3-11](image2.png)

**Figure 3-11.** Ideal Arm Voltage Waveform
3.2.3 Alternative Phase Opposition Disposition (APOD)

The alternative phase opposite disposition, or APOD, is based on two carriers that vary in the initial starting voltage level and phase. These two carriers are then multiplies over the entire voltage range. In Figure 3-12, the first plot illustrates all the carrier waveforms for an arm in one of the phases. The next 4 plots illustrate the switches pulses and control signals for the switches. Figure 3-13 represents an ideal output waveform for the arm voltage.

![Carriers and modulation signal, Switch pulses](image)

Figure 3-12. Carriers and modulation signal, $m_f = 20, m_a = 0.9$. Switch pulses

![Ideal Arm Voltage Waveform](image)

Figure 3-13. Ideal Arm Voltage Waveform

3.3 Conclusions

Using the same $m_f$ in the different modulation techniques, the equivalent switching frequency in the level shifted technique is significantly lower than in the phased shifted method. This turns into a better harmonic performance. Phase shifted method distributes the switching instants around the period, inherently providing a better individual balancing performance than the other carrier based methods.
4 ANALYSIS OF THE CONTROL TOPOLOGY

Even though phased shifted provides the best performance in terms of balancing, the problem persist. A constant predefined pattern will connect the same sub modules at the same current status, causing the same capacitor voltage deviation in every fundamental cycle. Unless treated the capacitor voltages will diverge causing unbalanced operation and introducing significantly disturbances in the output waveforms.

This chapter of the thesis deals with the PWM control method and the operating performance of Modular Multilevel Converters. A proper control method has to be designed in order to keep the sum of all capacitor voltages stable (averaging) and to ensure the correct voltage share among all individual capacitors (balancing), without any external balancing circuit. The averaging control relies on adjusting the circulating current from the DC link to the phase leg. While the balancing control has two parts: the individual balancing control, based on the load current and capacitor voltages, and the arm balancing control, which is characterized by reducing the average voltage difference between the positive and negative arms. Using the three control loops enables the converter to realize the stable voltage control in all operating conditions.

4.1 Circuit Configuration

Figure 4-1 shows one phase of a modular multilevel inverter. This leg consists of a stack of 10 bidirectional modules and the two arms inductors. Attention is paid to only one phase because the operating principle in each phase is identical and independent to one another.

![Figure 4-1. Circuit Configuration of a phase modular multilevel inverter [6]](image)

The circuit equation is shown in Eq. 4-1. Where, \( E \) is the supply DC voltage, \( v_{j_u} \) is the output voltage of each module and \( i_{p_u} \) and \( i_{n_u} \) are the positive and negative arms currents. Let the circulating current along the phase be \( i_{Z_u} \) as shown in Eq. 4-2. Using the same nomenclature as [6].
\[ E = \sum_{j=1}^{10} v_{js} + l \frac{d(i_P + i_N)}{dt} \]

Eq. 4.1

\[ i_Z = i_P - \frac{i}{2} = i_N + \frac{i}{2} = \frac{1}{2}(i_P + i_N) \]

Eq. 4.2

### 4.2 Averaging Control Based on the Leg Voltage

Figure 4-3 shows the block diagram of the averaging control. It forces the average voltage, \( \bar{v}_c \) from the phase leg to follow its reference \( v_{\text{Cref}} \), where \( \bar{v}_c \) is given by Eq. 4.3. Let the current reference of \( i_Z \) be \( i_{Z\text{ref}} \) and as shown in the block diagram, it is given by Eq. 4.4. The voltage command obtained from the averaging control \( V_A \) is given by Eq. 4.5.

\[ \bar{v}_c = \frac{1}{10} \sum_{j=1}^{10} v_{cj} \]

Eq. 4.3

\[ i_{Z\text{ref}} = K_1(v_{\text{Cref}} - \bar{v}_c) + K_2 \int (v_c - \bar{v}_c)dt \]

Eq. 4.4

\[ v_A = K_3(-i_{Z\text{ref}} + i_Z) \]

Eq. 4.5

When \( v_{\text{Cref}} \geq \bar{v}_c \), \( i_{Z\text{ref}} \) increases, forcing the actual circulating current \( i_Z \) to follow the reference \( i_{Z\text{ref}} \). As a result \( \bar{v}_c \) follows its reference \( v_{\text{Cref}} \) without affecting the load current \( i_L \) [6] [7].

![Block diagram of Averaging Control](image)

Figure 4-3. Block diagram of Averaging Control

### 4.3 Individual Balancing Control

The balancing control forces the individual capacitor voltage in each module to follow its reference \( v_{\text{Cref}} \), the block diagram of the individual balancing control is shown in Figure 4-4, where the voltage command obtained from this controller is \( v_{\text{B_{Bi}}} \). Since the individual balancing control is centered on either the positive or negative arm, the current polarity of \( v_{\text{B_{Bi}}} \) should change according to that in \( i_P \) (for \( i = 1 \leq 5 \)) or \( i_N \) (for \( i = 6 \leq 10 \)) [6] [7]. When \( v_{\text{Cref}} \geq v_p \), and the arm current is charging the capacitor, the energy should be transferred from the DC link to the capacitor, while if the arm current has the opposite polarity it should be the inverse.
Finally, $v_{Bl}$ is given by:

If $i_p, i_N \geq 0$

$$v_{Bl} = K5(v_{Cref} - v_l)$$

Eq. 4-6

If $i_p, i_N \leq 0$

$$v_{Bl} = -K5(v_{Cref} - v_l)$$

Eq. 4-7

![Figure 4-4. Block diagram of Individual Balancing Control](image)

4.4 Arm Balancing Control

The block diagram of the arm balancing control is shown in Figure 4-5. This control has the function of mitigating the voltage difference between the average of the upper and lower arm voltages $\overline{v_{GP}}$ and $\overline{v_{CN}}$, where they are given by:

$$\overline{v_{GP}} = \frac{1}{5} \sum_{j=1}^{5} v_{cj}$$

Eq. 4-8

$$\overline{v_{CN}} = \frac{1}{5} \sum_{j=6}^{10} v_{cj}$$

Eq. 4-9

Hence, $\overline{v_{GP}}$ and $\overline{v_{CN}}$ represent the average voltage of the positive and negative arms. Where $\varphi$ is the phase difference between the line-to-line voltage of the converter $v$ and the supply current $i$ [8].

$$v_{BA} = \pm K5(\overline{v_{GP}} - \overline{v_{CN}})$$

Eq. 4-10

![Figure 4-5. Block diagram of Arm Balancing Control](image)
4.5 Voltage Command using Averaging Control Based on the Leg Voltage

Figure 4-6 and Figure 4-7 show the voltage command for each module either in the positive or negative arm.

\[ v_{i \text{ref}} = v_A + v_{Bi} + v_{BA} - \frac{v_{ref}}{5} + \frac{E}{10} \]

Eq. 4-11

For \( i = 6 - 10 \)

\[ v_{i \text{ref}} = v_A + v_{Bi} + v_{BA} + \frac{v_{ref}}{5} + \frac{E}{10} \]

Eq. 4-12

The voltage command \( v_{i \text{ref}} \) is normalized by each dc-capacitor voltage \( v_i \), followed by comparison with a triangular waveform having a maximal value of unity and a minimal value of zero with a carrier frequency of \( f_{cr} \). The actual switching frequency of each chopper-cell, \( f_{cr} = f_{sw} \). The ten modules have the ten triangular waveforms with the same frequency but a phase difference of \( 72^{\circ} (= 360^{\circ}/5) \) to each other for achieving harmonic cancellation and enhancing current controllability [8].

4.6 Theoretical Analysis of the Control System

This analysis aims to estimate the correct controller gains that ensure stable operation. It was first described in [8] and it derives an open loop transfer function for \( i_x \). Then based on the “Routh-Hurwitz” criterion estimates the gains margins. Attention is paid to the circulating current because it determines the stability of the converter acting as a state variable [8]. The following relationships with respect to instantaneous active power exist:
\[ v_1 \cdot i_p = v_{c1} \cdot C \frac{dv_{c1}}{dt} = CV_c \frac{dv_{c1}}{dt} \]

Eq. 4-13

\[ v_6 \cdot i_p = v_{c6} \cdot C \frac{dv_{c6}}{dt} = CV_c \frac{dv_{c6}}{dt} \]

Eq. 4-14

Where \( V_c \) is DC component contained in \( v_{c1} \) and \( v_{c6} \). As the controller contributions are considered small, a reasonable approximation of \( v_{c1} = v_{c6} = V_c \). The first three terms of the right hand side of the equations of \( v_{i \text{ref}} \), mentioned before are negligible compared to the last two \( (v_A = v_B = v_{BA} = 0) \). Therefore, \( v_1 \) and \( v_6 \) are given by:

\[ v_1 = v_{1 \text{ref}} \approx -\frac{v_{\text{ref}}}{5} + \frac{E}{10} \]

Eq. 4-15

\[ v_6 = v_{6 \text{ref}} \approx +\frac{v_{\text{ref}}}{5} + \frac{E}{10} \]

Eq. 4-16

Substituting Eq. 4-15 and Eq. 4-16, into Eq. 4-13 and Eq. 4-14 respectively, yields:

\[ CV_c \frac{dv_{c1}}{dt} = -\frac{v_{\text{ref}2}}{5} + \frac{Ei}{10} - \frac{v_{\text{ref}1}}{10} + \frac{Ei}{20} \]

Eq. 4-17

\[ CV_c \frac{dv_{c1}}{dt} = +\frac{v_{\text{ref}1}}{5} + \frac{Ei}{10} - \frac{v_{\text{ref}2}}{10} - \frac{Ei}{20} \]

Eq. 4-18

Since the arms currents are common in all the modules of each arm, these last equations are valid for the rest of the modules. Hence its can be changed into:

\[ CV_c \frac{dv_{CP}}{dt} = -\frac{v_{\text{ref}2}}{5} + \frac{Ei}{10} - \frac{v_{\text{ref}1}}{10} + \frac{Ei}{20} \]

Eq. 4-19

\[ CV_c \frac{dv_{CN}}{dt} = +\frac{v_{\text{ref}1}}{5} + \frac{Ei}{10} - \frac{v_{\text{ref}2}}{10} - \frac{Ei}{20} \]

Eq. 4-20

Adding and subtracting Eq. 4-19 and Eq. 4-20:

\[ CV_c \frac{dv_c}{dt} = +\frac{Ei}{10} - \frac{v_{\text{ref}1}}{10} \]

Eq. 4-21

\[ CV_c \frac{d(v_{CP} - v_{CN})}{dt} = -\frac{2v_{\text{ref}2}}{5} + \frac{Ei}{10} \]

Eq. 4-22
Substituting Eq. 4-11 and Eq. 4.12 into Eq. 4-1 yields

$$10v_A + 10v_{BA} + \sum_{i=1}^{10} v_{Bi} + i \frac{di_z}{dt} = 0$$

Eq. 4-23

Where $v_A$ is the voltage coming from the averaging control, $v_{BA}$ is the voltage coming from the arm balancing control, $v_{Bi}$ is the voltage coming from the individual balancing control. These three voltages are represented as:

$$10v_A = 10K3(i_{zref} - i_z) = 10K3\left(-K1(v_{Cref} - \bar{v}_c) - K2 \int (v^*_c - \bar{v}_c) dt + i_z\right)$$

$$= 10K3i_z - 10K3K1(v_{Cref} - \bar{v}_c) - 10K3K2 \int (v^*_c - \bar{v}_c) dt$$

Eq. 4-24

$$10v_{BA} = 10K5(v_{CP} - \bar{v}_{CN})i$$

Eq. 4-25

$$\sum_{i=1}^{10} v_{Bi} = \sum_{i=1}^{5} v_{Bi} - \sum_{i=6}^{10} v_{Bi} = 5K4(v_{CP} - \bar{v}_{CN})i$$

Eq. 4-26

Substituting Eq. 4.24, Eq. 4-25 and Eq. 4-26 into Eq. 4-23 produce a differential equation in terms of $i_z$,

$$2i \frac{di_z}{dt} + 10K3i_z - 10K3K1v_{Cref} + \frac{K3K1E}{CV_c} \int i_z dt - \frac{K3K2}{CV_c} \int v_{refi} dt + \frac{K5K2}{CV_c} \int v_{ref}dt + K5Ei \int i dt$$

$$- \frac{K3K2E}{CV_c} \int v_{refi} dt - \frac{K4Ei}{2CV_c} \int i dt = 0$$

Eq. 4-27

In Eq. 4-27, the terms related to $i_{zu}$ contribute to the stability of the system, so special attention is paid to the term associated to $i_{zu}$. Furthermore, the output of the arm-balancing controller is multiplied by $\pm 1$, depending on the load phase, in order to get a positive sign in the following equation:

$$2i \frac{di_z}{dt} + 10K3i_z + \frac{K3K1E}{CV_c} \int i_z dt + \frac{K3K2E}{CV_c} \int i_z dt + \frac{2K5K4}{CV_c} \int v_{refi} dt + 2(2K5 - K4)i \int v_{refi} dt = 0$$

Eq. 4-28

The following assumptions are made in order to achieve the linearization by differentiating both parts of the equation:

- $i$ is a sinusoidal only including the fundamental component. Therefore, the relationship of $\frac{d^2i}{dt^2} = -\omega^2i$ is valid.
- In the expressions $v_{refi}$ and $v_{ref} \frac{d}{dt}i_{zu}$, only the DC components are considered this is because the AC does not affect the stability.

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Also assuming:

\[ (v_{ref}l_u)'_{dc} = \frac{Vl \cos \varphi}{\sqrt{3}} \]

Eq. 4-29

\[ (v_{ref} \frac{d}{dt} l_u)'_{dc} = \frac{\omega Vl \sin \varphi}{\sqrt{3}} \]

Eq. 4-30

\[ E = 10 V_c \]

Eq. 4-31

Finally, the equation obtained is:

\[
\frac{d^5}{dt^5} l_z + \frac{1}{T_i} \frac{d^4}{dt^4} l_z + \left( \omega^2 + \frac{1}{T_i T_{v1}} + \frac{\cos \varphi}{T_B^2} \right) \frac{d^3}{dt^3} l_z + \left( \omega^2 + \frac{1}{T_i T_{v1} T_{v2}} + \frac{\omega \sin \varphi}{T_B^2} \right) \frac{d^2}{dt^2} l_z
\]

\[
+ \frac{\omega^2}{T_i T_{v1}} \frac{d}{dt} l_z + \frac{\omega^2}{T_i T_{v1} T_{v2}} l_z = 0
\]

Eq. 4-32

Where,

\[ T_i = \frac{2 La}{10 K 3} \quad T_{v1} = \frac{2 C}{K 1} \quad T_{v2} = \frac{K 1}{K 2} \quad T_B = \sqrt[3]{\frac{3 C \cdot V_c \cdot 2 \cdot 2 l a}{2 (2K 5 - K 4) V I}} \]

Eq. 4-33

The system is stable when the coefficients in the first column, in the so-called “Routh Hurwitz stability criterion”, are all positive. Therefore the following assumption shown in Eq. 4-34 is introduced. Substituting the relations produces Eq. 4-35, where Eq. 4-36 gives \( \alpha \).

\[ T_i \ll T_{v1} \approx T_B \approx \frac{1}{\omega} \ll T_{v2} \]

Eq. 4-34

\[ \pi - \alpha < \varphi < 2\pi - \alpha \]

Eq. 4-35

\[ \alpha = \tan^{-1} \left( \frac{\omega T_{v1}}{1 - \omega^2 T_i T_{v1}} \right) \]

Eq. 4-36

Hence the system is stable as long \( \varphi \), satisfies the last relationship, however if Eq. 4-37 is valid then the system is stable in all operating conditions

\[ K 5 > \frac{K 4}{2} \]

Eq. 4-37

The system is stable in all operating conditions. Figure 4-5 shows the relation between the controller sign and \( \varphi \) [8].
4.7 Averaging Control Based On The Arms Voltages.

A similar controller that will lead to the same \( i_d \), so the stability of the system is not affected is introduced in this section. With the objective to avoid the nonlinearity introduced by the arm balancing loop.

Figure 4-9 and Figure 4-8 shows the block diagram of the averaging control for the positive and negative arms. It forces the average voltage of each arm, \( \bar{v}_{CP} \) and \( \bar{v}_{CN} \) from the phase leg to follow its reference \( v_{Cref} \), where \( \bar{v}_{CP} \) and \( \bar{v}_{CN} \) are given by:

\[
\bar{v}_{CP} = \frac{1}{5} \sum_{j=1}^{5} v_{Cj}
\]

Eq. 4-38

\[
\bar{v}_{CN} = \frac{1}{5} \sum_{j=6}^{10} v_{Cj}
\]

Eq. 4-39

![Figure 4-8. Block diagram of Averaging Control for the Negative Arm](image)

![Figure 4-9. Block diagram of Averaging Control for the Positive Arm](image)
Let the current reference of $i_p$ and $i_N$ be $i_{p,ref}$ and $i_{N,ref}$ and, as shown in the block diagram, are given by:

\[
i_{p,ref} = K_1(v_{Cref} - \bar{v}_{CG}) + K_2 \int (v_{C}^* - \bar{v}_{CG})dt
\]

Eq. 4.40

\[
i_{N,ref} = K_1(v_{Cref} - \bar{v}_{CN}) + K_2 \int (v_{C}^* - \bar{v}_{CN})dt
\]

Eq. 4.41

The voltage commands obtained from the averaging control $v_{AP}$ and $v_{AN}$ are given by:

\[
v_{AP} = K_3 \left(-i_{p,ref} + \frac{i_p}{2}\right)
\]

Eq. 4.42

\[
v_{AN} = K_3 \left(-i_{N,ref} + \frac{i_N}{2}\right)
\]

Eq. 4.43

When $v_{Cref} \geq \bar{v}_{CG}$, $i_{p,ref}$ increases, forcing the actual circulating current $i_p$ to follow the reference $i_{p,ref}$. As a result $\bar{v}_{CG}$ follows its reference $v_{Cref}$ without affecting the load current $i_u$. In a similar way the controller acts on the negative arm.

The control of $i_N$ comes from combining the contributions from the two arm based controllers, with equal shares as the same gains are used.

### 4.8 Voltage Command using Averaging Control Based on the Arms Voltages

Figure 4-10 and Figure 4-11 show the voltage command for each module either in the positive or negative arm, with the new proposed controller.
The positive and negative arm command are obtained as follow:

For $i = 1 - 5$

$$v_i \text{ref} = v_{AP} + v_{Bi} + v_{BA} - \frac{v_{ref}}{5} + \frac{E}{10}$$

Eq. 4-44

For $i = 6 - 10$

$$v_i \text{ref} = v_{AN} + v_{Bi} + v_{BA} + \frac{v_{ref}}{5} + \frac{E}{10}$$

Eq. 4-45

The voltage command $v_i \text{ref}$ is normalized by each dc-capacitor voltage $v_i$, followed by comparison with a triangular waveform having a maximal value of unity and a minimal value of zero with a carrier frequency of $f_{cr}$. The actual switching frequency of each chopper-cell, $f_{cr} = f_{sw}$. The ten modules have the ten triangular waveforms with the same frequency but a phase difference of $72^\circ (= 360^\circ/5)$ to each other for achieving harmonic cancellation and enhancing current controllability [8].
5 SIMULATION RESULTS

In this chapter, in order to validate the efficiency of the described control systems described above in Chapter 4, simulations have been carried out in MATLAB®/Simulink. The results from the simulation are presented and discussed. Simulations have been carried out in only one phase due to the controller in each phase is independent. The ratings used for the simulations are not large-scale converter ratings and they are not a target application for a M2C. In the lab, however, there is down scaled prototype where the control algorithms can be evaluated. In order to have a good overview of the gains orders of magnitude in the experimental verification, simulations parameter were chosen accordingly.

5.1 Averaging Control Based on the Leg Voltage, $f_e=4000$ Hz

The voltage reference $v_{ref}$ for the steady state operation was set to 225 V, which corresponds to a modulation index of 0.9. The switching frequency for each sub module was set to 4 kHz, which actually leads to a converter equivalent switching frequency of 40 kHz, since it consists of a total number of 10 modules per leg. Table 5-1 shows the parameters that were used in the simulations.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated Power S</td>
<td>10 KVA</td>
</tr>
<tr>
<td>Voltage Reference $v_{ref}$</td>
<td>225 V</td>
</tr>
<tr>
<td>Frequency $f_e$</td>
<td>50 Hz</td>
</tr>
<tr>
<td>DC Voltage $E$</td>
<td>500 V</td>
</tr>
<tr>
<td>Load Power Factor</td>
<td>0.95</td>
</tr>
<tr>
<td>Modules/Arm N</td>
<td>5</td>
</tr>
<tr>
<td>Module Capacitance $C$</td>
<td>3.33 mF</td>
</tr>
<tr>
<td>Arm Inductance $L$</td>
<td>3.6 mH</td>
</tr>
<tr>
<td>Arm Resistance $R$</td>
<td>0.1 Ω</td>
</tr>
<tr>
<td>Switching Frequency $f_{sw}$</td>
<td>4000 Hz</td>
</tr>
<tr>
<td>Load</td>
<td>10Ω, 10mH</td>
</tr>
<tr>
<td>Capac. Volt. Ref.</td>
<td>100 V</td>
</tr>
<tr>
<td>K1</td>
<td>1.26</td>
</tr>
<tr>
<td>K2</td>
<td>0.1</td>
</tr>
<tr>
<td>K3</td>
<td>2.78</td>
</tr>
<tr>
<td>K4</td>
<td>0.5</td>
</tr>
<tr>
<td>K5</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 5-1. Simulation Parameters for Control System

5.1.1 Steady State

In Figure 5-1, the output phase voltage shows 11-levels, as the expected. The current waveform in Figure 5-2 is very smooth, due to the high equivalent switching frequency that was used. Figure 5-3 and Figure 5-4 prove the efficiency of the circulating current controller, where the arms currents do not contain a strong second order harmonic, while the circulating current contains an obvious second order harmonic and the average in the circulating current is stable and around 4.5 A.
Figure 5-2. Steady State Output Current

Figure 5-3. Steady State Circulating Current

Figure 5-4. Steady State Arms Currents

Figure 5-6 shows that the average arm capacitors voltage variation does not exceed the value of 8 Volts peak to peak, 8%, and the controller keeps the voltage around the desired average of 100 Volts. It is also shown the impact on the individual capacitor voltages. Figure 5-5 shows that the balancing controller converges in steady state, where the arms voltages are unbalanced. The variation in the average voltage in the arms is larger on the lower than in the upper arm. The arm balancing mechanism does not guarantees that all the intermediate capacitor voltages are kept within the same limits.
The outputs of each loop of control are shown in Figure 5-7, which do not exceed the value of 15 Volts peak to peak, 15%. It is also shown how the individual controller reacts to the changes in the arms currents polarity due to the sign based nonlinearity.
Figure 5-8 and Figure 5-9 show the steady state FFT analysis for output voltage and output current. A small third harmonic may be observed, that is a result of the second order harmonic present in the circulating current. In a 3-phase system this is a common mode and does not appear in the line to line voltage. The Output current WTHD0 factor is 0.49%, without the use of any filters. Table 5-2 and Table 5-3 show the Fourier analysis for the output voltage and output current respectively.

<table>
<thead>
<tr>
<th>Harmonic Order</th>
<th>Amplitude [V]</th>
<th>Phase [°]</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC</td>
<td>0.13</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>211.33</td>
<td>-91.94</td>
</tr>
<tr>
<td>3</td>
<td>4.45</td>
<td>124.57</td>
</tr>
<tr>
<td>5</td>
<td>0.35</td>
<td>-132.61</td>
</tr>
</tbody>
</table>

Table 5-2. Fourier Analysis of the Output Voltage

Output Voltage Spectrum, Fundamental 50Hz

<table>
<thead>
<tr>
<th>Harmonic Order</th>
<th>Amplitude [A]</th>
<th>Phase [°]</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC</td>
<td>0.004</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>20.32</td>
<td>-109.55</td>
</tr>
<tr>
<td>2</td>
<td>0.24</td>
<td>140.70</td>
</tr>
<tr>
<td>4</td>
<td>0.08</td>
<td>-173.62</td>
</tr>
</tbody>
</table>

Table 5-3. Fourier Analysis of the Output Current

Output Current Spectrum, Fundamental 50 Hz
5.1.2 Load Step

In order to verify the effectiveness and transient behavior of the controller a load step was executed at second 0.4, driving from the converter the double of the current. Figure 5-10 shows the response of the output voltage, which has a fast transition. In Figure 5-11 is shown the response of the output current, which is really fast due to the quick recovery of the output voltage and the passive load.

Figure 5-10. Output Voltage Response for a Step Load

Figure 5-11. Output Current Response for a Step Load

Figure 5-12 shows the circulating current behavior, it is clear that there is a slow recovery until the next steady state, where the average is higher than the previous one. There is higher oscillation than the previous steady state, which is comprehensible due to the fact that there is higher power delivered to the AC side of the converter.

Figure 5-12. Circulating Current Response for a Step Load
Figure 5-13 shows the capacitor voltages in each arm during the transient. It is clear that the capacitors in the lower arm are discharged, which means that the power needed to drive the currents comes from the lower arm. The role of the controller once again is to keep each individual capacitor voltage within the same limits and around the desired voltage. The capacitor voltages are finally driven around 100 Volts as shown in Figure 5-14, after a long transient.

![Capacitors Voltages in Upper Arm](image1)

![Capacitors Voltages in Lower Arm](image2)

Figure 5-13. Capacitors Voltages Response for a Step Load

![Capacitors Voltages in Upper Arm](image3)

![Capacitors Voltages in Lower Arm](image4)

Figure 5-14. Capacitors Voltages after Step Load (Detailed)

The recovery time is around 0.3 seconds as shown in Figure 5-15. It is also shown that the voltage oscillation in the capacitor voltages are higher due to the higher output current and the imbalance in the average arms voltages is still present even one second after the transient as shown in Figure 5-16.

![Average Capacitors Voltages in Upper and Lower Arm](image5)

Figure 5-15. Average Voltage in Upper and Lower Arm Response for a Step Load
The outputs of each loop of control are shown in Figure 5-17. It can be seen that there are significant contributions from the averaging and arm balancing controller after the step. Significant contributions are avoidable, as they can lead other part of the control system to saturate.

Figure 5-16. Average Voltage in Upper and Lower Arm after the Step Load

Figure 5-17. Controller Response for a Step Load
5.2 Averaging Control Based on the Leg Voltage, $f_c=950$ Hz

An effort is made to reduce the switching frequency below 1 kHz. The switching frequency for each sub module was set to 950 Hz, which actually leads to a converter equivalent switching frequency of 9.5 kHz, since it consists of a total number of 10 modules per leg. The lower switching frequency was chosen in order to meet a reasonable trade off between the harmonic performance and the switching frequency. The voltage reference $V_{ref}$ for the steady state operation was set to 225 V, which corresponds to a modulation index of 0.9. Table 5-1 shows the parameters that were used in the simulations.

5.2.1 Load Step

A load step was executed at second 0.4 driving the converter the double of the current. It is interesting to show the impacts on all the variables of the converter in order to evaluate the performance of the controller. Figure 5-18 shows the response of the output voltage, the response is slower than the previous simulation case. In Figure 5-19 is shown the response of the output current, where some slight oscillations can be observed immediately after the step.

![Output Voltage Response for a Step Load](image1)

![Output Current Response for a Step Load](image2)
Figure 5-21 shows the circulating current behavior. The average of the current increased as expected, but low frequency oscillations and sudden disturbances are much apparent here than in the previous case.

![Circulating Current](image)

**Figure 5-20. Circulating Current Response for a Step Load**

The role of the controller once again is to keep each individual capacitor voltage within the same limits and around the desired voltage, which is 100 Volts as shown in Figure 5-21. The recovery time is around 0.65 seconds, slower than the previous simulation case as shown in Figure 5-22. It is clear the low frequency oscillations in the average voltage of the arms.

![Capacitors Voltages in Upper Arm](image)

![Capacitors Voltages in Lower Arm](image)

**Figure 5-21. Capacitors Voltages Response after the Step Load (Detailed)**

![Average Capacitor Voltage in Upper and Lower Arm](image)

**Figure 5-22. Average Voltage in Upper and Lower Arm Response for a Step Load**
It is also shown that the voltage oscillation in the capacitor voltages is higher due to the higher output current and the imbalance in the average arms voltages is still present and now magnified due to the lower switching frequency as shown in Figure 5-23.

![Average Capacitor Voltage in Upper and Lower Arm](image)

**Figure 5-23.** Average Voltage in Upper and Lower Arm after the Step Load (Detailed)

Even though that from the analytical study, where the stability should not be affected by the switching frequency, it is obvious that has some effects. Slower response, low frequency oscillations are some of the disturbances or effects present in the variables of the converter.
5.3 Averaging Control Based on the Arms Voltages, \( f_c = 4000 \text{ Hz} \)

This controller is proposed with the goal of deal with each arm separately in order to get a better performance and balancing. The voltage reference \( V_{\text{ref}} \) for the steady state operation was set to 225 V, which corresponds to a modulation index of 0.9. The switching frequency for each sub module was set to 4 kHz, which is an equivalent switching frequency of 40 kHz, due to 10 modules per leg. Table 5-4 shows the parameters that were used in the simulations.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated Power S</td>
<td>10 KVA</td>
</tr>
<tr>
<td>Modules/Arm N</td>
<td>5</td>
</tr>
<tr>
<td>Voltage Reference ( V_{\text{ref}} )</td>
<td>225 V</td>
</tr>
<tr>
<td>Frequency ( f )</td>
<td>50 Hz</td>
</tr>
<tr>
<td>DC Voltage ( E )</td>
<td>500 V</td>
</tr>
<tr>
<td>Module Capacitance ( C )</td>
<td>3.33 mF</td>
</tr>
<tr>
<td>Arm Inductance ( L )</td>
<td>3.6 mH</td>
</tr>
<tr>
<td>Arm Resistance ( R )</td>
<td>0.1 ( \Omega )</td>
</tr>
<tr>
<td>Load Power Factor</td>
<td>0.95</td>
</tr>
<tr>
<td>Switching Frequency ( f_{sw} )</td>
<td>4000 Hz</td>
</tr>
<tr>
<td>Load</td>
<td>10( \Omega ), 10mH</td>
</tr>
<tr>
<td>Cap. Voltage Ref.</td>
<td>100 V</td>
</tr>
<tr>
<td>K1</td>
<td>0.84</td>
</tr>
<tr>
<td>K2</td>
<td>0.1</td>
</tr>
<tr>
<td>K3</td>
<td>1.05</td>
</tr>
<tr>
<td>K4</td>
<td>0.05</td>
</tr>
<tr>
<td>K5</td>
<td>0.1</td>
</tr>
</tbody>
</table>

Table 5-4. Simulation Parameters for Control System

5.3.1 Steady State

In Figure 5-24 the output phase voltage shows 11-levels, as expected. The current waveform in Figure 5-25 is very smooth, due to the high equivalent switching frequency that was used. Figure 5-26 and Figure 5-27 prove the efficiency of the circulating current controller, where the arms currents do not contain a strong second order harmonic. The circulating current has a strong second order harmonic and the average the average values is kept constant around 4 A.
Figure 5-26. Steady State Circulating Current

Figure 5-27. Steady State Arms Currents

Figure 5-28. Steady State Capacitors Voltages

Figure 5-29 shows that the average arm capacitors voltage variation does not exceed the value of 7 Volts peak-to-peak, 7%, lower than the previous simulation cases. The balancing mechanism guarantees that all the intermediate capacitor voltages are kept within the same limits, around 100 Volts, and the balance between the arms voltages is achieved without any problem. Figure 5-29 shows that the balancing controller converges in steady state.
The outputs of each loop of control are shown in Figure 5-30, which do not exceed the value of 12.5 Volts peak to peak, 12.5%. It is also shown how the individual controller reacts to the changes in the arms currents polarity due to the sign based nonlinearity. It is notable how the output of the arm-balancing loop has been reduced.
5.3.2 Load Step

Again the same verification method will be simulated, that is the load step at second 0.4. It is interesting to show the results of how the mechanism impacts on all the variables of the converter. Figure 5-31 shows the response of the output voltage, the peak value is decreased, than the previous steady state. In Figure 5-32 is shown the response of the output current, which remains without significant disturbances.

Figure 5-31. Output Voltage Response for a Step Load

Figure 5-32. Output Current Response for a Step Load

Figure 5-33 shows the circulating current behavior. The harmonic oscillations are greater than the previous steady state, which is comprehensible due to the higher output power.
Figure 5-34 shows the capacitor voltages in each arm during the transient, which is quicker than in the previous controller. It is clearly to see that the capacitors in the upper arm are charged at the beginning of the transient, due to the higher current, while the capacitors in the lower arm are discharged. The discharge in the lower arm is less than in the previous cases. The capacitor voltages are kept around 100 Volts as shown in Figure 5-35, after a shorter transient than in the section 5.1.

The recovery time is around 0.1 seconds as shown in Figure 5-36, faster than in both previous cases. It is also shown that the voltage oscillation in the capacitor voltages is higher due to the higher output current. The imbalance persists, even if the arm-balancing controller is used as shown in Figure 5-37.
Figure 5-37. Average Voltage in Upper and Lower Arm after the Step Load (Detailed)

The outputs of each loop of control are shown in Figure 5-38. In this case the arm balancing controller contributions is comparable small.

Figure 5-38. Controller Response for a Step Load
5.4 Averaging Control Based on the Arms Voltages, $f_c=950$ Hz

An effort is made again to reduce the switching frequency below 1 kHz. The switching frequency for each sub module was set to 950 Hz, which actually leads to a converter equivalent switching frequency of 9.5 kHz, since it consists of a total number of 10 modules per leg. The lower switching frequency was chosen in order to meet a reasonable trade-off between the harmonic performance and the switching frequency. The voltage reference $v_{ref}$ for the steady state operation was set to 225 V, which corresponds to a modulation index of 0.9. Table 5-4 shows the parameters that were used in the simulations.

5.4.1 Load Step

A load step was executed at second 0.3 again, driving from the converter the double of the current. Figure 5-39 shows the response of the output voltage, the peak value is decreased, than the previous steady state. In Figure 5-40 is shown the response of the output current, which is fast but slower than the last simulation case. It is also shown some low frequency oscillations on the current waveform; due to the lower switching frequency compared to the last simulation case.

![Output Voltage Response for a Step Load](image1)
![Output Current Response for a Step Load](image2)
Figure 5-41 shows the circulating current behavior. There is higher oscillation than the previous steady state, which is comprehensible due to the fact that there is higher power delivered to the AC side of the converter. The low frequency oscillations are also present in circulating current waveforms.

Figure 5-42 show the capacitor voltages in each arm during the transient, it is also possible to see some low frequency oscillations in the response. The capacitor voltages are kept around 100 Volts as shown in Figure 5-43.
The recovery time is around 0.2 seconds as shown in Figure 5-44, faster than the last controller. It is also shown that the voltage oscillation in the capacitor voltages is higher due to the higher output current. The imbalance in the average arms voltages is still present as shown in Figure 5-45.

Figure 5-44. Average Voltage in Upper and Lower Arm Response for a Step Load

Figure 5-45. Average Voltage in Upper and Lower Arm after the Step Load (Detailed)

In this last case there is several similarities to the previous case, but the effect of the disturbances, imbalances and low switching frequencies are magnified.
5.5 Averaging Control Based on the Arms Voltages without the Arm Balancing Control, $f_c=4000$ Hz

For this simulation it was decided to remove the arm balancing control loop due to the reduced value of the output compared with the other loops’ outputs in the last simulation case, which turns into a simpler system. The voltage reference $v_{ref}$ for the steady state operation was set to 225 V, which corresponds to a modulation index of 0.9. The switching frequency for each sub module was set to 4 kHz, which actually leads to a converter equivalent switching frequency of 40 kHz, since it consists of a total number of 10 modules per leg. Table 5-7 shows the parameters that were used in the simulations.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated Power S</td>
<td>10 KVA</td>
</tr>
<tr>
<td>Modules/Arm N</td>
<td>5</td>
</tr>
<tr>
<td>Voltage Reference $v_{ref}$</td>
<td>225 V</td>
</tr>
<tr>
<td>Frequency $f$</td>
<td>50 Hz</td>
</tr>
<tr>
<td>DC Voltage E</td>
<td>500 V</td>
</tr>
<tr>
<td>Arm Inductance L</td>
<td>3.6 mH</td>
</tr>
<tr>
<td>Arm Resistance R</td>
<td>3.33 mF</td>
</tr>
<tr>
<td>Load Power Factor</td>
<td>0.95</td>
</tr>
<tr>
<td>Load</td>
<td>10Ω, 10mH</td>
</tr>
<tr>
<td>Switching Frequency $f_{sw}$</td>
<td>4000 Hz</td>
</tr>
<tr>
<td>Cap. Voltage Ref.</td>
<td>100 V</td>
</tr>
<tr>
<td>K1</td>
<td>0.84</td>
</tr>
<tr>
<td>K2</td>
<td>0.1</td>
</tr>
<tr>
<td>K3</td>
<td>1.05</td>
</tr>
<tr>
<td>K4</td>
<td>0.05</td>
</tr>
</tbody>
</table>

Table 5-5. Simulation Parameters for Control System

5.5.1 Steady State

In Figure 5-46, the output phase voltage shows 11-levels, as expected. The current waveform in Figure 5-47 is very smooth, due to the high equivalent switching frequency that was used. Figure 5-48 and Figure 5-49 prove the efficiency of the circulating current controller, where the arms currents do not contain a strong second order harmonic, while the circulating current contains a second order harmonic and the average is kept constant around 4A.
Figure 5-48. Steady State Circulating Current

Figure 5-49. Steady State Arms Currents

Figure 5-50. Steady State Capacitors Voltages

Figure 5-51 shows that the average arm capacitors voltage variation does not exceed the value of 7 Volts peak to peak, comparable to the last simulation cases, and the controller keeps the voltage around the desired average of 100 Volts. The balancing mechanism guarantees that all the intermediate capacitor voltages are kept within the same limits, without the need of any balancing circuit. And the balance between the arms voltages is achieved without any problem. Figure 5-50 shows that the balancing controller converges in steady state and shows also the details of how the controller impacts on the individual capacitor voltages.
The outputs of each loop of control are shown in Figure 5-52, which do not exceed the value of 13 Volts peak to peak. Is also shown how the individual controller reacts to the changes in the arms currents polarity. It is notable how the output of the individual-balancing loop has been reduced.
5.5.2 Load Step

With the aim to verify the efficacy and transient behavior of the new proposed controller a step load was executed at second 0.3, driving from the converter the double of the current. It is interesting to show the impacts on all the variables of the converter. Figure 5-53 shows the response of the output voltage, the peak value is decreased, than the previous steady state. In Figure 5-54 is shown the response of the output current, which remains without significant disturbances.

![Output Voltage Response for a Step Load](image1)

![Output Current Response for a Step Load](image2)

![Circulating Current Response for a Step Load](image3)

Figure 5-53. Output Voltage Response for a Step Load

Figure 5-54. Output Current Response for a Step Load

Figure 5-55 shows the circulating current behavior. It is also shown some low frequency oscillations on the current waveform. There is higher oscillation than the previous steady state, which is comprehensible due to the fact that there is higher current circulating in the arm as shown in Figure 5-56. This higher current it is product of the higher power given to the AC side.
The recovery time is around 0.15 seconds, comparable with the best response in the last simulations. Some low frequency oscillations compared to the last simulation cases. It is also shown that the voltage oscillation in the capacitor voltages is higher due to the higher output current as shown in Figure 5-57. And the balance between the arms voltages is achieved without any problem as shown in Figure 5-58.
The outputs of each loop of control are shown in Figure 5-59. In this case the individual balancing controller contributions is comparable small. The contributions from the averaging controller are smaller than in the previous cases.

![Figure 5-59. Controller Response for a Step Load](image)

5.6 Conclusions

From the simulations studied above, it is possible to conclude that:

- There is no significant effect of the Arm Balancing controller, if the Averaging Controller based on the arms voltages is used.
- There is a faster transient response when the Averaging controller based on the arm voltages is used.
- The Individual Balancing controller provides a really high efficiency.
- When a low switching frequency is used with just a few sub modules, some effects or disturbances are introduced or magnified. These effects are: low frequency oscillations and imbalance. These effects are not predicted by the theoretical analysis, and they are caused due to the less often action of the modulator.

From the numerical result it is favorable to start the experiments verification with a system similar to the one described in section 5.5.
6 EXPERIMENTAL RESULTS

In this part of thesis, the prototype, the procedure followed as well as the experiment results are presented. The results are discussed and compared to the ones obtained from the simulations as was explained in the previous chapter.

6.1 Prototype

The 3-phase prototype consists of 5 modules per arm, each module is rated at 100 Volts for a total rated power of 10 kVA and a total DC link of 500 Volts. The modules consist of a single leg unit with two MOSFETS used as switches as well as a capacitor. A driver that receives the control signal from the inner control drives these transistors in order to perform the modulation. For the inner control of the converter, three main parts are needed. They are, a processor, a data acquisition system and an embedded FPGA. The controller is implemented in the processing unit where the user interface also is. The calculations performed by this part are made in conjunction with analog measurements, of the arm voltages and currents, executed by the data acquisition system. The capacitor voltages are measured individually on each sub module and this signal is optically transferred to the FPGA and the processor, this contributes to the averaging and balancing implementation. The processor transfers the information to the FPGA, which contains a large amount of I/Os to control all the switches. Finally, the FPGA processes the data, and compares it to the phased shifted triangular waveforms thereby producing the control signals for the converter. The control mechanism was developed using National Instruments software LabVIEW v8.6. The Appendix at the end of this document contains diagram of the main control algorithm in the processor. These were created to run the converter prototype [2]. The final prototype form, which contains the control structure as well as the circuit configuration, is shown in Figure 6-1.
Figure 6-2 shows the interface cards for each phase. It also shown the optical receivers as well as the main connectors to the processor unit.

The 10 sub modules of one phase are shown in Figure 6-3.

The 10 capacitors of one phase are shown in Figure 6-4.
6.2 Procedure

The discussion in the previous section covered the 3-phase prototype. Although the aim of the thesis is to verify the control system, the experiments were performed using only one phase, as were the simulations too. This is acceptable because the 1-phase controller is independent to the other phases. Also the only difference is that the voltage references are shifted 120° in the other two phases.

The Averaging Control based on the arm currents, without the arm balancing, simulated in section 5.5, was the first to be examined. The results of this experiment were not as expected. The unbalanced voltages between the arms, as well low frequency oscillations, were present in the waveforms. In order to solve these difficulties deeper investigation was made, analyzing the sign contribution of the controller to the sinusoidal voltage reference. The result was that in particular cases the averaging control loops add the opposite contributions to the system as shown in Tables 6-2 and Table 6-3.

Table 6.1 shows that the correct contribution is made by the individual balancing controller in all the operating conditions.

<table>
<thead>
<tr>
<th>Correct Contribution</th>
<th>Output of the Controller</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{Gref}}&gt;V_{\text{GI}}$</td>
<td>Negative</td>
</tr>
<tr>
<td>$V_{\text{Gref}}&lt;V_{\text{GI}}$</td>
<td>Positive</td>
</tr>
</tbody>
</table>

Table 6.1. Sign contribution of the Individual Balancing Controller

Table 6-2 shows that the averaging controller based on the leg voltage does not make the correct in all the operating conditions. When $V_{\text{Gref}}<V_{\text{C}}$ and $I_{z}>I_{\text{zref}}$ the contribution from the controller is positive when it should be negative.

<table>
<thead>
<tr>
<th>Correct Contribution</th>
<th>Output of the Controller</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{z}&lt;I_{\text{zref}}$</td>
<td>$I_{z}&gt;I_{\text{zref}}$</td>
</tr>
<tr>
<td>$V_{\text{Gref}}&gt;V_{\text{C}}$</td>
<td>Positive</td>
</tr>
<tr>
<td>$V_{\text{Gref}}&lt;V_{\text{C}}$</td>
<td>Positive</td>
</tr>
</tbody>
</table>

Table 6-2. Sign contribution of the Averaging Controller based on the Leg Voltage

Table 6-3 shows that the averaging controller based on the arms voltages does not make the correct in all the operating conditions. When $V_{\text{Gref}}<V_{\text{CP}}/V_{\text{CN}}$ and $I_{p}/I_{N}>I_{\text{pref}}/I_{\text{Nref}}$ the contribution from the controller is positive when it should be negative. Also when $V_{\text{Gref}}>V_{\text{CP}}/V_{\text{CN}}$ and $I_{p}/I_{N}<I_{\text{pref}}/I_{\text{Nref}}$ the contribution from the controller is negative when it should be positive.

<table>
<thead>
<tr>
<th>Correct Contribution</th>
<th>Output of the Controller</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{p}/I_{N}&lt;0$</td>
<td>$I_{p}/I_{N}&gt;0$</td>
</tr>
<tr>
<td>$I_{p}/I_{N}&lt;0$</td>
<td>$I_{p}/I_{N}&gt;0$</td>
</tr>
<tr>
<td>$I_{p}/I_{N}&lt;0$</td>
<td>$I_{p}/I_{N}&gt;0$</td>
</tr>
<tr>
<td>$I_{p}/I_{N}&lt;0$</td>
<td>$I_{p}/I_{N}&gt;0$</td>
</tr>
</tbody>
</table>

Table 6-3. Sign contribution of the Averaging Controller based on the Arms Currents

In order to solve the problem just explained, a temporary controller was implemented. Only proportional gains were used in other words, the integral part of the Voltage major loop was removed. The correct contribution was added to an estimated circulating current reference. This estimation is based on the power transfer from the DC link to the load. The estimated circulating current is given by:

$$i_{Zref} = \frac{VI\cos\phi}{E + \sqrt{E^2 - 4* R * V I \cos\phi}}$$

Eq. 6-1
Where $E$ is the DC link voltage, $V$ is peak voltage of the $v_{\text{ref}}$, $I$ is the peak amplitude of the output current, $\cos \varphi$ is the load factor and $R$ is the arm resistance. This estimated current could be also calculated disregarding the losses in the arm, as shown in Eq. 6-2.

$$i_{z\text{ref}} = \frac{VI \cos \varphi}{2E}$$

Eq. 6-2

Figure 6-5 and Figure 6-6 shows the block diagram of the averaging control for the positive and negative arms. It forces the average voltage of each arm, $\bar{V}_{CP}$ and $\bar{V}_{CN}$ from the phase leg to follow its reference $v_{\text{ref}}$, when $v_{\text{ref}} \geq \bar{V}_{CP}$, $i_{z\text{ref}}$ increases, forcing the actual circulating current $i_z$ to follow the reference $i_{z\text{ref}}$. As a result $\bar{V}_{CP}$ follows its reference $v_{\text{ref}}$ without affecting the load current $i_w$. In a similar way the controller acts on the negative arm.

Finally the individual balancing part was added, but with an increased gain to compensated for any disturbance caused by the other controllers. Figure 6-7 and Figure 6-8 show the voltage command for each module either in the positive or negative arm, with the new proposed controller.
The voltage command $v_{i_{ref}}$ is normalized by each dc-capacitor voltage $v_i$, followed by comparison with a triangular waveform having a maximal value of unity and a minimal value of zero with a carrier frequency of $f_{cr}$. The actual switching frequency of each chopper-cell, $f_{er} = f_{sw}$. The ten modules have the ten triangular waveforms with the same frequency but a phase difference of $72^\circ (= 360^\circ / 5)$ to each other for achieving harmonic cancellation and enhancing current controllability [8].

This controller was tested with two different switching frequencies. The first, $f_{sw}=950$ Hz, where the converter presented low frequency oscillations in the capacitor voltages as well as the arms currents and circulating current. The second one, $f_{sw}=4000$ Hz, which results are presented in the next section. In order to verify the efficiency of the controller several experimentation methods were applied, including steps in the capacitor voltage reference and modulation index.
6.3 Results

In order to confirm the efficiency of the described control system as the solution, experiments have been performed using the prototype explained before. This control system includes the average control based on the arms currents and incorporating the estimated circulating current. Table 6-4 shows the parameters that were used in the experiment. For this experiment it was decided not to include the arm balancing control loop due to the reduced value of the output compared with the other loops’ outputs in the simulations.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated Power S</td>
<td>10 KVA</td>
</tr>
<tr>
<td>Voltage Reference $v_{ref}$</td>
<td>225 V</td>
</tr>
<tr>
<td>Frequency $f$</td>
<td>50 Hz</td>
</tr>
<tr>
<td>DC Voltage $E$</td>
<td>500 V</td>
</tr>
<tr>
<td>Load Power Factor</td>
<td>0.98</td>
</tr>
<tr>
<td>Switching Frequency $f_{sw}$</td>
<td>4000 Hz</td>
</tr>
<tr>
<td>Modules/Arm N</td>
<td>5</td>
</tr>
<tr>
<td>Module Capacitance C</td>
<td>3.33 mF</td>
</tr>
<tr>
<td>Arm Inductance L</td>
<td>3.5 mH</td>
</tr>
<tr>
<td>Arm Resistance R</td>
<td>0.8 Ω</td>
</tr>
<tr>
<td>Load</td>
<td>16Ω, 10mH</td>
</tr>
<tr>
<td>Cap. Voltage Ref.</td>
<td>100 V</td>
</tr>
<tr>
<td>K1</td>
<td>0.8</td>
</tr>
<tr>
<td>K2</td>
<td>0.26</td>
</tr>
<tr>
<td>K3</td>
<td>1.3</td>
</tr>
<tr>
<td>K4</td>
<td>0.8</td>
</tr>
</tbody>
</table>

Table 6-4. Experiments Parameters for Control System

Initially, the voltage reference $v_{ref}$ for the steady state operation was set to 225 V, which corresponds to a modulation index of 0.9. The switching frequency for each sub module was set to 4 kHz, which actually leads to a converter equivalent switching frequency of 40 kHz, since it consists of a total number of 10 modules per leg.

6.3.1 Steady State

In Figure 6-9, the output phase voltage shows 11-levels, as expected. The current waveform in Figure 6-10 is very smooth, due to the high equivalent switching frequency that was used. Figure 6-11 and Figure 6-12 prove the efficiency of the circulating current controller, where the arms currents do not contain a strong second order harmonic, while the circulating current contains a second order harmonic and a strong fourth order harmonic and the average is kept constant.
Figure 6.10. Steady State Output Current

Figure 6.11. Steady State Circulating Current

Figure 6.12. Steady State Arms Currents

Figure 6.13 shows that the average arm capacitors voltage variation does not exceed the value of 5 Volts peak-to-peak, 5 %, lower than the simulation cases, and the controller keeps the voltage around the desired average of 100 Volts. The balancing mechanism guarantees that all the intermediate capacitor voltages are kept within the same limits. The balance between the arms is achieved without any problem. Figure 6.14 shows that the balancing controller converges in steady state and shows also the details of how the controller impacts on the individual capacitor voltages.
Figure 6-13. Steady State Capacitors Voltages

Figure 6-14. Steady State Total Voltage in Upper and Lower Arm

The outputs of each loop of control are shown in Figure 6-15, which do not exceed the value of 6 Volts peak-to-peak. It is also shown how the individual controller reacts to the changes in the arms currents polarity. It is notable how the output of the individual-balancing loop is comparable to the other controller loops outputs. It is also shown the circulating current reference.

Figure 6-15. Steady State Output of the Controllers
Figure 6-16 and Figure 6-17 show the steady state FFT analysis for output voltage and output current. The output current WTHD0 factor is 0.32%, without the use of any filters, comparable to the simulation case. Table 6-5 and Table 6-6 show the Fourier analysis for the output voltage and output current.

### Output Voltage

<table>
<thead>
<tr>
<th>Harmonic Order</th>
<th>Amplitude [V]</th>
<th>Phase [°]</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC</td>
<td>2.94</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>218.32</td>
<td>-89.81</td>
</tr>
<tr>
<td>3</td>
<td>1.52</td>
<td>143.93</td>
</tr>
<tr>
<td>5</td>
<td>0.68</td>
<td>-52.24</td>
</tr>
</tbody>
</table>

**Table 6-5. Fourier Analysis of the Output Voltage**

![Output Phase Voltage Spectrum, Fundamental 50 Hz](image)

**Figure 6-16. Output Voltage FFT Analysis, WTHD0=0.36%**

### Output Current

<table>
<thead>
<tr>
<th>Harmonic Order</th>
<th>Amplitude [A]</th>
<th>Phase [°]</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC</td>
<td>0.14</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>14.16</td>
<td>76.98</td>
</tr>
<tr>
<td>2</td>
<td>0.09</td>
<td>83.06</td>
</tr>
<tr>
<td>4</td>
<td>0.03</td>
<td>90.71</td>
</tr>
</tbody>
</table>

**Table 6-6. Fourier Analysis of the Output Current**

![Output Current Spectrum, Fundamental 50 Hz](image)

**Figure 6-17. Output Current FFT Analysis, WTHD0=0.32%**
6.3.2 Step in the Capacitor Voltages Reference from 100 Volts to 110 Volts

In order to verify the effectiveness and transient behavior of the controller around second 1.5 when the system was in steady state a step in the Capacitor Voltage reference was executed, increasing in 10% the amount of energy stored in the capacitors. It is interesting to show the impact on all the variables of the converter. Figure 6-18 shows the response of the output voltage, the voltage waveform has only 9 levels; due to the fact that each level is represent a larger voltage than the previous steady state. In Figure 6-19 is shown the response of the output current, which does not change during the response.

![Figure 6-18. Output Voltage Response for a Step in the Capacitor Voltage Reference](image)

![Figure 6-19. Output Current Response for a Step in the Capacitor Voltage Reference](image)

Figure 6-20 shows the circulating current behavior, which increased momentarily in order to charge the capacitor therefore following the new reference. The same occurs with arms current as shown in Figure 6-21. After the capacitors are charge both arm currents as well as the circulating current went back to the previous state, stable.

![Figure 6-20. Circulating Current Response for a Step in the Capacitor Voltage Reference](image)
Figure 6-21. Arms Currents Response for a Step in the Capacitor Voltage Reference

Figure 6-22 and Figure 6-24 show the capacitor voltages and average voltage in each arm during the transient respectively. It is clearly to see that the voltages follow the reference really fast and reaches the desired value. The response time is around 0.05 seconds; the capacitor voltages are kept around 100 Volts and after the step around 110 Volts, as shown in Figure 6-23. Imbalance was introduced during the transient time but after that the balanced between the arms is achieved without any problem as shown in Figure 6-25.

Figure 6-22. Capacitors Voltages Response for a Step in the Capacitor Voltage Reference

Figure 6-23. Capacitors Voltages after the Step in the Capacitor Voltage Reference (Detailed)
The outputs of each loop of control are shown in Figure 6-25. It is also shown the Circulating current reference, which increased in order to charge the capacitor as was explained before. The output of the controller do not saturate in any case.
6.3.3 Step in the Modulation Index from 0.9 to 0.6

In order to prove the effectiveness and transient behavior of the controller around second 2.17 when the system was in steady state a step in the Modulation index was executed, from 0.9 to 0.6. It is interesting to show the impact on all the variables of the converter. Figure 6-27 shows the response of the output voltage, the peak value is decreased in order to follow the new reference the voltage waveform has only 7 levels, as expected. In Figure 6-28 is shown the response of the output current, which is really fast and reaches the expected value.

Figure 6-27. Output Voltage Response for a Step in the Modulation Index

Figure 6-28. Output Current Response for a Step in the Modulation Index

Figure 6-29 shows the circulating current behavior, which decreased due to the lower current that the converter is driving to the load. The average is kept constant after the step. The same transient response occurs in the current circulating in the arm as shown in Figure 6-30.

Figure 6-29. Circulating Current Response for a Step in the Modulation Index
Figure 6-30. Arms Currents Response for a Step in the Modulation Index

Figure 6-31 and Figure 6-32 show the capacitor voltages in each arm during the transient. The capacitors are discharged momentarily due to the decreasing in the circulating current. The recovery time is around 0.05 seconds, comparable with the best response. The capacitor voltages are kept around 100 Volts. And the balance between the arms is achieved without any problem therefore the stability of the system is ensured as shown in Figure 6-33 and Figure 6-34.

Figure 6-31. Capacitors Voltages Response for a Step in the Modulation Index

Figure 6-32. Capacitors Voltages after the Step in the Modulation Index (Detailed)
Figure 6-33. Total Voltage in Upper and Lower Arm Response for a Step in the Modulation Index

Figure 6-34. Total Voltage in Upper and Lower Arm after the Step in the Modulation Index (Detailed)

The outputs of each loop of control are shown in Figure 6-34. It is also shown the Circulating current reference, which decreased in order to follow the new reference as was explained before.

Figure 6-35. Controller Response for a Step in the Modulation Index
7 CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

Different control topologies using Phase Shift PWM techniques on Modular Multilevel Converters (M2C) were studied and explored in this work. These topologies included the following loops of control: Averaging Control based on the currents inside the converter, Individual Balancing Control based on the output current and capacitors voltages, and Arm Balancing Control based on the voltage difference between the arms of the converter.

This project also proposed a switching frequency that meets the two required criteria: low enough to maintain cost feasibility, and high enough to reach a harmonic performance target. Additionally, this work proposed an Analytic Expression for the output voltage spectrum of the converter, which enables prediction of harmonic performance.

The operation principle of an M2C was presented, describing the need for a correct balancing algorithm in order to have proper operation. Simulation results with different switching frequencies of the different controllers were also presented. Averaging Control based on the circulating current with Individual Balancing, as well as the Arm Balancing, was the first controller simulated. The circulating current in this case does not contain a strong second order harmonic. The capacitor voltages correctly follow their reference. The transient responses for the step load were fast and did not lead to system instability. The result also shows imbalance between the arm voltages.

In order to solve this difficulty a second controller was simulated, this time using Averaging Control based on the arms currents as well as the other control loops. The capacitor voltages correctly follow their reference. This time the arm voltages were more balanced than the previous case. The circulating current contains a stronger second order harmonic compared to the last case. The transient responses for the step load were faster than the previous case. The results of this simulation led us to eliminate the Arm Balancing Control due to the decrease in the output amplitude.

For the last case an Averaging Control based on the arm currents without the Arm Balancing was simulated. This achieved the balance between the arm voltages successfully unlike the previous cases. The circulating current in this case contains a strong second order harmonic and the capacitor voltages correctly follow their reference. The transient responses for the step load were faster than the previous scenarios. The system reaches stable operation.

Finally, these topologies were implemented and verified experimentally on a 10-KVA M2C prototype. The experiments were performed using only one phase. Several control systems were tested, using 11-level modulation methods. The final controller efficiency was verified through the different experimental methods discussed. Most importantly, the system reaches and maintains a stable operating point quicker than the prediction from simulation with a greater performance.

7.2 Future Work

Future work and studies, concerning the control systems and the experimentation procedure include:

- **Low Switching Frequency**: implementation of the described controller can be done using lower switching frequencies, exploring the limits, in order to achieve the two required criteria explained before.

- **3-phase Implementation**: the next step of the single-phase procedure analyzed in this work is implement 3-phase controller.

- **External Controllers**: Induction Motor drives using conventional speed and torque control, as well as negative sequence controller in order to connected to grids, is the next step of the 3-phase implementation.
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Figure A - 14. Control Simulation Model based on the Arm Currents without the Arm Balancing for M2C
function y=phi()

w=2*pi*50;
C=3.33e-3;
La=3.6e-3;
Lload=10e-3;
Rload=10;
K1=k1;
K3=k3;

alpha=atan(((w*2*C)/K1)/(1-w^2*(2*La/(10*K3))*((2*C)/K1)));
phi=atan(w*Lload/Rload);

if phi>(pi-alpha) && phi<(2*pi-alpha)
    y=1;
elseif phi>=-alpha && phi<=(pi-alpha)
    y=-1;
end

function V = M2C_Spec(p,M,nharm,theta0,N,Vdc)

% Analytic computation of harmonic spectra of N-level unconstrained modulation with
% Natural sampling. The file returns the corresponding
Fourier coefficients.
% p: pulse number
% M: Modulation index
% nharm: number of harmonics to compute
% theta0: phase of FUNDAMENTAL
% mmax=round(nharm/p)+2;
% V=zeros(1,nharm);
% V(1)=N*Vdc/2; % Assume bipolar signal
V(2)=N*Vdc*M*exp(j*theta0)/2;

for k=1:nharm-1,
    loop=1;
    m=1;
    Vc=0;
    while loop,
        n=k-p*m;
        for i=1:N
            Vc=harm(m,n,M)*exp(j*(theta0*n+((i-1)*2*pi/N))*m);
        end
        V(k+1)=V(k+1)+Vc;
    end
    m=m+1;
    if abs(Vc)<0.000001 & m>mmax,
        loop=0;
    end;
end;
function V = harm(m,n,M)
    if n==0,
        V=2*Vdc/m/pi*besselj(0,m*M*pi/2)*sin(m*pi/2);
    else
        V=2*Vdc/m/pi*besselj(n,m*M*pi/2)*sin((m+n)*pi/2);
    end
end

function wthd0()
WTHD=0;
THD=0;
for i=1:95
    P=5+i;
    V_2 = M2C_Spec(P,1,600,0,5,1);
    V2_2=V_2;
    for k=1:300
        V2_2(1,2*k)=V2_2(1,2*k)*-1;
    end
    V3_2=abs(V_2-V2_2);
    V = M2C_Spec(P,0.9,600,0,5,1);
    V2=V;
    for k=1:300
        V2(1,2*k)=V2(1,2*k)*-1;
    end
    V3=abs(V-V2);
    for j=1:598
        WTHD=WTHD+(V3(2+j)/(1+j))^2;
        THD=THD+(V3(2+j)/(V3(2)))^2;
    end
    WTHD0(1,i)=sqrt(WTHD)/(V3_2(2));
    THD0(1,i)=sqrt(THD);
    WTHD=0;
    THD=0;
end
Fs = 1;
T = 1/Fs;
L = 100;
p = (5:L-1)*T;
figure, plot(p,100*WTHD0)
figure, plot(p,100*THD0)
Appendix B: LabVIEW® Model

Figure B - 1. LabVIEW Model of the Controller