
Master thesis performed in Electronics Systems division by

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Analysis and implementation of a digital filter for wire guidance.

Master thesis in Electronics Systems at Linköping Institute of Technology by

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Abstract
This master thesis investigates the possibilities to implement a digital filter for wire guidance in a truck. The analog circuits in the truck, today, are analyzed to understand their signal processing. The component MAX261 is especially interesting and it is analyzed in a special Section to make sure that all needed details, to develop a digital filter, are available. When all theoretical calculation was finished, all the circuits were simulated to make sure that the calculations are correct. The digital filter is based on an analog filter which is expensive and not so easy to purchase. A requirement specification was developed by analysis of the properties of the analog filter and how it is currently used. The analog filter is a part of a chain of analog signal processing which mostly can be performed digitally instead.

The special type of the analog filter makes the requirements, on the digital filter, very tough and an extensive analysis of digital filter structures was performed in order to find a suitable filter. The digital filter is of WDF (Wave Digital Filter)-type and it is very special, because it has two variable coefficients, one for the steepness and one for the center frequency. The digital filter consists of a number of first order filters, because a higher order filter with desired properties has coefficient values that are large which makes the stability properties worse.

The best type of implementation of this filter and the signal processing are also analyzed. Finally, a prototype was developed on a development board where the main component is a DSP (Digital Signal Processor). The program for the prototype is written in C-code and the performance of the system was verified by different tests and measurements.
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<th>Abbreviation</th>
<th>Description</th>
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<tbody>
<tr>
<td>ADC</td>
<td>Analog to Digital Converter</td>
</tr>
<tr>
<td>AGC</td>
<td>Automatic Gain Control</td>
</tr>
<tr>
<td>CLK</td>
<td>Clock</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital to Analog Converter</td>
</tr>
<tr>
<td>DSP</td>
<td>Digital Signal Processor</td>
</tr>
<tr>
<td>EEPROM</td>
<td>Electrically Erasable Programmable Read-Only Memory</td>
</tr>
<tr>
<td>EMI</td>
<td>ElectroMagnetic Interference</td>
</tr>
<tr>
<td>FFT</td>
<td>Fast Fourier Transform</td>
</tr>
<tr>
<td>FIR</td>
<td>Finite Impulse Response</td>
</tr>
<tr>
<td>FPGA</td>
<td>Field Programmable Gate Array</td>
</tr>
<tr>
<td>IIR</td>
<td>Infinite Impulse Response</td>
</tr>
<tr>
<td>LED</td>
<td>Light-Emitting Diode</td>
</tr>
<tr>
<td>MCU</td>
<td>Main Control Unit</td>
</tr>
<tr>
<td>WDF</td>
<td>Wave Digital Filter</td>
</tr>
<tr>
<td>OP</td>
<td>OPerational amplifier</td>
</tr>
<tr>
<td>PSOC</td>
<td>Programmable System on Chip</td>
</tr>
<tr>
<td>PWM</td>
<td>Pulse-Width Modulation</td>
</tr>
<tr>
<td>SC</td>
<td>Switched Capacitor</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal to Noise Ratio</td>
</tr>
<tr>
<td>TMHE</td>
<td>Toyota Material Handling Europe</td>
</tr>
<tr>
<td>VGA</td>
<td>Variable Gain Amplifier</td>
</tr>
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1 Introduction

In the first chapter, a background for this thesis work is presented together with the objective of the thesis. There are also presented the problem constraints and limitations. At the end of this chapter, a report structure is outlined.

1.1 Background

Toyota Material Handling Europe (TMHE) is a world leader in material handling solutions [1]. The TMHE, in Mjölby, develops and manufactures different truck types for many types of purposes. One of them is the VCE150, see Figure 1. The VCE150 is a truck developed for narrow aisles and it operates in narrow aisles with help from rail or wire guidance. The narrow aisles truck makes the warehouse able to store more goods in a smaller area, because the area of the aisles can be much smaller. The problem is to operate a large truck fast in a small aisle and the solution is thus wire guidance [2].

![Figure 1. The VCE150 truck for narrow aisles from TMHE.](image)

The wire guidance system consists of a wire in the floor, two antennas, a filter on the truck, and a steering algorithm. The antenna is not just picking up the frequency of the wire but it is picking up all signals in the room. The truck also consists of a many electrical components that disturb the signal when it goes through a cable, from the antenna to the Main Control Unit (MCU). Therefore, the signal has to be filtered through a bandpass filter so the MCU can analyze how far the truck is, from the wire, to keep it straight in the aisle [3], see Figure 2.
The problem is that the current filter is analog and it has a specific filter component, MAX261 which is expensive and not so easy to obtain. The problem with the analog signal, sent through the truck, is that the electrical components in the truck can easily disturb the signal. A solution to these problems is to replace the analog filter with a digital filter implemented in some sort of Digital Signal Processor (DSP), Field Programmable Gate Array (FPGA), or Programmable System on Chip (PSoC). It would also be interesting to analyze the opportunities to replace more analog components with digital signal processing.

1.2 Wire guidance system basics
The wire, to follow in the wire guidance system, basically consists of a wire in the floor and a frequency generator, see Figure 3.

Each of the antennas consists of four coils. Two coils, in the center, are coupled in series which make the antenna have three output signals to the filter card. The magnetic field from the wire and the position of the coils on the antenna is shown in Figure 4.
The load antenna is placed in front of the truck and the tractor antenna in the rear of the truck, as in Figure 5.

1.3 Objective
The objective of this master thesis is to implement a digital filter that is at least as good as the analog filter component MAX261. This will be done by analyzing the current analog filter and analog signal processing. After analyzing the analog filter, a requirement specification for the digital filter based on the analog filter will be created. Based on the requirement specification, a suitable digital filter will be created. For implementation of a suitable solution, for digital signal processing, an investigation must be done to find the most suitable type of realization for the digital implementation. The realization also needs some type of software or programming. Therefore, developing prototype software is needed. In the end, this will result in a product that will be tested either in a testbench or in a truck.

1.4 Problem Constraints and Limitations
The master thesis includes the parts of the wire guidance system such as antenna card, filter card, and those parts of the MCU that communicate with the antenna card and filter card. The other part of the MCU, which is not communicating with the antenna card and filter card, is not included in this thesis. There is also a lot of software written for the MCU. The included parts are those responsible for calibrating the antenna card and filter card components. The parts, where the filter data is processed in the MCU, are not included.
1.5 Tools
The tools that are needed in this thesis are presented in this section.

1.5.1 MATLAB
MATLAB is a software analysis tool that can be used for example for signal processing and filter design.

1.5.2 Cadence Pspice
Pspice is a circuit analysis tool which is used for simulating the circuits.

1.5.3 Code composer studio
Code composer studio is a development and debugging tool for Texas Instruments components.

1.6 Report Structure
- The first chapter describes the background of the thesis and also the objectivities with the thesis.
- The second chapter analyzes the circuits and it contains detailed information about the current wire guidance system.
- Chapter three investigates the most suitable filter structure for this application.
- The fourth chapter describes how the implementation of a prototype is done.
- Chapter five provides the results.
- In Chapter six, the thesis is summarised and some future work is presented.
2 Theory – Analysis of the wire guidance system

This chapter contains the analysis of the antenna card, filter card, and the C-code. The theoretical analysis is complemented with simulations in Cadence Pspice to verify the theoretical analysis.

2.1 Analysis of circuit - Antenna card

The main function of the antenna card is to pick up the magnetic field from the wire in the floor and convert it into an electric signal. This is performed in the following way. The magnetic field is picked up by the coils, the signal from the coils are bandpass filtered by the passive RC-filter. The output from the RC-filter will then be amplified and lowpass filtered. Finally the signal passes through an EMI (Electro-Magnetic Interference) filter before it is transferred to the filter card.

The antenna card consists of a number of different parts that will be analyzed one by one. The whole circuit is as in Figure 6. The circuit is analyzed by starting with adjustable voltage regulator and then the parts one by one as they are placed in order in the block scheme. The switch is analyzed after Input OP-amplifier.

The function of the parts, in the system, is described largely by the block scheme in Figure 7.

2.1.1 The adjustable voltage regulator

The adjustable voltage regulator is used to get a stabilized voltage and its circuit diagram is shown in Figure 8.
The $V_{SUP}$ can be calculated as the voltage over the resistance $R_{25}$ is 1.25 V and the current through $R_{26}$ is $I_{ADJ} = 50 \mu V$, which is given by thedatasheet for the LM317L [4]. Then, the $V_{SUP}$ can be calculated as

$$V_{SUP} = 1.25 \left( 1 + \frac{R_{26}}{R_{25}} \right) + I_{ADJ} R_{26} = 7.4125 \text{ V}.$$ 

The voltage $V_{REF}$ can be calculated as

$$V_{REF} = \frac{C_{13} C_{15} C_6 C_{30} R_{27}}{R_{28} + C_{13} C_{15} C_6 C_{30} R_{27}} V_{SUP}.$$ 

It can be assumed that the supply voltage has low frequency. Ignoring the capacitances, the $V_{REF}$ can be expressed as

$$V_{REF} = \frac{R_{27}}{R_{28} + R_{27}} V_{SUP}$$

where $R_{27}$ and $R_{28}$ is 1 kΩ. Then

$$V_{REF} = \frac{V_{SUP}}{2} = 3.7062 \text{ V}.$$ 

In the rest of this report, $V_{SUP}$ is also called $VSUP$ and $V_{REF}$ is also called $VREF$.

### 2.1.2 The coil which induces voltage into the circuit.

The left, right, and near wire coils are connected to $V_{REF}$ to make the signal have an offset of $V_{REF}$ and vary around that level. The left and right coils are single, see Figure 9, but the near wire has double coils, see Figure 10, which should make it induce twice as much voltage in the circuit.

![Figure 8. The adjustable voltage regulator circuit on the antenna card.](image8)

![Figure 9. Left and right coil couplings.](image9)

![Figure 10. Near wire coil coupling.](image10)
2.1.3 **RC-filter after the coil.**

The passive RC circuit, after the coils, is performing passive filtering with bandpass characteristics. The circuit consists of two capacitances and two resistances coupled as in Figure 11.

![Figure 11. RC-circuit after the coils.](image)

The analysis of this circuit starts with calculating the parallel coupling as

\[
R_4 \parallel C_1 : \frac{1}{R} = \frac{1}{R_4} + j\omega C_1 \iff R = \frac{1}{\frac{1}{R_4} + j\omega C_1} = \frac{R_4}{1 + j\omega C_1 R_4}.
\]

Because of the voltage sharing, \(V_{OUT}\) can be expressed as

\[
V_{OUT} = \frac{R_4}{R_3 + \frac{1}{j\omega C_2} + \frac{R_4}{1 + j\omega C_1 R_4}} V_{IN} = \frac{R_4}{R_3 + j\omega C_1 R_4 R_5 + \frac{1}{j\omega C_2} + \frac{C_1 R_4}{C_2}} V_{IN} = \frac{j\omega C_2 R_4}{1 + j\omega(C_1 R_4 + C_2 R_5 + C_2 R_4) - \omega^2 C_1 C_2 R_4 R_5} V_{IN}.
\]

So, the transfer function is

\[
H_{\text{RC-input}} = \frac{V_{IN}}{V_{OUT}} = \frac{j\omega C_2 R_4}{1 + j\omega(C_1 R_4 + C_2 R_5 + C_2 R_4) - \omega^2 C_1 C_2 R_4 R_5}.
\]

With the component values, as in Figure 11, the magnitude and phase are shown in Figure 12. The magnitude and phase functions for the two coils, in series, are shown in Figure 13.

![Figure 12. The magnitude and phase characteristics for the transfer function, \(H_{\text{RC-input}}\).](image)
2.1.4 **OP after RC-filter**

The OP circuit, in Figure 14, will amplify the signal depending on whether $V_{R2}$ is connected to $V_{REF}$ or to a high impedance. So, the circuit has two different characteristics, e.g., two different levels of amplification depending on $V_{R2}$.

![Figure 14. The OP-amplifier circuit after the RC-filter.](image)

With the first case, when $V_{R2}$ has a high impedance, $R_2$ can be ignored. By using Kirchhoff’s law on the node $V_-$, negative input to the OP, gives

$$
\frac{V_{OUT} - V_-}{R_1} + \frac{V_{REF} - V_-}{R_3} = 0 \iff V_{OUT} = \frac{R_1 + R_3}{R_3} V_- - \frac{R_1}{R_3} V_{REF}.
$$

This gives the transfer function as

$$
H_{OP-inp} = \frac{V_{OUT}}{V_{IN}} = \frac{R_1 + R_3}{R_3}.
$$

In the second case, $V_{R2} = V_{REF}$ which gives

$$
\frac{V_{OUT} - V_-}{R_1} + \frac{V_{REF} - V_-}{R_2} + \frac{V_{REF} - V_-}{R_3} = 0 \iff V_{OUT} = \frac{R_2 R_3 + R_1 R_3 + R_3}{R_2 R_3} V_- - \frac{R_1 R_3 + R_2 R_3}{R_2 R_3} V_{REF}.
$$
The transfer function is
\[ H_{\text{OP-inp}} = \frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{R_3 R_2 + R_2 R_3}{R_2 R_3}. \]

For the first case, the gain is 4.32226 which is 12.7142 dB and for the second case, the gain is 5.14871 which correspond to 14.234 dB.

### 2.1.5 Switch Philips HEF4066B
The circuit in Figure 15 is used to create \( V_{R2} \). The function is that the \( V_E \) signal controls the switch and therefore \( V_{R2} \) [5].

![Image of the switch Philips HEF4066B](image)

**Figure 15.** The switch Philips HEF4066B.

### 2.1.6 Analog demultiplexer 74HC4051
The analog demultiplexer is used so that the signal can be sent through different resistances at the output. The desired output, i.e., X0-X7, is decided by the signals A, B, and C. There are also signals such as an active low enable, ground, and the voltage supply connections, as in Figure 16.

![Image of the analog demultiplexer 74HC4051](image)

**Figure 16.** The analog demultiplexer 74HC4051.

### 2.1.7 OP-amplifier at the output
The OP at the output, see Figure 17, has two different purposes. The first is to lowpass filter and the second is that, along with the analog demultiplexer, to create an 8 step variable gain. According to the output resistance, the gain will be different.
To calculate the transfer function, two things have to be taken in mind the term $V_{\text{REF}}$ is ignored because it is just an offset. The voltage $V_\text{.}$ will be kept low from the OP so it can be assumed that $V_\text{.} = 0$. Then

$$\frac{V_\text{IN}}{R_X} + \frac{V_\text{OUT}}{R_S C_S} = 0.$$  

The parallel coupling need to be calculated, which is done as

$$R_S C_S = \frac{1}{\frac{1}{R_S} + j\omega C_S} = \frac{R_S}{1 + j\omega C_S R_S}.$$  

So, the transfer function is

$$H_{\text{OP-OUT}} = \frac{V_{\text{OUT}}}{V_{\text{IN}}} = -\frac{R_S C_S}{R_X} = -\frac{R_S}{R_X} \frac{1}{1 + j\omega C_S R_S}.$$  

The magnitude and phase responses for the different $R_X$ are shown in Figure 18.

**Figure 17.** OP-amplifier at the output with the resistance after demultiplexer.

**Figure 18.** Magnitude and phase for 8 different values of $R_X$

### 2.1.8 Output capacitor and ferrite

At the output of the antenna card, there is a capacitor and a ferrite as in Figure 19. The capacitor is used to block DC-level and the ferrite is an EMI-filter. When the signal has passed through the ferrite, it will go to the filter card. The Magnitude characteristics for the ferrite are shown in Figure 20 where the used ferrite type is marked [6].
Total magnitude and phase of the whole circuit

The total transfer function for a cascaded system is obtained by multiplying all the transfer functions as [14]

\[ H_{\text{Total}} = H_{\text{RC-input}} \times H_{\text{OP-input}} \times H_{\text{OP-OUT}} \times H_{\text{Ferrite}}. \]

This will give the transfer function for the whole circuit whose magnitude and phase are shown in Figure 21. This transfer function appears when the switch is on and when the demultiplexer output is X7. The other transfer functions look similar but the gain is different so the curve can be about 35 dB lower with the smallest possible gain. The phase characteristics are the same for all different gains.
2.1.10 Control signals from filter card

From the filter card, there are four control signals sent to the antenna card, one to control the switch and three to control the demultiplexer. The control signal lines have pull up resistances to make the signal have the right voltage level, as in Figure 22.

![Figure 22. The control signal lines from the filter card.](image)

The control signal, to the demultiplexer $V_{OUT}$, has a maximum voltage of $VSUP$, 7.2 V, when no current flows to $V_{IN}$. The minimum voltage is

$$V_{OUT} = VSUP \cdot \frac{R_{24}}{R_{24} + R_{23}} = 2.96V.$$

2.2 Analysis of circuit - Filter card

The main function of the filter card is to filter the signal from the antenna card. The functions of the filter card are to amplify, rectify, smooth, and filter the signal, as in Figure 23. The filter card supplies the antenna card with the supply voltage and the control signals from the MCU [7].

The signal from the antenna card passes the filter card as follows: First, it passes through an amplifier and a lowpass filter. Then, the signal passes the component MAX261 that is managed as a double second order switched capacitor (SC) bandpass filter. The embedded OP in the MAX261 is used as a lowpass filter. After the MAX261, the signal passes through three OPs which rectify, smooth, and amplify the signal. Finally, the signal comes to a sample and hold circuit which freezes the output signal at the input voltage level.

![Figure 23. Block scheme of the whole filter card.](image)
2.2.1 Input OP circuit – Lowpass filter
The OP is a part of the circuit that amplifies the signal and lowpass filters it as well, see Figure 24. The resistances are chosen so the gain is one. The capacitor $C_{50}$ is just a decoupling capacitor.

![Figure 24. Input OP-amplifier and lowpass circuit.](image)

Node analysis of $V_{\text{in}}$ gives

$$\frac{V_{\text{IN}} - V_{\text{in}}}{R_{115}} + \frac{V_{\text{OUT}} - V_{\text{in}}}{R_{116} C_{55}} = 0.$$  

The transfer function is

$$H_{\text{OP-inp-\text{lp}}} = \frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{R_{116}}{R_{115} + j \omega C_{55} R_{115} R_{116}} = -\frac{R_{116}}{R_{115}} \frac{1}{1 + j \omega C_{55} R_{116}}.$$  

The resistances $R_{115}$ and $R_{116}$ have the same values so the transfer function can be rewritten as

$$H_{\text{OP-inp-\text{lp}}} = -\frac{1}{1 + j \omega C_{55} R_{116}}.$$  

The magnitude and phase characteristics for the transfer function are shown in Figure 25.

![Figure 25. Magnitude and phase for the transfer function for the input OP-amplifier.](image)

2.2.2 Analog SC filter MAX261
The component MAX261 is a time-discrete analog SC-filter [8]. The coupling of MAX261 is shown in Figure 26. The component MAX261 is fully analyzed in Section 2.4.
The capacitors $C_{25}$, $C_{28}$, $C_{31}$, and $C_{34}$ are the decoupling capacitors to avoid disturbances in the supply voltage. First, the voltage $V_+$ is calculated as

$$V_+ = \frac{R_{92} + R_{93} + R_{87}}{R_{96} + R_{92} + R_{93} + R_{87}} 12 = 0.9989 \cdot 12 = 11.9874 \approx 12V.$$ 

Then, the voltage for GND connection is computed as

$$V_{GND} = \frac{R_{96} + R_{92}}{R_{96} + R_{92} + R_{93} + R_{87}} 12 = \frac{1}{2} 12 = 6V.$$ 

And finally the voltage for $V_-$ becomes

$$V_- = \frac{R_{96}}{R_{96} + R_{92} + R_{93} + R_{87}} 12 = 0.0011 \cdot 12 = 0.0126 \approx 0V.$$ 

### 2.2.3 Embedded OP in MAX261

The component MAX261 contains an embedded OP which is used as both an amplifier and a lowpass filter. The gain depends on the values resistances shown in Figure 27, $16.2/20 = 0.81$.

The calculations are the same as in the OP in Section 3.2.1, see Figure 24. So, the transfer function is

$$H_{OP-emb\text{-}lp} = \frac{V_{OUT}}{V_{IN}} = -\frac{R_{84}}{R_{81}} \frac{1}{1 + j\omega C_{22} R_{84}}$$

The magnitude characteristics and phase of the transfer function are shown in Figure 28.
2.2.4 Transfer function from input to the rectifier

The transfer function from the input on the filter card to the rectifier circuit, is shown in Figure 29. The transfer function for MAX261 is calculated in Section 2.4. The component MAX261 has two standard center frequencies of 5.2 kHz and 6.25 kHz but the center frequency can vary from about 1 kHz up to 11 kHz.

2.2.5 The rectifier and amplifier circuit.

The OPs after the MAX261 converts the AC-amplitude to a DC-level, see Figure 30. In Figure 33, the input amplitude is plotted against the output DC-voltage.
The first OP and the diodes, along with the resistors, is a rectifier circuit. Because of the diodes, the circuit has two different transfer functions: one when \( V_{IN} > 6 \text{ V} \) and one when \( V_{IN} < 6 \text{ V} \). So, the transfer function is not a good way to describe the function of this circuit, instead it is better to analyze the signal in the time domain. The second OP is a lowpass filter with very low cut off frequency. The transfer function is

\[
H_{LP} = \frac{R_{19}}{R_3} \cdot \frac{1}{1 + j\omega C_3 R_{19}}.
\]

The 3 dB cut off frequency for the transfer function can be calculated as

\[
|j\omega C_3 R_{19}| = 1 \Leftrightarrow \omega = \frac{1}{C_3 R_{19}} \Leftrightarrow 2\pi f = \frac{1}{C_3 R_{19}} \Leftrightarrow f = \frac{1}{2\pi C_3 R_{19}} = 5.97 \ [Hz] \approx 6 \ [Hz].
\]

So, this circuit will make an average of the signal.

The circuit is easiest to analyze in two parts as shown in Figure 31 and Figure 32.

To analyze the rectifier circuit, assume that the input signal is \( v_{IN} = 6 - A\sin(\omega t) \). This circuit operates around a bias point of 6 volts and two cases of \( V_{IN} > 6 \text{ V} \) and \( V_{IN} < 6 \text{ V} \).

The analysis starts with \( V_{IN} > 6 \text{ V} \). Then the circuit can be simplified because one of the diodes conducts. So, current can flow from node \( V_1 \) to the output of the OP but not from the output of the OP to \( V_X \). The OP will compensate with a current from \( V_1 \) to the output of the OP. The nodes \( V_1 \) and \( V \) have the same potential and now current flows through \( V_X \). Then, \( V_X \) has the same potential as the bias of 6 volts.

The second case is when \( V_{IN} < 6 \text{ V} \). Then, the OP will draw a current from the output to \( V_X \) to compensate for the lower input voltage. Because no current will flow into the minus input on the OP, all the current through \( R_{23} \) also flows through \( R_{17} \). Then,
\[ V_X = 6 + A \sin(\omega t). \]

Because the second OP makes an average of the signal, this time-averaged signal will be analyzed to describe the function of the circuit. The time-average of \( v_{\text{IN}} \) is just six because the time-average of a sinusoidal over a single period is zero. The time average of the node \( V_X \) is a bit different and is calculated as

\[
V_{X, \text{AVG}} = \frac{1}{T} \int_{0}^{T/2} 6 \, \text{d}t + \int_{T/2}^{T} 6 + A \sin(\omega t) \, \text{d}t = 6 + \frac{1}{T} \left[ \frac{A \cos(\omega t)}{\omega} \right]_{T/2}^{T} = 6 + \frac{A}{\pi}.
\]

To hold the \( V_- \) at the same level as the other input of the OP, the OP will compensate the output with

\[ V_{\text{OUT,AVG}} = 6 - \frac{R_{19} A}{R_{24} \pi}. \]

The inverter has two different purposes, i.e., to invert the input and to amplify the signal.

![Figure 32. The inverter and amplifier after the rectifier.](image)

The analysis starts with calculation of the gain. Node analysis for the nodes \( V_- \), \( V_+ \), OP-inputs, and \( V_{\text{OUT}} \) give

\[
\frac{V_{\text{IN}} - V_-}{R_7} + \frac{V_X - V_-}{R_1} = 0 \iff V_X = R_1 \left( \frac{V_-}{R_1} + \frac{V_{\text{IN}} - V_-}{R_7} \right) = V_- \left( 1 + \frac{R_1}{R_7} \right) - \frac{V_{\text{IN}}}{R_7} = \frac{V_- R_1}{R_7} \tag{1}
\]

\[
\frac{V_{\text{REF}} - V_-}{R_{13}} + \frac{V_{\text{OUT}} - V_-}{R_{14}} = 0 \iff V_+ = \frac{R_{14}}{R_{13} + R_{14}} V_{\text{REF}} + \frac{R_{13}}{R_{13} + R_{14}} V_{\text{OUT}} \tag{2}
\]

\[
V_- = V_+ \tag{3}
\]

\[
\frac{V_{\text{REF}} - V_{\text{OUT}}}{R_{13} + R_{14}} + \frac{V_X - V_{\text{OUT}}}{R_9} + 0 - \frac{V_{\text{OUT}}}{R_{21}} = 0 \tag{4}
\]

Combination of (2) and (3) gives

\[ V_- = \frac{R_{14}}{R_{13} + R_{14}} V_{\text{REF}} + \frac{R_{13}}{R_{13} + R_{14}} V_{\text{OUT}}. \tag{5} \]

Inserting (1) in (4) gives

\[
\frac{V_{\text{REF}} - V_{\text{OUT}}}{R_{13} + R_{14}} + \frac{V_- \left( 1 + \frac{R_1}{R_7} \right)}{R_9} - \frac{V_{\text{IN}}}{R_7 R_9} - \frac{V_{\text{OUT}}}{R_9} - \frac{V_{\text{OUT}}}{R_{21}} = 0. \tag{6}
\]

Then, inserting (5) in (6) gives
\[
\frac{V_{\text{REF}} - V_{\text{OUT}}}{R_{13} + R_{14}} + \frac{R_{14}}{R_{13} + R_{14}} \frac{V_{\text{REF}}}{R_9} \left(1 + \frac{R_{1}}{R_7}\right) + \frac{R_{13}}{R_{13} + R_{14}} \frac{V_{\text{OUT}}}{R_9} \left(1 + \frac{R_{1}}{R_7}\right) - V_{\text{IN}} \frac{R_{1}}{R_9} - \frac{V_{\text{OUT}}}{R_{21}} = 0
\]

which can be rewritten as
\[
V_{\text{OUT}} = V_{\text{REF}} \frac{R_{1} R_{21} + R_{21} \left(R_{1} + R_{7}\right)}{R_{1} R_{9} R_{21} - R_{1} R_{21} \left(R_{1} + R_{7}\right) + R_{1} R_{21} \left(R_{13} + R_{14}\right) + R_{1} R_{9} \left(R_{13} + R_{14}\right)} - V_{\text{IN}} \frac{R_{13} + R_{14}}{R_{1} R_{9} R_{21} - R_{1} R_{21} \left(R_{1} + R_{7}\right) + R_{1} R_{21} \left(R_{13} + R_{14}\right) + R_{1} R_{9} \left(R_{13} + R_{14}\right)}.
\]

The gain from the input to the output is calculated as \( V_{\text{OUT}}/V_{\text{IN}} = 1.09598 = 0.7961 \text{ dB} \).

The whole circuit in Figure 30 is converting the amplitude of the input signal to a DC voltage on the output, see Figure 33.

![Figure 33](image-url)  
**Figure 33.** The output DC levels vs. the input signal amplitude. The blue line (dots) is the output DC level from the rectifier and the red line (no dots) is the output from the whole amplitude to DC converter.

### 2.2.6 The sample-and-hold circuit

The component SMP04ES is a sample-and-hold circuit which locks the signal level output from an input signal, see Figure 34. Its functionality is as a switch which is controlled by the S/H signal. At any moment, the switch can make the output signal freeze to the actual level [9], see Figure 35.

![Figure 34](image-url)  
**Figure 34.** The sample and hold circuit SMP04ES and the components around it. The resistances on the output are pull-down resistances to keep the analog signal path intact.
2.2.7 Adjustable voltage regulator LP2951ACM

The adjustable voltage regulator LP2951ACM, see Figure 36, creates a constant voltage from $V_{IN}$. It has also a maximum output current to protect the circuit from short circuits [10].

![Figure 36](image)

The voltage level $V_{REF}$ is kept constant by the LP2951ACM to 1.235 V and, from that, the output voltage level is

$$V_{OUT} = V_{REF} \left(1 + \frac{R_{183}}{R_{184}}\right) = 1.235V \left(1 + \frac{100}{20}\right) = 7.41V.$$  

2.2.8 Circuit to detect if a pulse circuit is connected

Detection of a pulse circuit connection is performed by the circuit in Figure 37.

![Figure 37](image)

The OP wants to hold its inputs at the same voltage level. Then, $V_+$ is calculated as
\[ V_+ = \frac{R_{136}}{R_{134} + R_{136}} \cdot V_{\text{IN}} = 5.902V \approx 6V. \]

Further, \( V \) is calculated as
\[ V_- = V_+ \cdot \frac{R_{141}}{R_{139} + R_{141}} + V_{\text{OUT}} \cdot \frac{R_{139}}{R_{139} + R_{141}}. \]

So, to keep the \( V \) at the same voltage level if \( V_1 \) drops, \( V_{\text{OUT}} \) has to rise by
\[ \frac{R_{141}}{R_{139} + R_{141}} \cdot \frac{R_{139}}{R_{139} + R_{141}} = \frac{R_{141}}{R_{139}} \]

times more than \( V_1 \) falls. So, the circuit amplifies the voltage loss over \( R_{131} \) by
\[ \frac{R_{141}}{R_{139}} = 3.914 = 11.8524\text{dB}. \]

The circuits in Figure 36 and Figure 37 are connected to each other and the resulting circuit is shown in Figure 38.

![Figure 38](image_url)  
*Figure 38. The whole circuit with voltage regulator and amplifier*

### 2.2.9 Clock circuit

The main component clock circuit is the crystal XO-56BR785.4kHz and with two d-flip-flops and a multiplexer, the circuit can create 3 different clock frequencies of 785.4 kHz, 392.7 kHz and 196.35 kHz, see Table 1 and Figure 39. Depending on how the multiplexer input is chosen, the output frequency can be chosen [11]. The circuit has also four lowpass filters, see Figure 40, to remove overtones, a capacitor that acts as a DC-blocker, and a voltage keeper to keep the voltage around 8.5 V, see Figure 41.

<table>
<thead>
<tr>
<th>MUX_B</th>
<th>MUX_A</th>
<th>Output frequency (kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>196.35</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>392.7</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>785.4</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

*Table 1. Frequency multiplexer properties.*
The transfer function for the lowpass filter can be calculated as

\[ V_{OUT} = \frac{1}{j\omega C} V_{IN} R + \frac{1}{j\omega C} \Leftrightarrow H = \frac{V_{OUT}}{V_{IN}} = \frac{1}{1 + j\omega CR} \]

The magnitude and phase characteristics of the transfer function are shown in Figure 42.

![Figure 39. The whole clock circuit with output CLK0.](image)

![Figure 40. Lowpass filter to remove overtones.](image)

![Figure 41. DC-blocker and voltage keeper.](image)

The voltage level for the voltage keeper can be calculated as

\[ V_x = \frac{R_{151}}{R_{151} + R_{147}} V = 8.4956V \approx 8.5V. \]

The circuit is also a highpass filter with the following transfer function

\[ V_{OUT} = V_{IN} \frac{j\omega C_2 (R_{147} || R_{151})}{1 + j\omega C_2 (R_{147} || R_{151}) + j\omega (C_2 + C_9) R_{187} - \omega^2 C_2 C_9 R_{187} (R_{147} || R_{151})}. \]

The magnitude and phase characteristics are shown in Figure 43. Their purpose is to remove undesired frequencies from the desired clock signal.
2.2.10 Schmitt trigger on inductive sensor

The inductive sensor is connected to a Schmitt trigger circuit on the filter card, see Figure 44. The diode D\textsubscript{23} and the capacitor C\textsubscript{89} protect the input.
The current through the resistance $R_{138}$ is very small which makes the voltages $V_x$ and $V_z$ be almost the same. The voltage drop over the diode is 0.7 V and the Schmitt trigger has a hysteresis with $V_p = 3.0$ V and $V_N = 2.2$ V [12], see Figure 45.

![Figure 45. Schmitt trigger transfer function](image)

These hysteresis levels corresponding $V_{IN}$ levels will then be $V_{IN,P} = V_p - 0.7$ V = 2.3 V and $V_{IN,N} = V_N - 0.7$ V = 1.5 V.

### 2.2.11 Serial input to parallel output

The serial input to parallel output circuit is used to set the gains to achieve suitable voltage levels. It is also used to make the analog filters, MAX261, have the correct filter properties. The output ports have inverters at the outputs so if a “1” is sent to the unit, a “0” appears at the corresponding output [13]. The serial-to-parallel component is shown in Figure 46.

![Figure 46. Serial to parallel circuit which is used to set the analog filters and amplifier gain levels.](image)

The smallest voltage output from A2676ELW is $V_{OL} \leq 0.4$ V which makes

$$V_K \leq V_{OUT} - R_{160} \cdot I = 12 - 6.65V = 5.35V.$$  

### 2.2.12 Sockets

The filter card has two sockets. One is for connection with antenna card and pulse sensor and the other is for connection with the MCU, see Figure 47.
2.2.13 Current supply input filter
To avoid disturbances from the supply voltage, there is a coil with iron core and two capacitors at the input as in Figure 48. They will reduce disturbances virtually from frequencies.

![Figure 48. The input supply voltage filter](image)

2.2.14 Voltage regulator 12V and voltage regulator 5V
To create the supply voltages 12V and 5V from the input voltage of 15V, two voltage regulators are used. The first one uses 15V to create 12V, see Figure 49, where the second one uses the 12V, created from the first regulator, to create 5V, see Figure 50. The capacitors around the voltage regulator are just decoupling capacitors to reduce disturbances on the supply voltage.

![Figure 49. The voltage regulator that creates 12V from 15V](image)

![Figure 50. The voltage regulator that creates 5V from 12V](image)
2.3 Analysis of C-code for settings on the antenna card and filter card

There is a microprocessor, in the MCU, which is running a C-code responsible for setting up the gain for the antenna card as well as the gain and filter parameters of the filter card.

2.3.1 The file responsible for input and output from filter card – wgio.c

The communication from the MCU, to the filter card, is performed by three signals that are presented in Table 2.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOSI</td>
<td>Serial data line</td>
</tr>
<tr>
<td>SCLK</td>
<td>Clock</td>
</tr>
<tr>
<td>STROBE</td>
<td>Controls when the registered values in the serial-to-parallel unit appear at the output.</td>
</tr>
</tbody>
</table>

Table 2. Description of the data lines from the MCU to the filter card.

The data, that will be sent to the serial-to-parallel converters, is built by four (indexed zero to three) unsigned bytes which will be converted into a data stream of 32 bits. The serial-to-parallel unit, on the filter card, will invert the signals so an input “1” will be an output “0” on the corresponding output port, see Table 3.

<table>
<thead>
<tr>
<th>Data buffer byte</th>
<th>Bit number</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0-7</td>
<td>--</td>
<td>Not used</td>
</tr>
<tr>
<td>1</td>
<td>8-11</td>
<td>L3-L0</td>
<td>Load antenna gain</td>
</tr>
<tr>
<td>1</td>
<td>12-15</td>
<td>T3-T0</td>
<td>Tractor antenna gain</td>
</tr>
<tr>
<td>2</td>
<td>16-21</td>
<td>--</td>
<td>Not used</td>
</tr>
<tr>
<td>2</td>
<td>22-23</td>
<td>MUX_B-MUX_A</td>
<td>Signals to clock multiplexer</td>
</tr>
<tr>
<td>3</td>
<td>24</td>
<td>--</td>
<td>Not used</td>
</tr>
<tr>
<td>3</td>
<td>25</td>
<td>(\overline{WR})</td>
<td>Write signal to filters (inverted)</td>
</tr>
<tr>
<td>3</td>
<td>26-27</td>
<td>D1-D0</td>
<td>Data to filters</td>
</tr>
<tr>
<td>3</td>
<td>28-31</td>
<td>ADDR3-ADDR0</td>
<td>Address to filters</td>
</tr>
</tbody>
</table>

Table 3. Description of one data packet sent from MCU to the filter card.

The write signal, to the filters, is a bit special because it is inverted and the output from the serial-to-parallel unit is also inverted. If a “0” is written to it in the C-program, no write will be performed because the \(\overline{WR}\) signal will be one which is active low. If a “1” is written to the \(\overline{WR}\) signal, a write will be performed.

Sending data to the antenna card and filter card is performed in two steps. First, the data will appear on the lines. Then, in the next instruction, the strobe signal will be enabled and after that the next instruction, the strobe signal will be disabled. The strobe signal is a signal to the serial-to-parallel converter that the registered data should be output on the output lines. To send all the settings to the filters, this behaviour must be repeated 16 times.

To get the six input signals, one from each coil, a signal will be sent to the sample-and-hold circuits to manage them to hold the signals. Then, the processor reads the signals one by one from the input multiplexer and it releases the sample-and-hold circuits so the signal can change again. The input signals contain ten bits each and by right-shifting those twice, the two least significant bits will be removed and the antenna signals now contain eight bits each.
The file responsible for gain and parameters – wglfreq.c

The filters can be programmed with three different frequency settings. The first one is 5.2 kHz, the second one is 6.25 kHz, and the last one is a learned frequency. The filter settings for each frequency are shown in Table 4.

<table>
<thead>
<tr>
<th>Filter parameter</th>
<th>5.2 kHz frequency</th>
<th>6.25 kHz frequency</th>
<th>Learned frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Filter mode</td>
<td>2</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>Filter frequency</td>
<td>4</td>
<td>49</td>
<td></td>
</tr>
<tr>
<td>Filter Q-value</td>
<td>121</td>
<td>115</td>
<td></td>
</tr>
<tr>
<td>Clock frequency</td>
<td>2</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Antenna gain</td>
<td>0x99</td>
<td>0x77</td>
<td></td>
</tr>
</tbody>
</table>

Table 4. Parameters for the filters depending on the frequency of the wire.

The settings in Table 4 correspond to the following setting on the filters in Table 5.

<table>
<thead>
<tr>
<th>Filter settings</th>
<th>5.2 kHz frequency</th>
<th>6.25 kHz frequency</th>
<th>Learned frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Filter mode</td>
<td>2</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>Clock frequency</td>
<td>75.53</td>
<td>125.51</td>
<td></td>
</tr>
<tr>
<td>Filter Q-value</td>
<td>12.9</td>
<td>6.96</td>
<td></td>
</tr>
<tr>
<td>Clock frequency</td>
<td>392.7 kHz</td>
<td>785.4 kHz</td>
<td></td>
</tr>
<tr>
<td>Antenna gain</td>
<td>6</td>
<td>8</td>
<td></td>
</tr>
</tbody>
</table>

Table 5. The corresponding setting depending on the parameters sent to the filter card.

When the mode parameter, in the filter, is changed the SC-filter changes some switches to make the filter have different properties. The main difference between filter mode one and two is that filter mode two allows higher Q-values. A higher Q-value makes the magnitude function steeper and it adds more gain. The gain factor is $Q^2$ for mode one and $Q^2/2$ for mode two.

The center frequency of the bandpass filter is calculated as $f_C = f_{CLK}/f_0$. The $F_{CLK}$ is the clock frequency and $f_0$ is a division factor. The learning process, when the truck learns a frequency, is performed in the following way. Try to find a frequency with the tractor antenna and adjust the gain to it. Then, adjust the gain so that it fits for both antennas. If no frequency is learned, an error will occur. When the truck is set to learn a new frequency, it starts with initializing the parameters and these initial parameters are shown in Table 6.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Filter mode</td>
<td>2</td>
<td>Start with mode 2 and change to mode 1 if needed</td>
</tr>
<tr>
<td>Filter frequency number</td>
<td>0x3f</td>
<td>Start with high value and decrease it if needed</td>
</tr>
<tr>
<td>Filter Q-value</td>
<td>0x06</td>
<td>Start with Q-value 12.9 and decrease it if needed</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>1</td>
<td>Start with 785.4 kHz</td>
</tr>
<tr>
<td>Antenna gain</td>
<td>0xf0</td>
<td>Start with max gain on tractor antenna</td>
</tr>
</tbody>
</table>

Table 6. Start parameter when the truck starts to learn a new frequency to follow.

To learn the right frequency, the scan starts with changing the frequency until the filter frequency parameter is zero and the clock frequency parameter is three, which corresponds to increasing the filter center frequency until the maximum is reached. Then, decrease the clock frequency to try with a lower clock frequency. If the signal level is not high enough with filter mode two then filter mode one is tried and the same procedure for filter mode two is
performed. If no signal level high enough is found, the learning failed. Otherwise, the new filter parameters are saved and the learning succeeded. The signal ranges are shown in Table 7.

<table>
<thead>
<tr>
<th></th>
<th>Mode 1</th>
<th>Mode 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q-value</td>
<td>2.46 to 12.9</td>
<td>3.48 to 12.9</td>
</tr>
<tr>
<td>Clock frequency (kHz)</td>
<td>196.35</td>
<td>196.35</td>
</tr>
<tr>
<td>Center frequency (kHz)</td>
<td>0.984 to 1.2376</td>
<td>1.392 to 2.762</td>
</tr>
<tr>
<td>Gain on antenna card (dB)</td>
<td>-5 to 30</td>
<td>-5 to 30</td>
</tr>
</tbody>
</table>

Table 7. Range of the values that are swept in the learning mode.

Then, a check is performed to see if the signal levels, for tractor and load antenna, are between the largest and smallest accepted values. If the check is successful, the learned parameters are ready for use. If the signal level is too large, a lower gain is tried and the signal level is checked again. Otherwise, the signal level is too small the learning failed. If a frequency is learned, send the new gain to the truck. If the learning process succeeds, the parameters are saved in the EEPROM. If no learning has been performed, the values in the EEPROM are just random values and the program checks whether the parameters in the EEPROM are correct. Otherwise, an error will occur.

The filter data array consists of ten unsigned bytes each responsible for a setting in the antenna card and filter card. Each filter data byte consists of the following parts. The first bit is unused the second bit is the strobe signal which should be set to “0”. The bits 3 and 4 are the data bits that are described in Table 8, while the bits 5-8 are the address bits. They are also described in Table 8. The component MAX261 contains dual second order filters, part A and part B, which differ by the first address bit. In reality, the difference is 8, so by adding 8 to the filter A, the address to filter B is achieved. The addresses are shown in Table 8.

<table>
<thead>
<tr>
<th>Filter data byte</th>
<th>Filter data</th>
<th>Filter A address</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>M0-M1</td>
<td>0000</td>
<td>Filter mode signals</td>
</tr>
<tr>
<td>1</td>
<td>F0-F1</td>
<td>0001</td>
<td>Filter frequency settings bit 0 and 1</td>
</tr>
<tr>
<td>2</td>
<td>F2-F3</td>
<td>0010</td>
<td>Filter frequency settings bit 2 and 3</td>
</tr>
<tr>
<td>3</td>
<td>F4-F5</td>
<td>0011</td>
<td>Filter frequency settings bit 4 and 5</td>
</tr>
<tr>
<td>4</td>
<td>Q0-Q1</td>
<td>0100</td>
<td>Filter Q-value settings bit 0 and 1</td>
</tr>
<tr>
<td>5</td>
<td>Q2-Q3</td>
<td>0101</td>
<td>Filter Q-value settings bit 2 and 3</td>
</tr>
<tr>
<td>6</td>
<td>Q4-Q5</td>
<td>0110</td>
<td>Filter Q-value settings bit 4 and 5</td>
</tr>
<tr>
<td>7</td>
<td>Q6</td>
<td>0111</td>
<td>Filter Q-value settings bit 6, bit 7 unused</td>
</tr>
<tr>
<td>8</td>
<td>--</td>
<td>--</td>
<td>Antenna gain</td>
</tr>
<tr>
<td>9</td>
<td>--</td>
<td>--</td>
<td>Clock settings</td>
</tr>
</tbody>
</table>

Table 8. Description of what the filter data byte contains.

2.3.3 Flowcharts for the file wgio.c

The file that communicates with the antenna card and filter card is also analyzed in flowcharts. All functions, in the file, have their own flowchart. The Send data function is responsible to send parameters to antenna gain and the data to the filters. The send gains function is just responsible for sending the gain parameters to the antenna card. The readAnalogCoils function is responsible to set the sample-and-hold signal so the antenna signal locks, then read them and release them when it has been read.
2.3.4 Flowcharts for the file wglfreq.c

The file responsible for learning and setting the parameters which are sent to the filter card, also contains functions for learning of a new frequency to follow. The prog_filters function sets the parameters for the filters depending on what frequency it should look for. The iniLearnFrequency function is responsible for setting the parameters so the truck is ready to learn a new frequency. The learnFrequency function is a kind of state machine and to learn a new frequency, the program has to go through all states. Otherwise, it will fall into the fail state.

The function responsible to find a frequency which is not prepared for the truck must scan all frequencies, change gain, and check other parameters, see Figure 51.

![Flowchart](image)

**Figure 51.** Easier flowchart for the function that searches for a suitable frequency for wire guidance.

When the truck has found a new frequency, the signal levels have to be checked so that they are suitable for wire guidance. If it is suitable, the learned frequency can be used for wire guidance. Otherwise, the learning has failed.

2.4 Analysis of component - MAX261

The filter component MAX261 has a partly digital interface. All its input signals are digital besides the antenna signal that is analog and the output signal, which also is analog but time discrete. This Section will describe the function of the MAX261 and how it is used for filtering on the filter card.

2.4.1 Overview of MAX261

The component MAX261 contains a dual second order universal SC active filter and it can handle center frequencies up to 57 kHz for a bandpass filter [8]. An overview structure of MAX261 is shown in Figure 52.
The filter component contains two filters which can be identical or totally different depending on the settings. The structure of each filter is shown in Figure 53.

### 2.4.2 Pin connections

The component has 24 pins and description of each pin is shown in Table 11.

<table>
<thead>
<tr>
<th>Pin number</th>
<th>Pin</th>
<th>Description</th>
<th>Additional information</th>
</tr>
</thead>
<tbody>
<tr>
<td>9</td>
<td>V+</td>
<td>Positive supply voltage</td>
<td>V+ is connected to +12 V, GND to +6V and V. to 0V.</td>
</tr>
<tr>
<td>16</td>
<td>V-</td>
<td>Negative supply voltage</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>GND</td>
<td>Analog ground</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>CLKA</td>
<td>Input clock for section A</td>
<td>CLKA and CLKB is connected to the clock circuit</td>
</tr>
<tr>
<td>12</td>
<td>CLKB</td>
<td>Input clock for section B</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>CLK out</td>
<td>For crystal</td>
<td>Not connected</td>
</tr>
<tr>
<td>18</td>
<td>OSC out</td>
<td>For crystal</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>INA</td>
<td>Input to section A</td>
<td>Antenna signal goes in here</td>
</tr>
<tr>
<td>1</td>
<td>BPA</td>
<td>BP output from section A</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>INB</td>
<td>Input to section B</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>BPB</td>
<td>BP output from section B</td>
<td>Band pass filtered signal</td>
</tr>
<tr>
<td>24, 22</td>
<td>LPB</td>
<td>BP output</td>
<td>Not connected</td>
</tr>
<tr>
<td>3, 20</td>
<td>HPA, HPB</td>
<td>HP output</td>
<td>Not connected</td>
</tr>
<tr>
<td>15</td>
<td>WR</td>
<td>Write enable input</td>
<td>Active low</td>
</tr>
<tr>
<td>14, 13</td>
<td>A0, A1</td>
<td>Address inputs for ( f_0 ) and Q</td>
<td>Data from serial-to-parallel unit (from MCU)</td>
</tr>
<tr>
<td>10, 7</td>
<td>A2, A3</td>
<td>input data locations</td>
<td></td>
</tr>
<tr>
<td>19, 6</td>
<td>D0, D1</td>
<td>Data inputs for ( f_0 ) and Q</td>
<td>Data from serial-to-parallel unit (from MCU)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>programming</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>OP out</td>
<td>Output from the embedded OP</td>
<td>Low pass filtered signal</td>
</tr>
<tr>
<td>4</td>
<td>OP in</td>
<td>Inverting input to the embedded OP</td>
<td>Connected to BPB</td>
</tr>
</tbody>
</table>

**Table 9.** Pin description for the MAX261 component.
2.4.3 Usage of different types of MAX261

There are a lot of different types of MAX261 components and not all are suitable for the application on the filter card. The TMHE has the following priority:

- First choice: MAX261AENG -40°C to +85°C Plastic DIP 1%.
- Second choice: MAX261BENG -40°C to +85°C Plastic DIP 2%.
- Third choice if cold temperatures not needed: MAX261ACNG 0°C to +70°C Plastic DIP 1%.

2.4.4 Transfer function for the band pass filter

The transfer function for each of the two parts in the MAX261 component is

\[ G(s) = H_{OBP} \frac{s(\omega_0/Q)}{s^2 + s(\omega_0/Q) + \omega_0^2}. \]

Here, \( H_{OBP} \) is \(-Q/\sqrt{2}\) for filter mode 2 [8]. The other parameters are shown in Table 10. The factor \( H_{OBP} \) is just a gain factor and it does not affect the characteristics of the bandpass filter. So, the factor \( H_{OBP} \) can be put aside to get a magnitude maximum of 0 dB when the transfer function for the bandpass filter is calculated.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>5.2 kHz center frequency</th>
<th>6.25 kHz center frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q-value</td>
<td>12.9</td>
<td>6.96</td>
</tr>
<tr>
<td>( \omega_0 )</td>
<td>2\cdot\pi\cdot5200</td>
<td>2\cdot\pi\cdot6250</td>
</tr>
<tr>
<td>( H_{OBP} ) (dB)</td>
<td>38.4030</td>
<td>27.6838</td>
</tr>
</tbody>
</table>

Table 10. Parameters for the two standard frequencies.

The magnitude and phase characteristics for the 5.2 kHz center frequency are presented in Figure 54 and for the 6.25 kHz center frequency in Figure 55. The gain factor \( H_{OBP} \) is ignored in the magnitude characteristics.

![Figure 54](image-url)
2.4.5 Analysis of tolerances

The MAX261 component has some variations so there is a possibility of error. The maximum errors are presented in Table 11.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MAX261A</th>
<th>MAX261B</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_0$ center frequency error (%)</td>
<td>±1</td>
<td>±2</td>
</tr>
<tr>
<td>Q-value error (%)</td>
<td>±6</td>
<td>±10</td>
</tr>
</tbody>
</table>

Table 11. Maximum errors in percents for MAX261A and MAX261B series.

In the worst case, the center frequency can have 2% error and the Q-value can have 10% error. The worst cases are shown as red lines and green lines, for the respectively component, in Figure 56. The Q-value is important for the analog filter and it is defined by $Q = -|s_p|/(2 \cdot \text{Re}\{s_p\})$, where $s_p$ is the pole placement.

The gain factor $H_{OBP} = Q^2/2$ makes the gain difference significant and it is shown in Figure 57.
for the two different center frequencies. The four lines represent the worst cases as in Table 12.

<table>
<thead>
<tr>
<th>Line</th>
<th>Center frequency error</th>
<th>Q-value error</th>
</tr>
</thead>
<tbody>
<tr>
<td>Solid line</td>
<td>0%</td>
<td>0%</td>
</tr>
<tr>
<td>Left dashed and dotted line</td>
<td>-1%</td>
<td>-6%</td>
</tr>
<tr>
<td>Right dashed and dotted line</td>
<td>+1%</td>
<td>+6%</td>
</tr>
<tr>
<td>Left dashed line</td>
<td>-2%</td>
<td>-10%</td>
</tr>
<tr>
<td>Right dashed line</td>
<td>+2%</td>
<td>+10%</td>
</tr>
</tbody>
</table>

Table 12. Errors for the different lines in Figure 57.

![Graph of transfer function](image)

**Figure 57.** Transfer function for the band pass filter with center frequency 5.2 kHz and 6.25 kHz respectively. The blue (solid) line is the ideal impulse response.

### 2.5 Simulations

Most of the theoretically analyzed circuits, are also simulated with Cadence Orcad. The problems with the theoretical analysis are that the frequency limit of the OPs has not been taken care of. Therefore, for large frequencies the attenuation will be a bit larger than what is shown in all theoretical calculations. The ferrite, on the output of the antenna card is not included in the simulations.

#### 2.5.1 Simulations of the antenna card

The theoretically calculated transfer function, in Figure 21, and the simulated transfer function, in Figure 58, are almost the same up to 1 MHz. Then, the simulated magnitude falls a lot more than the calculated which is a result of the fact that the OPs have a limited bandwidth.
2.5.2 Simulations of the filter card

The calculated transfer function for the lowpass filter on the input of the filter card, in Figure 28, and the simulated version, in Figure 60, are almost the same. The stagnation between 1 MHz and 10 MHz is a result of the limited bandwidth of the OP.
The rectifier circuit converts the input amplitude into a DC level output and the calculations are close to the simulation results. The main difference is that the output signal has a sharp turnover when it stagnates at 5.6 V but the simulated version has a smooth turn.

**Figure 61.** Simulated output DC voltage according to the input amplitude. The squares represent the rectified DC level.
3 Design of digital filters

This chapter investigates the possibilities to replace the analog filter with a digital filter. The analog filter has an adjustable center frequency so that the wire guidance system can tune in on the right frequency. For that reason, the digital filter also needs to have an adjustable center frequency.

3.1 Specification of requirements

This section starts with an analysis of the system performance. According to that, a specification of requirements is built up.

3.1.1 Sampling frequency

The existing filter can handle center frequencies from 0.9843 kHz up to 11.048 kHz as

\[ f_{0,\text{MAX}} = \frac{f_{\text{CLK,MAX}}}{f_{d,\text{MIN}}} = \frac{785.4\text{[kHz]}}{71.09} = 11.048\text{[kHz]} \]

\[ f_{0,\text{MIN}} = \frac{f_{\text{CLK,MIN}}}{f_{d,\text{MAX}}} = \frac{196.35\text{[kHz]}}{199.49} = 0.9843\text{[kHz]} \]

According to Nyquist sampling theorem, the sample frequency must be at least twice as large as the signal frequency to avoid aliasing. This means

\[ f_{\text{sample}} > 2 \cdot f_b \]

where \( f_{\text{sample}} \) is the sampling frequency and \( f_b \) is the signal bandwidth [15]. So, the sample frequency has to be at least twice as large as the maximum center frequency which gives

\[ f_{\text{sample}} > 2 \cdot 11.048\text{[kHz]} = 22.096\text{[kHz]} \]

If the sample frequency is larger, then the anti-aliasing filter will be much simpler. So, a good choice is 40 kHz sampling frequency.

3.1.2 Requirements on the anti-aliasing filter

Aliasing is avoided if the signal is lowpass filtered before the ADC. Then, the larger frequencies are removed and not aliased over the desired frequencies. In this thesis, the signal bandwidth \( f_b \) is 11 kHz and the sampling frequency is 40 kHz. Then, the filter cut-off frequency will be 11 kHz and the stopband frequency is 29 kHz. Then, some aliasing will occur but the aliasing is just on frequencies from 11 kHz up to 20 kHz which is filtered away by the digital filter. The attenuation requirement, on the filter, is that the signals in the stopband should be attenuated at least 40 dB which corresponds to that disturbances will be attenuated 100 times and the signal energy of the disturbances will be reduced 10000 times.

3.1.3 Filter specification for the analog filter

On the datasheet of MAX261, the transfer function for the filter is given as a formula. The transfer function is implemented in MATLAB and the attenuation values are presented in Table 13 and Table 14. These attenuation values are for the whole filter component. In other words, two cascaded second order filters.
The 5.2 kHz filter has the following attenuation characteristics

<table>
<thead>
<tr>
<th>Attenuation (dB)</th>
<th>Lower frequency (kHz)</th>
<th>Higher frequency (kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.01</td>
<td>5.19316</td>
<td>5.20685</td>
</tr>
<tr>
<td>0.05</td>
<td>5.18471</td>
<td>5.21534</td>
</tr>
<tr>
<td>0.1</td>
<td>5.17836</td>
<td>5.22173</td>
</tr>
<tr>
<td>0.5</td>
<td>5.15117</td>
<td>5.24929</td>
</tr>
<tr>
<td>1</td>
<td>5.13007</td>
<td>5.27088</td>
</tr>
<tr>
<td>3</td>
<td>5.07216</td>
<td>5.33107</td>
</tr>
<tr>
<td>10</td>
<td>4.91207</td>
<td>5.50481</td>
</tr>
<tr>
<td>20</td>
<td>4.63038</td>
<td>5.83969</td>
</tr>
<tr>
<td>30</td>
<td>4.20293</td>
<td>6.43360</td>
</tr>
<tr>
<td>40</td>
<td>3.56790</td>
<td>7.57870</td>
</tr>
<tr>
<td>50</td>
<td>2.73386</td>
<td>9.89078</td>
</tr>
<tr>
<td>60</td>
<td>1.85286</td>
<td>14.59370</td>
</tr>
<tr>
<td>70</td>
<td>1.13611</td>
<td>23.80050</td>
</tr>
<tr>
<td>80</td>
<td>0.66003</td>
<td>40.96810</td>
</tr>
</tbody>
</table>

Table 13. Attenuation data for 5.2 kHz center frequency

The 6.25 kHz filter has the following attenuation characteristics

<table>
<thead>
<tr>
<th>Attenuation (dB)</th>
<th>Lower frequency (kHz)</th>
<th>Higher frequency (kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.01</td>
<td>6.23478</td>
<td>6.26526</td>
</tr>
<tr>
<td>0.05</td>
<td>6.21598</td>
<td>6.28421</td>
</tr>
<tr>
<td>0.1</td>
<td>6.20187</td>
<td>6.29850</td>
</tr>
<tr>
<td>0.5</td>
<td>6.14166</td>
<td>6.36025</td>
</tr>
<tr>
<td>1</td>
<td>6.09513</td>
<td>6.40881</td>
</tr>
<tr>
<td>3</td>
<td>5.96826</td>
<td>6.54503</td>
</tr>
<tr>
<td>10</td>
<td>5.62454</td>
<td>6.94501</td>
</tr>
<tr>
<td>20</td>
<td>5.04652</td>
<td>7.74048</td>
</tr>
<tr>
<td>30</td>
<td>4.24113</td>
<td>9.21040</td>
</tr>
<tr>
<td>40</td>
<td>3.21504</td>
<td>12.14990</td>
</tr>
<tr>
<td>50</td>
<td>2.15798</td>
<td>18.10150</td>
</tr>
<tr>
<td>60</td>
<td>1.31532</td>
<td>29.69800</td>
</tr>
<tr>
<td>70</td>
<td>0.76217</td>
<td>51.25180</td>
</tr>
<tr>
<td>80</td>
<td>0.43293</td>
<td>90.22730</td>
</tr>
</tbody>
</table>

Table 14. Attenuation data for 6.25 kHz center frequency

3.1.4 Analysis of requirements

The digital filter needs to have at least as large passband as the original analog filter which is here defined as where the filter has up to 0.1 dB attenuation. The stopband requirements are also that the digital filter needs to have an attenuation that is a combination of the two different attenuations in Table 13 and Table 14. A maximum of 0.1 dB ripple in the passband will make the signal amplitude be at least 98.8 % of the original amplitude and the signal energy will be at least 97.7 % of the original energy. The digital filter must handle the same frequency range as the analog filter which means that center frequencies from 0.98 kHz to 11.1 kHz must be supported.
Another requirement, that should be fulfilled, is that the control loop has the cycle time of 20 ms which is the absolutely maximum value of delay through the filter. The digital filter must also be able to handle the same temperature range as the analog filter which operates between -40ºC and +85ºC. The number of bits in the ADC and DAC must be at least 10 because the ADC, in the MCU, is using 10 bits. Using 12 bits, instead, will add some margins which are necessary. The internal number of bits must be at least 14 but adding some extra bits will increase the margins.

3.2 Specification of requirements summary

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( A_{\text{max}} )</td>
<td>Maximum pass band ripple</td>
<td>0.1 dB</td>
</tr>
<tr>
<td>( A_{\text{min}} )</td>
<td>Minimum stop band attenuation</td>
<td>40 dB, 60 dB, 80 dB</td>
</tr>
<tr>
<td>( f_{s1} )</td>
<td>Lower stop band frequency (minimum)</td>
<td>( f_0 - 3 \cdot f_0/f_1 ), ( f_0 - 4 \cdot f_0/f_1 ), ( f_0 - 5 \cdot f_0/f_1 ) [kHz]</td>
</tr>
<tr>
<td>( f_{c1} )</td>
<td>Lower pass band frequency (maximum)</td>
<td>( f_0 - 0.03 \kHz )</td>
</tr>
<tr>
<td>( f_{c2} )</td>
<td>Higher pass band frequency (minimum)</td>
<td>( f_0 + 0.03 \kHz )</td>
</tr>
<tr>
<td>( f_{s2} )</td>
<td>Higher stop band frequency (maximum)</td>
<td>( f_0 + 4 \cdot f_0/f_1 ), ( f_0 + 10 \cdot f_0/f_1 ), ( f_0 + 20 \cdot f_0/f_1 ) [kHz]</td>
</tr>
<tr>
<td>( T_{\text{delay,max}} )</td>
<td>Maximum time delay through the filter</td>
<td>20 ms, 10 ms recommended</td>
</tr>
<tr>
<td>( f_{0,\text{min}} )</td>
<td>Center frequency lower edge</td>
<td>( 0.98 \cdot f_{c1} + f_0 ) kHz = 1.01 kHz</td>
</tr>
<tr>
<td>( f_{0,\text{max}} )</td>
<td>Center frequency higher edge</td>
<td>( 1.1 \cdot f_{c2} + f_0 ) kHz = 11.07 kHz</td>
</tr>
<tr>
<td>( T_{\text{min}} )</td>
<td>Minimum operating temperature</td>
<td>-40ºC</td>
</tr>
<tr>
<td>( T_{\text{Max}} )</td>
<td>Maximum operating temperature</td>
<td>+85ºC</td>
</tr>
<tr>
<td>Bits(_{\text{AD}})</td>
<td>Number of needed bits in the ADC</td>
<td>10 at least, 12 recommended</td>
</tr>
<tr>
<td>Bits(_{\text{DA}})</td>
<td>Number of needed bits in the DAC</td>
<td>10 at least, 12 recommended</td>
</tr>
<tr>
<td>Bits(_{\text{INT}})</td>
<td>Number of needed bits in the filter</td>
<td>14 at least, 16 recommended</td>
</tr>
</tbody>
</table>

*Table 15. Requirements on the digital system.*

The \( f_0 \) is the center frequency and \( f_1 \) is the 5.2 kHz. The filter also needs to be stable and realisable. The requirements on the stop band are not trivial because the analog filter changes logarithmic in the frequency domain.

3.3 Cauer filters

The filters that will are most suitable are Cauer filters because it has the lowest filter order and a rather low group delay. Cauer filters are also known as elliptic filters or Zolotarev filters [16].

3.4 Different filter types

There exist different filter types such as Finite Impulse Response (FIR) and Infinite Impulse Response (IIR). Some are more reliable for implementation than others. Each of them has advantages and disadvantages so it is not easy to just choose the best for an implementation. The main factors that are considered here is filter order and stability.

3.4.1 FIR filters

The term FIR stands for finite impulse response which means that a finite input will create a finite output. They are always stable because they have no feedback and the only scaling, needed, is at the output [17]. The negative properties with FIR filters are that to achieve a
steep filter, they require a long impulse response. In comparison with other filters, the filter order becomes high. So, the FIR filters become a bit expensive in terms of hardware.

### 3.4.2 IIR filters

The term IIR stands for infinite impulse response which means that a limited input creates an infinite output. They have an advantage in that they have low filter orders and need not so many components. The negative properties are stability. Even though the poles are inside the unit circle, they can be unstable because of feedback. They also need scaling and control of the saturation to make them stable.

### 3.4.3 WDF filters

The term WDF stands for wave digital filter which means that they in principle are simulating propagation waves. The advantages are stability properties and low sensitivity with respect to variations in element values according to ordinary IIR filters. The poles and zeros are laying on top of each other and are moved together [18]. The disadvantages are that the design is a bit complicated and the signal flow is not so easy to understand. These filters are of IIR type which means that they can have stability problems.

### 3.5 Implementation of digital filter

This section investigates the tradeoffs to implement different types of digital filters and which of these filter types that is most suitable to be realized.

#### 3.5.1 Low pass to band pass structure

The implementation of the lowpass to bandpass structure is performed by replacing $z^{-1}$ in the transfer function by $z^{-1}(z^{-1} - \beta)/(\beta z^{-1} - 1)$. This realisation will not create delay free loops in the design. This will create a bandpass filter from a lowpass filter and $\beta$ can be adjusted from -1 to 1 to create different center frequencies. A special case is when $\beta$ is zero. Then, the band pass filter center frequency will appear at a quarter of the sampling frequency because $z^{-1}$ will be replaced by $-z^{-2}$ [19].

The design of a suitable lowpass filter with a small passband would normally be done by frequency masking. But in this case, it is not suitable to use frequency masking because it will replace each delay element with a number of delay elements. Frequency masking also requires an extra filter to remove undesired images that also are masked in between zero and $\pi$.

#### 3.5.2 Requirements when the lowpass to bandpass structure not is used

To get filters of the same order, the specification differs from when the lowpass to bandpass structure not is used. The same filter order is required because the filters need to have the same number of coefficients to make them sweepable over the different center frequencies.

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_{\text{MAX}}$ (Maximum ripple in pass band)</td>
<td>0.1 dB</td>
</tr>
<tr>
<td>$A_{\text{MIN}}$ (Minimum attenuation in stop band)</td>
<td>60 dB</td>
</tr>
<tr>
<td>$F_{C1}$ (Lower pass band edge)</td>
<td>$f_0(1-5.2\ \text{kHz} \cdot 0.03/f_0)$</td>
</tr>
<tr>
<td>$F_{C2}$ (Higher pass band edge)</td>
<td>$f_0(1+5.2\ \text{kHz} \cdot 0.03/f_0)$</td>
</tr>
<tr>
<td>$F_{S1}$ (Lower stop band edge)</td>
<td>$f_0(1-5.2\ \text{kHz} \cdot 0.6/f_0)$</td>
</tr>
<tr>
<td>$F_{S2}$ (Higher stop band edge)</td>
<td>$f_0(1+5.2\ \text{kHz} \cdot 1.2/f_0)$</td>
</tr>
</tbody>
</table>

*Table 16. The general requirements for all center frequencies*
The $f_0$ is the center frequency for the desired bandpass filter. The filter must also be realisable and stable.

### 3.5.3 FIR filter implementation

FIR filters have advantages in stability but have instead large filter order which makes them expensive to implement. The FIR filter can be implemented in two different ways. The first one is just to make a suitable bandpass filter and then adjust the coefficients for different center frequencies.

#### 3.5.3.1 FIR with sweepable coefficients

By MATLAB calculations, the filter order is calculated to 61 which make the filter have 31 distinct multiplications with different coefficient values and this solution also needs about 67 different filters to cover all frequencies between 1 kHz and 11 kHz which make the total number of coefficients to $31 \cdot 67 = 2077$. The coefficients for different center frequencies are shown in Figure 62.

![Figure 62. Filter coefficients for FIR-filter with center frequencies from 3.1 kHz up to 10 kHz.](image)

#### 3.5.3.2 FIR with lowpass to bandpass structure

The second type of solution is to make a lowpass FIR filter which is stable and then use the lowpass to bandpass solution. This solution will transfer the FIR filter into an IIR filter and it will reduce the stability properties for the filter and the order of the filter will be unnecessarily high. The number of coefficients will however be reduced.

### 3.5.4 IIR filter implementation

The IIR filters in direct form can also be implemented in two ways. The first one is to implement a large number of bandpass filters and the second one is to implement a lowpass filter and use the lowpass to bandpass structure.

The IIR filter will be realized by the direct form $I^1$ structure which makes the number of delay elements and multipliers minimal [20], see Figure 63.
3.5.4.1 IIR filter with sweepable coefficients
To implement a suitable bandpass filter, the filter order is calculated by MATLAB to six, which is not so high and the number of coefficients will be 13, Figure 64.

![Figure 64. IIR-filter parameters for frequencies from 1 kHz up to 11 kHz.](image)

3.5.4.2 IIR filter with lowpass to bandpass structure
The second choice is to implement a lowpass filter and then use the lowpass to bandpass structure. This is not a good choice because the IIR filters have stability problems even before the lowpass to bandpass structure is used.

3.5.5 WDF implementation
The WDF is also a type of IIR filter but with better stability which makes it interesting. This filter can also be implemented with and without the lowpass to bandpass structure. The WDF design consists of a number of symmetric two-port adaptors of all pass form, see Figure 65.

![Figure 65. The symmetric two-port adaptor structure.](image)
3.5.5.1 WDF with sweep able coefficients
Implementation of WDF with small passband is hard because the poles will be placed near the unit circle. The filter order will be around six which makes the filter to have six coefficients for each filter and the scaling coefficient. This will result in a lot of coefficients because there will be around, the bandwidth divided by the passband size, which will result in around 67 different filters to implement. So, the total number of coefficients will be around \(67 \times 7 = 469\) which is quite high. The filter coefficients have some similarities, see Figure 66.

![WDF coefficients](image)

Figure 66. WDF coefficient values for center frequencies from 1 kHz up to 11 kHz.

3.5.5.1 WDF with lowpass to bandpass structure
The second opportunity for WDF is to implement a lowpass filter and use the lowpass to bandpass structure. The problem here is to implement a WDF of lowpass type because when the filter order is higher than one, some of the coefficients will be close to one. A filter coefficient near one is not good because the scaling is performed by division by the gain factor \(1/(1-\alpha)\), where \(\alpha\) is the coefficient. When \(\alpha\) is close to one, for example 0.98, the gain factor will be 50 and division by this large value will make the filter not use the bits that are available for the filter. A solution to this problem is to use first order sections and cascade them. This will make all the first order sections to have the same coefficient which is an advantage. Another advantage is that the \(\alpha\) coefficient can be adjusted to make the filter have different steepness properties. One detail that still has to be remembered is that the WDF is of IIR type and so is the lowpass to bandpass structure. Therefore, the stability issue is very important for implementation of this filter.

3.6 Most suitable filter for implementation
The filters that are chosen for implementation are the WDF of lowpass filter type and, then, the lowpass to bandpass structure is used to create the desired bandpass filter. The solution is chosen because the filter properties will be very likely to the analog filter, because the center frequency and steepness of the filter can be adjusted. The advantage for the digital filter according to the analog filter is that the adjustability is just limited by the number of bits in the filter and not by fixed values.
3.6.1 Lowpass to bandpass realisation

The implementation of the lowpass to bandpass filter is to replace $z^{-1}$ in the transfer function by $z^{-1} - \beta / \beta z^{-1} - 1$. The realisation of this function can be performed by using the inverse $z$ transform on the function as

$$H(z) = \frac{Y(z)}{X(z)} = z^{-1} \frac{z^{-1} - \beta}{\beta z^{-1} - 1} \iff Y(z)(\beta z^{-1} - 1) = X(z)z^{-1}(z^{-1} - \beta).$$

By using the inverse $z$ transform, this becomes $\beta y(n-1) - y(n) = x(n-2) - \beta x(n-1)$ which can be rewritten as $y(n) = \beta y(n-1) - x(n-2) + \beta x(n-1)$. The implementation of this is shown in Figure 67.

![Figure 67. Realisation of the low pass to band pass structure.](image)

3.6.2 First order WDF of lowpass type

The constructed filter is a lowpass WDF of first order, whose benefits are that the coefficient value will not be near one to avoid instability and also that the filter structure is quite simple. The first order filter does not have the steepest filter properties but when a number of them are cascaded, the attenuation becomes very good. The structure of the lowpass filter is shown in Figure 68.

![Figure 68. First order WDF of low pass type.](image)

The coefficient value of the first order lowpass filter, $\alpha$, can be adjusted to change the passband and steepness of the filter, see Figure 69.

![Figure 69. The magnitude characteristics of the first order low pass WDF. The lines represent nine coefficient values from 0.9 down to 0.1 with a step of 0.1.](image)
3.6.3 Second order WDF of bandpass type

The first order lowpass WDF is used to create a bandpass filter where the delay elements are replaced by the lowpass to bandpass structure.

\[ H(z) = \frac{-\alpha + z^{-1}}{1 - \alpha z^{-1}}. \]

By replacing \( z^{-1} \) with \( z^{-1} - \beta)/(\beta z^{-1} - 1) \), the transfer function is

\[ H(z) = \frac{-\alpha - \beta z^{-1} + z^{-2}}{-1 + \beta(1 + \alpha)z^{-1} - \alpha z^{-2}}. \]

The total transfer function for the filter is \( H_{\text{tot}}(z) = (H(z) + 1)/2 \) where

\[ H_{\text{tot}}(z) = \frac{1}{2} \cdot \frac{-1 - \alpha + \alpha \beta z^{-1} + (1 - \alpha)z^{-2}}{-1 + (1 + \alpha)\beta z^{-1} - \alpha z^{-2}}. \]

Inverse z-transformation gives that

\[ y(n) = -(1 + \alpha)\beta y(n - 1) + \alpha y(n - 2) + 0.5(1 + \alpha)x(n) - 0.5\alpha\beta y(n - 1) - 0.5(1 - \alpha)x(n - 2). \]

The magnitude function of the filter is shown in Figure 71.

![Figure 70](image.png)  
Figure 70. The second order band pass WDF design. The symmetric two-port adaptor is shown in Figure 65 and BP-section design is shown in Figure 67.

The magnitude function is not steep enough and to achieve a steeper filter a number of these filters can be cascaded. Then the transfer functions are multiplied together and the magnitude for each of the filters will be added and create a steeper filter.

![Figure 71](image.png)  
Figure 71. Magnitude function for the second order band pass structure with \( \alpha = 0.5 \) and \( \beta \) have the following values 0.99, 0.66, 0, -0.66 and -0.99.
3.6.4 The resulting WDF of bandpass type

After the initial investigation, a suitable number of cascaded second order bandpass WDF structures are 10, because 10 cascaded filters matches the requirements best. The good properties with this realisation is that the realisation only needs three different coefficients, $\alpha$ that is the coefficient value of the two-port adaptor, $\beta$ that is the coefficient of the BP-section and one scaling coefficient. Another property with this structure is that the steepness of the filter can be adjusted by the $\alpha$ value, the center frequency can be adjusted by the $\beta$ value which is very similar to the analog bandpass filter which has adjustable Q-value and center frequency. The realisation of this filter is to cascade ten filters, all with the same $\alpha$ and $\beta$ coefficients.

The bad property with this type of structure is that the number of needed bits inside the filter needs to be a bit higher than a filter of higher order would be used. The advantage is that the coefficients are not so close to one which makes the stability properties better. The magnitude function for three different $\alpha$ coefficients is shown in Figure 72. Observe that the steepness is much higher when the $\alpha$ coefficient is higher.

![Transfer function for different alpha values](image)

**Figure 72.** The magnitude function for the cascaded filters with $\alpha = 0.1, 0.5$ and, $0.9$ and $\beta = 0.99, 0.66, 0, -0.66$, and $-0.99$.

3.7 Stability issues for the chosen filter

The chosen filter is a WDF which is of IIR type and it can be unstable. Therefore, scaling and suppression of parasitic oscillations in the filter are needed. This is performed by addition of some extra blocks in the design, see Figure 73 [21].
3.7.1 Scaling of the filter
Scaling is performed on the input of the filter and the signal is scaled back at the output. The scaling is performed to ensure that the absolute value of the signal, inside the filter, is not larger than one. Scaling will be performed by a multiplication with $\frac{1}{2}$ at the input. Then the signal is scaled back by multiplication with 2 at the output.

3.8 Coefficient values to match the requirements
The coefficients must make the filter match the requirements on the digital filter, the range of coefficient values that matches is large. This makes the digital filter a bit flexible and the coefficients can be changed a bit to change the properties of the digital filter. The $\alpha$ value is the steepness of the filter and a higher $\alpha$ value makes the filter steeper where a lower $\alpha$ makes it less steep. The $\beta$ value decides what center frequency the filter should have and a lower $\beta$ value means higher center frequency and vice versa.

3.8.1 Coefficient range
The coefficients have a large range the properties depends on the following:
- Lowest $\alpha$ value depends on the stopband requirements.
- Highest $\alpha$ value depends on the passband requirements.
- Lowest $\beta$ value depends on the highest center frequency.
- Highest $\beta$ value depends on the lowest center frequency.

For 40 kHz sampling frequency, the value range is

$$0.4 \leq \alpha \leq 0.8$$
$$-0.16 \leq \beta \leq 0.988$$

3.8.2 Suitable coefficient values
Suitable values on coefficient are where it matches the requirements which can be near the middle of the range in Section 3.8.1. For 40 kHz, the suitable values are

$$\alpha = 0.6$$
$$-0.15 \leq \beta \leq 0.987$$

Figure 73. Quantization and suppression of parasitic oscillations in the second order band pass filter.
3.9 Number of bits in the digital filter

The number of needed bits is investigated by comparing the ideal impulse response of the filter with the filter where a limited number of bits are used. The number of needed bits, internally, in the filter is hard to analyze, because when a limited number of bits are used the signal will have some errors. The question is how large this error is. In this case, the ideal signals are compared with the signals with limited number of bits. When the differences are smaller than 1/1000 then the number of bits is enough. By the analysis, the minimum number of bits is calculated to 14. It is recommended to use some more bits, 16, to make the error smaller.
4 Implementations

This chapter investigates how the implementation should be and what parts that are most suitable for the implantation.

4.1 Analysis of implementation

The implementation can be done in many ways and with different components. The DSP and FPGA have different advantages and properties that need to be taken care of.

4.1.1 Investigation of alternatives

There are some alternatives in which the digital filter can be implemented and they all have advantages and disadvantages. The two alternatives for this implementation are DSPs and FPGAs which will be investigated. The digital filter and its surroundings, that are going to be implemented here, do not require so much performance because it is simple filter. The sampling frequency is low so the most interesting properties here are the price and flexibility.

The advantage with FPGA is that the six channels of data can be processed at the same time. The DSP needs to be so fast that the six channels can be processed in series. If a DSP processor is used, the calculation power of DSP must be enough for the actual application. The needed speed of the DSP can be calculated as

\[
\text{Sample frequency} \cdot \text{number of channels} \cdot \text{number of calculations per sample} = 40000 \cdot 6 \cdot \text{calculations per sample (Hz)} = 0.24 \cdot \text{calculations per sample (MHz)}.
\]

This calculation is only valid if the processor can not do anything in parallel and if the processor only can do one calculation per clock cycle.

4.1.2 Price comparison

The price comparison is based on the prices on the web shop [http://se.farnell.com/](http://se.farnell.com/). The large requirement on the devices is that they must be able to handle temperatures between -40 °C and +85°C.

There are some alternatives in DSP section. The first alternative is fixed point or floating point processor but the floating point processor costs almost 4-6 times more than a fixed point processor. The next alternative is a DSP processor with embedded ADC and DAC or without. The processor with embedded ADC and DAC costs almost twice as much but if the processor without ADC and DAC is used, an external ADC and DAC is needed. An external ADC and DAC cost almost as much as the cheapest DSP itself [22].

The FPGA is a bit more expensive than the DSP almost three times and does not contain embedded ADC and DAC. So, the summary of this price comparison is that a DSP with embedded ADC and DAC is the cheapest solution in this case and it also saves two external units.

4.1.3 Most suitable implementation

The DSP is a bit cheaper than the FPGAs and it is also a bit more flexible. The DSPs can also have built-in ADC and DAC and still being cheap. So, in this case the DSPs are cheaper and also more flexible which makes it more suitable for this application.
4.2 Circuit realisation

The circuit realisation is shown in Figure 74.

![Figure 74. Overview of the system.](image)

4.2.1 Anti-aliasing filter calculations

The anti-aliasing filter must follow the specification in Section 3.1.2 and the components have values from the E24 series [25]. The E24 series means that there are 24 available component values for each decade. The anti-aliasing filter is active and of Butterworth type with an order of eight, see Figure 75. The component values are calculated from the pole placements of the Butterworth filter and the calculation are made as in [23].

The transfer function is shown in Figure 76 and the requirements are fulfilled because the attenuation at 29 kHz is 45.7 dB and the passband edge goes up to 13.75 kHz which is more than 11 kHz.

![Figure 75. Schematic of the anti-aliasing filter and the component values.](image)

![Figure 76. Transfer function of the anti-aliasing filter.](image)
4.2.2  Requirements on the analog amplifier

To use the whole range of the ADC, there is need for an amplifier before the A/D conversion, to use all the available bits in the ADC. The most cost-effective solution on VGA (Variable Gain Amplifier) is to put two VGAs that can amplify the signal up to 30 dB in series. The total amplification of the signal is then up to 60 dB, which is as much as the original system. The gain of the VGA is controlled by the DSP processor which holds the signal as near the max of the range of the ADC but not too high to use all available bits.

An AGC (Automatic Gain Control) is not useful in this case because the AGC take a reference voltage and amplifies the signal up to that level. The system has six different antenna signals that must be amplified with the same gain. Otherwise, the signal difference is destroyed and the system can not detect where the wire is located.

4.2.3  Requirements on the ADC

If the ADC has a built in sample-and-hold circuit, no external sample-and-hold circuit is needed. In other case, an external sample-and-hold circuit is needed. The ADC must be able to handle at least 40 kHz sampling frequency, with at least 10 bits, but at least 12 bits is preferred because the MCU samples 10 bits. There are six coils on the antennas so the ADC must have at least 6 channels. Otherwise, a number of ADCs with less than 6 channels can also be used.

4.2.4  Digital filter hardware implementation

The most suitable hardware for the digital filter is a DSP because it is cheaper and more flexible. The sampling frequency and data throughput is so low that almost all DSPs and FPGAs have enough performance to be used here. The DSPs and FPGAs must be able to work in temperatures between -40ºC and +85 ºC.

4.2.5  Requirements on the DAC

The DAC must have at least 10 bits resolution to match the 10 bits in the MCU, but a few more bits would be preferable to make sure that the 10 bits in the MCU are fully used. A lowpass filter, after the DAC, is needed to remove harmonics from the signal. The requirements are that the passband edge must be at least up to 2πf_0 and the stopband edge must be 2π · (f_s - f_0), (angular frequencies).

4.3 Implementation of a DSP with embedded ADC and DAC

The DSP is better because it is cheaper and more flexible. One of these flexibilities is that many DSP processors contain an embedded ADC with sample-and-hold and a DAC which can be implemented with the PWM (Pulse-Width Modulation) output. In this case, the only components that are needed for the realisation, are an amplifier, an anti-aliasing filter, the DSP, and maybe a lowpass filter after the DAC, see Figure 77.

![Figure 77. Overview of the system when a DSP with embedded ADC and DAC are used.](image-url)
5 Results

This chapter describes the creation of a prototype and the measurements on the prototype to make sure that the theoretical calculation really works.

5.1 Hardware for the prototype

The hardware that is used for the prototype is a development board, TMS320C6713 also called DSK6713. This is a development board with a DSP processor as the main component.

5.1.1 TMS320C6713 development board

The development board contains components such as an AIC23 audio codec. The Audio codec has a built-in ADC and DAC which can handle frequencies from 8 kHz up to 96 kHz. An overview of the board is shown in Figure 78 [24].

![Figure 78. Development board block diagram.](image_url)

5.1.2 Interface

The board has 3.5 mm stereo plug connection for headphone, line out, line in, and microphone. There are also four DIP switches on the board which can be used to change the center frequency. On the board are also four LEDs (Light-Emitting Diodes) available for the user.

5.2 Software development

The programming language that will be used for this application is C-code which will be transferred to assembler code and further to machine code. The transformations are performed by the development program for the board Code Composer studio. The DSP processor will use 16 bits in this application which makes the SNR (Signal to Noise Ratio) = 16·6.02 + 1.8 dB = 98.12 dB.

5.2.1 Development of a filter program

The digital filter is developed in Section 3.6 and implemented in C-code. The software development is performed in such a way that the program code should be as near the reality as possible. This is performed by that all nodes and the structure of the filter is kept in the software according to the theory. The program code is attached to Appendix A - C-code.
5.2.2 Development of amplitude to DC-level converter

The signal in the analog application is transformed from the AC signal into a DC-level in the way that the amplitude of the signal is transformed into a DC-level. This transformation is also implemented in digital domain now but the difference is the signal still needs to be converted into a DC-level so that the interface with the MCU still is the same. This is not included in this prototype because the output from the development board is AC-coupled so the DC-level will not appear on the output. Because of this behaviour, the software for this function is unnecessary because the function can not be verified.

5.3 Measurements

To be sure that the filter really works in reality, some measurements are needed. The connections on the development board are just 3.5 mm headphone plugs so modifications are needed if some units, more than a computer is used for measurements.

The drawbacks with the measurements is that the resolution in the computer ADC is just 8 bits and the oscilloscope also has 8 bits of resolution which makes the SNR = 8·6.02+1.8 dB = 49.96 dB. This is less than desired but enough to analyze the filter with.

5.3.1 Signal generator and oscilloscope measurements

To get less noise in the measurements, the input will be created by a signal generator. The signal will then be processed by the DSP and then sent to the oscilloscope. The signal generator creates a sinusoidal signal and the frequency can be adjusted to measure all interesting center frequencies which in this case are 1-11 kHz. The oscilloscope is of digital type and can be used in two ways. The first is to just check the sinusoidal in the time domain and check how much it is attenuated by the filter. The other way is to use the built in FFT function to check which frequencies pass the filter.

The easier one of these two measurements is to use the FFT because in the time domain, the amplitude of the signal becomes very small and the amplitude is hard to measure accurately. The FFT transforms the signal from time domain into frequency domain. Unfortunately, the measurements are limited by the number of bits in the ADC. The noise floor is about 50 dB lower than the signal itself so it is hard to say if the requirements on attenuation of 60 dB and 80 dB are fulfilled.

The measurements are performed in a way that the center frequency of the filter is locked on a frequency. Then, the input signal, a frequency sweep of a sinusoidal, is sent through the filter and the pass band and stop band is analyzed.

5.3.2 Results of the measurements

The measurements where performed by that the filter has an input from a signal generator and the output is analyzed by an oscilloscope. The view on the oscilloscope is shown in Figure 79 and Figure 80 with two different test cases. The test just uses a single tone because the signal generator can just generate one tone at the same time. The results of the measurements are presented in Table 17.

The measurements have been done in the following way. The FFT on the oscilloscope is used to analyze the most of the attenuation points and for the smallest attenuation values (0.1 dB) is just the time domain analyzed because the accuracy is better for this small attenuation.
The $\alpha$ is 0.6 because that is in the middle of the range for $\alpha$ that theoretically meets the requirements.

<table>
<thead>
<tr>
<th>Attenuation (dB)</th>
<th>Beta value</th>
<th>Freq (kHz)</th>
<th>Freq (kHz)</th>
<th>Freq (kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>0.99</td>
<td>0.66</td>
<td>0.2</td>
<td>-0.2</td>
</tr>
</tbody>
</table>

| Center frequency | ~1.02      | ~5.95      | ~9.65      | ~12.45     |

| 0.1              | 1.14       | 6.12       | 9.76       | 12.55      |
| 1                | 1.41       | 6.28       | 9.91       | 12.78      |
| 3                | 1.57       | 6.47       | 10.11      | 12.91      |
| 10               | 2.26       | 6.90       | 10.51      | 13.33      |
| 20               | 2.97       | 7.40       | 10.98      | 13.76      |
| 40               | 4.52       | 8.38       | 11.81      | 14.51      |
| 50               | 5.12       | 8.82       | 12.18      | 14.84      |

Table 17. Attenuation measurements on the filter prototype.

Figure 79. The signal with the same frequency as the filter center frequency, without the filter to the left and with the filter to the right.

Figure 80. The signal with a frequency far from the filter center frequency, without the filter to the left and with the filter to the right.
The measurements are plotted according to the requirements in Figure 81. The requirements on the passband are minimum requirements and in the stopband are maximum requirements.

![Figure 81. Measurements and requirements plotted in the same graph. The requirements on the pass band and minimum requirements and in the stop band maximum requirements.](image)

**5.3.3 Conclusions**

These attenuation values can be compared to the specification of requirements in Chapter 3.2 and the conclusion is that the requirements are fulfilled for the three higher center frequencies and not fulfilled for the lowest center frequency. The higher attenuation values can not be compared here because the ADC must have more than 8 bits to do that. Observe that the high $\beta$ has very steep attenuation curve in the lower side and not so steep on the higher side compared to the beta values that are not near one.

The measurements have shown that there are margins to the requirements for 40 dB attenuation. For the larger center frequencies the attenuation requirements on 60 dB and 80 dB are probably satisfied. For the smaller center frequencies the same subject as discussed above will probably make that the requirements on the higher attenuation not are satisfied.

A comparison of the analog filters and the digital filters are shown in Figure 82 for center frequency 5.2 kHz and in Figure 83 for center frequency 6.25 kHz. The requirements are also plotted see chapter 3.2 for an explanation of the requirements. To see the pass band more accurate have two plots been added Figure 84 and Figure 85 which is just an enlargement of Figure 82 and Figure 83 respectively. In all four figures the alfà coefficient is 0.6 and the Q-value for the analog filter is 12.9 for 5.2 kHz and 6.96 for 6.25 kHz.
Figure 82. Comparison of the measured values on the digital filter, the digital filter in theory and the analog filter in theory for center frequency 5.2 kHz.

Figure 83. Comparison of the measured values on the digital filter, the digital filter in theory and the analog filter in theory for center frequency 6.25 kHz.
Comparison for center frequency 5.2 kHz

Figure 84. Comparison of the measured values on the digital filter, the digital filter in theory and the analog filter in theory for center frequency 5.2 kHz.

Comparison for center frequency 6.25 kHz

Figure 85. Comparison of the measured values on the digital filter, the digital filter in theory and the analog filter in theory for center frequency 6.25 kHz.
6 Summary
This chapter summaries this master thesis and also mentions some future work.

6.1 Summary and conclusions
The thesis investigates the opportunities to implement the analog signal processing with digital. There were very small documentations on the analog circuits when the thesis started so all of that was analyzed to know what type of signal processing were performed by the analog circuits. The analog circuits are controlled by the MCU which send the control signals to the circuits and to understand what the purpose of the circuits are the C-code for the MCU had to be analyzed to fully know what setting on the analog circuits are used.

The digital filter was developed by that a lot of different filter types was analyzed and their properties and advantages was analyzed to understand what type of filter was most suitable for this application. The filter also needed to be tuneable and by that fact that the lowpass to tuneable band pass filter structure was very suitable for this application. The most suited filter to be implemented with the lowpass to tuneable bandpass structure was the wave digital filter because it had a mixture of good properties in stability and low filter order. Another advantage with this solution is that the filter has only two coefficients one for control of the steepness of the filter and for control of the center frequency.

The prototype was developed in C-code and implemented in a DSP-processor on a development card. The C-code is implemented in that way so the code follows the real node values to make it easy to recognize the function of it. Finally the digital filter was implemented on the DSP-processor and the function of it was investigated and verified by measurements. The tools that were used for that purpose was a signal generator, the development board and an oscilloscope.

The conclusions from the thesis are that it is difficult to develop a filter with adjustable center frequency and small passband. The difficulties with small passband are that the filter has a poor stability property which makes it unstable on not useable in reality. The adjustable center frequency has also difficulties because the lowpass to bandpass structure that are used here are of IIR type and there can be problems with the stability.

6.2 Future work
Some improvements can still be performed on this thesis and the most important improvements are:

- Find a cheap and suitable DSP that meets the requirements on the hardware and have enough calculation power.
- Investigate the connection between the beta coefficient and the center frequency
- Find out if there is any possibility to make the digital meet the requirements for low center frequencies.
- Investigate under which circumstances the filter is stable or not and find a worst case for the filter to know what can be improved by that knowledge.
- Write c-programs for the control of the VGAs, for conversion of AC-amplitude to DC-level and for control of the ADC-input and DAC-output from the DSP.
- Find out a way how to use the dynamic range in the ADC in the most efficient way.
- Analyze where the new signal processing component should be located on the truck to minimize the disturbances.
- Optimize the C-code to make the need of performance smaller.
7 Bibliography


8 Appendix A – C-code

This appendix contains the C-code for the prototype that is described in Section 5.2.

8.1 Filter program

/*
* Include needed files */
#include "tonecfg.h"  // Config file
#include "dsk6713.h"
#include "dsk6713_aic23.h"  // Audio codec
#include "dsk6713_led.h"  // LEDs
#include "dsk6713_dip.h"  // Switches

/*
* Codec configuration settings */
DSK6713_AIC23_Config config = {
 0x0017,  // 0 DSK6713_AIC23_LEFTINVOL  Left line input channel volume
0x0017,  // 1 DSK6713_AIC23_RIGHTINVOL Right line input channel volume
0x00FF,  // 2 DSK6713_AIC23_LEFTHPVOL  Left channel headphone volume
0x00FF,  // 3 DSK6713_AIC23_RIGHTHPVOL Right channel headphone volume
0x0011,  // 4 DSK6713_AIC23_ANAPATH Analog audio path control
0x0000,  // 5 DSK6713_AIC23_DIGPATH  Digital audio path control
0x0000,  // 6 DSK6713_AIC23_POWERDOWN Power down control
0x0043,  // 7 DSK6713_AIC23_DIGIF Digital audio interface format
0x0001,  // 8 DSK6713_AIC23_SAMPLERATE Sample rate control
0x0001  // 9 DSK6713_AIC23_DIGACT Digital interface activation
};

/*
* Set the coefficient values */
#define alfa_coeff 19660 //alfa = 0.639 when 16 bits is used
#define beta_init 22938; //beta = 0.7 when 16 bits is used

/*
* Filter coefficients */
#define number_of_filters 10
#define filter_order 2
#define node_number 9  //Number of nodes in the filter

/*
* Define the filter function */
Int16 wdf_bp_filter(Int16 *dly_buffer, Int16 xn, Int16 beta, Uint16 filter_n);

/*
* Define saturation function */
Int16 saturation(Int16 signal);

/*
* Define dynamic scale function */
Uint16 dynamic_scaling(Int16 beta_coeff);

/*
* Define the beta switch controller function */
Int16 beta_switch_controller(Int16 beta_value, Uint16 *add_control, Uint16 *sub_control);

void main()
{
  /* Declaration of useful things */
  Int16 dly_buffer[number_of_filters*filter_order] = {0};
  Int16 filter_input[number_of_filters+1];
  Uint16 j = 0;
  Uint32 rcvBuffer = 0;
  Uint16 add_control = 0;
  Uint16 sub_control = 0;
  DSK6713_AIC23_CodecHandle hCodec;

  Int16 beta_coeff = beta_init;

  /* Initialize the board support library, must be called first */
  DSK6713_init();
  DSK6713_LED_init();
  DSK6713_DIP_init();
  /* Start the codec */
  hCodec = DSK6713_AIC23_OpenCodec(0, &config);

  /* Set sample freq */
  DSK6713_AIC23_setFreq(hCodec, DSK6713_AIC23_FREQ_44KHZ);
  /* Turn off all LEDs */
  DSK6713_LED_off();
}
DSK6713_LED_off(1);
DSK6713_LED_off(2);
DSK6713_LED_off(3);

while(1){
    /* Read new values */
    while(!DSK6713_AIC23_read(hCodec, &rcvBuffer));
    filter_input[0] = (Int16)rcvBuffer;

    /* For changing of beta value */
    beta_coeff = beta_switch_controller(beta_coeff, &add_control, &sub_control);

    /* Scale the input to the filter */
    filter_input[0] = filter_input[0]/dynamic_scaling(beta_coeff);

    //Filter main loop
    if(DSK6713_DIP_get(3) == 0){
        for(j = 0 ; j < number_of_filters ; j++ ){
            filter_input[j+1] = wdf_bp_filter(dly_buffer, filter_input[j],
            beta_coeff, 2*j);
        }
    }
    else{
        DSK6713_LED_off(3);
        filter_input[number_of_filters] = filter_input[0];
    }

    /* Send a sample to the left channel */
    while (!DSK6713_AIC23_write(hCodec, (Uint16) filter_input[number_of_filters]*dynamic_scaling(beta_coeff)));

    /* Send a sample to the right channel */
    while (!DSK6713_AIC23_write(hCodec, (Uint16) filter_input[number_of_filters]*dynamic_scaling(beta_coeff)));
}

/* Close the codec */
    // DSK6713_AIC23_closeCodec(hCodec);
}

/* Dynamic scaling function */
Uint16 dynamic_scaling(Int16 beta_coeff){
    if(beta_coeff>32000){
        return 4;
    }
    else if(beta_coeff>30000){
        return 3;
    }
    else{
        return 2;
    }
}

/* Define the beta switch controller function */
Int16 beta_switch_controller(Int16 beta_value, Uint16 *add_control, Uint16 *sub_control){

    Uint16 steps = 700;
    if(DSK6713_DIP_get(2) == 1){
        *sub_control = 0;
        DSK6713_LED_off(2);
    }
    else{
        if(*sub_control == 0 && beta_value>(-6000)+steps){
            beta_value = beta_value-steps;
        }
        *sub_control = 1;
        DSK6713_LED_on(2);
    }

    if(DSK6713_DIP_get(1) == 1){
        *add_control = 0;
        DSK6713_LED_off(1);
    }
    else{
        if(*add_control == 0 && beta_value>(32768-steps)){
            beta_value = beta_value+steps;
        }
    }
}
*add_control = 1;
DSK6713_LED_on(1);
}

if(beta_value<-5000 || beta_value>32000){
DSK6713_LED_on(0);
}
else{
DSK6713_LED_off(0);
}
return beta_value;

//Filter function
Int16 wdf_bp_filter(Int16 *dly_buffer, Int16 xn, Int16 beta, Uint16 filter_n){
/* Coefficients needed for the filter */
Int16 xns = 0;
Int16 u[node_number+1]; // Declaration of nodes
Int16 v[filter_order+1]; // Temporary delay values to make the code easier to read
Int16 alfa = alfa_coeff; // Steepness coefficient
Int16 y = 0;

/* Set the local delay values */
v[0] = 0;
v[1] = dly_buffer[filter_n];
v[2] = dly_buffer[filter_n+1];

/* Calculation of node values - many calculations, but they follow the real node values */
xns = xn>>1; //Sign extend;
u[0] = 0;
u[6] = v[2];

u[2] = (alfa*u[1])>>15; //Shift depends of bits of coeff
u[3] = saturation(xns + u[2]);

u[5] = xn + u[4];

u[8] = (beta*u[7])>>15; //Shift depends of bits of coeff
y = u[5]/2; //Output signal

/* Update delay elements */
dly_buffer[filter_n] = u[3];
dly_buffer[filter_n+1] = saturation(u[9]);

return y;
}

Int16 saturation(Int16 signal){
/* Add one if signal < 0 */
if((signal & 0x8000) == 0x8000){
signal = signal+1;
}
/* Saturation if |signal|>(2^14 - 1) */
if(abs(signal) > 0x3FFF){
DSK6713_LED_on(3);
if((signal & 0x8000) == 0x8000){
signal = 0xC001;
}
else{
signal = 0x3FFF;
}
}
return signal;
}
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