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High Speed (MHz) Switch Mode Power Supplies (SMPS) using Coreless PCB Transformer Technology

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Dedicated to the divine lotus feet of

Bhagawan Sree Satya Sai Baba

&

Sree Sadguru Krishnendra Santani

'HELP EVER, HURT NEVER'
ABSTRACT

The most essential unit required for all the electronic devices is the Power Supply Unit (PSU). The main objective of power supply designers is to reduce the size, cost and weight, and to increase the power density of the converter. There is also a requirement to have a lower loss in the circuit and hence in the improvement of energy efficiency of the converter circuit. Operating the converter circuits at higher switching frequencies reduces the size of the passive components such as transformers, inductors, and capacitors, which results in a compact size, weight, and increased power density of the converter. At present the switching frequency of the converter circuit is limited due to the increased switching losses in the existing semiconductor devices and in the magnetic area, because of increased hysteresis and eddy current loss in the core based transformer. Based on continuous efforts to improve the new semiconductor materials such as GaN/SiC and with recently developed high frequency multi-layered coreless PCB step down power transformers, it is now feasible to design ultra-low profile, high power density isolated DC/DC and AC/DC power converters. This thesis is focussed on the design, analysis and evaluation of the converters operating in the MHz frequency region with the latest semiconductor devices and multi-layered coreless PCB step-down power and signal transformers.

An isolated flyback DC-DC converter operated in the MHz frequency with multi-layered coreless PCB step down 2:1 power transformer has been designed and evaluated. Soft switching techniques have been incorporated in order to reduce the switching loss of the circuit. The flyback converter has been successfully tested up to a power level of 10W, in the switching frequency range of 2.7-4 MHz. The energy efficiency of the quasi resonant flyback converter was found to be in the range of 72-84% under zero voltage switching conditions (ZVS). The output voltage of the converter was regulated by implementing the constant off-time frequency modulation technique.

Because of the theoretical limitations of the Si material MOSFETs, new materials such as GaN and SiC are being introduced into the market and these are showing promising results in the converter circuits as described in this thesis. Comparative parameters of the semiconductor materials such as the
energy band gap, field strengths and figure of merit have been discussed. In this case, the comparison of an existing Si MOSFET with that of a GaN MOSFET has been evaluated using a multi-layered coreless PCB step-down power transformer for the given input/output specifications of the flyback converter circuit. It has been determined that the energy efficiency of the 45 to 15V regulated converter using GaN was improved by 8-10% compared to the converter using the Si MOSFET due to the gate drive power consumption, lower conduction losses and improved rise/fall times of the switch.

For some of the AC/DC and DC/DC applications such as laptop adapters, set-top-box, and telecom applications, high voltage power MOSFETs used in converter circuits possess higher gate charges as compared to that of the low voltage rating MOSFETs. In addition, by operating them at higher switching frequencies, the gate drive power consumption, which is a function of frequency, increases. The switching speeds are also reduced due to the increased capacitance. In order to minimize this gate drive power consumption and to increase the frequency of the converter, a cascode flyback converter was built up using a multi-layered coreless PCB transformer and this was then evaluated. Both simulation and experimental results have shown that with the assistance of the cascode flyback converter the switching speeds of the converter were increased including the significant improvement in the energy efficiency compared to that of the single switch flyback converter.

In order to further maximize the utilization of the transformer, to reduce the voltage stress on MOSFETs and to obtain the maximum power density from the power converter, double ended topologies were chosen. For this purpose, a gate drive circuitry utilising the multi-layered coreless PCB gate drive transformer was designed and evaluated in both a Half-bridge and a Series resonant converter. It was found that the gate drive power consumption using this transformer was less than 0.8W for the frequency range of 1.5-3.5MHz. In addition, by using this gate drive circuitry, the maximum energy efficiency of the series resonant converter was found to be 86.5% with an output power of 36.5W.
SAMMANDRAG

Den viktigaste delen i alla elektroniska apparater är strömförsörjningsehnet och idag sker en konstant utveckling att minska storlek, kostnad och vikt, och att öka effektivitet för dessa. Det finns också ett krav att minska förlusten i omvandlaren och därmed öka verkningsgraden. Vid högre switchfrekvens minskar storleken på de passiva komponenter såsom transformatorer, induktorer och kondensatorer, vilket resulterar i en kompakt storlek, vikt och ökad effektivitet i omvandlaren. För närvarande är switchfrekvensen begränsad av förluster i befintliga halvledarkomponenter men även i magnetiska komponenter, på grund av ökad hysteres- och virvel-strömmar i kärnbasierade transformatorer. Nylig utveckling inom komponenter i kiselkarbid och galliumnitrid tillsammans med utvecklade kärnfria transformatorer möjliggör kompakt design med mycket låg bygghöjd av isolerade AC/DC och DC/DC omvandlare. Denna avhandling fokuserar på design, analys och utvärdering av omvandlare är MHz frekvenser konstruerade med de senaste halvledarkomponenter och flerlagers kärnfria kretskortstransformatörer.

En högfrekvent isolerad flyback DC-DC-omvandlare baserade på kärnfri 2:1 kretskortstransformator har konstruerats och utvärderats. Mjukswitchade tekniker har införts i syfte att minska förluster i kretsen. Flybackomvandlaren har verifierats upp till ca 10W, i frekvensområdet 2.7-4 MHz. Verkningsgraden hos den kvasiresonanta flyback omvandlare är 72-84% under nollspänningsswitchning (ZVS). Utspänningen från omvandlaren reglerades genom modulation med konstant frånsträning.

På grund av de teoretiska begränsningarna i kisel MOSFETs, visar nya komponenter i GaN lovande resultat i omvandlarkretsar i denna avhandling. I en jämförelse mellan en befintlig kisel och en GaN MOSFET i en högfrekvent isolerad 45 till 15V återkopplad omvandlare visade GaN 8-10% högre verkningsgrad. Förbättringar kan härledas framför allt lägre ledningsförluster, snabbare till och frånsträng samt lägre effektkonsumtion för gaterivningen
För högfrekventa omvandlare vid höga spänningar ökar förlusterna i gatedrivningen både p.g.a. frekvensen men även spänningsnivån. En cascode omvandlare har designats och utvärderas vilken kräver en mycket lägre gatedrivning då Millereffekten elimineras. Både simuleringar och experimentella resultat har visat att denna design kunnat öka prestandan jämfört med en traditionell design.

För att maximera utnyttjandegraden av transformatorn, och minska spänningsnivån på transistorerna har en högfrekvent halv-brygga dessutom implementerats och utvärderats. En flytande gatedrivare som arbetar upp till 350V i MHz området har därför också utvecklats som bygger på en mindre kretskortstransformator. Effektförbrukningen för gatedrivningen av båda transistorer har verifierats till att vara mindre än 0.8W i frekvensområdet mellan 1.5-3.5MHz. Den realiserade halvbryggen har karakteriserats i en serie-resonant konfiguration till att kunna ge upp till 86.5% verkningsgrad med en uteffekt av 36.5W.
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Sundsvall, May 2011
Kotte Hari Babu
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<tr>
<td>AC</td>
<td></td>
<td>Alternating Current</td>
</tr>
<tr>
<td>BJT</td>
<td></td>
<td>Bipolar Junction Transistor</td>
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<tr>
<td>CAD</td>
<td></td>
<td>Computer Aided Design</td>
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<tr>
<td>CCM</td>
<td></td>
<td>Continuous Current Mode</td>
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<td>DC</td>
<td></td>
<td>Direct Current</td>
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<tr>
<td>DCM</td>
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<td>Discontinuous Current Mode</td>
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<td>DSP</td>
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<td>Digital Signal Processing</td>
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<td>DVD</td>
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<td>Digital Versatile Disc</td>
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<tr>
<td>EMC</td>
<td></td>
<td>Electro Magnetic Compatibility</td>
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<td>EMI</td>
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<td>Electro Magnetic Interference</td>
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<tr>
<td>FEA</td>
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<td>Finite Element Analysis</td>
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<td>FM</td>
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<td>Frequency Modulation</td>
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<td>FR4</td>
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<td>Flame Retardant 4</td>
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<tr>
<td>GaN</td>
<td></td>
<td>Gallium Nitride</td>
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<td>IGBT</td>
<td></td>
<td>Insulated Gate Bipolar Transistor</td>
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<tr>
<td>IPM</td>
<td></td>
<td>Intelligent Power Modules</td>
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<tr>
<td>MEEF</td>
<td></td>
<td>Maximum Energy Efficiency Frequency</td>
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<tr>
<td>MHz</td>
<td></td>
<td>Mega Hertz</td>
</tr>
<tr>
<td>MIF</td>
<td></td>
<td>Maximum Impedance Frequency</td>
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<td>MLCLPCB</td>
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<td>Multi Layered Core Less Printed Circuit Board</td>
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<tr>
<td>MOSFET</td>
<td></td>
<td>Metal Oxide Semiconductor Field Effect Transistor</td>
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<tr>
<td>PCB</td>
<td></td>
<td>Printed Circuit Board</td>
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<tr>
<td>PSU</td>
<td></td>
<td>Power Supply Unit</td>
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<tr>
<td>PoE</td>
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<td>Power over Ethernet</td>
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<tr>
<td>PWM</td>
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<td>Pulse Width Modulation</td>
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<td>RF</td>
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<td>SMPS</td>
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<td>SMPS</td>
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<tr>
<td>WLAN</td>
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<td>Wireless Local Area Network</td>
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<tr>
<td>ZCS</td>
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<td>Zero Current Switching</td>
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<tr>
<td>ZVS</td>
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This thesis is mainly based on the following publications, herein referred to by their Roman numerals:

Paper I  A ZVS Flyback DC-DC Converter Using Multilayered Coreless Printed Circuit Board (PCB) Step-down Power Transformer
Kotte Hari Babu, Radhika Ambatipudi and Kent Bertilsson
Proceedings of World Academy of Science, Engineering and Technology, Issue 70, ISSN: 1307-6892, pp. 148-155, October 2010

Paper II  Comparative Results of GaN And Si MOSFET in a ZVS Flyback Converter using Multilayered Coreless Printed Circuit Board Step Down Transformer.
Kotte Hari Babu, Radhika Ambatipudi and Kent Bertilsson

Paper III  High Speed Cascode Flyback Converter using Multilayered Coreless Printed Circuit Board (PCB) Step-Down Power Transformer
Hari Babu Kotte, Radhika Ambatipudi and Kent Bertilsson
Accepted for 8th International Conference on Power Electronics, ICPE 2011 - ECCE Asia, May 30- June 3, 2011, The Shilla Hotel, and Jeju, Korea.

Paper IV  Coreless Printed Circuit Board (PCB) Step-down Transformers for DC-DC Converter Applications
Radhika Ambatipudi, Hari Babu Kotte, and Kent Bertilsson
Proceedings of World Academy of Science Engineering and Technology (WASET), Paris, France, October 2010, Issue. 70, pp. 380-389, ISSN 1307-6892
Paper V  High Frequency Half-Bridge Converter using Multilayered Coreless Printed Circuit Board Step-Down Power Transformer
Abdul Majid, Hari Babu Kotte, Stefan Haller, Radhika Ambatipudi, Jawad Saleem and Kent Bertilsson
Accepted for 8th International Conference on Power Electronics, ICPE 2011 - ECCE Asia, May 30- June 3, 2011, The Shilla Hotel, and Jeju, Korea.

Related papers not included in thesis

Paper VI  Comparison of Two Layered and Three Layered Coreless Printed Circuit Board (PCB) Step-Down Transformers
Radhika Ambatipudi, Hari Babu Kotte and Kent Bertilsson

Paper VII  Radiated Emissions of Multilayered Coreless Printed Circuit Board Step-Down Power Transformers in Switch Mode Power Supplies
Radhika Ambatipudi, Hari Babu Kotte and Kent Bertilsson
Accepted for 8th International Conference on Power Electronics, ICPE 2011 - ECCE Asia, May 30- June 3, 2011, The Shilla Hotel, and Jeju, Korea.

Paper VIII  Series Resonant Converter using Multilayered Coreless Printed Circuit Board(PCB) Step-Down Power Transformer
Hari Babu Kotte, Radhika Ambatipudi, and Kent Bertilsson
Submitted for 33rd International Telecommunications Energy Conference, 9-13 October, Amsterdam, The Netherlands
1 INTRODUCTION

Traditionally linear power supplies utilize a bulky power transformer in order to step down the voltage from AC mains and to provide isolation. This step-down voltage is then rectified, filtered and fed to the load through a series pass element. The power transformer utilized in this power supply usually operates at a low frequency of 50/60Hz due to which it is bulky in size and heavy in weight. Because of the bulky transformer and losses in the series pass element, the linear power supply is considered as an inefficient means of transferring the power from the primary source to the loads. For this reason, it is necessary to introduce a high frequency transformer, filter components such as inductor and capacitor which are lighter in weight and smaller in size and a switching element to reduce the losses in the converter. In this process, power supplies which operate in the switching mode of operation were introduced. In these switch mode power supplies (SMPS), the low frequency power transformer is replaced by a high frequency transformer which operates at higher frequencies as well as providing the isolation between the primary and secondary side of the converter. The basic block diagram relating to the SMPS is illustrated in fig. 1. In this case, the input voltage is rectified and then filtered by the input filter capacitor. This filtered and unregulated DC voltage is then fed to the high frequency transformer using fast power semiconductor switching devices such as power MOSFETs or BJTs as shown in fig. 1.

Figure 1. Block diagram of offline Switch Mode Power Supply [1]
This high frequency square wave signal is then fed to the primary side of the high frequency transformer and a suitable voltage magnitude corresponding to the turn’s ratio appears on the secondary side of the transformer. This voltage is then rectified by using fast recovery diodes such as Schottky diodes and thereby filtered and fed to the loads. The output voltage is then regulated by using a proper feedback circuit and then employing appropriate modulation techniques such as pulse width modulation (PWM), frequency modulation (FM) etc.

1.1 ADVANTAGES OF SMPS OVER LINEAR POWER SUPPLIES

The advantages of using a SMPS as compared to linear regulators are given as follows.

- High energy efficiency
- Reduction in size of passive elements (Transformers, inductors and capacitors)
- Light weight, low profile
- High power density (SMPS: 30W/in³ and Linear: 0.3W/in³) [2]

However, in terms of line and load regulations, output ripple, transient recovery and hold up time requirements, the linear power supplies display a superior performance as compared to that of the SMPS [1], [3]. But, in order to design the compact, light weight and energy efficient power supply, SMPS is considered as the better choice compared to its counterpart linear power supplies.

1.2 IMPORTANCE OF INCREASING SWITCHING FREQUENCY

The present switching frequencies of isolated converters such as single ended topologies flyback, forward and double ended topologies, half bridge, full bridge etc., are limited in the frequency range of 100 kHz - 1MHz [3], [4]. However, as the switching frequency of converter is increased, the size of the passive elements such as inductors, capacitors and transformers gets reduced. This results in the increased power density of converter and hence the higher energy efficiencies of the converters can be obtained. Apart from the above advantages, by increasing the switching frequency of converter, the closed loop response of the converter can be greatly improved. The requirements of the light weight, compact, higher efficiency...
of the converter discussed earlier can be feasible with the increase of switching frequency of converter.

The selection of switching frequency plays an important role because the electromagnetic noise produced by the fundamental switching frequency and the corresponding harmonic frequencies may interfere with that of the other electronic devices in its vicinity. For example, AM radio receivers suffer from interference if the switching frequency is in the range of 530 - 1710 kHz [5]. Therefore, a switching frequency for the converter, which exceeds the upper limit of the AM radio receiver frequency range, is beneficial which eliminates the interference from these signals.

1.3 CHALLENGES DUE TO HIGHER SWITCHING FREQUENCIES

In the previous section we discussed the benefits of operating the converter at higher switching frequencies. However, in order to operate these converters at the higher frequencies, limitations exist in relation to the magnetic materials. In high frequency magnetics, the hysteresis and eddy current losses produced in the core materials acts as hindrance for the operation of the core based transformers at higher frequencies. Though the core materials are available at higher operating frequencies up to few MHz frequency regions, proper winding structure of the transformer is also required in order to reduce the skin and proximity effects at higher frequencies.

Apart from the above mentioned challenges in magnetics, the switching losses of the power converter and gate drive power consumption which are frequency dependent gets elevated when the frequency of converter is increased.

Due to these challenges in the magnetic and the semi conductor area, the operation of the switching power converters are limited to few hundreds of kHz to 1MHz as mentioned in earlier section.

1.4 MEASURES TO INCREASE THE SWITCHING FREQUENCY OF CONVERTER

The advantages and challenges of increasing switching frequencies were discussed in the previous sections. The challenges in the high frequency magnetics and semi conductor devices can be met with the recent developments in both the areas.
Due to the advancements in the switching power devices such as the introduction of new semiconductor materials (GaN and SiC) and the progress in the magnetic area i.e., using coreless PCB transformer technology for power transfer applications [6], the scope of increasing the switching frequency of power converter is increased. The coreless PCB transformers reported in [6] are limited to unity turns ratio, but most of the SMPS applications demand the step-up/step-down conversions, it is required to design a high frequency step-up/step-down power transformer. For this purpose, multilayered coreless PCB transformers for step-down/step-up conversion ratio were designed and evaluated and these transformers were proven to be highly energy efficient for power transfer applications in MHz frequency region.

1.5 THESIS OBJECTIVE AND METHOD

The objective of this thesis is to investigate whether it is possible to design a high frequency, highly energy efficient SMPS with high power density by using multilayered coreless PCB step-down power transformers developed in Mid Sweden University. Therefore, the main focus of the thesis is on the design and analysis of the high frequency power converters utilising the multilayered coreless PCB transformers. In this process, several steps should be considered for the determination of suitable components required for high frequency operation such as power MOSFETs, gate drivers, diodes, filter components etc., It is necessary to build a proper high frequency model for the converter circuits where parasitic elements plays an important role. For this purpose, the high frequency model of the designed power converters was obtained with the assistance of simulation tool, SIMetrix software. After the successful evaluation of these converters using the simulation tool, the desire is then to develop a prototype converter with the designed multi-layered coreless PCB transformer with higher energy efficiencies, which provides the scope for future generation ultra low profile power converters.

In this process, the following aspects should be covered:

- Study, evaluation and characterization of various power MOSFETs, high resolution microcontrollers, rectifier diodes suitable for high frequency converters.
• Determination of the low gate drive power consumption MOSFET driver applicable for high speed switching converters with the objective of low rise/fall times.

• Building up of the converters such as flyback/cascode flyback suitable for the given power applications and evaluating their performance in the MHz frequency region using coreless PCB transformers.

• Evaluation of the newly arrived semiconductor switching devices such as GaN MOSFET in converter circuits and comparing its performance with that of the existing Si MOSFETs.

• Evaluation of gate drive circuitry required for driving high side MOSFETs in double ended topologies such as half-bridge and series resonant converter.

1.6 THESIS OUTLINE

The thesis is organized as follows:

Chapter 1: This chapter provides a brief introduction to linear and switch mode power supplies and the advantages associated with switch mode power supplies. The requirement for the increase of switching frequencies is also discussed in addition to the challenges and possibilities of achieving high frequency converters. The objective, method and outline of the thesis are provided at the end of the chapter.

Chapter 2: In this chapter, different types of MOSFET gate drivers are evaluated. These drivers are compared in terms of their drive power consumption, rise/fall times, EMI which are the required parameters for high speed MOSFET gate drivers together with the operation of the MOSFET during turn-on and turn-off conditions.

Chapter 3: In this chapter, the inductance required for the given power transfer application in a flyback converter as a function of frequency was estimated and
discussed. The benefits of soft switching techniques such as zero voltage switching compared to hard switching flyback converter are presented.

The simulation and experimental results of quasi resonant flyback converter using high frequency multilayered coreless PCB step-down power transformer are also presented.

Chapter 4: In this chapter, various semiconductor materials and their prominent features required in high speed converters are discussed. The benefits of using the newly arrived GaN MOSFET compared to Si MOSFET are presented with the experimental analysis.

Chapter 5: In this chapter, a cascode converter utilizing a low/high side MOSFETs is demonstrated. The benefit of utilizing the cascode converter as compared to a single switch flyback converter in terms of switching speed, gate drive power consumption and the converter energy efficiency are discussed.

Chapter 6: This chapter introduces a high speed gate drive circuitry utilised for driving the high side MOSFET in double ended topology. The gate drive power consumption and the successful application of gate drive circuitry in MHz frequency region with the help of Series Resonant Converter are discussed.

The contents of the thesis and publications are summarized together with the conclusions and author’s contribution corresponding to different publications is presented.

In the end, papers related to the proposed work have been included for the ready reference of reader.
2 MOSFET GATE DRIVERS FOR HIGH SPEED SMPS

A MOSFET gate driver is necessary whenever the controller circuit is unable to drive the power MOSFET directly due to its low current capability. A power MOSFET gate driver is a power amplifier which takes power from the controller circuit and amplifies it in order to drive the switching power MOSFETs. By maintaining individual controller and driver circuits, it is possible to ensure that the controller runs under cooler and stable conditions, due to the high peak currents flowing in the driver circuit, while driving the power MOSFETs. The drivers can be classified as either discretized, using bipolar devices such as NPN and PNP emitter follower circuits, or as a single IC driver, which uses logic gates. However, the use of an IC gate driver has several advantages in comparison to using one which is discretized in terms of space [7], delay, other safe operating conditions, reduced noise and voltage drops across the trace between the gate and MOSFET gate driver.

2.1 Switching Model of Power MOSFET

The simplified switching model of a MOSFET including a gate driver IC is illustrated in fig. 2. Figure 2 illustrates the MOSFET model consisting of the parasitic elements such as the gate-source, drain-source, gate-drain/miller capacitances which all have a significant influence on the switching behaviour in terms of switching transients.

Figure 2. Switching Model of power MOSFET with the gate driver IC [7]
‘L’ and ‘L’ are the parasitic inductances corresponding to the MOSFETs whereas ‘R’ is the internal resistance which has a significant impact on the switching transients and the MOSFET’s $dv/dt$ immunity [8]. The switching speed of the MOSFET is mainly determined by the Miller effect which is produced by the gate-drain capacitance ‘$C_{gd}$’. This capacitance is highly non-linear in nature with respect to both the gate-source and the drain voltages.

In general the current required to drive the MOSFET during the turn-on and turn-off times is high due to the gate/input capacitance of the MOSFET which includes the gate-source ‘$C_{gs}$’ and the gate-drain ‘$C_{gd}$’ capacitances.

2.2 Switching behaviour of power MOSFET

In high frequency SMPS, it is important to make the correct selection of components and gate drive circuitry as these play prominent roles. Therefore, it is necessary to have a sound knowledge regarding the switching behaviour of the power MOSFETs in order to select the correct MOSFET gate driver and its components. Hence, a brief description of the turn-on and turn-off procedure of the power MOSFETs is discussed in this section.

2.2.1 Turn-on and Turn-off procedure in Power MOSFET

The switching behaviour of the MOSFET under turn-on and turn-off conditions [8] including the current flow in the circuits is illustrated in fig. 3 and fig. 4 respectively.

Fig. 3 and fig. 4 shows the gate-source voltage ‘$V_{gs}$’, gate current ‘$I_{g}$’, drain-source voltage ‘$V_{ds}$’ and drain current ‘$I_{d}$’ of power MOSFET during turn-on and turn-off conditions respectively.

The switching behaviour can be explained during the turn-on process in its different modes as follows.

Mode 1 ($0 < V_{gs} < V_{th}$): In this mode of operation, the input capacitance ‘$C_{gs}+C_{gd}$’ becomes charged from 0 to the gate threshold voltage ‘$V_{th}$’. The majority of the gate current flows into the gate-source capacitance as compared to the gate-drain capacitance. As the gate voltage fed to the MOSFET is increasing in nature, the potential of the gate terminal of the MOSFET increases, which in turn reduces the
voltage across the gate-drain capacitance of the MOSFET. From fig. 3 it can be observed that, in this mode the drain-source voltage ‘\(V_{ds}\)’ and drain current ‘\(I_d\)’ remain unchanged and this represents the fact that the switch is not turned-on. This period is known as the turn on delay time of the MOSFET.

**Mode 2 \((V_{th} \leq V_{gs} < V_{gs_miller})\):** When the gate-source voltage ‘\(V_{gs}\)’ reaches its gate-threshold voltage ‘\(V_{th}\)’, the MOSFET enters the turned on state and the current starts to rise. In this mode, the current starts to increase in a linear proportional manner to ‘\(V_{gs}\)’ until it reaches the Miller plateau region i.e., ‘\(V_{gs_miller}\)’. The gate current remains so as to flow in the input capacitance as in the previous case. Unless and until all the current is transferred into the MOSFET, the drain-source voltage, ‘\(V_{ds}\)’ remains constant which can be observed from fig. 3.

**Mode 3 \((V_{gs} = V_{gs_miller})\):** Once the drain current is completely transferred into the MOSFET, the drain-source voltage ‘\(V_{ds}\)’ across the MOSFET starts to fall. The gate-

![Figure 3. Circuit and timing diagram during turn-ON process [8]](image1)

![Figure 4. Circuit and timing diagram during turn-OFF process [8]](image2)
source voltage remains constant and this is known as the Miller plateau region of the gate voltage, while the drain-source voltage falls. In order to bring the rapid voltage change across the drain-source terminal, the gate current of the driver flows into the gate-drain capacitance \( C_{gd} \) to discharge this capacitor. Providing the sufficient gate drive to traverse the miller plateau region of power MOSFET at a faster rate is the main characteristic of the MOSFET gate driver. In this mode, the drain current is maintained at a constant rate, which is mainly determined by the load conditions.

**Mode 4 \((V_{gs, miller} \leq V_{gs} \leq V_{gsopt})\):** In this mode of operation, the gate-source voltage, \( V_{gs} \) is further increased in order to fully enhance the MOSFET. Additionally, in order to maintain a low on-state resistance of the MOSFET, it is further increased to its optimal gate-source voltage \( V_{gsopt} \), thereby reducing the conduction losses of the power MOSFET. In this mode the gate-source and gate-drain capacitances become charged by maintaining the constant drain current with the decreased drain-source voltage, \( V_{ds} \).

In the same manner, the turn-off procedure of MOSFET [8] can be explained from fig. 4. From the procedure explained for the turn-on and turn-off processes, it can be concluded that in all these different modes of operation the parasitic elements play an important role. Therefore, it is necessary to determine the correct devices and gate drive circuitry for high speed SMPS, as discussed at the beginning of this section.

### 2.2.2 Gate drive power consumption

As discussed earlier, whenever the MOSFET is fed with the gate-source voltage \( V_{gs} \), during turn-on the gate/input capacitance of MOSFET gets charged while it gets discharged during turn-off condition. In this process some inevitable losses exist in the MOSFET gate driver which cannot be directly obtained by the gate/input capacitance of the MOSFET due to its non-linear behavior [9] with respect to the gate-source and drain voltages. Therefore, in order to determine the gate drive power consumption, the total gate charge specified at a particular gate-source voltage and drain voltage of the MOSFET, which is given in the gate drive characteristics of the power MOSFET datasheet is considered. The power dissipated in the gate driver due to the total charge is given in [8-10] as follows.
\[ P_{\text{gate}} = V_{gs} \cdot Q_g \cdot f_{sw} \]  \hspace{1cm} (1)

where,

\( Q_g \) \hspace{1cm} total gate charge at specified '\( V_{gs} \)’ and ‘\( V_{ds} \)’

\( V_{gs} \) \hspace{1cm} gate-source voltage

\( f_{sw} \) \hspace{1cm} switching frequency

Apart from the above loss, a transient power loss exists due to the output voltage transitions and, in addition, a quiescent power loss [10] which is very small compared to the gate drive power consumption due to total gate charge and hence can be ignored.

2.3 COMPARISON OF DIFFERENT DRIVERS FOR HIGH SPEED SMPS

Based upon the above analysis, four different gate drivers from different manufactures have been tested in order to check the performance characteristics such as the rise/fall times and the gate drive power consumption of these drivers in high frequency switching power supplies. Even though the details of the rise/fall times, propagation delays, gate drive power consumption do all exist in their datasheets, it is difficult to compare different manufacturer’s drivers because these details correspond to specific test conditions.

Some of the details corresponding to these MOSFET drivers including manufacturer are listed in table 1.

<table>
<thead>
<tr>
<th>Drivers</th>
<th>( V_{in} ) (V)</th>
<th>( T_{rise}/T_{fall} ) (ns)</th>
<th>( T_{d1}/T_{d2} ) (ns)</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM5111</td>
<td>3.5-14</td>
<td>14/12@2nF</td>
<td>25/25@2nF</td>
<td>National Semiconductor</td>
</tr>
<tr>
<td>EL7222</td>
<td>4.5-15</td>
<td>10/13@1nF</td>
<td>18/20@1nF</td>
<td>Intersil</td>
</tr>
<tr>
<td>TC4451</td>
<td>4.5-18</td>
<td>30/32@15nF</td>
<td>44/44@15nF</td>
<td>Microchip</td>
</tr>
<tr>
<td>FAN3111</td>
<td>4.5-18</td>
<td>9/8@470pF</td>
<td>15/15@470pF</td>
<td>Fairchild Semiconductor</td>
</tr>
</tbody>
</table>

Here, \( T_{d1}/T_{d2} \) corresponds to turn-on and turn-off propagation delay times.

The LM5111, EL7222 and TC4451 drivers considered are of 8-pin SOIC package whereas the FAN3111 considered is of 5-pin SOT23 as illustrated in fig. 5.
Since, the MOSFET is considered as a capacitive load, a capacitor of 150pF is considered as the load capacitance and estimation is made in relation to the gate drive power consumption of all the MOSFET drivers within the switching frequency range of 1-5MHz.

The circuit diagram for testing various MOSFET gate drivers is illustrated in fig. 6.

The power consumption was estimated for two different input voltages of 5V and 10V and illustrated in figs.7 and 8 respectively. From these figures it can be observed that the gate drive power consumption of the TC4451 is highest followed by the MOSFET drivers FAN3111 and EL7222. The power consumed by the
MOSFET driver LM5111 in both cases is found to be less than that of the other drivers.

Apart from determining the power consumption of the drivers, the gate drive signals of all these drivers for 5V input were captured and illustrated in fig. 9.

![Figure 7. Measured MOSFET gate drive power for $V_{in}$ of 5V](image1)

![Figure 8. Measured MOSFET gate drive power for $V_{in}$ of 10V](image2)

Figure 7. Measured MOSFET gate drive power for $V_{in}$ of 5V  
Figure 8. Measured MOSFET gate drive power for $V_{in}$ of 10V

Figure 9. Measured gate drive pulses of different MOSFET drivers

a) LM5111  
b) EL7222  
c) TC4451  
d) FAN3111
The rise/fall times for all the gate signals of the MOSFET drivers at approximately 2.5MHz for a load capacitance of 150pF are displayed in fig. 9 (a)-(d). From these figures it can be observed that the rise and fall times of LM5111 are small compared to those for the other MOSFET drivers. This is one of the desirable characteristics of the MOSFET gate drivers which reduce the switching losses of the power MOSFET. However, due to the fast rise and fall times, a high radiated EMI exists as compared to that for the slow turn-on and turn-off processes. This is one of the trade-offs in the MOSFET gate drivers which should be considered while designing gate drive circuitry and high speed SMPS.

Since, the MOSFET driver LM5111 has consumed a low gate power with fast rise/fall times, it was considered as being the best of the tested drivers and was utilised in the converter circuits which will be discussed in further chapters.

The theoretical gate drive power consumption of this driver for 10V input voltage with respect to the frequency is plotted in fig. 10. It can be observed that there is a good agreement in the theoretical and measured values. Since, the requirement was to determine the drive consumption for various load conditions, this was considered and is depicted in fig. 11.
3 HARD AND SOFT SWITCHED FLYBACK DC-DC CONVERTER WITH MULTILAYERED CORELESS PRINTED CIRCUIT BOARD (MLCLPCB) TRANSFORMER

In general, a DC –DC converter consists of both active and passive elements such as MOSFETs, diodes, transformers, inductors and capacitors. The size of the passive elements is inversely proportional to the switching frequency of the converter. In order to achieve a high power density, a reduction of volume and weight and also for fast transient response of DC-DC converters [11], [12], the converter is required to be operated at higher switching frequencies as discussed earlier. However the commercially available isolated DC-DC converters such as the flyback and forward converters operate well below 500 kHz-1MHz, because of the limitations on existing magnetic and semiconductor devices.

At higher frequencies the core based transformers have limitations such as core losses, magnetic saturation and very bad high frequency characteristics, because of the presence of the magnetic cores [13]. In the late 1990s, research was concentrated on circumventing these problems by using coreless PCB transformers whose characteristics are given in [14]. Recent investigations [15] have shown that coreless PCB transformers can be used for signal and energy transfer applications, however, these transformers are limited to smaller voltage transformations of 1:1. Therefore, in order to design a high frequency DC-DC converter a highly energy efficient 2:1 multi-layered coreless PCB step down transformer for power transfer application has been designed [16].

Also, when the switching frequency of the converter is increased, the switching losses of the power MOSFET increase which leads to a reduced efficiency of the hard switched power converter resulting high electromagnetic interference (EMI). With the advancements in semiconductor technology such as the introduction of CoolMOS, Schottky diodes [17] and with the soft switching techniques, the energy efficiency of the DC-DC converters can be improved. In addition, with the soft switching techniques such as zero voltage switching (ZVS) and zero current switching (ZCS), the electromagnetic interference can be reduced [18].
In this section a DC-DC converter using a designed multi-layered coreless PCB 2:1 step-down transformer operating in both hard switched and soft switched flyback converter is discussed.

3.1 FLYBACK DC-DC CONVERTER

A flyback converter is an isolated version of the basic buck-boost converter [17]. It is the most widely used SMPS topology for power transfer applications falling below 150 watts [19] since it utilizes a single magnetic element as compared to other SMPS topologies. It can be used for several AC-DC and DC-DC applications including a laptop adapter, a computer monitor, telecom, Power over Ethernet (POE), WLAN access points. In this case the transformer serves the purpose of isolation, can be utilized for multiple outputs, and leads to better converter optimization for very large/very small conversion ratios [20]. The basic schematic of the flyback DC-DC converter is shown in fig. 12.

In the flyback converter, transformer ‘T1’ is connected in series with switch ‘SW1’. In this case, the flyback transformer is acting as an energy storage device instead of acting as a true transformer [21]. Briefly, the operation of the flyback converter can be explained as follows. In the steady state operation, when the switch ‘SW1’ is ON for a period of ‘Ton’, the dot end of the winding is positive compared to its non dot end and the energy is stored in the primary winding of the transformer ‘T1’. In this period the flyback diode is in reverse biased condition and the capacitor ‘C1’ supplies the load current to the load resistance ‘RL’. When the switch ‘SW1’ is OFF for a period of ‘Toff’, the flyback diode is forward biased and the energy is
delivered to load. During the OFF period, the drain source voltage of the ‘SW1’ is the sum of the input voltage ‘$V_{in}$’ and the output voltage ‘$V_o$’ reflected back through the turns ratio ‘$n$’, whilst the leakage spike voltage due to the leakage energy is ignored.

$$V_{sw} = V_{in} + n \cdot V_o$$  (2)

Flyback converters can normally operate in two different modes of operation.

1. Discontinuous mode (DCM)
2. Continuous mode of operation (CCM).

The factors determining the operation mode of the flyback converter are the primary inductance and the load current. In the case of DCM or Complete energy transfer mode [22], the energy that was stored in the primary winding of the transformer during the ‘$T_{on}$’ period is completely transferred to the output during the ‘$T_{off}$’ period. Otherwise, it is the case that the flyback converter would be considered as being in an incomplete energy transfer mode or in CCM.

DCM or CCM operation of the flyback converter will have its own advantages and disadvantages. In the case of DCM, switching losses of the secondary side flyback diode,’$D1$’ are reduced, and size of the transformer gets reduced because the primary inductance is smaller compared to the CCM System. Also in the case of DCM, the RMS currents flowing in the windings are high compared to CCM. The conduction losses in the switching devices like MOSFET or BJT are higher and the stress on the output filter capacitor,’$C1$’ gets increased.

Generally DCM is preferable for high voltage and low current applications whereas CCM is preferable for low voltage and high current applications. In case of CCM, the voltage conversion ratio ($V_o/V_{in}$) depends on the duty cycle, Where $V_o$ is output voltage of the converter, $V_{in}$ is the input voltage fed to the converter. In the DCM, the voltage conversion ratio not only depends on the duty cycle but also on the load condition, ‘$R_l$’, switching frequency, ‘$F_{SW}$’ and primary inductance, ‘$L_p$’.

The output voltage of the flyback converter operated in CCM mode is given by

$$V_o = V_{in} \cdot \frac{D}{1 - D} \cdot \frac{1}{n}$$  (3)
where ‘D’ is the duty cycle of the switch, 
\[ D = \frac{T_{on}}{T_{on} + T_{off}} = \frac{T_{on}}{T} \]

‘n’ is the transformer turns ratio.

The output voltage of the flyback converter operated in DCM mode [23] is given by
\[ V_{o} = V_{in} \cdot D \cdot \sqrt{\frac{R_i}{2 \cdot L_p \cdot F_{SW}}} \]  
(4)

As discussed previously, in order to design a compact SMPS, the switching frequency ‘\( F_{sw} \)’ of the converter must be increased. When the switching frequency of the converter is increased, the size of the passive elements such as the transformers, and capacitors must be determined. Therefore, for the given power transfer application the inductance required for the flyback transformer as a function of frequency is estimated.

3.1.1 Design guide line of flyback transformer in DCM

In this section, the design guide line for the flyback transformer operating in the discontinuous mode of operation (DCM) [22] is discussed briefly.

STEP 1: In core based transformers, the first step is to select the core type and size in order to meet the given power requirements.

STEP 2: The selection of the turn’s ratio, ‘\( n \)’, so as to estimate the maximum stress across on the switch (SW1) in the off state, ignoring the leakage inductance spike. The maximum voltage stress on the switch, ‘SW1’, at \( V_{in,\text{max}} \), by considering the 1volt drop across the flyback diode is given as.
\[ V_{d\text{max}} = V_{in,\text{max}} + n \cdot (V_{o} + 1) \]  
(5)

STEP 3: In order to maintain a DCM operation, the volt-sec product during the ‘\( T_{on} \)’ period must be equal to the volt-sec product during the reset time ‘\( T_{r} \)’. The on-state voltage drop across the switching device is taken as approximately 1volt. The total time period ‘\( T \)’ also consists of the dead time ‘\( T_{dl} \)’ and is given by equation (7). The dead time is usually considered as 20% of the total time period, ‘\( T \)’.
\[(V_{\text{in, min}} - 1) \cdot T_{\text{on}} = (V_o + 1) \cdot n \cdot T_r \quad (6)\]

\[T = T_{\text{on}} + T_r + T_{dt} \quad (7)\]

**STEP 4:** From equation (6) and (7), the on-period ‘Ton’ can be obtained as follows.

\[T_{\text{on}} = \frac{(V_o + 1) \cdot n \cdot (0.8 \cdot T)}{(V_{\text{in, min}} - 1) + (V_o + 1) \cdot n} \quad (8)\]

**STEP 5:** By considering the energy efficiency of the converter as 80%, the inductance of the primary winding is given from (9), where ‘P.’ is the Load power.

\[L_P = \frac{(V_{\text{in, min}} \cdot T_{\text{on}})^2}{(2.5 \cdot T \cdot P_o)} \quad (9)\]

**STEP 6:** The primary peak current flowing through the switching devices is computed from equation (10). In the case of power MOSFETS, the peak current rating should be 5-10 times [22] higher than the calculated value obtained from (10) in order to achieve a lower conduction loss of the MOSFET.

\[I_{\text{peak}} = \frac{(V_{\text{in, min}} \cdot T_{\text{on}})}{L_P} \quad (10)\]

The primary/secondary RMS currents flowing in the flyback transformer can be computed from (11) and (12).

\[I_{p, \text{rms}} = \frac{I_{\text{peak}}}{\sqrt{3}} \cdot \sqrt{\frac{T_{\text{on}}}{T}} \quad (11)\]

\[I_{s, \text{rms}} = \frac{I_{\text{peak}}}{\sqrt{3}} \cdot \sqrt{\frac{T_r}{T}} \cdot n \quad (12)\]

Since one ampere of RMS current requires 500 circular mils, the required wire size can be computed from, ‘I_{p,\text{rms}}’ and ‘I_{s,\text{rms}}’ as follows.
\[ W_p = 500 \cdot I_{p\_rms} \]  

(13)

\[ W_s = 500 \cdot I_{s\_rms} \]  

(14)

where \( W_p/W_s \) – Primary/Secondary width of conductor

### 3.1.2 Design guide line of flyback transformer in CCM

In the previous section, the design guide lines in relation to that of flyback transformer operating in DCM have been discussed and in this section the design guide lines when operated in CCM [22] will be discussed.

**STEP 1:** In this case also, the first step for the core based transformers is to select the core type and size in order to meet the given power requirements.

**STEP 2:** The turn’s ratio is determined in the same manner as discussed in STEP 2 of section 3.1.1.

**STEP 3:** Since no dead time exists, as was the case of DCM, the total time period ‘\( T \)’ is the summation of the ‘\( T_{on} \)’ and ‘\( T_{off} \)’. The duty cycle ratio (\( D \)) in continuous mode of operation is obtained as follows.

\[ T_{on} = \frac{(V_o + 1) \cdot T}{(V_{in\_min} - 1) \cdot n^{-1} + (V_o + 1)} \]  

(15)

**STEP 4:** From the given output power ‘\( P_o \)’, the current at the centre of the ramp of the secondary current pulse can be obtained by knowing the duty cycle and output voltage

\[ I_{cs} = \frac{P_o}{V_o \cdot (1 - D)} \]  

(16)

**STEP 5:** By assuming the energy efficiency to be 80%, the current at the centre of the ramp of the primary pulsed current can be obtained as follows
\[ I_{CP} = \frac{1.25 \cdot P_o}{V_{in\_min} \cdot (D)} \]  \hspace{1cm} (17)

**STEP 6:** At the minimum specified value of the output power, ‘\( P_{o\_min} \)’, the primary inductance of the transformer is given as

\[ L_{p} = \frac{(V_{in\_min} - 1) \cdot (V_{in\_min} \cdot T_{on}^2)}{2.5 \cdot (P_{o\_min} \cdot T)} \]  \hspace{1cm} (18)

\[ L_{s} = L_{p} \cdot (n^2)^{-1} \]  \hspace{1cm} (19)

### 3.1.3 Design Example

Consider a 30W, 12V flyback converter utilized for PoE application, with an input voltage range of 36V-72V and a turn’s ratio ‘\( n \)’ of 2 with an assumption of a minimum output power of 1/10\(^n\) nominal power.

The primary/secondary inductances of the transformer for the given power under DCM and CCM were determined with respect to the frequency variation by using the above mentioned design procedure and are illustrated in fig. 13 and fig. 14 respectively.

![Figure 13. Frequency vs Inductance in DCM flyback converter](image1)

![Figure 14. Frequency vs Inductance in CCM flyback converter](image2)

It can be observed that the inductances of the primary/secondary of the transformer are drastically reduced as the switching frequency is varied from 500 kHz to 5 MHz, in both cases. In the DCM mode of operation, the inductance value is further reduced as compared to that for the CCM mode of operation. However, larger peaks exist for the primary/secondary currents flowing through the
windings of the transformer when operated in the DCM conditions as compared to those for the CCM which can be verified from Table 2 at a switching frequency of 3MHz.

Table 2. Comparison of different parameters in DCM and CCM

<table>
<thead>
<tr>
<th></th>
<th>DCM</th>
<th>CCM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Primary/Secondary Inductance, [µH]</td>
<td>1.27/0.318</td>
<td>19.3/4.84</td>
</tr>
<tr>
<td>Primary/Secondary Peak current, [A]</td>
<td>4.42/8.85</td>
<td>1.77/3.03</td>
</tr>
<tr>
<td>Duty Cycle</td>
<td>0.4706</td>
<td>0.5882</td>
</tr>
<tr>
<td>Wp/Ws, [mm]</td>
<td>0.84/0.95</td>
<td>0.56/0.60</td>
</tr>
</tbody>
</table>

Even though the primary/secondary inductance of transformer is reduced as the switching frequency is increased, the existing core based transformers are limited to several hundreds of KHz because of the core losses [24]. Therefore, a high frequency multi-layered coreless PCB (MLCLPCB) step-down transformer operating at a few MHz for power transfer application has been designed [16]. In the next section, the characteristics of this transformer will be discussed.

3.2 MLCLPCB Step-down Power Transformer

A printed circuit board step down transformer which can be utilized for DC-DC converter applications such as PoE, telecom etc., has been designed in four layer PCB. The PCB laminate, considered is of FR4 material with breakdown strength of approximately 50kV/mm [25]. In this case, in order to achieve a good coupling coefficient ‘K’ between the primary and secondary, the two primaries are on either side of secondary winding with a primary-secondary-primary (PSP) structure as illustrated in fig. 15. The aforementioned procedure of section 3.1.2 has been utilized in the design of this transformer in order to operate the converter in the CCM mode of operation based on load power, input voltage range and output voltage. STEP 1 described in the procedure is ignored because these transformers do not have any magnetic cores.
The electrical parameters such as inductance, capacitance and resistance of transformer depend on their corresponding geometrical parameters. The geometrical parameters of the MLCLPCB step-down 2:1 power transformer are tabulated in table 3.

Table 3. Geometrical parameters of transformer

<table>
<thead>
<tr>
<th>S.No</th>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>No. of Primary/Secondary turns</td>
<td>32/16</td>
</tr>
<tr>
<td>2</td>
<td>Width of conductor [mm]</td>
<td>0.6</td>
</tr>
<tr>
<td>3</td>
<td>Track separation [mm]</td>
<td>0.4</td>
</tr>
<tr>
<td>4</td>
<td>Height of conductor [µm]</td>
<td>70</td>
</tr>
<tr>
<td>5</td>
<td>Outermost Diameter [mm]</td>
<td>30</td>
</tr>
<tr>
<td>6</td>
<td>Board Thickness [mm]</td>
<td>1.48</td>
</tr>
</tbody>
</table>

In order to determine the exact parameters of the MLCLPCB step-down transformer, the parameters of the designed transformer were initially measured at 1MHz using a high precision RLC meter HP4284A. The self / leakage inductance of the primary ‘Lp’/’Llp’ was obtained by open circuiting and short circuiting the secondary winding respectively and vice versa. Another method was also used for measuring the leakage inductances of the flyback transformer i.e., the four wire measuring method [26]. The leakage inductances of below 1µH were determined by using the following equation.
\[ L_{lk} = \frac{50}{2\pi f} \frac{V_{\text{dut}}}{V_{50\Omega}} \]  

where ‘\( L_a \)’ is the leakage inductance, \( V_{\text{dut}}/V_{50\Omega} \) is the voltage across the device under test/voltage across a 50\( \Omega \) resistor and ‘\( f \)’ is the excitation frequency. The exact parameters of the transformer were obtained by passing these initial parameters into the high frequency model of the transformer shown in fig. 16. These parameters were fine tuned to match the modelled performance characteristics to those that had been measured within the frequency range of 1-10MHz. Hence, the actual parameters of transformer [16], [27] were obtained and are given in table 4.

![High frequency model of MLCLPCB transformer](image)

**Table 4. Electrical parameters of the transformer**

<table>
<thead>
<tr>
<th>S.No</th>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Primary/Secondary DC resistance [( \Omega )]</td>
<td>1.1/0.55</td>
</tr>
<tr>
<td>2</td>
<td>Primary/Secondary self inductance [( \mu H )]</td>
<td>17.23/4.54</td>
</tr>
<tr>
<td>3</td>
<td>Primary/Secondary leakage inductance [( \mu H )]</td>
<td>0.46/0.23</td>
</tr>
<tr>
<td>4</td>
<td>Primary/Secondary Mutual inductance [( \mu H )]</td>
<td>16.77/4.31</td>
</tr>
<tr>
<td>5</td>
<td>Inter winding capacitance [pF]</td>
<td>178</td>
</tr>
<tr>
<td>6</td>
<td>Coefficient of coupling</td>
<td>0.95</td>
</tr>
</tbody>
</table>

### 3.2.3 Energy efficiency of designed MLCLPCB 2:1 power transformer

Since, it is necessary to have a highly energy efficient transformer in order to obtain the energy efficient DC-DC converter, power tests were carried out for the transformer. The sinusoidal excitation was given to the transformer using a radio frequency (RF) power amplifier BBM0A3FKO and the energy efficiency of the transformer was determined before utilizing it in the flyback converter. The measured energy efficiency of the transformer at ‘\( R_L \)’ of 50\( \Omega \) with a resonant
capacitor ‘C’ of 820pF across the secondary winding of the transformer is illustrated in fig. 17. The resonant capacitor is placed across the secondary winding of the transformer in order to increase the transfer function $V_{sec}/V_{pri}$ input impedance of the transformer ‘Zin’ [28]. The maximum energy efficiency of the transformer is found to be 95% at a frequency of 2MHz and can be observed that it is above 90% in the frequency range of approximately 1-5MHz.

![Figure 17. Measured Energy efficiency of MLCLPCB step-down power transformer](image)

3.3 HARD SWITCHED CONVERTER

In switching power converters, when the switch transition takes place from the ON state to the OFF state and vice versa, both a voltage and current exist simultaneously for a short period of time. In this case the converter is said to be operated in a hard switched condition.

3.3.1 Problems associated with Hard switched converter

The above mentioned situation leads to a power loss in the switching device which degrades the energy efficiency of the converter. The corresponding switching power loss across the device during transition times is illustrated in fig. 18. Particularly in the case of high frequency DC-DC converters, the switching losses of a power MOSFET which are a function of the switching frequency and the switch transition times ‘$t_{sw\ (on)}$’ and ‘$t_{sw\ (off)}$’ [29] are significantly increased.
As the losses in the MOSFET increase, the temperature of the converter, the stresses on the MOSFET and the cooling requirement also raise, whereas the energy efficiency of the converter gets reduced. In addition, the rate of change of the current \((\text{di/dt})\) and voltage \((\text{dv/dt})\) in the devices are high and uncontrollable which results in high electromagnetic magnetic interference (EMI) as mentioned earlier and hence the reliability of converter is reduced. It then becomes vulnerable if any stray capacitance and leakage inductance occurs in the layout of the chosen converter and components. Because of these associated problems which are involved by increasing switching frequency, the operating frequency of the converter is forced to be at lower frequencies in the case of the hard switched converter which leads to an increase in the size of the converter.

\[
P_{SW} = f_{SW}(t_{sw(on)} + t_{sw(off)})
\]

Figure 18. Switching Losses of Hard Switched Converter [30]

3.3.2 Measures to minimize losses in Hard switched converter

In the above section, the problems associated with a hard switched converter are discussed. It is very important to minimize these losses and their related consequences; therefore the corresponding measures are discussed in this section.

3.3.2.1 Circuit layout
By reducing the parasitic capacitances and inductances, the circuit layout can be improved.

### 3.3.2.2 Utilizing passive or active snubbers to control high di/dt and dv/dt

Generally, snubbers are classified as passive/active and dissipative/non-dissipative in nature. Passive snubber circuits consist of resistors, capacitors, inductors and diodes whereas the active snubber is built by using active switches such as transistors, with additional external drive circuitry which reduces the switching losses but, additionally, on the other hand, increases the power consumption and complexity of the circuit [31]. Therefore, it is not applicable for all the applications which require snubber circuits.

In the case of dissipative snubbers, the stored energy in the snubber is dissipated in the resistor. However, if the stored energy is utilized by pumping it into the source or load, it is called a non-dissipative snubber. In the case of non-dissipative snubbers the elements ‘L’ and ‘C’ are utilized to shape the current waveform during the turn-off process. However, these are relatively complex compared to those for the dissipative snubbers.

In the case of the passive dissipative snubbers, the rate of change of the voltage/current is reduced by shaping the switching trajectory [19]. Also by using the passive snubber, the stress and loss of the switching devices are merely transferred to the snubber instead of the switching element thereby resulting in more or less the same energy efficiency of the converter. Therefore, the switching frequency of the converter is limited to lower frequencies since the switching loss is proportional to the switching frequency according to equation (21).

### 3.3.2.3 Controlling turn-on and turn-off times to reduce di/dt and dv/dt

The rise and fall times associated with the turn-on and turn-off times can be controlled by adjusting the gate voltages of the switching devices such as the MOSFET. Usually, by varying the gate voltage of the MOSFET, the rise and fall times of the gate pulse can be controlled. By reducing the voltage, the rise time of the pulse increases and this results in a reduced $dv/dt$ and $di/dt$. However, by doing this, the reduction of EMI is possible at the cost of switching losses in relation to the MOSFET.
3.3.2.4 Employing soft-switching techniques

The above discussed measures provide a partial solution for the problems allied to the hard switched converter. Also these measures don’t result into the compact SMPS which can be obtained by increasing the switching frequency of converter. Therefore, a method which is useful for minimizing the problems associated with a hard switched converter together with a solution which involves increasing the switching frequency are discussed in the next section.

3.4 SOFT SWITCHED FLYBACK CONVERTER

The aforementioned problems and limitations imposed by a hard switched converter can be eliminated by adopting some changes in terms of the circuit parameters of the converter. For this purpose, soft switching circuits have been introduced. These can be mainly classified as

- Zero Current Switching (ZCS)
- Zero Voltage Switching (ZVS)

3.4.1 Zero Current Switching (ZCS)

In order to operate the switching power converter at higher frequencies, the turn-on/off loss of the switching device must be reduced as discussed in earlier sections. In the case of a resonant converter, the resonant elements such as the inductor ‘\(L\)’ and capacitor ‘\(C\)’ are used with the transistor. These resonant elements help to shape the waveform of the current in a sinusoidal form rather than, for example, a square or triangular waveform. When the circuit is turned-on and turned-off at zero current, it is called a zero current switching converter [9]. In this case, the switching loss at the switch transient periods is reduced.

3.4.2 Zero Voltage Switching (ZVS)

In order to operate the converters at higher switching frequencies for a few hundreds of kHz-MHz ranges, the MOSFETs are generally considered as being switching devices [32]. During the OFF state of the MOSFET, a considerable amount of energy is stored in its output capacitance as given by equation (22). This energy becomes dissipated in the MOSFET once the switch is turned-on [19]. In the case of a hard switched converter, this energy is directly dissipated into the
MOSFET when the switch is turned-on at high voltage. Turning on the MOSFET at higher voltage levels, results in a switching noise which is known as the Miller effect \cite{33}. This leads to a considerable noise and to the instability of the gate drive circuitry. To circumvent this problem of discharging the energy into the MOSFET during turn-on, a zero voltage switching technique is employed.

\[ P_{\text{Loss}} = \frac{1}{2} \cdot C_{\text{oss}} \cdot V^2 \cdot f_{sw} \]  

(22)

In ZVS converters, the switch is usually turned-on when the drain-source voltage of the MOSFET reaches zero \cite{18}, \cite{29}. Hence, the loss across the MOSFET during turn-on is significantly reduced by the ZVS. Usually, the ZVS of converter is achieved by using the resonant elements ‘L’ and ‘C’ which form a resonant circuit. In section 3.3 the discussion was that parasitic elements cause more serious problems in the case of hard switched converters. However, in the case of ZVS converters, the undesirable parasitic elements of the circuit can prove to be useful in achieving the ZVS condition by forming a resonant tank circuit. In this case, ‘L’ includes the transformer leakage inductance, the parasitic wire inductance and the external resonant inductor. The resonant capacitor, ‘C’ consists of the output capacitance of the MOSFET, the winding capacitance of the transformer and other parasitic capacitances.

\section*{3.5 Switching Trajectory of MOSFET}

Switching trajectory is a good measure in determining the power lost in the MOSFET. Therefore, the switching trajectory of the MOSFET in the hard switched converter with and without a snubber network and together with the soft switching converter are presented in fig. 19. It can be observed that a significant amount of energy is saved in the case of the soft switching converters because of the decreased switching losses of the MOSFET.
For a high frequency isolated converter application where large step-down ratio is required, a quasi resonant flyback converter [11] is considered to be a good choice. The reason for this is because it requires very few components and can thus be highly integrated into modern electronic systems. The basic circuit of a quasi resonant converter is illustrated in fig. 20 and the corresponding theoretical waveforms are shown in fig. 21. The turn’s ratio of a transformer is considered as ‘N’. As discussed previously, the passive elements ‘L,’ and ‘C’ form the resonant tank circuit.

The characteristic impedance ‘$Z_n$’, resonant frequency ‘$f_r$’, normalized load resistance ‘$r$’ and voltage conversion ratio ‘$M$’ of the circuit are given as follows.

\[ Z_n = \frac{LR}{CR} \]  

\[ f_r = \frac{1}{2\pi LR CR} \]  

\[ r = \frac{RL}{Z_n} \]  

\[ M = \frac{V_o}{V_{in}} \]
3.6.1 Modes of operation of quasi resonant flyback converter

The operation of a quasi resonant flyback converter [11] based on fig. 20 and 21 can be divided into several modes and these are briefly explained as follows.

**Mode.1** \( (0 < t < t_0) \): The gate signal is applied to the MOSFET during this period and the switch ‘S’ comes into the conduction state. The input voltage ‘\( V_{in} \)’ is applied to the primary winding of the transformer and the flyback diode ‘\( D_{SCH} \)’ is reverse biased because of the polarity of the transformer. In this mode, the entire primary current or magnetizing current flows through the switch ‘S’.

Figure 20. Basic circuit of ZVS Quasi Resonant Flyback Converter [11]

![Basic circuit of ZVS Quasi Resonant Flyback Converter](image)

Figure 21. Waveforms of ZVS Quasi Resonant Flyback Converter [11]

![Waveforms of ZVS Quasi Resonant Flyback Converter](image)
Mode.2 \((t_0<t<t_1)\): In this mode of operation at \(t_0\), the switch ‘S’ is turned-off and the primary current is diverted from the switch to the resonant capacitor. The drain-source voltage across the switch starts to rise in a linear fashion. Hence, it is known as the linear charging resonant capacitor, ‘\(C_R\)’.

Mode.3 \((t_1<t<t_2)\): As soon as the drain source voltage reaches a magnitude of \(V_{in}+NV_o\) the diode ‘\(D_{SCH}\)’ comes into picture after getting into forward biased condition. During this period ‘\(Lx\)’ and ‘\(Cx\)’ resonate and the drain-source voltage ‘\(V_{ds}\)’ reaches its maximum value given by the following equation.

\[
V_{ds_{\max}} = V_{in} + N \cdot V_o + I_n \cdot Z_n
\]  

(27)

At this instant ‘\(t_2\)’, voltage across the switch ‘S’ is reduced to zero value resulting in a ZVS condition of the converter and the diode ‘\(D_s\)’ becomes forward biased and the voltage of \((V_{in}-NV_o)\) is applied to the resonant inductor which results in the linear increase of the inductor current ‘\(i_{Lx}\)’. When this current reaches the value of the magnetizing current, the flyback diode ‘\(D_{SCH}\)’ becomes reverse biased and the cycle repeats itself.

3.6.2 Condition required for Zero Voltage Switching

In order to achieve a zero voltage switching in the quasi resonant converter, the following equation must be satisfied.

\[
r \leq \frac{M}{N}
\]  

(28)

3.6.3 Expression for (\(f_{sw}\)) in quasi resonant converter

The expression for determining the switching frequency [18] ‘\(f_{sw}\)’ of converter is given as follows

\[
f_{sw} = f_r \left( \frac{2\pi}{(1+MN)\left[\alpha + \frac{rN}{2M} + \frac{M}{rN} (1 - \cos \alpha)\right]} \right)
\]  

(29)

where,

\[
\alpha = \pi + \arcsin \left( \frac{rN}{M} \right)
\]  

(30)
3.7 SIMULATION AND EXPERIMENTAL RESULTS OF HARD AND SOFT SWITCHED CONVERTER

The designed coreless PCB step down 2:1 transformer was simulated and tested in a quasi resonant flyback converter shown in fig. 22 with input voltage specifications of 25 to 40V and a nominal voltage of 32.5V.

Here, the load resistance $R_L$ range of 15-50Ω was considered with the switching frequency range of 2.7-4.3MHz.

**POWER MOSFET ‘Q1’:** The power MOSFET switch considered is a ZXMN15A27K whose drain-source voltage is 150V with an on-state resistance $R_{ds, on}$ of 0.65Ω at $V_{gs}$ of 10V. The typical rise and fall times of the switch ‘Q1’ are 12.7 and 13.3ns respectively. The rise and fall times of the MOSFET should be as low as possible in order to achieve lower switching losses of the MOSFET as discussed previously. The typical output capacitance $C_{oss}$ of a MOSFET from the datasheet is 64.5pF [34].

**SCHOTTKY DIODE ‘Df’:** Because of low forward voltage drop of 0.46V a Schottky diode STPS15L45CB whose blocking capacity is of 45V with a forward current rating of 15 A [35] was used.

**DSPIC33FJ016GS502 Microcontroller:** The PWM signals required to drive the MOSFET were generated from the PWM channels of the micro-controller and fed to the MOSFET driver in order to strengthen the signal. The micro-controller possesses a resolution of 1.04ns for the duty cycle, dead-time, phase shift and...
frequency [36] which is a highly desirable feature for high frequency converter circuits.

**MOSFET Driver:** The power MOSFET ‘Q1’ was driven with a MOSFET driver LM5111 whose rise/fall times are 14/12ns at 2nF load respectively. The typical propagation delay of the driver is 25nS [10].

The flyback circuit was tested for both hard switched and soft switched conditions using a multi-layered coreless PCB transformer. As discussed previously, ‘L’ and ‘C’ form the resonant tank which leads to the ZVS condition for the flyback converter. The estimated resonant capacitor is 168pF including the parasitic and output capacitance of the MOSFET. In table 4, it was mentioned that the leakage inductance of the transformer is 0.46µH which is not sufficient to meet the ZVS condition according to equation (28). Therefore, an external inductor of 5.2µH was placed in series to the transformer. Since, core losses dominate at these higher frequencies in core based inductors, a PCB inductor operating in this frequency region was designed and utilized. The characteristic impedance and resonant frequency of the circuit were obtained by using equations (23) and (24) and were found to be 183.5Ω and 5.16MHz respectively.

### 3.7.1 ZVS flyback converter simulations

The simulations of the ZVS flyback converter were performed by using SIMetrix software. In this case, the high frequency model of the multi-layered coreless PCB transformer discussed in [16] was utilized.

#### 3.7.1.1 Modelling of MOSFET

The zetex MOSFET utilized in converter is ZXMN15A27K as discussed previously. Since, no SPICE model exists for this MOSFET, the device has been modelled prior to its utilization in the converter circuit. In order to model the MOSFET, the important parameters [37-39] to be considered are listed in table 5.

By considering these parameters, a spice model for the ZXMN15A27K has been developed using SIMetrix software.
Table 5. Required Simulation SPICE parameters of MOSFET

<table>
<thead>
<tr>
<th>S.No</th>
<th>Parameters</th>
<th>Symbol</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Length of channel</td>
<td>L</td>
<td>m</td>
</tr>
<tr>
<td>2</td>
<td>Width of channel</td>
<td>W</td>
<td>M</td>
</tr>
<tr>
<td>3</td>
<td>Oxide Thickness</td>
<td>Tox</td>
<td>M</td>
</tr>
<tr>
<td>4</td>
<td>Zero bias Threshold Voltage</td>
<td>VTO</td>
<td>V</td>
</tr>
<tr>
<td>5</td>
<td>Transconductance</td>
<td>KP</td>
<td>A/V²</td>
</tr>
<tr>
<td>6</td>
<td>Substrate doping density</td>
<td>NSUB</td>
<td>1/cm³</td>
</tr>
<tr>
<td>7</td>
<td>Fast surface state density</td>
<td>NFS</td>
<td>1/cm²</td>
</tr>
<tr>
<td>8</td>
<td>Saturation field factor</td>
<td>KAPPA</td>
<td>-</td>
</tr>
<tr>
<td>9</td>
<td>Surface mobility</td>
<td>UO</td>
<td>cm²/V.Sec</td>
</tr>
<tr>
<td>10</td>
<td>Source/Drain ohmic resistance</td>
<td>R5/RD</td>
<td>Ω</td>
</tr>
<tr>
<td>11</td>
<td>Bulk p-n saturation current</td>
<td>IS</td>
<td>A</td>
</tr>
<tr>
<td>12</td>
<td>Gate drain overlap capacitance/channel width</td>
<td>CGDO</td>
<td>F/m</td>
</tr>
<tr>
<td>13</td>
<td>Gate source overlap capacitance/channel width</td>
<td>CGSO</td>
<td>F/m</td>
</tr>
<tr>
<td>14</td>
<td>Bulk drain zero bias p-n capacitance</td>
<td>CBD</td>
<td>F</td>
</tr>
</tbody>
</table>

The output and the transfer characteristics of the MOSFET from the manufacturer’s data sheet and for the modelled MOSFET have been illustrated in figs. 23-26. From these figures it can be observed that a perfect model of the ZXMN15A27K has been obtained and hence it was utilized in the converter circuit. This modelled MOSFET is then placed in the quasi resonant flyback converter circuit shown in fig. 22 and simulated. At nominal input voltage of 32.5V and a load resistance of 10Ω the converter was switched at a frequency of 3.26MHz. The simulated waveforms of the ZVS converter including the transformer under these conditions are illustrated in fig. 27 and 28.

Figure (27) illustrates the gate source voltage, ‘\( V_{gs} \)' fed to the MOSFET, the drain-source voltage ‘\( V_{ds} \)' across ‘\( Q \)' , the mean current flowing through the switch ‘\( I_{mean} \)' and the output voltage ‘\( V_o \)' . From this figure, it can be observed that the converter is operating at almost zero voltage switching conditions. Figure. 28 illustrate the primary/secondary voltages and currents of the multi-layered coreless PCB transformer utilized in the converter circuit. The coreless PCB transformers behaviour in the switching circuit was initially examined by using the simulation software and based upon the high frequency model and simulations, after which the converter prototype was built and the experiments were carried out.
Figure 23. Output Characteristics of ZXMN15A27K

Figure 24. Output Characteristics of modelled ZXMN15A27K

Figure 25. Transfer Characteristics of ZXMN15A27K

Figure 26. Transfer Characteristics of modelled ZXMN15A27K

Figure 27. Waveforms of \( V_o \), \( V_{gs} \), \( V_{ds} \) and \( I_{mean} \) of ZVS flyback Converter
3.7.2 Experimental results of ZVS flyback converter

The energy efficiency of the unregulated converter under both hard and soft switched conditions at a load resistance of 30Ω for the varied input voltage, ‘Vin’ of 25-40V are shown in fig. 29. In this case, the duty cycle ratio ‘D’ considered is of 50%. As discussed in the previous sections and from fig. 29, it was verified that the energy efficiency of converter can be improved by implementing one of the soft switching techniques i.e., ZVS. In addition, the calculated stress on MOSFET under ZVS conditions using equation (27) was in good agreement with that of the measured one as shown in fig. 30.
3.7.3 Regulation of ZVS flyback converter

The output voltage of the ZVS flyback converter was also regulated to 13V for the input voltage variation of 25-40V at a constant load resistance of 30Ω and is shown in fig. 31. To regulate the output voltage of the quasi resonant flyback converter, a constant off time frequency modulation technique was utilized as the converter switching frequency is varied in order to maintain the output voltage. The energy efficiency of the converter is maximum at the nominal input voltage of 32.5V and becomes reduced at lower input voltages because of the increased conduction losses due to the increased duty cycle (61%) and at higher voltages because of the increased switching losses of the converter.

The calculated and measured switching frequencies of the converter for varied input voltages in order to remain at a constant output voltage are depicted in fig. 32. The measured switching frequencies were in good agreement with those calculated by using equation (29).

The measured energy efficiency of the unregulated converter at different load conditions of 15-50 Ω at a constant input voltage of 35V is illustrated in fig. 33 at a switching frequency of 3.26MHz.
Under these conditions the output voltage of converter was within 10-14 Volts. As in the previous case, here also the output voltage can be regulated to 13V by using the frequency modulation technique described in the previous section. The measured wave forms of the flyback converter at load resistances of 15Ω and 50Ω respectively are illustrated in figs. 34 and 35. It can be observed that in the first case i.e., in fig. 34 the circuit was operating under full ZVS condition whereas the circuit loses its ZVS property in light load condition which can be observed from fig. 35.

**Figure 33.** Energy efficiency for varied load resistances at constant input voltage of 35V

**Figure 34.** Measured waveforms of flyback converter with $R_L=15\Omega$. CH1 $-$ $V_{gs}$ (5V/div), CH3 $-$ $V_{ds}$ (50V/div), CH4 $-$ $V_{out}$ (20V/div)

**Figure 35.** Measured waveforms of flyback converter with $R_L=50\Omega$. CH1 $-$ $V_{gs}$ (5V/div), CH3 $-$ $V_{ds}$ (50V/div), CH4 $-$ $V_{out}$ (20V/div)
3.7.4 Loss estimation of multilayered coreless PCB transformer in ZVS flyback converter

The energy efficiency of the ZVS flyback converter using multilayered coreless PCB step down transformer is found to be approximately 82% with the load power of 10.05 W. The input voltage fed to the converter is of 40V, at a load resistance of 30Ω. The total power loss in the converter circuit is found to be 2.27W. The estimated losses of the transformer in the power converter are as follows:

In these coreless PCB transformers, since no core exists, the majority of the losses in the transformer are associated with copper losses. Under the above mentioned conditions, the RMS currents flowing through the primary/secondary winding of the transformer are 0.364/0.70A respectively. From table 4, the DC resistances of the primary/secondary winding of the transformers are 1.1/0.5Ω. The AC resistance of the windings at the switching frequency of 3.45MHz were found to be 2.51/1.25Ω respectively. These AC resistances were obtained by using the following equation by approximating the winding [40] into a circular spiral in nature and the copper loss was found to be 0.947 W.

\[
R_{ac} = \frac{R_{dc}h}{\delta(1-\exp(-h/\delta))}
\]

(31)

where,

- \( R_{dc} \) DC resistance of primary/secondary winding
- \( h \) Height of conductor
- \( \delta \) Skin depth

Since, these transformers were not covered by the core material, the radiative power losses were estimated from antenna theory [41], [42]. According to this theory, the transformer can be considered as a good loop radiator when the radius of the transformer is at least half of the wavelength of the corresponding operating frequency signal. The radiative loss of the transformer was estimated using the following equation (32).

\[
Pr_{ad} = 160\pi^6 I_o^2 \left( \frac{f_{sw}}{c} \right)^4
\]

(32)
The radiative power loss of the transformer was calculated for the fundamental component of the secondary current which is 0.701 amp RMS and was found to be 0.138nW by considering only the outermost loop i.e., 18mm radius of the transformer. However, the radiative power loss of the transformer is not only dependent on the fundamental but also on the harmonic components [42]. Therefore, the radiated power loss including the harmonic components for all the turns of the transformer was calculated up to 40 MHz harmonic frequency and is illustrated in fig. 36. From this it can be concluded that the overall loss of the transformer is due to copper losses because of the negligible radiative power losses.

![Figure 36. Radiative power loss of transformer used in ZVS flyback converter](image)

The remaining losses of the converter were shared by the MOSFET, Diode and other circuit elements.
3.7.5 Thermal profile of ZVS flyback converter

Under the same operating conditions, the thermal profile of the transformer and the converter are illustrated in fig. 37 and fig. 38 respectively which provides the better idea of the lossy components in the converter circuit.

![Figure 37. Thermal profile of Transformer in Flyback Converter](image1)

![Figure 38. Thermal profile of Flyback Converter, Ar1-Area of Switch (Q1), Ar2- Area of Schottky Diode](image2)

From the estimated losses of the transformer, it was found that transformer contributes to nearly 40% of the total loss in relation to the total converter losses and the remaining losses were shared by the other elements. Thus, by adopting a proper optimal design for the transformer and by reducing the losses in the MOSFET and the Schottky diode of the converter, it is possible to build a highly energy efficient compact power supply.
4  GALLIUM NITRIDE POWER MOSFET FOR MULTI MEGA Hertz SMPS

As discussed in previous chapters, the operation of the converter circuit at higher switching frequencies results in a size reduction of the energy storage elements such as the inductors, transformers and capacitors. At the higher switching frequency of the operation, the power MOSFETs are considered to be the best choice in comparison to power BJT’s according to [43], [44]. This is because of their remarkable behaviour such as the higher current gain, more ruggedness and, moreover, MOSFETs are the majority carrier devices because of which they are considered as being faster devices compared to their counterparts, the BJTs. Based on these characteristics, over the past three decades the silicon based power MOSFETs have ruled the power management area. However during this period several developments in ‘Si’ devices have been made in an attempt to bring out their best in relation to power converters for high frequency applications.

4.1  NEED FOR NEW SEMICONDUCTOR MATERIALS

By increasing the switching frequency of the converter to a few MHz, the losses in the traditional ‘Si’ MOSFET such as switching losses and gate drive power consumption, increase rapidly. The gate charge ‘Qg’ of a Si MOSFET at its respective operating voltage is high and leads to the increased gate drive power consumption. Due to these limitations in relation to the Si MOSFET, the overall energy efficiency of a converter with a traditional ‘Si’ MOSFET reduces.

4.2  ADVANCEMENTS IN SEMICONDUCTOR MATERIALS

Due to the above mentioned theoretical limitations of the ‘Si’ material [45], another state of the art material was required which is useful in relation to meet the current trends in the market. Therefore, in order to overcome the limitations imposed by the traditional ‘Si’ MOSFET at higher switching frequencies, a tremendous research effort was made in order to introduce new materials and structures for semiconductor devices. In this process a great deal of research was conducted into several new semiconductor materials such as GaAs, AlAs, SiC, GaN and AlN and their impact on power electronic applications and reported in [46]. For high power
and high temperature applications, it is necessary to have a large band gap material. The band gap energy of all these materials is illustrated in fig. 39.

Figure 39. Bandgap Energy of different semiconductor materials [46]

4.2.1 Properties of semiconductor materials

A few comparable material and electrical properties [43], [47] of Si, SiC and GaN materials useful for power electronic converters at room temperature are listed in table. 6.

Table 6. Electrical and Material properties of Si, 4H-SiC and GaN

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Si</th>
<th>4H-SiC</th>
<th>GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Band gap, E₉(eV)</td>
<td>1.1</td>
<td>3.25</td>
<td>3.4</td>
</tr>
<tr>
<td>Critical electric field strength, Ec(MV/cm)</td>
<td>0.3</td>
<td>3</td>
<td>3.3</td>
</tr>
<tr>
<td>Electron Mobility, μₑ (cm²/V.s)</td>
<td>1350</td>
<td>1000</td>
<td>1200</td>
</tr>
<tr>
<td>Thermal Conductivity, λ (W/cm.K)</td>
<td>1.3</td>
<td>4.9</td>
<td>2.3</td>
</tr>
<tr>
<td>BFOM¹ (Relative to Si)</td>
<td>1</td>
<td>608</td>
<td>794</td>
</tr>
<tr>
<td>JFOM² (Relative to Si)</td>
<td>1</td>
<td>400</td>
<td>1089</td>
</tr>
<tr>
<td>CFOM³ (Relative to Si)</td>
<td>1</td>
<td>397</td>
<td>383</td>
</tr>
</tbody>
</table>

BFOM¹: Baliga’s figure of merit- A measure which indicates the resistive losses in switching devices
JFOM: Johnson’s figure of merit - A measure which indicates the high frequency capability of a material
CFOM: Combined figure of merit for high temperature, high power and high frequency applications.

4.2.2 Advantages of GaN MOSFET compared to other devices

From fig. 39 and table 6, it can be observed that the materials SiC and GaN possess higher band gap energies as compared to the traditional Si material. With this knowledge, it is possible to use these materials for high temperature operations. However, the commercially available, and recently introduced by Efficient Power Conversion (EPC) in 2009, enhancement mode GaN MOSFET [45] offered a better performance as compared to the Si and SiC equivalents because of the following advantages [48].

1. **Conductivity:** Lower $R_{ds(on)} \times \text{Area}$, because of high electron mobility which allows for a higher current in a very small device package. The on state resistance, $R_{ds(on)}$ for a given switching device area is an important feature in the determination of the costs of the product. The theoretical limits of the $R_{ds(on)}$ for a given area can be given in terms of device breakdown voltages for Si, SiC and GaN devices and are illustrated in fig. 40.

2. **Higher switching speeds:** Due to the lateral device structure, the capacitances/area are very low compared to trench MOSFETs which results in very high switching speeds of transistors. Due to low capacitances, the device is capable of switching hundreds of voltages in very few nanoseconds and hence can be utilized for multi megahertz frequency converters. This is a desirable and crucial feature which leads to compact power supplies.

3. **Zero reverse recovery:** Because there are no minority carriers, no stored charge exists and hence no reverse recovery, ‘$Q_r$’ for these MOSFETs

4. **On state resistance ($R_{ds(on)}$):** Due to higher electron mobility and the higher band gap energy, $R_{ds(on)}$ of the GaN MOSFET was significantly reduced when compared to the Si and SiC devices
5. **Low temperature coefficient**: GaN MOSFETs consists of a much lower temperature coefficient as compared to Si MOSFETs which enables it to operate at higher temperatures with low $R_{ds(on)}$.

6. **High breakdown voltage**: From the table 6, it can be observed that the critical electric field strength of the GaN is higher as compared to the Si MOSFET which enables the GaN device to withstand higher breakdown voltages.

### 4.3 Evaluation of GaN and Si MOSFET in ZVS Flyback Converter Using Multilayered Coreless PCB Step Down Transformer

Because of the above discussed exceptional features of the GaN device, it was evaluated in a quasi resonant ZVS flyback converter operated in the MHz frequency region by using the multi-layered coreless PCB step down power transformer. These results were compared with the converter operated using the traditional Si MOSFET and discussed in the coming sections. In this case, the designed multi-layered coreless PCB transformer discussed in the previous chapter was utilized.

#### 4.3.1 Comparison of GaN and Si MOSFET parameters

For evaluating the performance of the GaN and Si MOSFETs in the ZVS flyback converter based upon the input and output voltage specifications, a 200V drain-source voltage capacity of GaN (EPC1012) and Si (IRFR220PBF) MOSFETs were
chosen. The physical dimensions of these MOSFETs are illustrated in fig. 41 with packages of land grid array (LGA 1.7x0.9 mm) and DPAK respectively.

![Figure 41. Dimensions of 200V Si (DPAK) –left and GaN (LGA) right enhancement mode MOSFET](image)

The continuous drain current ‘I’ of GaN/Si MOSFETs for ambient temperature are 3/4.8A respectively. The on-state resistance, \( R_{ds, on} \) of GaN/Si MOSFETs is 0.1/0.8Ω at their respective ‘\( V_G \)’ and ‘I’ conditions. The total gate charge ‘\( Q_G \)’ of GaN/Si is 1.9/14nC at ‘\( V_G \)’ of 5/10V respectively. The typical reverse recovery charge ‘\( Q_{rr} \)’ of the GaN device is zero as discussed previously, whereas for the Si MOSFET it is about 0.91nC. The reverse transfer capacitance of the GaN/Si is 7.5/30pF. This low transfer capacitance for the GaN device means that it possesses a fast voltage switching capacity as compared to the Si MOSFET because of the lower Miller effect. As discussed at an earlier stage, it is very important to choose the correct switching device especially in high frequency switching power converters. The reason is that a trade off exists between the on-state resistance ‘\( R_{ds, on} \)’ and the gate charge ‘\( Q_G \)’ of the switching element MOSFET and it is always beneficial to determine figure of merit (FOM) for the device before utilizing it in a converter circuit. FOM in terms of \( R_{ds, on} \) and ‘\( Q_G \)’ can be given as follows.

\[
FOM(V_G, V_{ds}) = R_{ds, on}(V_G, V_{ds}) \cdot Q_G(V_G, V_{ds})
\]  
(33)

The calculated FOM of the GaN/Si MOSFET is approximately 1.33/31.3
FOM of the GaN device is much lower than that of the Si device which has been calculated at their corresponding optimal operating regions and it shows that the GaN device is better compared to Si MOSFET in terms of the product of its on-state resistance and gate charge.

### 4.3.2 Experimental results of ZVS flyback converter using GaN and Si MOSFET

The ZVS flyback converter illustrated in fig.22 was tested with the following specifications using both the switching devices.
- **Input supply voltage range** \((V_{in})\): 30-60V with nominal voltage \((V_{in,nom})\) of 45V
- **Regulated output voltage** \((V_o)\): 15V
- **Load resistance range** \((R_L)\): 30-60Ω
- **Switching frequency range** \((f_{sw})\): 3 - 5MHz

In both cases, the resonant capacitor ‘\(C_R\)’ including the drain-source capacitance and the parasitic capacitance was found to be 80pF approximately. Since, the leakage inductance ‘\(L_{k}\)’ of the transformer is insufficient to reach the ZVS conditions of the converter, an external resonant PCB inductor of 5.2µH is added to the leakage inductance forming a resonant inductor ‘\(L_k\)’. In this way, the operating frequency of the converter was maintained within the desired frequency range by the resonant tank circuit elements ‘\(L_k\)’ and ‘\(C_R\)’ as discussed in previous chapter. The characteristic impedance ‘\(Z_{CH}\)’ and the resonant frequency ‘\(f_r\)’ of this circuit are calculated by using equations (23) and (24) and obtained as 284Ω and 8MHz respectively.

**Case (i):** Initially the energy efficiency of the unregulated converter was measured by using both devices and is illustrated in fig. 42

![Energy efficiency graph](image)

**Figure 42. Energy efficiency of ZVS flyback converter with GaN and Si MOSFETs**

In this case, the measured energy efficiency of the converter includes the gate drive power consumption. It is found to be 82.5/74.2% with the GaN/Si MOSFET at the nominal input voltage ‘\(V_{in,nom}\)’ of 45V. The output power of the converter at the maximum input voltage of 60V in both cases is approximately 12Watts. In this case, the duty cycle ratio of the converter was maintained as 50%.
**Case (ii):** The converter was regulated by using the constant off time frequency modulation technique as discussed in previous chapter and the energy efficiency was recorded. Here, the output voltage of the converter was regulated to 15Volts with ±1% tolerance band for input voltage variations over its entire range. The load resistance considered is of 30Ω. The corresponding energy efficiency of the converter is depicted in fig. 43.

**Case (iii):** The converter was also regulated to 15Volts by changing the load resistance from 30-60Ω at a $V_{in,\text{nom}}$ of 45V. The measured energy efficiency under these conditions is illustrated in fig. 44.

![Figure 43](image1.png) **Figure 43. Efficiency Comparison of Converters for $V_{in}$ Change**

![Figure 44](image2.png) **Figure 44. Efficiency Comparison of Converters for $R_L$ Change**

In this case for the converters operated with both switching devices, the ZVS conditions were maintained up to a certain load resistance and it ceases to follow after this limit. This condition was observed at the light load of 60Ω and the waveforms were captured for the converter operated with the GaN device and shown in fig. 45. This figure shows the nominal input voltage $V_{in,\text{nom}}$ fed to the converter, gate to source voltage $V_{gs}$, drain source voltage $V_{ds}$ of the MOSFET and the output voltage $V_o$ of the converter. In this case it can be observed that the converter has lost its ZVS properties.

In all three cases it can be observed that the energy efficiency of the ZVS flyback converter with the GaN MOSFET is always higher than that for the converter using the Si MOSFET. This can be explained by the following factors.
4.3.3 Gate drive Power consumption

The theoretical gate drive power consumption by the MOSFET driver [10] as given earlier is as follows.

\[ P_{\text{gate}} = V_g \cdot f_{sw} \cdot Q_g \]  \hspace{1cm} (34)

where,

\begin{itemize}
  \item \( V_g \) - Gate voltage
  \item \( f_{sw} \) - Switching Frequency of the MOSFET
  \item \( Q_g \) - Total gate charge of the MOSFET
\end{itemize}

While driving the Si MOSFET, a gate voltage of 10V was considered in order to have a low \( R_{d\text{.,on}} \) of MOSFET. For the GaN MOSFET, the gate voltage \( V_g \) was considered as being 5V, since this MOSFET becomes fully enhanced at this voltage. The theoretical and measured gate drive power consumed by both the devices is listed in table 7. Here, the power consumption of the driver was calculated and measured under the worst case condition i.e., at a maximum switching frequency of 5MHz and when the converter was fed with a 60V input voltage.
Table 7. Gate drive power consumption with GaN/Si MOSFET

<table>
<thead>
<tr>
<th>Device</th>
<th>Theoretical and Practical gate drive power consumption</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$V_{gs}$(V)</td>
<td>$Q_g$(nC)</td>
</tr>
<tr>
<td>GaN</td>
<td>5</td>
<td>1.9</td>
</tr>
<tr>
<td>Si</td>
<td>10</td>
<td>10</td>
</tr>
</tbody>
</table>

From table 7, it can be observed that the gate drive power consumed by the driver in the converter with the GaN was negligible as compared to that of the converter with the Si MOSFET. This gate drive power consumption has a great influence apart from the switching and conduction losses of the MOSFET, while determining the energy efficiency of the converter and can be observed from fig. 43. The static losses are higher in the converter with the Si MOSFET because of its $R_{ds, on}$ which is almost 8 times greater than that of the GaN MOSFET. From fig 43, it can be observed that the energy efficiency of the converter is maximum at $V_{in, nom}$ and it is reduced as the input voltage is reduced because of the conduction losses. At higher input voltages the energy efficiency is reduced because of the increased switching losses [11].

At a nominal input voltage of 45V, with a load resistance of 30Ω the converter was regulated to 15V with ±1V tolerance in both cases. The switching frequency of the converters in both cases was approximately 4MHz. The circuit was operated in ZVS conditions and the energy efficiencies with the GaN MOSFET and the Si MOSFET were found to be 82.5/74.2% respectively. The measured losses due to the gate power consumption, the conduction losses and the switching losses in both cases were estimated and are illustrated as a pie chart in fig. 46. This figure provides the percentage improvement for the energy efficiency of the converter in terms of the gate drive power, conduction and switching losses by using the GaN MOSFET over Si MOSFET.
In relation to the cost per unit for 100pcs, the GaN costs about 2.62$ whereas the Si MOSFET is only 0.95$. However, all the above exceptional features of the GaN MOSFET together with the multi-layered coreless PCB transformers provides the way to build a new generation of MHz frequency ultra-low profile power converters.

Figure 46. Pie chart representation of improvement with GaN MOSFET over Si MOSFET
5 CASCODE FLYBACK CONVERTER

In AC-DC and DC-DC converters such as laptop adapters, set-top-box and telecom applications the most commonly used switching device is the power MOSFET. Based upon the output power levels, the input voltage range and topology, the required drain source blocking voltages of these MOSFETs are in the range of 500-1000V. Generally, these MOSFETs consist of higher gate charges compared to low voltage rating MOSFETs. However, in order to achieve compact and high power density SMPS, as discussed previously, the switching frequency of the converter must be increased. If the switching frequency is increased, the power required to turn on the MOSFETs is also increased which in turn leads to a higher gate drive power consumption. In order to obtain the lower conduction/static losses, low on-state resistance is required for the power MOSFET. However a trade-off exists in the commercially available MOSFETs between the gate charge and the on-state resistance of the MOSFET according to FOM which was discussed in previous chapter. For example, if a high voltage MOSFET consisting of a low ‘\( Q_g \)’ is selected, it consists of high \( R_{ds,on} \) which leads to higher conduction losses. In order to reduce the conduction losses of these MOSFETs, either the die area should be increased or paralleling of the MOSFETs is required. In either case, the switching losses of the MOSFET are increased due to the increased gate capacitance which in turn increases the gate drive power and reduces the switching speed of the MOSFET. Therefore, it is necessary to look for an alternative solution to build a highly energy efficient, high frequency converter with low gate drive power consumption and without increasing the conduction and switching losses significantly. For high power applications, a cascode converter was composed of a single low voltage MOSFET and a high voltage BJT [49] since a high voltage MOSFET consists of a large on-state resistance. However, to attain a high speed converter, a MOSFET is the better option as compared to the BJT due to the stored charge effects. In this chapter, a cascode converter using a low voltage Si/GaN MOSFET with a high voltage Si MOSFET were compared with that of the single switch flyback converter. The benefits obtained by using a cascode converter especially with a GaN low voltage MOSFET have been discussed.

5.1 MULTILAYERED CORELESS PCB STEP DOWN 8:1 TRANSFORMER

It has been reported that multi-layered 2:1 coreless PCB step-down power transformers are highly energy efficient of about 90-97% in the MHz frequency
region [16] and can be used for DC-DC converter applications. Since, this provided the scope for increasing the step-down ratio of transformer, a transformer of approximately 8:1 which is of primary-secondary-secondary-primary (PSSP) structure for SMPS application was designed on a four layered FR4 PCB laminate. The two secondaries are connected in parallel in order to obtain the low resistance and the desired inductance for the secondary winding. These secondaries are sandwiched in between the two primaries which are connected in series in order to achieve better coupling between the primary and the secondary. In this case, the number of turns of the primary/secondary in each layer is 24/6 with a primary/secondary DC resistance \( R_p/R_s \) of the transformer as 2.71/0.08Ω. The electrical parameters of the transformer such as the self/leakage inductance of the primary and secondary are 29.38\( \mu \)H/1.9\( \mu \)H and 0.548\( \mu \)H/0.038\( \mu \)H respectively and these are obtained as described in section 3.2.2. The interwinding capacitance of the transformer is 125pF and the intrawinding capacitances of these transformers are considered as almost negligible as mentioned earlier. The coupling coefficient ‘K’ of this transformer obtained is 0.93. The designed multi-layered coreless PCB transformer utilized for both cascode and single switch flyback converter discussed in this chapter is shown in fig.47.

![Figure 47. Multi-layered coreless PCB step down 8:1 transformer](image)

This multi-layered coreless PCB transformer was utilized in both the cascode and single switch flyback converter and the performance of these converters was evaluated at higher switching frequencies.
5.2 **OPERATION OF CASCODE FLYBACK CONVERTER**

The circuit diagram of the cascode flyback converter is illustrated in fig. 48. In the case of the cascode flyback converter, a low voltage MOSFET ‘Q₁’ having low gate charge ‘Qₙ’ is connected in series with the high voltage MOSFET ‘Q₂’.

![Figure 48. Cascode converter using multilayered coreless PCB step down 8:1 power transformer](image)

In this case, the low voltage MOSFET ‘Q₁’ is driven directly from one of the output pins of the MOSFET gate driver, LM5111. A capacitor ‘C₁’ is placed across the drain source of the low voltage MOSFET ‘Q₁’ in order to limit the drain-source voltage of the low voltage MOSFET ‘Q₁’ within its maximum drain-source breakdown voltage ‘V₃ds,max’ and also gate-source voltage of the high voltage MOSFET ‘Q₂’ within its gate-source voltage limits. An external reservoir capacitor ‘C₂’ is placed across the gate of the high voltage MOSFET ‘Q₂’ and it is charged with the DC source.

The operation of the cascode converter [50], [51] using two MOSFETs can be explained in different modes as follows.

**Mode (i)-(V₃gs>V₁th & V₃gs>V₂th):** When the gate-source voltage of the low voltage MOSFET ‘Q₁’ i.e., V₃gs is greater than its gate threshold voltage, V₁th, the MOSFET ‘Q₁’ fully enhances and it is turned ON. As soon as the low voltage MOSFET ‘Q₁’ turns ON, because of the voltage across the capacitor ‘C₁’, across the gate-source of the high voltage MOSFET ‘Q₂’, it becomes turned ON. At this instant of time, the
cascode converter achieves its conduction state and hence the current starts flowing through the primary winding of the flyback transformer and the two switches (Q1 and Q2). In this state, the voltage drop across both MOSFETs is equal to their on-state voltage drops. Here, the flyback diode 'D' is reverse biased and therefore the filter capacitor, 'Cf' supplies the load current.

Mode (ii)-(Vgs1<Vth1): When the gate-source voltage 'Vgs' is less than its gate threshold voltage 'Vth', MOSFET 'Q1' is turned into the OFF condition. Since, the voltage across the MOSFET 'Q1' is constant, when the MOSFET 'Q1' is OFF, the current takes the path through the parallel capacitor across 'Q1' i.e., Ci and the gate-source capacitance of the high voltage MOSFET 'Q2'. Now the drain-source voltage 'Vds' across the low voltage MOSFET starts to increase. At this instant of time, the potential of the source terminal of the high voltage MOSFET 'Q2' starts to rise.

Mode (iii)-(Vgs<Vth2): As the potential of the source terminal of the high voltage MOSFET 'Q2' builds up, the gate-source voltage 'Vgs' of the high voltage MOSFET is reduced and when it reaches its gate threshold voltage 'Vth', the high voltage MOSFET 'Q2' is turned OFF. At this instant, the drain-source voltage 'Vds' of the high voltage MOSFET 'Q2' is raised. Under this condition, the current in both the switches now attempts to flow in the drain-source capacitance of the high voltage MOSFET 'Q2', the drain-source capacitance of low voltage MOSFET 'Q1', its parallel capacitor 'C1' and into the reservoir capacitor 'Cf'. To a small extent miller capacitance also shares this current.

Mode (iii)-(Vgs1<Vth1 & Vgs2<Vth2): When gate-source voltage of both switches 'Q1' and 'Q2' are less than their corresponding gate threshold voltages, these switches come into the turn OFF condition. In this case, the flyback diode 'D' comes into the ON state and the stored energy in the secondary winding is fed to the load resistance, RL.

Under ideal conditions, the gate-source / drain-source voltage of the high and low voltage MOSFETs in different modes of operation conditions are illustrated in fig. 49.

Because of the low gate charge of the low voltage MOSFET, 'Q1', the gate drive power consumption due to 'Q1' is considered to be negligible.
The DC current flowing in the gate of the high voltage MOSFET ‘Q’ is also negligible because of the equalization of the amount of charge entering and leaving the capacitor ‘C’ [52] during turn ON/OFF process respectively. The whole gate charge is thus charging/discharging the external capacitor and hence not wasted. In this way the drive power required to switch the high voltage MOSFET is almost zero and that of the low voltage MOSFET is negligible.

Figure 49. Timing Diagram of Cascode Flyback Converter

5.3 EXPERIMENTAL RESULTS OF CASCODE AND SINGLE SWITCH FLYBACK CONVERTER

Initially, the cascade and single switch flyback converters were simulated with the assistance of SIMetrix simulation software. Since soft switching techniques enable the high frequency operation, highly energy efficient, compact and light weight converters, [49], [53], [54], both the cascode and single switch flyback converters were maintained to operate under ZVS conditions as done in chapter 3. Based upon simulation results the prototype was designed and then tested with the following specifications:

- Input Voltage range 60-120V, nominal voltage: 90V
- Switching Frequency range: 2.6 - 3.7 MHz
- Full load resistance: 10 Ω
In the cascode flyback converter, the low voltage MOSFETs ‘Q1’ considered are 1) Si MOSFET ZXMN15A27K and 2) GaN MOSFET EPC1013 and the high voltage MOSFET ‘Q2’ considered is Si MOSFET STP3NK60ZFP and their corresponding characteristics are listed in table 8. The secondary side diode is of Si Schottky SR1660 with reverse blocking voltage capacity of 60V and a forward current rating of 16A.

<table>
<thead>
<tr>
<th>S.No</th>
<th>MOSFET (Material)</th>
<th>Vds_max (V)</th>
<th>Id (A)</th>
<th>Rds_on (Ω)</th>
<th>Qg (nC)</th>
<th>Coss (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>ZXMN15A27K (Si)</td>
<td>150</td>
<td>2.4</td>
<td>0.65</td>
<td>6.6</td>
<td>64.5</td>
</tr>
<tr>
<td>2</td>
<td>EPC1013 (GaN)</td>
<td>150</td>
<td>3.0</td>
<td>0.1</td>
<td>1.7</td>
<td>85</td>
</tr>
<tr>
<td>3</td>
<td>STP3NK60ZFP (Si)</td>
<td>600</td>
<td>2.4</td>
<td>3.3</td>
<td>11.8</td>
<td>43</td>
</tr>
</tbody>
</table>

In the case of the flyback converter, the Si high voltage MOSFET STP3NK60ZFP is considered for comparison with the cascode flyback converter. The following tests were carried out for the converter prototype by using the multi-layered coreless PCB step-down transformers and the three cases are listed as follows.

**Case (i):** Cascode converter with ‘Q1’ as Si LV MOSFET: ZXMN15A27K and ‘Q2’ as Si HV MOSFET: STP3NK60ZFP

**Case (ii):** Cascode converter with ‘Q1’ as GaN MOSFET: EPC1013 and ‘Q2’ as Si HV MOSFET: STP3NK60ZFP

**Case (iii):** Flyback converter with ‘Q1’ as Si HV MOSFET: STP3NK60ZFP

In the first two cases, the high voltage MOSFET ‘Q2’ is driven with a supply voltage of 12V dc with a capacitor of 10µF. The duty cycle of the converter was maintained to be 50%. The simulated and measured energy efficiency of the converter in all the three cases is illustrated in fig. 50 including the gate drive power consumption. This figure shows that the simulated and measured energy efficiency of the converters is in good agreement with each other. From fig. 50 it can be also observed that the maximum energy efficiency of the converter is achieved in the case of the cascode converter with the GaN MOSFET followed by the cascode converter with the Si MOSFET. At a nominal voltage of 90V, the energy efficiency of the cascode converter with the GaN/Si MOSFETs is 80.4%/79.5% respectively.
and for the single switch flyback converter it is only 76.4%. This can be explained due to the improved gate drive power consumption and the fast rise / fall times of the lower voltage MOSFET ‘Q1’ in the cascode flyback converter. From fig. 50 it can be observed that the energy efficiency of the single switch flyback converter is drastically reduced at low input voltages due to the gate drive power consumption compared to that for the cascode converter. The measured gate drive power consumption in case (i) is 0.28W, in case (ii) is 0.05W and in case (iii) it is 0.6W. This shows that the gate drive power consumption in the cascode flyback converter using the GaN MOSFET is negligible because of the low ‘Qg’.

In the cascode converter, because of two MOSFETs, the static /conduction loss is increased which is dependent on the $R_{ds, on}$ of MOSFETs. Therefore, the conduction losses of the MOSFETs in the single switch flyback converter and the cascode converter were measured at a given power and with nominal input voltage. The measured conduction loss in case (i) is 0.133 W, in case (ii) it is 0.118 W whereas in case (iii) it is only 0.115 W. From the measured gate drive power consumption and the conduction losses in all the three cases, it can be observed that the gate drive power consumption is the dominant factor as compared to the conduction losses of the MOSFETs. Even though the low $R_{ds, on}$ MOSFET is placed in a single switch flyback converter, the gate charge of the MOSFET is increased according to figure of merit which was discussed in previous chapter for the given power application which increases the gate drive power consumption with lower conduction losses. Therefore, the gate drive power, which is a function of the frequency finds its

![Figure 50. Simulated (Solid) and Measured (Symbol) Energy efficiency of cascode and single switch flyback](image)
advantages in high frequency SMPS with a cascode topology particularly in low power and light load conditions as compared to the single switch flyback converter. In cases (i) and (ii), at higher input voltages, no significant improvement exists in terms of energy efficiency. However, at lower input voltages, the energy efficiency in case (i) is increased because of the gate drive power consumption as discussed previously. Also, in terms of size, a significant improvement exists in case (ii) as compared to case (i) where ZXMN15A27K is of DPAK and EPC1013 is a land grid array (LGA 1.7x0.9mm) package as was discussed earlier. The GaN MOSFET utilized in the cascode converter costs about 2.42$/unit whereas for the ZXMN15A27K it is only about 0.57$/unit. But these exceptional features such as low conduction loss and low gate drive power consumption can only be obtained by utilizing a GaN MOSFET together with a coreless PCB step down power transformer which is beneficial for the future generation ultra low profile converters. The maximum switching frequency of the cascode converter at $V_{in}$ of 120V with a GaN/Si as its low voltage MOSFET was found to be 3.65/3.64MHz respectively whereas in the case of the single switch flyback converter it is only 2.88MHz. This represents the fact that it is possible to achieve higher switching speeds using the cascode converter as compared to the single switch flyback converter.

The maximum load power attained in all three cases is approximately 30Watts and the load power profile with respect to input voltage variation is illustrated in fig. 51.

![Load Power Profile](image)

---

Figure 51. Measured load power of cascode and single switch flyback converter

Fig. 51 shows that all the measurements and comparisons were made at approximately the same power levels in all three cases for varied input voltages. At a nominal input voltage, the output voltage of the converter in all cases is
approximately 13V and this can be regulated to 12V for wide input voltage & load variation using a constant off time frequency modulation technique discussed in chapter 3.

At an input voltage of 70V, the simulated waveforms of the cascode flyback converter with the Si MOSFET at a load resistance of 10Ω i.e., case (i) are illustrated in fig. 52. The figure shows the output voltage of the converter \( V_o \), gate-source voltage fed to the MOSFET \( Q_1 \) (\( V_{gs} \)), drain-source voltages \( V_{ds,max} \) of both MOSFETS \( Q_1 \) & \( Q_2 \) and the voltage across shunt resistor \( R_sh \) i.e., \( V_{sh} \).

![Simulated waveforms of Cascode converter, case (i) with RL=10Ω](image)

**Figure 52.** Simulated waveforms of Cascode converter, case (i) with \( RL=10\Omega \), top-bottom: Output Voltage \( V_o \), Gate voltage \( V_{gs} \), Drain Voltage of \( Q_1 \) \( V_{ds,max,Q1} \), Drain Voltage of \( Q_2 \) \( V_{ds,max,Q2} \), Shunt voltage \( V_{sh} \).

Under the same conditions, the measured waveforms were captured from oscilloscope and are shown in fig. 53.

![Measured waveforms with RL=10Ω](image)

**Figure 53.** Measured waveforms with \( RL=10\Omega \). CH1 - \( V_{gs} \) (10V/div), CH2 - \( V_{ds} \) (100mV/div), CH3 - (Q1) \( V_{ds} \) (20V/div), CH4 - (Q2) \( V_{ds} \) (50V/div)
In fig. 53, CH1-CH4 shows the gate to source voltage ($V_{gs}$) applied to the switch $Q_1$, voltage across the shunt resistor $R_s$ of 0.33Ω, drain to source voltage ($V_{ds}$) of low voltage switch $Q_1$ and drain to source voltage ($V_{ds}$) of high voltage switch $Q_2$ of the converter circuit. It can be observed from fig. 53, that the MOSFETs are operated in almost zero voltage switching conditions.

The stress on the high side MOSFETs in the cascode converter and the single switch converter with the input voltage variation are depicted in fig. 54. In addition to the above mentioned advantages of the high speed cascode converter, the stress on the high voltage MOSFET $Q_2$ becomes reduced as compared to that for the single switch flyback converter.

![Figure 54](image)

Figure 54. Measured drain-source voltage of the HV MOSFETs with the input voltage variation

From fig. 53 and fig. 54, at an input voltage of 70V the stress on the high voltage MOSFET is reduced by approximately 22V in the cascode converter as compared to that for the single switch flyback converter.

### 5.4 LOSS ESTIMATION OF CASCODE CONVERTER

The loss estimation of cascode converter utilising low/high voltage Si MOSFETs was made under the nominal input voltage and full load conditions. Under these conditions, the input/output power of the converter is 21.1/16.8W respectively with a total power loss of about 4.3W. At this instant, the switching frequency of the converter is 3.45MHz.
Transformer Losses: The measured mean/rms currents flowing through the primary are 0.235/0.252 A. The rms current flowing through the secondary winding of the flyback transformer is 1.7 A. The AC resistance of the primary/secondary are 9.77Ω/0.310Ω and the copper losses of the transformer [51] which can be given by the following equation are 0.62/0.89W respectively.

\[
P_{\text{loss}} = \left( i_p^2 \cdot R_{\text{ac}(p)} + i_s^2 \cdot R_{\text{ac}(s)} \right)
\]

where,

- \(i_p/ i_s\) - RMS currents through primary/secondary winding
- \(R_{\text{ac}(p)}/ R_{\text{ac}(s)}\) - Primary/secondary winding ac resistance

MOSFET Losses: A MOSFET loss consists of both the conduction and the switching losses [20]. The average conduction losses [55] of low/high voltage MOSFET whose \(R_{\text{ds,on}}\) is 0.65/3.3 are 0.017/0.088W respectively which can be computed by the equation (36) as follows.

\[
P_{\text{c.avg}} = I_{\text{mean}}^2 \cdot R_{\text{ds,on}} \cdot D
\]

where,

- \(I_{\text{mean}}\) - mean current flowing through the switch
- \(R_{\text{ds,on}}\) - on state resistance of MOSFET
- \(D\) - Duty cycle ratio

Since, the converter was not fully operated under ZVS conditions, it experiences some of the turn on losses. The turn on loss of the MOSFET [56] can be estimated as follows.

\[
P_{\text{sw}} = \frac{1}{2} \cdot \left( T_{\text{sw.on}} + T_{\text{sw.off}} \right) \cdot V_{\text{ds}} \cdot I_d \cdot f_{\text{sw}}
\]

where

- \(T_{\text{sw.on}}\) - turn on switch transition time
- \(T_{\text{sw.off}}\) - turn off switch transition time
- \(V_{\text{ds}}\) - drain source voltage
- \(I_d\) - current though MOSFET
- \(f_{\text{sw}}\) - switching frequency
Under the above mentioned conditions, the estimated turn on losses of the low voltage/high voltage MOSFET using the above equation are 0.439/0.604W whereas turn off losses are considered to be negligible.

**C) MOSFET driver loss:** The power consumption of the gate driver was estimated by using equation (34). The calculated/measured MOSFET driver loss is found to be 0.27/0.28W.

**D) Diode Losses:** The flyback diode conduction loss [55] obtained by using the following equation loss is 0.388W.

\[
P_{\text{diode}} = V_f \cdot I_{D\text{-avg}} \cdot (1 - D)
\]  

where,
- \( V_f \) - Diode forward voltage drop
- \( I_{D\text{-avg}} \) - average current flowing through flyback diode

**E) Miscellaneous losses:** It consists of ‘\( C_{on} \)’ loss of MOSFETs which can be computed by equation (22), switching losses of the secondary rectifier diode and the remaining circuit losses.

These computed losses are illustrated as a pie diagram in fig. 55.

![Pie Chart](image)

**Figure 55. Loss estimation of cascode converter [51]**
Under these conditions, the temperature profile of the cascode converter circuit including the transformer, low / high voltage MOSFETs, driver and flyback diode are illustrated in fig.56.

![Thermal profile of Cascode flyback converter](image)

**Figure 56. Thermal profile of Cascode flyback converter**

Area of the Switch STP3NK60ZFP (Q2), Ar2 - Area of the Transformer, Ar3 - Area of the Switch ZXMN15A27K (Q1), Ar4 - Area of the schottky diode SR1660, Ar5 – MOSFET Driver LM5111

The loss contributed by the multi-layered coreless PCB transformer is around 36% of the total loss. With the proper design of this coreless PCB transformer i.e., by reducing the primary resistance, also by maintaining the exact ZVS conditions a highly energy efficient, low profile cascode flyback converter can be achieved.
6 GATE DRIVE CIRCUITRY FOR HIGH SPEED DOUBLE ENDED TOPOLOGIES

In all the above chapters, the discussions have involved single ended topologies such as the single switch flyback and cascode flyback converters operating in the MHz frequency.

In the cascode and single switch flyback converter, it can be observed that the peak voltage stress on the semiconductor devices is high for the given input/output voltage and the transformer operating in the ZVS conditions. For example in the cascode flyback converter, the stress on the HV MOSFET is about 480V for an input voltage of 120V which is operated in the MHz frequency region. If this is the case, a MOSFET rating of approximately greater than 1kV is required for the universal input voltage range of 85-265VAC. If a double ended topology such as, half bridge or series resonant converters are chosen the stress of one MOSFET can be shared by two MOSFETs. Also, for a given power transfer application, the size of the transformers can be reduced in double ended topologies due to the full utilization of the winding area as compared to that for single ended topologies [57]. However, in order to drive the high side MOSFET at higher input voltages (125V) and frequencies (>1MHz) to the author’s knowledge there exists no commercially available MOSFET drivers [58]. Therefore, it is necessary to design individual gate drive circuitry for operating the converters at higher frequencies. For this purpose, multi-layered gate drive transformers to reduce the transformer area, reduced winding resistance, and to reduce the EMI emissions [42] as compared to the two layered transformers have been designed in Mid Sweden University. In this chapter, the design of gate drive circuitry and its application in double ended topologies have been discussed.

6.1 GATE DRIVE CIRCUIT DESIGN USING MULTILAYERED CORELESS TRANSFORMER

Floating gate drive circuitry is required in all the double ended topologies such as half-bridge, full-bridge and resonant converters to drive high side MOSFET. For this purpose, either a gate drive transformer or an optocoupler can be utilised. In this case, the function of using a gate drive transformer/optocoupler is to transfer the ground referenced signals across the high potential differences in order to drive the floating ground gate of the MOSFET. However, the traditional
optocouplers are very slow and the high speed digital optocouplers are quite expensive. Therefore, an alternative solution is to use transformer isolated gate drive circuitry. The high side gate drive circuitry together with the high frequency model of multi-layered coreless PCB transformer is illustrated in fig. 57. The transformer structure is of primary-secondary-secondary-primary (PSSP) with an outermost diameter of 10mm. The high frequency material NiZn ferrite is used on both sides for achieving higher inductance as well as for reducing the magnetizing current which leads to low gate drive power consumption. Here, the driver output is coupled to the transformer with the help of a DC blocking capacitor ‘C’.

![Diagram](image)

Figure 57. High side gate drive circuitry using multilayered coreless PCB gate drive transformer

The secondary side of the transformer is connected to a level shifter using a capacitor ‘C1’ and the zener diode ‘D1’. Here the zener diode also utilized for transient protection. Whenever the secondary side capacitor is used, the core becomes saturated when the MOSFET is in the turn-off condition [59]. This situation leads to a malfunction of the MOSFET due to the saturation of the core material [60]. Here, a large air gapped NiZn ferrite core material is also used for evaluation purpose. After the level shifter, a series resistor ‘R1’ is used in order to reduce EMI [59], [61] due to fast turn-on/turn-off, the noise of the PWM controller, clock jitter etc., Since, the gate drive circuitry is designed for a MOSFET load which is capacitive in nature, a parallel combination of large value of resistor ‘R5’ and capacitor ‘C3’ is considered as the load.

The simulated waveforms of this drive circuit for duty cycle ratios of 20% and 50% are depicted in figs. 58 and 59.
Figures 58 and 59 illustrate the driver output ‘\(V_{\text{driver}}\)', primary/secondary signals of gate drive transformer ‘\(V_{\text{pri}}/V_{\text{sec}}\)' and the gate signal ‘\(V_{\text{gate}}\)’ fed to MOSFET load.

![Figure 58. Drive signals of high side MOSFET using coreless PCB transformer for duty cycle ratio of 20%](image)

![Figure 59. Drive signals of high side MOSFET using coreless PCB transformer for duty cycle ratio of 50%](image)
6.2 Experimental Setup of Gate Drive Circuit

The designed gate drive circuitry was tested in half-bridge [62] and also in series resonant converter topologies. The series resonant converter including the gate drive circuitry is shown in fig. 60.

![Series Resonant Converter](image)

Figure 60. Series Resonant Converter using coreless PCB gate drive and power transformer

The low side MOSFET is directly driven from one of the out pins of LM5111 MOSFET gate driver. The high side MOSFET is driven by using a gate drive transformer and a few gate drive elements in between the MOSFET driver and the gate of the HV MOSFET as discussed previously. The MOSFETs utilized in this circuit are ZXMN15A27Ks whose breakdown voltage is of 200V. A multi-layered coreless PCB power transformer of 4:1 step-down ratio whose outermost diameter is 20mm is utilized. The gate drive signals fed to the LV and HV MOSFETs are depicted in fig. 61.

![Gate Drive Signals](image)

Figure 61. Measured gate drive signals of LV/HV MOSFETs in Series Resonant Converter
From figure 61, it can be observed that the rise/fall times of the LV and HV MOSFETs are 12.5/12.5ns and 18/20.3ns respectively.

6.3 Gate Drive Power Consumption

The block diagram representation of a practical gate drive circuit from a DC input voltage \( V_{in} \) is represented in fig. 62. A buck regulator which steps down the voltage from 12V to 3.3V is chosen to drive the dsPIC micro-controller dsPIC33FJ16GS502. The driver is fed directly from the supply voltage which is of 12V DC. One of the outputs is directly fed to the LV MOSFET and the other is via the gate drive transformer as discussed in the previous section.

![Figure 62. Block diagram of gate drive circuitry](image)

The total power consumption of the gate drive circuit is measured and illustrated in fig. 63. This figure gives the power consumption of the total circuit \( P_{\text{total}} \), the power consumption of the switching regulator, \( P_{\text{sw}} \), the MOSFET gate driver power given as \( P_{\text{driver}} \) and also the microcontroller loss represented as \( P_{\text{ctrl}} \).
By using the above gate drive circuitry the half bridge converter circuit as well as series resonant converter were successfully tested in the MHz frequency region. The maximum energy efficiency reported in high frequency half bridge converter is approximately with the maximum load power of 40W. The energy efficiency in case of series resonant converter is 86.5% with the maximum load power of 34.5W. The energy efficiency of the series resonant converter for one of the load conditions is illustrated in fig. 64.

Figure 63. Gate drive power consumption in Series Resonant Converter

Figure 64. Energy Efficiency of Series Resonant Converter
7 PAPERS SUMMARY

7.1 PAPER I

In this paper, a multi-layered coreless PCB transformer is utilized for building a high speed SMPS. The analytical and experimental analysis of zero voltage switching converters is discussed. Comparative results of hard switched and soft switched converters in the MHz frequency region are presented. Both the converters are operated within the voltage range of 25-40V and up to the output power level of 10W in the frequency range of 2.7-4.3MHz. Here, the converter was regulated to 13V from 25-40V with the help of a constant-off time frequency modulation technique. In this paper, the feasibility of operating the converters in the MHz frequency region for power transfer applications with multi-layered coreless PCB step-down transformers having high energy efficiency are analysed and discussed.

7.2 PAPER II

This paper provides the comparative results of the ZVS flyback regulated converter using two different material (Si and GaN) MOSFETs. The converter was regulated from 45V input voltage to 15V output, by using the frequency modulation technique. Here, the converter was also operated at the higher frequency range of 3.2-5MHz with increased power levels of up to 12Watts. The importance of choosing a proper MOSFET in high frequency converter circuits was discussed in terms of their gate charge and the on-state resistance. An energy efficiency improvement of 8-10% was achieved including the gate drive power consumption by using a GaN device compared to a Si MOSFET. This paper shows that it is possible to design ultra-low profile converters by utilising the GaN MOSFETs and the multi-layered coreless PCB step-down power transformers.

7.3 PAPER III

In this paper, the importance of a cascode flyback converter as compared to a single switch flyback converter was discussed. Here, a higher step-down ratio of 8:1 multi-layered coreless PCB power transformer is introduced which was of primary-secondary-secondary-primary structure. The design and analysis of the cascode converter with the help of simulation and experiments was presented. The converter was operated with the input voltage range of 60-120V and at switching
frequencies of 2.6-3.7MHz was demonstrated. A cascode flyback converter using GaN and Si MOSFETs was compared to that of the single switch flyback converter in terms of energy efficiency, switching frequency, gate drive power consumption and voltage stress. This paper proves that the energy efficiency of the cascode flyback converter is better as compared to that of the single switch flyback converter with increased switching speeds for the given power transfer application.

7.4  PAPER IV

In this paper, a set of multi-layered coreless PCB step-down 2:1 power transformers operating in the MHz switching frequency was introduced. The modelling of these transformers using a high frequency model and hence the procedure for obtaining the parameters of transformers was discussed. The characterization of these transformers with both sinusoidal and square wave excitations was presented. The comparative results of these transformers in terms of self, leakage, mutual inductances, resistances and energy efficiencies were reported. These transformers were tested up to the output power levels of about 30W and it was found that the energy efficiency is in the range of 90-97% in MHz frequency range. This paper shows the possibility of utilizing the step-down transformers for power transfer applications with higher energy efficiencies.

7.5  PAPER V

In this paper, a high speed half bridge converter circuit using multi-layered coreless PCB gate drive and power transformer was demonstrated. Due to the limitations imposed by the commercially available high side MOSFET gate drivers in terms of voltage and frequency, a low power consumption passive gate drive circuitry was built up using multi-layered coreless PCB gate drive transformer to drive the high side MOSFET of a half bridge converter circuit. Here, a step-down power transformer of 4:1 turn ratio which is of 22mm diameter is utilized. The energy efficiency of this multi-layered coreless PCB step-down centre tapped transformer is found to be greater than 92%. The converter was tested within the frequency range of 2-3MHz with the maximum DC input voltage of 170V. The maximum energy efficiency of the unregulated converter is found to be 82% with maximum load power of 40W.
7.6 AUTHORS CONTRIBUTIONS

The exact contributions of the authors of five papers in this thesis are summarized in table 9. In this, table M and C represents main author and co-author respectively.

Table 9. Authors’ Contributions

<table>
<thead>
<tr>
<th>Paper #</th>
<th>HK</th>
<th>RA</th>
<th>KB</th>
<th>AM</th>
<th>Contributions</th>
</tr>
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<tbody>
<tr>
<td>I</td>
<td>M</td>
<td>C</td>
<td>C</td>
<td>-</td>
<td>HK: Estimation of transformer parameters for flyback converter, Implementation of flyback topology, experimental and theoretical analysis of hard switching and soft switching of converter, Loss estimation of converter RA: Transformer design, parameter extraction and analysis of transformer in converter circuit KB: Review of paper and Supervision</td>
</tr>
<tr>
<td>II</td>
<td>M</td>
<td>C</td>
<td>C</td>
<td>-</td>
<td>HK: Idea, implementation and analyzing the Converter results using two different MOSFETs (Si and GaN) RA: Transformer design, analysis of transformer in converter circuit KB: Review of paper and Supervision</td>
</tr>
<tr>
<td>III</td>
<td>M</td>
<td>C</td>
<td>C</td>
<td>-</td>
<td>HK: Idea and implementation of using GaN switch for low side MOSFET in Cascode flyback converter both in simulation and experiment RA: Transformer design, Modelling, analyses of transformer operation in Converter KB: Review of paper and Supervision</td>
</tr>
<tr>
<td>IV</td>
<td>C</td>
<td>M</td>
<td>C</td>
<td>-</td>
<td>HK: Modelling, Analysis and discussion on application potentials RA: Estimation of inductive, resistive and capacitive parameters using MATLAB code, Design and modelling of transformers, Power tests of transformers KB: Review of paper and Supervision</td>
</tr>
<tr>
<td>V</td>
<td>C</td>
<td>C</td>
<td>C</td>
<td>M</td>
<td>HK: Design of gate drive circuitry, discussion and review of paper RA: Power and Signal transformer design, secondary inductor design, parameter extraction KB: Review of paper and Supervision MA: Implementation and experiments of Half bridge Converter</td>
</tr>
</tbody>
</table>

1. Hari Babu Kotte (HK)  
2. Radhika Ambatipudi (RA)  
3. Kent Bertilsson (KB)  
4. Abdul Majid
8 THESIS SUMMARY AND CONCLUSIONS

The overall thesis is summarized as follows.

Chapter 1: In this chapter, the advantages and limitations of linear power supplies are discussed. The need for the introduction of switch mode power supply is presented. The various advantages of increasing the switching frequency of converter are also discussed. The challenges to be faced in high frequency converters in both magnetics and semiconductor areas are also presented. The possibilities of overcoming these limitations are given. The objective, method for achieving high frequency converters including outline of the thesis are given at the end of this chapter.

Chapter 2: This chapter introduces the necessity of the gate drivers for driving the power MOSFETs utilized in SMPS. It gives a brief idea of a switching model of a MOSFET and describes various modes of operation during turn-on and turn-off operation of a power MOSFET along with a gate driver which signifies the importance of parasitic elements. The importance of the gate drive power consumption in switching converters is described and also various types of gate drive losses caused by total gate charge, quiescent currents and output voltage transitions were introduced. Different commercially available MOSFET drivers were compared in terms of their rise/fall times and gate drive power consumption both analytically and practically.

Chapter 3: In this chapter a brief introduction to a flyback converter and their different modes of operation were discussed. The design guideline of a flyback transformer in continuous and discontinuous mode of operation for coreless PCB transformer was also presented. The amount of required inductance for the flyback transformer with respect to frequency was estimated in both the DCM and CCM modes of operation. An introduction to multi-layered coreless PCB transformer, its geometrical, electrical parameters and its energy efficiency was discussed. A hard switched flyback converter, the problems corresponding to it and the solutions to those problems were discussed briefly. Different types of soft switched flyback converters such as ZVS and ZCS, the operation and condition for ZVS in quasi resonant flyback converters were presented. The modelling of a MOSFET and the analysis of a converter using a coreless PCB transformer using simulation software
was presented. Finally, the experimental results of the ZVS flyback converter for a power level up to 10W and the associated waveforms were illustrated. The losses of the multi-layered coreless PCB transformer in a converter using analytical equations and thermal images were also estimated and shown. The radiated power losses of transformers and their causes were discussed. The estimated radiated power loss shows that the amount of EMI radiated from multi-layered coreless PCB transformers is negligible.

Chapter 4: This chapter introduces the importance of power MOSFETs in modern high frequency switch mode power supplies and the limitations of Si material for these applications. The need for the new semiconductor materials for the latest power management developments was discussed. Also a brief idea about the new semiconductor materials and their important features utilised for power MOSFETs were presented. The advantages of GaN material MOSFETs were discussed compared to its counterpart Si MOSFET. A comparison of GaN and Si MOSFETs parameters utilised for ZVS flyback converters operating in the MHz frequency region were examined. A figure of merit in terms of conduction loss and gate drive power consumption was also calculated for both devices and presented. The experimental results of the converter with GaN and Si MOSFETs was carried out and it was found out that for the same output power, the energy efficiency with the GaN MOSFET was increased by 8-10% as compared to the Si MOSFET. In the case of the converter with the GaN MOSFET, the gate drive power consumption is approximately reduced by a factor of 10 as compared to that for the Si MOSFET converter operating at 5MHz. The percentage improvement of the energy efficiency in terms of the gate drive power consumption, switching and conduction losses with the GaN MOSFET as compared to the Si MOSFET was illustrated in a pie diagram.

Chapter 5: In this chapter, initially the significance for implementing the cascode converter using two MOSFETs in high speed SMPS is discussed. The electrical parameters of multi-layered coreless PCB step-down 8:1 power transformer utilized in the converter circuit are discussed. The operating principle of the cascode converter with a low voltage (GaN/Si) and a high voltage (Si) MOSFET in different modes of operation is presented. Simulation and experimental results of the cascode flyback converter in one of the cases is demonstrated. The energy efficiency improvement in the cascode converter with the low voltage GaN MOSFET as compared to that for the single flyback converter is obtained due to the
improvement in gate drive power consumption, high rise/fall times and lower stress on high voltage MOSFET. Detailed loss estimation of the cascode converter in terms of switching/conduction losses of MOSFET, transformer losses, diode conduction losses etc., is presented. The comparison of the cascode converter with a single switch flyback converter shows that there is a significant improvement in the energy efficiency and higher switching speeds with the help of the cascode converter for the given power.

Chapter 6: This chapter gives a brief introduction to the requirement of gate drive transformer design for high speed SMPS. Different possibilities of building floating gate drive circuitry are described. The gate drive circuitry including multi-layered coreless PCB transformer was simulated for different duty cycle ratios. The application of the designed gate drive circuit was implemented in double ended topologies and described. The measured gate drive signals and its power consumption over the frequency range are shown. The maximum energy efficiency of the series resonant converter driven by the designed gate drive circuitry is found to be 86.5% with a load power of 34.5W. The MOSFET driver consumes the power of less than 0.8W within the frequency range of 1.5-3.5MHz.

8.1 Future Work

From the work presented in this thesis, it can be concluded that it is feasible to design the high frequency low profile converters utilizing multilayered coreless PCB step-down power transformers. With respect to EMI point of view, utilization of transformer and also energy efficiency these resonant converters are best suited compared to other topologies. Further this work can be extended with the assistance of GaN devices and synchronous rectification to achieve the best energy efficiency and high power density converters. The designed converters were regulated for both line and load changes by using open loop control. However, for the commercialization of these converters, the research should be focussed on implementing the closed loop control of these high frequency converters.
9 REFERENCE


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