Abstract
This project consists of designing a class D amplifier and selecting a proper speaker to use with it. Focus lies on high soundpressure, low powerconsumption and a wide operating temperature range. The current version of the amplifier uses a self-oscillating modulator, a full-bridge power stage and a second order passive low-pass Butterworth filter. Project specifications were not met with the current setup, but suggested improvements can be found in the report.
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1 Introduction
In many parts of the electronics industry the trend leans towards smaller, more mobile and more energy efficient products, whether it may involve making a TV thinner, or extending the battery-life on a laptop. The same goes for the electronics used in audio applications. MP3-players need better audio quality and higher output power while maintaining a small size. Outdoor sound systems need to be playing music at longer distances without using extremely large amplifiers. All this, while still keeping power consumption at a minimum level. This is where the class D audio amplifier comes in.

The class D audio amplifier uses a switching technique that results in a much higher efficiency than traditional amplifier topologies. With higher efficiency, less power is converted to heat and thus the size of the cooling unit can be greatly reduced or removed completely. The high efficiency also makes the class D audio amplifier very suitable for battery powered solutions, greatly extending the runtime on a single charge.

These features open up endless possibilities for the class D audio amplifier, often providing a more energy efficient and practical solution than traditional audio amplifiers.

1.1 Project Specifications
This project consists of two parts; Designing and constructing a class D amplifier and selecting a proper speaker to use with it. Project specifications as given by the company Salvator HB is presented in table 1.

The major thing to have in mind when designing the class D audio amplifier for this project is that this amplifier is not intended for applications where high quality audio is needed. The main reason for that are the types of speakers that will be used. The horn-speakers used in these applications are capable of producing sound at very high pressure but has a narrow frequency response. That means that they can only produce audio at a small range of frequencies.

The other major concern is that the amplifier is intended to run on batteries, therefore power consumption needs to be low. The idea was to use only one battery, but with the possibility of adding one extra if necessary. The second battery however is in use by another
circuit which leaves dual supply as a last resort. One important notice is that the amplifier should be able to operate for at least 60 minutes at full power. In this case it means that sound is being played for a few seconds at a time, with several minutes of silence between each interval.

Another important notice is the audio quality mentioned in table 1. “Audible difference” is a somewhat vague specification. It was therefore decided that the sound-pressure at a distance of 200 meters from the speaker should be equal to that of a normal conversation, approximately 60dB\(^1\).

Finally, as the title states, the amplifier should be able to operate in rough environments. This basically comes down to the temperature range the amplifier should be able to operate in, as casing and weather-protection was not part of the project specifications. The amplifier should be able to operate in temperatures ranging from -30 to +30 degrees Celsius (Swedish climate).

<table>
<thead>
<tr>
<th>Specifikation</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output power, soundpressure</td>
<td>Approx. 60 Watts, 60dB @ 200 meters</td>
</tr>
<tr>
<td>Minimum runtime</td>
<td>Approx. 60 minutes @ full power</td>
</tr>
<tr>
<td>Powersupply</td>
<td>One battery; 12V, 5Ah</td>
</tr>
<tr>
<td>Audioquality</td>
<td>Audible difference between gunshot and explosion @ 200 meters from speaker, mono audio</td>
</tr>
<tr>
<td>Connectors and levers</td>
<td>RCA and 3.5mm input connectors, volumeknob</td>
</tr>
<tr>
<td>Temperature range (°C)</td>
<td>-30 - +30</td>
</tr>
<tr>
<td>Speaker</td>
<td>Horn, 6-8Ω, IP65-classified</td>
</tr>
</tbody>
</table>

Table 1: Project specifications

\(^1\) [http://www.physicsclassroom.com/class/sound/u11j2b.cfm](http://www.physicsclassroom.com/class/sound/u11j2b.cfm), 2011-02-03
1.2 Report Organization
This report follows the progress of each step made throughout the project. Chapter 2 gives the reader a bit of background on the subject of amplifiers in general and class D amplifiers in particular. Chapter 3 describes the process of designing and constructing the preliminary design and chapter 4 discusses some of the results from testing the preliminary design, as well as improvements that will be made. Chapter 5 shows the construction of the second revision of the amplifier while chapter 6 discusses further testing of both the amplifier and the selected speaker. Finally chapter 7 sums up all the conclusions made in the project and chapter 8 discusses further improvements needed.
2 Background

2.1 Common Power Amplifier Classes
The basic idea of an amplifier is that it receives a signal from some kind of input source and provides a larger version of that signal to either another amplifier stage or some output device. While the properties of small-signal amplifiers usually consists of amplification linearity and magnitude of gain, large-signal amplifiers or power amplifiers main features are the circuit’s power efficiency and the impedance matching to the output device.

Below follows some of the basic classes of power amplifiers. Though several more exists, these are generally not used for basic audio purposes.

2.1.1 Class A
Class A uses 100% of the input signal. This means that the active element (often bipolar transistors or MOSFETs) remains conducting all of the time. Since class A amplifiers are relatively easy to construct and more linear than other classes, they are mostly used in small-signal applications were efficiency is not a consideration; i.e. as headphone amplifiers.

2.1.2 Class B
In class B amplifiers only 50% of the input signal is used, which means that the active element works in its linear range half of the time and remains “turned off” the other half. Most class B amplifiers uses two output devices that each conducts one half cycle of the input signal. This however leads to some troubling issues if the transition from one active element to the other is not perfect. This result in errors referred to as crossover distortion.

2.1.3 Class AB
As the name suggests, class AB amplifiers provides an operating point somewhere between class A and class B. The two active elements in class AB conduct more than half of the cycle each, which is a way to try to minimize crossover distortion of class B amplifiers.

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2.1.4 Class C
Class C uses less than 50% of the input signal for each output device, resulting in high crossover distortion but potentially higher efficiency.

2.2 Class D Amplification
Class D amplifiers is not something that is entirely new, it has been around for the last 15-20 years but is not as widespread as Class A, B, AB and C topologies. Historically, class D amplifiers were used in a limited number of applications such as motor controllers, because it was more difficult to generate the high quality signals demanded for audio applications. This however has changed and class D amplifiers have advanced sufficiently to be able to function in high-end audio products.

2.2.1 Basic Concepts of Class D Amplifiers
The basic concept with class A, B, AB and C amplifiers, as discussed earlier, is that one of the output devices conduct at any given time. This behavior results in power dissipation since a small current must pass through the transistor even if there is no output. When the output voltage increases, at some point in regards to given supply rails the voltage drop across the transistor will fall, but the current increases. When the transistors saturate, the voltage from collector to emitter or from drain to source will be low but the current will be high. In other words, at low power levels, there will be a large voltage drop but the current is small. This ultimately leads to a power dissipation curve that is not linear with output power. Class A and B amplifiers thus have a point where maximum efficiency is reached, about 25% and 78% respectively.

In class D on the other hand, the amplifier works by rapidly switching the output devices between “on” and “off”, rather than working in the linear region of the transistors or MOSFETs. This means that when in the off state, the amplifier behaves like an open-circuit, therefore the voltage will be the total supply rails and only a very small current will flow. In the on state, a specific current will flow through the mechanism, dependant on output power, and there will be no voltage present from drain to source, which gives theoretically

4 http://sound.westhost.com/articles/pwm.htm, 2010-10-06
zero power dissipation. This gives class D amplifiers almost 100% efficiency, in theory at least. Although, in practice results of up to 96% has been achieved\textsuperscript{5}.

The entire class D audio amplifier consists of roughly three stages: The modulation stage that modulates the input sine wave into “digital” pulses, the power stage that does all the switching and amplification and finally the filtering stage that filters out the high frequency pulses from the modulation stage.

\textbf{2.2.2 Advantages and Disadvantages of Class D}

The most prominent advantage of the class D amplifier, when comparing to topologies such as class A, B, AB and C, is the increased power efficiency\textsuperscript{6}. This is very useful in high power applications when small improvements in efficiency results in large decrease in waste heat coming from the amplifier. This reduction in heat serves particularly well for low power applications, most often entirely removing the need for heat sinks and therefore reducing the overall size of the amplifier unit. Since the overall size of the amplifier unit is decreased, costs associated with the enclosure can be reduced.

Although class D amplifiers have been around for many years, they only recently became more widely used in high quality audio applications. This is because class D amplifiers have a number of disadvantages making them less suitable for audio amplification. This was however a bigger issue a couple of years ago, since recent advancements in technology has solved many of the problems associated with class D audio amplification.

A well-known disadvantage with class D amplifiers is the large amount of high-frequency noise produced by the switching design mentioned earlier. It is therefore very important to keep the noise at a frequency that is much higher than that of the signal to be amplified, to keep the noise out of the audible region. In this way, it is possible to filter out the high frequency pulses with a simple low pass, passive filter. This however adds complexity, weight and cost to the entire amplifier. Although not that big of an issue, these things have to be taken into account.

\textsuperscript{5} \textit{http://www.irf.com/whats-new/nr071002.html}, 2010-10-06
\textsuperscript{6} Briana, M. “Class D Audio Amplifier the design of a live audio Class D audio amplifier with greater than 90% efficiency and less than 1% distortion”, 2008
Another disadvantage of class D amplifiers is the potentially complex design. This is something that may result in higher expenses and increased design time. High design expenses may be acceptable if it results in lower manufacturing costs, because manufacturing expenses are recurring whereas design is a singular expense.

The last major disadvantage of class D amplifiers is, or more correctly was, distortion. High THD or Total Harmonic Distortion indicates high levels of noise, which is something that significantly detracts from the overall audio quality of the output audio. However, faster modulation techniques have significantly reduced THD to well below one percent.

2.4 The Modulation Stage
All class D modulation techniques work by encoding the input audio signal into a stream of pulses. In most cases, the amplitude of the input audio signal is linked to the pulse width and the audio, as well as unwanted high-frequency noise, is contained in the spectrum of the pulses.

Several methods exist for modulating the signal in a class D audio amplifier. Some are better than others in regards to simplicity, availability and effectiveness. All these requirements must be taken into account when constructing the modulation stage. Simplicity is important because a portable and light weight design is appealing when dealing with several amplifiers in one system and when navigating rough environments. Effectiveness is important since the modulation is essential to sound quality and to keep the distortion as low as possible. Finally, availability is important when developing an independent product where some modulation techniques would be too impractical to use. The three most common techniques to use are PWM, PDM and self-oscillating modulation.

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2.4.1 Pulse Width Modulation (PWM)
Pulse width modulation or PWM is the most commonly used modulation technique. It basically involves using a comparator to compare the input signal with a triangular or ramping waveform that runs at a fixed carrier frequency. The result is a pulse-train that runs at the fixed frequency of the carrier signal. Within that period of the carrier, the pulse width of the PWM changes proportionally to the amplitude of the input audio signal. If the amplitude of the audio signal exceeds the amplitude of the triangular waveform, something called full modulation occurs. This is when the duty ratio within individual periods is either 100% or 0%.

There are a couple of advantages with using PWM in audio amplifiers. PWM allows 100 dB, or even better, audio-band SNR (Signal to Noise Ratio) when using a carrier frequency of only a few hundred kHz. This frequency is also low enough to limit losses in the output stage due to the switching mechanism. It is possible to achieve almost 100% percent modulation due to the high stability in most PWM modulators, permitting high output power up to the point of overloading, at least in concept.

There is however a few drawbacks with using PWM. In many implementations, PWM has the disadvantage of adding distortion. Second, harmonics of the carrier frequency may produce EMI (Electro Magnetic Interference) somewhere within the AM radio band. Finally there is the problem with the pulse widths of the PWM near full modulation. When the pulses become very small, the output stage gate-driver cannot switch properly due to the extreme speed needed to produce these short pulses. This ultimately leads to an output power that is somewhat lower than the theoretical maximum.

2.4.2 Pulse Density Modulation (PDM)
Another alternative to PWM is pulse density modulation or PDM. In this method, the number of pulses in a predefined time window is relative to the common value of the input audio signal. One form of PDM is 1 bit sigma-delta modulation. Sigma-delta modulation

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provides an advantage over PWM in regards to EMI. This is because much of the high
frequency energy in sigma-delta modulation is distributed over a wide range of frequencies,
as opposed to PWM where noise is concentrated in tones at the fixed carrier frequency and
its multiples. Since typical PDM clock frequencies lay around 3-6 MHz, these are way out of
the audible region and easily filtered out.

Sigma-delta also has the advantage that the minimum pulse width is one sampling-clock
period, even when approaching full modulation of a signal. Although safe operation up to
theoretical full power is achievable, conventional 1-bit sigma-delta modulators are only
stable to about 50% and therefore not widely used in class D amplifiers. Also, to achieve
sufficient SNR, at least 64-oversampling is needed.

2.4.3 Self-Oscillating Modulation and Pulse Position Modulation (PPM)
The not so widely used self-oscillating modulation, or sometimes called sliding mode control,
is a form of VSC (Variable Structure Control)\textsuperscript{10}. This method basically consists of applying a
high-frequency switching control to a nonlinear system in order to alter its dynamics.

Amplifiers using self-oscillating modulation always use a feedback loop that determines the
switching frequency of the modulator, instead of an externally provided clock. An advantage
compared to PWM is that the high-frequency energy is often more evenly distributed.
Thanks to the feedback loop it is possible to achieve very high quality audio, but
synchronization with other switching circuits is problematic because of the loop being self-
oscillating. This also means that digital audio first needs to be converted to analog in order
to be used in an amplifier using self-oscillating modulation.

Another method for signal modulation is pulse position modulation (PPM). Here, the pulses
are of uniform amplitude and width but the position of each pulse varies with the amplitude
of the input signal\textsuperscript{11}. One self-oscillating circuit, producing a pulse density modulated output,
is easily built using the standard LMC555-timer.

\textsuperscript{10} http://en.wikipedia.org/wiki/Sliding_mode_control, 2010-10-15
\textsuperscript{11} http://www.argospress.com/Resources/CommunicationsSystems/pulpositimodula.htm, 2011-01-26
2.5 The Power Stage
After the input signal has been modulated into pulses it needs to be amplified. There are basically two ways of doing this, a half-bridge or a full-bridge (sometimes called H-bridge) configuration. The bridge circuit most often consists of MOSFETs for the switching part and some kind of gate driver powering the MOSFETs. This switching design ensures very high efficiency in class D amplifiers.

2.5.1 Half-Bridge
In a half-bridge configuration, two MOSFETs are used but only one is turned on at every time-instance. Figure 2.1 shows a simple half-bridge with separate drivers for each MOSFET. The modulator and filtering stages have been left out.

![Figure 2.1: A basic Half-Bridge Amplifying Stage](image)

This kind of circuit is very simple and can provide a sufficient solution if audio quality is not a major concern.

2.5.2 Full-Bridge
The full-bridge or H-bridge amplifier is another common configuration. Figure 2.2 shows the basic configuration for a full-bridge amplifier. As with the previous figure, the modulator and filter stages have been left out for easier understanding.
The full-bridge amplifier is basically two half-bridges connected to the same output impedance, or speaker in this case. This means that two MOSFETs are on at a time, giving the full-bridge three possible states: positive, neutral and negative. Positive is achieved when Q1 and Q4 are on at the same time, negative when Q3 and Q2 are on and neutral when Q2 and Q4 are on, grounding the load.

It is very important that two MOSFETs that are on the same side, i.e. Q1 and Q2, are never on at the same time. This will short the rails and positively damage both the speaker and the amplifier itself.

2.5.3 A Comparison Between Half-Bridge And Full-Bridge

There are advantages and disadvantages with each configuration of amplifiers. Presented in an International Rectifier application note\(^\text{12}\) is a comparison between half-bridge vs. full-bridge with the respect to class D amplification. As seen in table 2, the biggest issue with the full-bridge topology is that it uses more components. Additional drivers and MOSFETs are needed and thus making the full-bridge more expensive than its half-bridge counterpart. The advantages outweigh the disadvantages however. DC offset is potentially harmful to the speaker and harmonic distortion (HD) affects the quality of the output signal in a negative way. The application note also states that “a full-bridge is better in audio performance”\(^\text{10}\).

<table>
<thead>
<tr>
<th></th>
<th>Half-Bridge</th>
<th>Full-Bridge</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>0,5 x 2ch</td>
<td>1</td>
</tr>
<tr>
<td>Current ratings</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>MOSFET</td>
<td>2 MOSFETs/channel</td>
<td>4 MOSFETs/channel</td>
</tr>
<tr>
<td>Gate driver</td>
<td>1 Gate Driver/channel</td>
<td>2 Gate Drivers/channel</td>
</tr>
<tr>
<td>Linearity</td>
<td>Even and odd order HD</td>
<td>No even order HD</td>
</tr>
<tr>
<td>DC Offset</td>
<td>Adjustment is needed</td>
<td>Can be canceled out</td>
</tr>
<tr>
<td>Modulation Pattern</td>
<td>2 level</td>
<td>3 level can be implemented</td>
</tr>
</tbody>
</table>

Table 2: Half-Bridge vs. Full-Bridge

2.6 The Filtering Stage

Since the signal from the amplifying stage is a modulated pulse train, it is often mandatory to use a filter, although the output modulation may be adapted so that the amplifier may be connected to the speaker without the use of a filter. This is called *filterless class D*\(^\text{13}\). This form of class D amplifiers can many times be used, provided the wire to the speaker is less than about 10 cm. One must however distinguish between *filterless class D* and class D without filter, the last one mentioned not being recommended since it will reduce battery life and possibly damage the speaker.

There are basically two types of filters, active or passive. Active filters use amplifying elements such as operational amplifiers to synthesize the desired characteristics of the filter\(^\text{14}\). Gains and drawbacks of active filters are mostly related to the operational amplifier that is used. I.e. op amps provide high input impedance and low output impedance but limitations in bandwidth and noise generated by the amplifying circuit may lead to unwanted results or pricy filter-designs. Passive filters on the other hand require no power supplies and do not have the same bandwidth limitations as active filters do. However, the components used in passive filters can be expensive if high accuracy is needed and passive filters provide no signal gain.


When designing a filter for the class D amplifier, it is important that components are chosen carefully. The ideal case would be to design a filter that has no effect on the desired output signal while filtering out all the high frequency noise coming from the switching mechanism\(^{15}\). Since switching noise is of much higher frequency than the audio signal, the best filter to use would be a low-pass topology. It is also desirable to have as flat pass-band as possible when filtering audio signals, therefore the best filter type would be a Butterworth filter.

When designing filters for class D amplifiers, one must also consider impedance matching to the speaker used. The cut-off frequency of the filter is directly dependant on the impedance of the speaker. Therefore it is not possible to swap speakers with different impedances without first recalculating the values of the filter components.

### 2.6.1 Low-Pass Filter

The principles of a low-pass filter are that it allows only signals of low frequencies to pass\(^{16}\). The cut-off frequency point is determined by the values of the passive filter components (resistors, capacitors and inductors) and the combination and number of components used determines filter-order. Figure 2.3 show a second-order passive low-pass filter-design.

![Second-Order Passive Low-Pass Filter](http://i.cmpnet.com/audiodesignline/2006/05/TIFig3.JPG)

**Figure 2.3: Second-Order Passive Low-Pass Filter\(^{17}\)**

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\(^{15}\) [http://www.eetimes.com/design/audio-design/4015847/Understanding-output-filters-for-Class-D-amplifiers](http://www.eetimes.com/design/audio-design/4015847/Understanding-output-filters-for-Class-D-amplifiers), 2010-10-28

\(^{16}\) [http://www.electronics-tutorials.ws/filter/filter_2.html](http://www.electronics-tutorials.ws/filter/filter_2.html), 2010-11-26

\(^{17}\) [http://i.cmpnet.com/audiodesignline/2006/05/TIFig3.JPG](http://i.cmpnet.com/audiodesignline/2006/05/TIFig3.JPG), 2011-02-03
2.7 Speaker Selection
As stated in table 1, the speaker to be used in the project was to be of horn-type. The major advantage with horn speakers is that the horn increases the overall efficiency of the driving element\textsuperscript{18}. This means that the acoustic output of a specific driver is increased using the horn. Horn speakers also have the advantage of directing the sound towards a single spot, in other words altering the horizontal and vertical coverage angels of the soundwave emanating from the speaker. This is important when the speaker is far away from the intended “listening position”.

In order to achieve the desired 60dB at a distance of 200 meters from the speaker, specified in table 1, the sound pressure close to the speaker needs to be calculated using the following equations, were $L_1$ is the sound pressure at a distance $r_1$ close to the speaker and $L_2$ the sound pressure at a distance $r_2$ further away:

\[
\begin{align*}
  r_1 &= 1 \text{ m} \\
  r_2 &= 200 \text{ m} \\
  L_1 &= \text{Unknown} \\
  L_2 &= 60\text{dB}
\end{align*}
\]

\[
L_1 = L_2 + 20 \cdot \log \frac{r_2}{r_1} = 60\text{dB} + 20 \cdot \log \frac{200}{1} = 106 \text{dB}
\]

This means that the speaker must be able to output a sound pressure level of 106 dB in order to be considered.

3 Preliminary Design and Construction
The following section describes all the steps involved in designing and building the first version of the class D audio amplifier, from simulation to PCB.

Since almost all class D amplifiers consist of three stages (modulation, amplification and filter) the overall outline of the amplifier was more or less settled. Although the final design was going to be a single card with all stages included, it was determined that the best way to simplify error-handling was to construct each stage separately.

\textsuperscript{18} http://en.wikipedia.org/wiki/Horn_loudspeaker, 2011-02-28
As manufacturing of PCBs, soldering components and checking for errors on surface-mounted cards is a very time-consuming and costly process, simulations and test builds on breadboards of each stage were conducted where possible. All components were chosen so that the temperature requirements specified in table 1 are fulfilled. Figure 3.1 shows a block diagram of the entire circuit.

![Block Diagram of a Class D Amplifier](image)

**3.1 The Modulationstage**
The modulationstage in class D amplifiers is crucial to audio quality. Any loss in signal quality or added noise at the modulationstage decreases the maximum quality achievable at the output. Since high quality audio was not needed, see table 1, it is possible to utilize a simple design for the modulationstage. It is also necessary to use components that use low power, in order to save battery-life.

**3.1.1 The Pulse Width Modulator**
As discussed in section 2.3.1, the most commonly used method in class D amplifiers is pulse width modulation, PWM. As the method basically involves comparing a triangular waveform to the audiosignal, the circuit would be fairly simple and not utilizing a lot of components. Being the most commonly used method in class D, another advantage is that a lot of topics and reading-material exists on the subject which in turn helps with the design. As mentioned in 3.1, audio quality was not the biggest concern; therefore a simple solution would be sufficient. Based on these requirements, it was decided that PWM could be a feasible solution for this project.

An easy triangle wave generator using two operational amplifiers can be seen in figure 3.2. This circuit consists of two parts, the square wave generator and an integrator. The triangle wave generated at the output of the integrator is fed back to the first op amp which
functions as a comparator, comparing the signal at the positive input with GND on the negative input.

**Figure 3.2: Triangle Wave Generator Using Operational Amplifiers**

The amplitude of the triangle wave is set by the ratio \( R_2/R_1 \). It is very important that \( R_2 \) is larger than \( R_1 \) in order for this circuit to function. The values of \( C \) and \( R_t \) affect the frequency of the triangle wave. The full equation for the operating frequency is:

\[
    f_{out} = \frac{1}{4R_tC} \left( \frac{R_2}{R_1} \right)
\]

The triangle wave will act as a carrier for the audio and needs to have a frequency of at least twice the highest frequency present in the audio signal. In order to determine the required output frequency of the triangle wave, the dynamic range of the audio signal must be taken into account. The human ear can detect pressure changes in the air if they are in the audible region, which ranges from approximately 20 Hz – 20 kHz. Because of this, there is no need to try to sample audio with frequencies higher than 20 kHz.

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22 [http://hyperphysics.phy-astr.gsu.edu/hbase/sound/earsens.html](http://hyperphysics.phy-astr.gsu.edu/hbase/sound/earsens.html), 2011-01-25
Components were chosen so that a sampling-frequency of approximately 173 kHz was achieved, giving a sampling rate of 8.65. Since the amplifier should run on single supply if possible, instead of dual supply required by the circuit in figure 3.1, the two operational amplifiers needed a virtual ground of half the supply-voltage at their grounded input\textsuperscript{23}.

The complete modulator used a quad op amp (OPA4350) for the triangle wave generator, a high-speed comparator (TLV3501) to compare the audio with the triangle wave and a LDO voltage-regulator (LM1117IMD) to provide the ICs with 5 V and the required virtual ground of 2.5 V, see appendix A. If designed correctly, the modulator should provide pulses that change in width when the amplitude of the input audio changes.

3.1.2 PCB Layout
The problem with the first version of the modulator was that several components did not exist in the library of the used simulation tool, Multisim. Therefore, the modulator was constructed directly on a PCB using EAGLE, a cad-tool for developing PCBs, and the mill at the university. Figure 3.3 shows the PCB for the modulator.

![](Figure 3.3: PCB-Layout Of The Pulse Width Modulator)

3.2 The Power stage
The power stage consists of two key-components, the MOSFETs and the gate drivers. Choosing the correct components and using the appropriate power stage configuration is essential to the overall performance of the amplifier.

3.2.1 Amplifier Configuration
As discussed in section 2.4, there are two different configurations to consider when constructing the power stage, the half-bridge and the full-bridge. Section 2.4.3 clearly states the benefits of using a full-bridge configuration instead of the half-bridge. Important aspects such as the ability to use a single power rail, elimination of DC offset and less distortion clearly outweighs the drawback of the increased cost involved in using the full-bridge.

3.2.2 MOSFET Selection
Choosing the correct MOSFET is essential to the overall performance of the amplifier and the output power produced. Parameters to consider when choosing MOSFET for this application are the peak drain-source voltage (V\text{DS}) it can handle, the continuous drain current (I\text{D}), the drain-source resistance (R\text{DS(on)}), the total gate charge (Q\text{g}) and rise- and fall-times (t\text{r} and t\text{f}).

**Peak Voltage And Drain Current**
Table 1 state that the system must be able to deliver an average of 60 Watts into an 8 Ω speaker, therefore surviving peaks of up to 120 Watts. Since the project specifications in table 1 states that a 12V supply should be used if possible, the MOSFETs must be able to handle a lot of current. The current can be derived from the following equations:

\[ U = 12V \]
\[ P = 120 \text{ Watts} \]
\[ P = U \times I \]
\[ 120W = 12V \times I \]
\[ I = \frac{120W}{12V} \]
\[ I = 10A \]

Based on this result, the MOSFET must be able to handle 10A peak drain current. Should however the opportunity rise to be able to increase rail voltage, the current required would be significantly lower. Using the same peak power and speaker impedance, but only focusing on peak voltage, the equation yields:

\[ R = 8 \Omega \]
\[ P = 120 \text{ Watts} \]
\[ P = \frac{V_{\text{peak-RMS}}^2}{R} \]
In this case, the MOSFETs must be able to handle a 44V rail in order to be considered.

Selecting the right MOSFET for this application was not an easy task. Several MOSFETs meet the peak voltage and continuous drain current requirement and there is really not much difference between them. The final pick was International Rectifiers IRF7665 stated to be “optimized for Class-D audio amplifier applications”\(^{24}\). This MOSFET has relatively low drain-source resistance and gate charge while maintaining fast rise- and fall-times. The ability to handle a high drain-source voltage of 100 V and drain current of maximum 14.4 A allows for increased power output without the need of changing MOSFET.

3.2.3 Gate Drivers
Components originating from the same manufacturer often work very well together. Since the MOSFET used in the power stage is manufactured by International Rectifier, the best choice would be to use an International Rectifier gate driver to charge the MOSFETs. Once again, there is an ocean of ICs to choose from. One however stands out, the IRS20124S. This driver has programmable dead time which will be very useful in order to minimize shoot-through and optimize harmonic distortion.

These specific gate drivers use external resistors to set dead-time and over-current (OC) threshold, see appendix B for gate driver datasheet. Appropriate resistor values were chosen according to the suggestions shown in table 3, to obtain the shortest possible dead time (DT1). Resistor values used were R1 = 8,2kΩ and R2 = open.

\[ V_{\text{Peak-RMS}} = \sqrt{PR} \]
\[ V_{\text{Peak-RMS}} = \sqrt{8 \cdot 120} \]
\[ V_{\text{Peak-RMS}} = 30.98 \text{ V} \]
\[ V_{\text{Peak}} = V_{\text{Peak-RMS}} \cdot \sqrt{2} \]
\[ V_{\text{Peak}} = 43.8 \text{ V} \]

\(^{24}\) See MOSFET datasheet, appendix C
OC threshold is set by three additional resistors, see figure 3.5. The threshold is set to allow a maximum current of 10 A to flow to the speaker. This can later on be adjusted simply by recalculating the values.

Values for the resistors can be derived from the following equations:

$I_{TRIP} = \pm 10A$

$R_{DS(ON)} = 51 \text{ m}\Omega$

$V_{ISET1} = V_{TH} + 2.21V = I_{TRIP+} \cdot R_{DS(ON)} + 2.21V = 10A \cdot 51m\Omega + 2.21V = 2,261V$

$V_{ISET2} = V_{TH} + 2.21V = I_{TRIP-} \cdot R_{DS(ON)} + 2.21V = -10A \cdot 51m\Omega + 2.21V = 1,7V$

$R_{tot} = R_3 + R_4 + R_5 = \frac{V_{cc}}{I_{bias}} = \frac{12V}{1\mu A} = 12k\Omega$

$V_{R3} = 12V - 2,261V = 9,739V$

$V_{R4} = 2,261V - 1,7V = 0,561V$

$V_{R5} = 1,7V$

---

See Gate Driver datasheet, appendix B
After calculating theoretical values, real world values were identified:

\[ R_3 = \frac{9.739V}{1\mu A} = 9.739 \text{k}\Omega \]
\[ R_4 = \frac{0.561V}{1\mu A} = 0.561 \text{k}\Omega \]
\[ R_5 = \frac{1.7V}{1\mu A} = 1.7 \text{k}\Omega \]

One important notice is that the equations in the datasheet for the gate drivers are incorrect. \( R_{DS(ON)} \) should be in m\( \Omega \), not in \( \mu \Omega \) as used in the datasheet.

### 3.2.4 PCB Layout

Since the MOSFETs and gate drivers are surface mounted, the power stage has to be fabricated on a PCB. This was done the same way as with the pulse width modulator, using EAGLE and the PCB mill at the university.

One problem that arose during the design of the PCB was that some components did not exist in the library of EAGLE, specifically the gate driver and the MOSFETs. Therefore new components had to be made, which was a bit time consuming since none of the group-members had ever tried this before.

Using the mill at the university gave room for errors in the board-design; since the waiting time for a new PCB was significantly shorter than if each new revision had to be ordered. Although, waiting times was a bit longer for the first revision since none of the team members were familiar with the PCB mill.

As mentioned in section 3, each stage was constructed separately for easier error handling. The power stage is divided in a high- and low-side which each accept a positive square-wave. Figure 3.6 shows the PCB for the power stage. The complete schematic of the power stage can be viewed in appendix A.
3.3 The Filtering Stage
As explained in section 2.6, the best filter to use in this application would be a passive low-pass Butterworth filter. Since the power stage is a full-bridge, the filter needs to be a balanced filter. A balanced filter is basically two identical filters on either side of the load. This does increase the complexity and cost of the final product, but is necessary due to the full-bridge used. A balanced filter and full-bridge however help reduce noise in the output by eliminating odd harmonics and thereby improving THD.

In order to have a relatively sharp slope for the cut-off but still maintaining a simple design, it was decided to use a second order filter. A second order filter results in a slope of -40 dB/decade, which should be sharp enough to reduce the high frequency noise to acceptable levels.

When the first filter was designed, it was not clear which speaker to use. The cut-off frequency was therefore based only on the frequency range of audible sound, the highest being approximately 20 kHz as mentioned in section 3.1.1. To provide a slight buffer above the audio band, while still attenuating most of the out-of-band noise, a cut-off frequency of 30 kHz was selected. When filter topology, cut-off frequency and the slope of the cut-off are chosen, it is possible to determine specific filter components.
3.3.1 Filter Components
Because of the full-bridge used, it is possible to construct a filter using the BTL-configuration shown in figure 3.7.

![Figure 3.7: Complete BTL Output Filter](image)

Values for the filter components can be derived using the following equations\(^{26}\), using 30 kHz as cut-off frequency \(f_c\) and the approximate value of 6Ω for the speaker \(R_L\):

\[
R_L = 6 \, \Omega
\]

\[
f_c = 30 \, \text{kHz}
\]

\[
C_L = \frac{1}{2\pi f_c \sqrt{2R_L}} = \frac{1}{2\pi \times 30000 \, \text{Hz} \times \sqrt{2 \times 6 \, \Omega}} \approx 0.625 \, \mu F
\]

\[
L = \frac{\sqrt{2} \cdot R_L}{4\pi f_c} = \frac{\sqrt{2} \cdot 6 \, \Omega}{4\pi \times 30000 \, \text{Hz}} \approx 22 \, \mu H
\]

\[
C = \frac{2sC_L}{10} = 0.125 \, \mu F
\]

One important notice is that the impedance of the speaker used in the filter calculations is 6Ω, rather than 8Ω used in section 3.2.2. This is because the speaker used for the preliminary design arrived after the completion of the power stage, but before designing the filter. The effects of this difference in impedance are discussed in section 4.2.

Once ideal components are chosen, real world components were identified. 22 µH is a real world value for the inductance, but as 0.625 µF and 0.125 µF are not standard capacitance values, this resulted in a problem. However, 0.680 µF and 0.1 µF are real values that could

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\(^{26}\) “Design considerations for Class D audio power amplifiers”, 1999.
provide an appropriate cut-off frequency. Using the real world values, the frequency of the cut-off is
\[ f_c = \frac{1}{2\pi \sqrt{LC}} = \frac{1}{2\pi \sqrt{2 \times 22 \mu H \times 0.680 \mu F}} \approx 29000 \text{ Hz} \]

It is important that the inductors have low Equivalent Series Resistance (ESR), since they are in series with the load and all of the power from the amplifier will flow thru them. Since the capacitors are in parallel with the load, their ESR is of less importance. Components chosen for the preliminary design were:

- Capacitor - Kemet C0805C684K3NACTU (0.680μF)
- Capacitor - Avx 08051C104K4T2A (0.1μF)
- Inductor - Bourns JW Miller 2305-H-RC (22μH, 7mΩ)

The complete schematic for the filtering stage can be viewed in appendix A.

### 3.4 Speaker

The initial idea was that the speaker would be selected during the design process of the preliminary design, but due to limitations in time, this was not possible. Therefore Salvator HB provided the project-group with a basic horn speaker. Speaker specifications are as follows:

- Model: LBC3491/12
- Max power: 15 W
- Frequency range: 480 Hz – 5.5 kHz
- Sound pressure level at rated output: 118 dB

This speaker was not intended to be used in the final product but merely to function as a test platform during the build, the reason being really bad sound quality. That is why some stages, such as the power stage, were not designed with the specifications of this specific speaker in mind.
4 Preliminary Results
The following section discusses the results from the preliminary design of the amplifier. This first step in the design-process was intended as a way of getting to know the class D amplifier topology. The design was not expected to perform well enough to be considered a final product, but merely to test one approach for a solution.

4.1 Functionality Testing

4.1.1 The Modulationstage
When testing began with the modulationstage, several design-flaws were discovered. One problem was that the input audio signal had a small amplitude of about 0.1 V while the triangle wave had several times larger amplitude, resulting in the comparator saturating. This was fixed by reducing the ratio R2/R1 on the triangle wave generator, see section 3.1.1.

Another issue was that since the comparator was of the high-speed type, it started oscillating when the audio-signal and triangle wave had approximately the same amplitude. This resulted in heavy distortion of the pulses. To avoid this, a slower comparator had to be used, replacing the TLV3501 with the LM311D. After several tests and fine-tuning of the modulator, the results were still bad and because of long waiting-times for components to arrive, it was clear that this circuit would not meet the demands for the final product.

4.1.2 The Power stage
The power stage had to be tested to ensure proper behavior without having the risk of damaging the speaker. The easiest way of doing this is to apply a positive square wave to either the high- or low-side and watch the results on the oscilloscope. Both gate drivers and MOSFETs use the same 12 V supply rail. The power stage was proven to be functional when an amplified square wave was observed at the output.

Since the modulator was not working as planned, the power stage could not be tested with the actual modulated signal. Figure 4.1 shows the input square wave and the amplified output of the power stage, both centered at zero.
4.1.3 The Filtering Stage
Due to the balanced nature of the filter, it was difficult to test either side without using the entire system. Since the modulator was not functioning, the filter could not be tested for full functionality during this stage of the design process. However, when applying a sine wave to either side of the filter, a noticeable “ringing” can be heard from the ceramic capacitors used. The reason and solution for this is discussed in section 4.2.

4.2 Problems And Improvements
The major problem with the preliminary design lay with the modulator. Since it did not function as depicted, the whole circuit could not be tested for functionality. Another issue with the modulation stage was that it was built on a PCB. Since many operational amplifiers use the same pin-configuration, like the ones used in the triangle wave generator, it would have been better to try the circuit on a breadboard. This would have simplified error handling and saved a lot of time, since changing components would have been easier. This was however difficult since some of the components did not exist as through-hole.

The power stage also used a “unique” IC, specifically the gate driver, that was not available as through-hole. Because the gate driver did not exist in the library, the circuit could not be simulated in Multisim either. This did not turn out to be a problem since the power stage seemed to function as it should. However, one issue discovered with the power stage was that the gate drivers and MOSFETs were using the same rail. This results in a limitation when testing functionality. Since the gate driver is configured to use a 12 V rail, voltage to the
MOSFETs could not be increased without having the risk of damaging the gate drivers. This also adds the possibility that the large drain-current will be affecting the entire circuit at high output levels. These supply rails needs to be separated in the second revision of the amplifier.

The power stage also had the drawback of using some “unique” components which were not present in the library of the CAD software, see section 3.2.4. Since designing new components was an unfamiliar experience, some design-flaws in the footprints of the components were discovered during soldering of the PCB. The pads for the gate driver were quite small, greatly complicating the soldering process. These pads were redesigned for the second revision.

The filter had an issue with capacitor microphonics, causing the filter-PCB to “sing” when applying an input signal. This is due to physical movement of the dielectric in the ceramic capacitors. When operating at a frequency within the audio band and with a signal that has a high enough amplitude, the effect is audible. This also has the possibility to add distortion to the output signal. The solution is to change the ceramic capacitors, see figure 4.2, to film-capacitors for the second filter-revision.

The preliminary design also suffered from a difference in speaker impedance-matching. The power stage used 8Ω when calculating peak voltage and drain current. The filter however used 6Ω when calculating cut-off frequency. The difference was due to a late arrival of the speaker, when the power stage was already soldered. The effect of this disparity is that it would take more power to drive the speaker than the calculations in section 3.2.2 originally suggested. This did not turn out to be a big problem since changes in the design was to be made for the improved version of the amplifier.
5 Improved Design And Construction
The preliminary design had a few flaws that were discussed in section 4.2. These were all addressed and corrected for the second revision of the amplifier. The major change involved a completely new approach to the modulation stage and a new speaker that could be used in the final product. The following section outlines the changes in each stage. As with the preliminary design, components were chosen to match the temperature requirement specified in table 1.

5.1 Changing Speaker
The improved design would have to feature a new speaker so that extensive testing could be conducted. The speaker used must be able to output 106dB as stated in section 2.7. A good option was the DSP3012A which provided a maximum output of 131dB. This particular speaker however had a slightly different IP-classification, namely IP56. This means that the dust-protection was not as good but protection against water is better, compared to IP65. It was decided, in coordination with Salvator HB, that this classification would still be sufficient for the purpose of this project. Full specifications for the speaker can be seen in appendix D. As the new speaker probably would be used in the final product, the amplifier could be designed to match all specifications.

5.2 The Modulationstage
When constructing the new modulation stage, it was important to find a solution that was tried and working. Simplicity in design was important to be able to quickly determine if the new solution would be feasible or not. Also, a simple design often requires the use of fewer active components, which in turn drains less power.

5.2.1 Self-Oscillating Modulator
A not so widely used method in class D amplifiers is self-oscillating modulation. As described in section 2.3.3, the modulator works by using a feedback-loop to determine the switching frequency. With this type of modulation it is possible to achieve high-quality audio with few components. Since the only drawback is difficulties when synchronizing with other switching devices and no such synchronization is needed in this project, self-oscillating modulation could provide a feasible solution.
One easy way of achieving self-oscillating modulation is to use the LMC555-timer circuit. An oscillator circuit with 50% duty cycle can be found in the datasheet for the LMC555-timer, see figure 5.1.

![Diagram of LMC555-timer circuit](image)

**Figure 5.1: 50% Duty Cycle Oscillator**

The Disch-pin may be discarded, using only the Output-pin as output and as feedback. The frequency of operation is determined by the equation:

\[
 f = \frac{1}{1.4R_cC}
\]

The frequency was set to approximately 152 kHz using 4.7 kΩ and 1μF as Rc and C respectively. Applying a sinusoidal-wave at the Control-pin results in a modulated output referred to as PPM, see 2.3.3. The output of this circuit has quite a lot of distortion and so the feedback-loop needs to be self-biased thru the help of a 2N3904 transistor\(^\text{27}\). The output of the final circuit should be a clean pulse-train. See figure 5.2 for a schematic of the circuit using the NE555-timer.

In order to be able to use this circuit in the project, some changes to the schematic had to be made. 12 V instead of 5 V is used, changes in resistor-values are needed for correct DC-offset adjustments at the CV pin and the LMC555-timer was used instead of the NE555. This is because the LMC555 requires lower supply current, is capable of operating at a higher frequency and has lower power dissipation.

In order to provide the full-bridge used as power stage with low- and high-side signals, the output of the modulator needs to be split in half and converted to positive pulses only. This is easily achieved by using a standard logic XOR-gate (CD4030). The XOR-gate acts as a phase splitter, effectively dividing the modulated AC-signal into high- and low-side, see figure 5.3, low being the same as the high-side but with inverted pulses.
Let us take the high-side as an example. Input signals with negative voltage are compared to Vcc on the second input of the XOR-gate, resulting in a positive output. The result becomes more evident when looking at the truth table of the XOR-gate, see table 4. The low-side uses GND as reference instead of Vcc and thus provides a positive output when the input signal is positive.

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vcc</td>
<td>high-side</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 4: Truth Table Of High-Side XOR-Gates

5.2.2 Breadboard- And PCB Layout
The new version of the modulator was possible to construct on a breadboard, in order to simplify error handling and test the functionality of the circuit. It was assumed that the output of the modulator on the breadboard would be fairly noisy, but since this step was only to ensure proper behavior, noise was accepted.

Once the functionality of the breadboard modulator was confirmed, a PCB was manufactured and all components soldered into place. Figure 5.4 and 5.5 shows the evolution of the modulator from breadboard to PCB. The full schematic for the modulationstage can be viewed in appendix E.
5.3 The Power stage

The power stage from the preliminary design was proven functional in regards to amplifying a square wave. However, as discussed in section 4.2, the power stage had some major flaws that needed to be corrected for the improved design.

The first issue to be solved was to separate the supply for the gate driver and the MOSFETs. This was easily done in the CAD-software. Also the pads for the gate drivers were redesigned to simplify soldering. The second issue was the mismatch of speaker impedance described in section 4.2. The speaker used in the improved version however had an impedance of 8Ω, thus not requiring any changes in the power stage due to the change of speaker. The PCB for the improved version of the power stage can be seen in figure 5.6. The full schematic for the power stage can be viewed in appendix E.
5.4 The Filtering Stage
The filter needed different capacitors to avoid the “ringing” described in section 4.2. The solution was to use film-capacitors as these are better suited for audio purposes\(^2\). With the new and “final” speaker selected, it was also possible to match the cut-off to the impedance and frequency range of the speaker.

Since the speaker had an upper limit of 18 kHz, it was decided that the cut-off frequency could be lowered to further filter out unwanted noise. Using the equations in 3.3.1 and the new values of 1,5\( \mu \)F and 0,3\( \mu \)F for the capacitors, the cut-off frequency is approximately 19590 Hz. The PCB for the improved filtering stage can be seen in figure 5.7. The full schematic for the filtering stage can be viewed in appendix E.

6 Improved Version Results
Once all parts of the improved version were constructed, it was possible to test the entire amplifier for functionality. Listening tests as well as sound pressure measurements were conducted to ensure proper behavior.

6.1 Functionality Testing
6.1.1 The Modulation stage
Initial testing with the modulator involved just connecting the supply-rails and looking at the output without any input signal to modulate. The results were identical pulses on both the

\(^2\) [http://www.audiocaps.com/](http://www.audiocaps.com/), 2011-03-02
high- and low-sides of the XOR-gate, see figure 6.1. The pulses were not entirely clean, but was assumed to be good enough to be able to use when testing the full system.

![Figure 6.1: Modulator Output (High-Side), No Input Signal](image1)

The next step was to apply a sine wave to the CV-pin to see if the result was a modulated output. The modulation stage was confirmed to be functional when a modulated output was observed at both the low- and high-side of the XOR-gate, see figure 6.2 and figure 6.3.

![Figure 6.2: Modulated Output, Low-Side](image2)
6.1.2 The Power stage
The improved version of the power stage was tested the same way as the preliminary design, by applying a square wave to both the high- and low-side of the gate driver. The results can be viewed in figure 6.4.
6.1.3 The Filtering Stage
With the new film-capacitors, the issue with microphonics described in section 4.2 was solved. Since the filter still was of the balanced type, testing would be easier to conduct using the modulator. The modulator was connected to the filter and a sine wave was used as input. The results using a 10 kHz and 20 kHz sine wave is showed in figure 6.5 and figure 6.6 respectively. At 20 kHz, the amplitude of the sine wave has dropped about -3 dB and thereby verifies the calculated cut-off frequency of approximately 19590 Hz.

Figure 6.5: Filter Output Using A 10 kHz Sine Wave

Figure 6.6: Filter Output Using A 20 kHz Sine Wave
6.1.4 Full system Assembly
Since all stages were working for the improved version of the amplifier, it was possible to assemble the entire circuit and conduct testing with sound as input. The tests used a large CD-player as source to get a high quality audio signal.

Each stage uses one or two power supplies depending on needs. This was to see if different supply voltages had different effects on the entire amplifier, so that correct voltage regulators could be picked out for a final circuit.

6.2 Speaker Testing
The following section outlines some tests done with the speaker connected directly to the CD-player and to the class D amplifier constructed in this project. The CD-player acted as a reference for audio quality as well as allowing measurements of the maximum sound-pressure the speaker would be able to produce.

6.2.1 Listening Test
Listening tests are quite subjective and could vary a lot between each tester. Therefore, listening tests were conducted using both the CD-player and the class D amplifier. Using two different amplifiers allowed for a reference so that the quality of the audio from the class D amplifier could be compared to the "clean" audio from the CD-player. Various sounds such as high quality music, gunshots, explosions etc, were listened to at different volumes by several people.

One thing became very clear when listening to the audio from the class D amplifier. At low volumes (small input signal), the sound was very good. Everything from music to gunshots could be heard with very little distortion. As the volume was increased however, distortion became more and more prominent finally resulting in a very bad “crackling”- noise at high volumes. Possible reasons for this noise are discussed in section 7.

6.2.2 Sound pressure
Sound pressure was measured using a Velleman AVM2050 analogue sound level meter. The sound pressure was measured while increasing the amplitude of the input signal until the desired output sound pressure of 106 dB was achieved. Three different sounds were used for measuring; a part of a music track, helicopter sound and gunshot sound. The speaker was
more than capable of producing audio with higher than 106 dB of soundpressure, when connected directly to the CD-player. Noticeable is that too much distortion is present in the output audio from approximately 100 dB and upwards, resulting in a crackling sound, when using the class D amplifier. Increasing the amplitude of the input signal even more could possibly damage the speaker; therefore no further increase in volume was made. The results of the measurements can be viewed in figure 6.7, 6.8 and 6.9. Discussions regarding the results can be viewed in section 7.

As a comparison, the soundpressure was measured using 24 V as supply for the MOSFETs. With the higher supply-voltage, the desired soundpressure of 106 dB was achieved for all three sounds used, without heavy distortion.

Tables with all measurement values can be viewed in appendix E.
6.3 Power Consumption
Since the amplifier is intended to run on batteries, power consumption is very important. Because of the way the amplifier is intended to operate, see section 1.1, power consumption needed to be measured in several ways. Measurements were done during a time period of 10 minutes, with a sampling-frequency of 1/30 Hz, using a digital multimeter. Power consumption is important both when the amplifier is on standby as well as when sound is being played, since battery-life is restricted.

One notice is that the modulator consumes more power in the standby mode than when running, see figure 6.7
As seen in figure 6.11, the power consumption for the power stage is quite low. It only slightly increases over time, which could be the result of a temperature increase in the circuits. However, the difference in supply-current between startup and after 10 minutes is only 0.226 mA, which is easily negligible.

Measuring the power consumption of the power stage when it is running is difficult, due to large current-fluctuations depending on the type of sound being played. However, the largest noticeable value when trying to measure was something around 85 mA (for music),
which is only a minor increase from standby-current. The largest value for the current for the entire circuit would then be;

\[ I_{\text{Amp}} = I_{\text{Mod \ standby \ max}} + I_{\text{Power \ running \ max}} = 13.3 \ mA + 85 \ mA = 98.3 \ mA \]

This would result in a runtime of approximately 50 hours, using one 5 Ah battery. A table with all the measurement values can be viewed in appendix F.

7 Problems With The Improved Version
The improved version of the amplifier incorporated a series of changes from the preliminary design. A completely new modulator was constructed and implemented, the power stage required some small changes and the filter was redesigned for increased functionality. This section outlines the problems with the improved design. Some possible solutions to these problems are discussed in section 9.

Problems with the improved version consist mainly of distortion in the output audio at high volumes. There could be several reasons for this. The main problem is the limited supply-voltage of 12 V. This greatly limits the voltage swing of the modulator, allowing for a rather small input signal to be handled and also limiting the amplitude of the output from the modulator. Increasing the supply-voltage also increases the total amplification, as discussed briefly in section 6.2.2. With a supply of 24 V, the desired soundpressure of 106 dB was achieved with very little distortion in the output audio. But with only 12 V, the maximum soundpressure was approximately 100 dB and even then, a lot of distortion could be heard.

Another issue is the modulator itself. The self-oscillating modulator used in this project is not designed to produce high-quality audio, especially not at extremely high volumes; therefore distortion is inevitable as some point. A possible problem is the feedback of the modulator. Large input signals result in a lot of variation in the position of the pulses in the output. This could possibly push the feedback transistor out of its linear region, resulting in distortion. Adjusting the modulation frequency could also help reduce noise in the output.

One issue discovered with the power stage was that when the rails for the MOSFETs and the gate drivers were separated, the MOSFETs did not have any dedicated bypass capacitors.
This caused the MOSFETs to fail consistently which resulted in very bad sound from the amplifier. The solution was to attach large electrolytic capacitors at the rails, see figure 7.1.

Figure 7.1: Bypass Capacitors At Rails

8 Conclusion
The ultimate goal of this project was to design a class D audio amplifier with 60 W output power, capable of producing audio with a soundpressure of 106 dB close to the speaker. The audio quality was of less importance but should be good enough to distinguish between an explosion and a gunshot at 200 meters from the speaker. A speaker to use with the amplifier should also be selected according to desired IP-classification and the ability to output enough sound pressure.

The initial phase of the project involved getting to know the existing audio power amplifiers as well as obtaining more in-depth knowledge of the class D audio amplifier. Different stages for a first prototype were developed. Circuit-designs were simulated where possible before moving on to a breadboard or directly on to a PCB. An evaluation of the entire circuit was not possible with the first version, since some stages were not working properly. Instead, the aim was to construct an improved version of the amplifier.

The improved version of the amplifier included a self-oscillating modulator built using the LMC555-timer circuit and a standard logic XOR-gate. The power stage used International rectifier MOSFETs and gate drivers and the filtering stage was a second-order passive low-
pass Butterworth filter with large toroidal inductors and film-capacitors. An appropriate speaker was also selected for the improved version. The speaker is able to output a maximum of 131 dB which is well above the desired 106 dB required for this project. The IP56-classification on the speaker also met the demands.

Listening tests, as well as sound pressure measurements were conducted on the improved version of the amplifier. The listening tests showed that the amplifier was able to produce “good” quality audio at low volumes, but had a lot of distortion when the volume was increased. The desired soundpressure of 106 dB was not achieved during tests with 12 V as supply; instead the maximum soundpressure without heavy distortion is approximately 100 dB. The project specification regarding soundpressure was however met when increasing the supply voltage to at least 24 V, i.e. using two batteries.

Powerconsumption was also of major importance and specifications were met, with almost 51 hours of runtime using the current setup. Changes in amplifier-design, such as redesigning the modulator or construct the entire circuit on one PCB, will however affect powerconsumption and further calculations are needed before making these changes. This however shows the major advantage that class D has towards regular class AB amplifiers in regards to efficiency.

Connectors and volume-control were not implemented because some parts of the amplifier may be changed for the final product.

Although not meeting all the criteria for a finished product, the improved version of the class D amplifier still was a major step towards that goal. Some errors were expected while others showed up during the design-process. Improvements can be made, as with any design, to achieve the best possible results given the current project specifications. But due to the narrow time frame, these further improvements were beyond the scope of this project.
9 Improvements And Future Work
Although an almost working prototype, the amplifier still has a long way to go before it would be considered a finished product. In the following sections, several possible improvements are discussed for the different stages of the amplifier.

9.1 The Modulation stage
The modulator proved to be a working design in regards to successfully modulating the input audio into pulses. However, several restrictions were discovered during testing of the improved version of the amplifier.

First off, there are a few improvements that can be made to the existing modulator. One possible way of reducing distortion would be to adjust resistor values for appropriate feedback at high volumes, as discussed in section 7. The modulation frequency could also be adjusted to further optimize noise handling. This is not guaranteed to work however and the current modulator is still restricted to the 12 V supply.

Another alternative would be to investigate whether or not the second battery mentioned in section 1.1 could be used to create a dual supply. This would increase the number of possible designs to use for the modulator and also increase the headroom for the input signal. If a complete change of modulation technique is needed, the dual supply would allow the implementation of a sigma-delta modulator, which could yield several advantages:

- Superior noise handling due to several feedback-paths in higher-order sigma-delta modulators
- Increased headroom for the input signal due to the dual power-supply used
- The high modulation frequency used in sigma-delta modulators pushes noise further out of the audio-band and increases the overall efficiency of the amplifier

Using a sigma-delta modulator would also broaden the area of use, making the amplifier suitable for applications where high-quality audio is needed.

9.2 The Power Stage
The power stage was proven to be functional in the improved version of the amplifier. The major improvement needed is dedicated bypass capacitors at the rails in order to have a correct functionality of the MOSFETs. Dead time could also be adjusted for increased efficiency, but this is dependent on the modulation technique used.
9.3 The Filtering Stage
The filter used for the improved version of the amplifier has a cut-off frequency that is quite low. This is because of the type of speaker used, which only handles frequencies up to 18 000 Hz and also because of the rather low modulation frequency. The low cut-off does however affect the audible sound so that high-frequencies get attenuated. This will color the listening experience in a negative way, resulting in a sound picture that is less dynamic than would be optimal. Should however the modulation technique change so that a higher modulation frequency could be used, it would be possible to increase the cut-off to obtain better sound-quality.

Another improvement would be to use inductors that have a lower resistance. This change increases the efficiency of the filter.

9.4 Pre-amplification Stage
When doing tests with the amplifier, the input of the modulator was connected to the headphone output of a CD-player. In this way, it was possible to adjust the amplitude of the input signal simply by adjusting the volume on the CD-player. This will however not be possible in the final product, where the likely audio source will be a low-power MP3-player; thus demanding the use of a pre-amplifier. It would also be possible to implement volume control in the pre-amplification stage, by using a simple potentiometer to limit the input signal.

There are several ways of constructing a pre-amplifier. Transistor-based versions are widely used where the input signal is very small, i.e. as microphone pre-amps. These generally only need a single supply, but with the downside of easily being overdriven when increasing the input signal. Another alternative would be to use a ready-made pre-amp, based on operational amplifiers designed specifically for audio purposes. These however often require the use of a dual power-supply, but benefits from the ability to handle larger variations in amplitude of the input audio.
Both designs have their benefits and downsides, but in order to select the appropriate design, further research is needed.

9.5 General Improvements
Although each stage of the amplifier needs specific improvements, there are several issues that need to be addressed regarding the entire circuit.

The current version of the amplifier is tied to the lab-bench since several different power-supplies are used. In order to have a finished product, each stage will need dedicated voltage regulators and line protection so that the large current-fluctuations caused by the MOSFETs do not affect the other stages.

The finished amplifier will also have to be constructed on a single PCB. This will possibly reduce noise currently caused by the cables connecting the stages to each other. Error handling is however complicated when using one single PCB, therefore each stage must be finalized before progressing further.
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Appendix A

Preliminary Design Schematics
Appendix B

Gate Driver Datasheet

**International Rectifier**

**IRS20124(S)PbF**

Digital Audio Driver with Discrete Deadtime and Protection

**Features**
- 200 V high voltage ratings deliver up to 1000 W output power in Class D audio amplifier applications
- Integrated deadtime generation and bi-directional over-current sensing simplicity design
- Programmable compensated preset deadtime for improved THD performances over temperature
- High noise immunity
- Shutdown function protects devices from overloading conditions
- Operates up to 1 MHz
- 3.3 V/5 V logic compatible input
- RoHS compliant

**Product Summary**
- **V_{SUPPLY}** 200 V max.
- **I_{O+/-}** 1 A / 1.2 A typ.
- Selectable Deadtime 15 ns, 25 ns, 35 ns, 45 ns typ.
- Prop Delay Time 60 ns typ.
- Bi-Directional Over-Current Sensing

**Typical Application Diagram**

[Diagram of IRS20124 component connections]
Description
The IRS20124S is a high voltage, high speed power MOSFET driver with internal deadtime and shutdown functions specially designed for Class D audio amplifier applications.

The internal dead time generation block provides accurate gate switch timing and enables tight deadtime settings for better THD performances.

In order to maximize other audio performance characteristics, all switching times are designed for immunity from external disturbances such as VCC perturbation and incoming switching noise on the DT pin. Logic inputs are compatible with LSTTL output or standard CMOS down to 3.0 V without speed degradation. The output drivers feature high current buffers capable of sourcing 1.0 A and sinking 1.2 A. Internal delays are optimized to achieve minimal deadtime variations. Proprietary HVIC and latch immune CMOS technologies guarantee operation down to VCC = 4 V, providing outstanding capabilities of latch and surge immunity with rugged monolithic construction.

Absolute Maximum Ratings
Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. All currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VGS</td>
<td>High-side floating supply voltage</td>
<td>-0.3</td>
<td>220</td>
<td>V</td>
</tr>
<tr>
<td>VGS</td>
<td>High-side floating supply voltage</td>
<td>-0.3</td>
<td>220</td>
<td>V</td>
</tr>
<tr>
<td>Vgs0</td>
<td>High-side floating output voltage</td>
<td>Vgs+0.3</td>
<td>Vgs+0.3</td>
<td>V</td>
</tr>
<tr>
<td>VCC</td>
<td>Low-side fixed supply voltage</td>
<td>-0.3</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>VLD</td>
<td>Low-side output voltage</td>
<td>-0.3</td>
<td>Vcc+0.3</td>
<td>V</td>
</tr>
<tr>
<td>VSH</td>
<td>Input voltage</td>
<td>-0.3</td>
<td>Vcc+0.3</td>
<td>V</td>
</tr>
<tr>
<td>VDD</td>
<td>OC pin input voltage</td>
<td>-0.3</td>
<td>Vcc+0.3</td>
<td>V</td>
</tr>
<tr>
<td>VCCETT</td>
<td>OCSET1 pin input voltage</td>
<td>-0.3</td>
<td>Vcc+0.3</td>
<td>V</td>
</tr>
<tr>
<td>VCCETT2</td>
<td>OCSET2 pin input voltage</td>
<td>-0.3</td>
<td>Vcc+0.3</td>
<td>V</td>
</tr>
<tr>
<td>VDS</td>
<td>Allowable Vs voltage slew rate</td>
<td>-</td>
<td>50</td>
<td>V/μs</td>
</tr>
<tr>
<td>PD</td>
<td>Maximum power dissipation</td>
<td>-</td>
<td>1.25</td>
<td>W</td>
</tr>
<tr>
<td>RthJA</td>
<td>Thermal resistance, junction to ambient</td>
<td>-</td>
<td>100</td>
<td>°C/W</td>
</tr>
<tr>
<td>TJ</td>
<td>Junction temperature</td>
<td>-</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>TS</td>
<td>Storage temperature</td>
<td>-85</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>TL</td>
<td>Lead temperature (soldering, 10 seconds)</td>
<td>-</td>
<td>300</td>
<td>°C</td>
</tr>
</tbody>
</table>
### Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. The \( V_S \) and COM offset ratings are tested with all supplies biased at a 15 V differential.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_S )</td>
<td>High-side floating supply absolute voltage</td>
<td>( V_S+10 )</td>
<td>( V_S+18 )</td>
<td></td>
</tr>
<tr>
<td>( V_C )</td>
<td>High-side floating supply offset voltage</td>
<td>( V_S+10 )</td>
<td>200</td>
<td></td>
</tr>
<tr>
<td>( V_O )</td>
<td>High-side floating output voltage</td>
<td>( V_S )</td>
<td>( V_C )</td>
<td></td>
</tr>
<tr>
<td>( V_{DC} )</td>
<td>Low-side fixed supply voltage</td>
<td>10</td>
<td>18</td>
<td></td>
</tr>
<tr>
<td>( V_{LO} )</td>
<td>Low-side output voltage</td>
<td>0</td>
<td>( V_{DC} )</td>
<td></td>
</tr>
<tr>
<td>( V_{IN} )</td>
<td>Logic input voltage</td>
<td>0</td>
<td>( V_{DC} )</td>
<td></td>
</tr>
<tr>
<td>( V_{OC} )</td>
<td>OC pin input voltage</td>
<td>0</td>
<td>( V_{DC} )</td>
<td></td>
</tr>
<tr>
<td>( V_{OCSET1} )</td>
<td>OCSET1 pin input voltage</td>
<td>0</td>
<td>( V_{DC} )</td>
<td></td>
</tr>
<tr>
<td>( V_{OCSET2} )</td>
<td>OCSET2 pin input voltage</td>
<td>0</td>
<td>( V_{DC} )</td>
<td></td>
</tr>
<tr>
<td>( T_A )</td>
<td>Ambient Temperature</td>
<td>-40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

**Note 1:** Logic operational for \( V_S \) equal to -8 V to 200 V. Logic state held for \( V_S \) equal to -8 V to \( V_{BB} \).

### Dynamic Electrical Characteristics

\( V_{BB} \) = 15 V, \( C_L = 1 \mu F \) and \( T_A = 25 \) °C unless otherwise specified. Fig. 2 shows the timing definitions.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{on} )</td>
<td>High &amp; low-side turn-on propagation delay</td>
<td>60</td>
<td>80</td>
<td></td>
<td></td>
<td>( V_S=0 ) V</td>
</tr>
<tr>
<td>( t_{off} )</td>
<td>High &amp; low-side turn-off propagation delay</td>
<td>60</td>
<td>80</td>
<td></td>
<td></td>
<td>( V_S=0 ) V</td>
</tr>
<tr>
<td>( t )</td>
<td>Turn-on rise time</td>
<td>25</td>
<td>40</td>
<td></td>
<td></td>
<td>( V_S=0 ) V</td>
</tr>
<tr>
<td>( t )</td>
<td>Turn-off fall time</td>
<td>15</td>
<td>35</td>
<td></td>
<td></td>
<td>( V_S=0 ) V</td>
</tr>
<tr>
<td>( t_{osc} )</td>
<td>Shutdown propagation delay</td>
<td>140</td>
<td>200</td>
<td></td>
<td></td>
<td>( V_S=0 ) V</td>
</tr>
<tr>
<td>( t_{oc} )</td>
<td>Propagation delay time from ( V_S ) to ( V_{OCSET1} ) to ( V_{OCSET2} )</td>
<td>260</td>
<td></td>
<td></td>
<td>ms</td>
<td>( V_S=0 ) V</td>
</tr>
<tr>
<td>( t_{OC,max} )</td>
<td>OC pulse width</td>
<td>100</td>
<td></td>
<td></td>
<td></td>
<td>( V_S=0 ) V</td>
</tr>
<tr>
<td>( t_{OC,min} )</td>
<td>OC input filter time</td>
<td>200</td>
<td></td>
<td></td>
<td></td>
<td>( V_S=0 ) V</td>
</tr>
<tr>
<td>( DT_1 )</td>
<td>Deadtime: LO turn-off to HO turn-on (( DT_1 ) ( LO=H ) &amp; ( HO ) turn-on to ( LO ) turn-on (( DT_1 ) ( HO=LO ))</td>
<td>0</td>
<td>15</td>
<td>40</td>
<td></td>
<td>( V_{DT1} )</td>
</tr>
<tr>
<td>( DT_2 )</td>
<td>Deadtime: LO turn-off to HO turn-on (( DT_2 ) ( LO=H ) &amp; ( HO ) turn-on to ( LO ) turn-on (( DT_2 ) ( HO=LO ))</td>
<td>5</td>
<td>25</td>
<td>50</td>
<td></td>
<td>( V_{DT1} )</td>
</tr>
<tr>
<td>( DT_3 )</td>
<td>Deadtime: LO turn-off to HO turn-on (( DT_3 ) ( LO=H ) &amp; ( HO ) turn-on to ( LO ) turn-on (( DT_3 ) ( HO=LO ))</td>
<td>10</td>
<td>35</td>
<td>60</td>
<td></td>
<td>( V_{DT1} )</td>
</tr>
<tr>
<td>( DT_4 )</td>
<td>Deadtime: LO turn-off to HO turn-on (( DT_4 ) ( LO=H ) &amp; ( HO ) turn-off to ( LO ) turn-on (( DT_4 ) ( HO=LO ))</td>
<td>15</td>
<td>45</td>
<td>70</td>
<td></td>
<td>( V_{DT1} )</td>
</tr>
</tbody>
</table>
### Static Electrical Characteristics

\[ V_{BSAG} (V_{CC}, I_{DS}) = 15 \text{ V} \] and \[ T_A = 25 \text{ °C} \] unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IH} )</td>
<td>Logic high input voltage</td>
<td>2.5</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>( V_{CC}=10 \text{ V} ), ( I_{IN}=0 \text{ A} )</td>
</tr>
<tr>
<td>( V_{IL} )</td>
<td>Logic low input voltage</td>
<td>—</td>
<td>—</td>
<td>1.2</td>
<td>—</td>
<td>( V_{CC}=10 \text{ V} ), ( I_{IN}=0 \text{ A} )</td>
</tr>
<tr>
<td>( V_{OH} )</td>
<td>High level output voltage, ( V_{BSAG}-V_{OL} )</td>
<td>—</td>
<td>1.2</td>
<td>—</td>
<td>—</td>
<td>( V_{CC}=10 \text{ V} ), ( I_{IN}=0 \text{ A} )</td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>Low level output voltage, ( V_{O} )</td>
<td>—</td>
<td>—</td>
<td>0.1</td>
<td>—</td>
<td>( V_{CC}=10 \text{ V} ), ( I_{IN}=0 \text{ A} )</td>
</tr>
<tr>
<td>( U_{OCC+} )</td>
<td>( V_{CC} ) supply UVLO positive threshold</td>
<td>9.0</td>
<td>9.0</td>
<td>9.7</td>
<td>mA</td>
<td>( V_{IN}=3.3 \text{ V} ), ( I_{IN}=0 \text{ A} )</td>
</tr>
<tr>
<td>( U_{OCC-} )</td>
<td>( V_{CC} ) supply UVLO negative threshold</td>
<td>8.2</td>
<td>8.2</td>
<td>8.9</td>
<td>mA</td>
<td>( V_{IN}=0 \text{ V} ), ( I_{IN}=0 \text{ A} )</td>
</tr>
<tr>
<td>( U_{Vgs}+ )</td>
<td>High-side well UVLO positive threshold</td>
<td>9.0</td>
<td>9.0</td>
<td>9.7</td>
<td>mA</td>
<td>( V_{IN}=15 \text{ V} ), ( I_{IN}=10 \mu\text{A} )</td>
</tr>
<tr>
<td>( U_{Vgs}– )</td>
<td>High-side well UVLO negative threshold</td>
<td>8.2</td>
<td>8.2</td>
<td>8.9</td>
<td>mA</td>
<td>( V_{IN}=15 \text{ V} ), ( I_{IN}=10 \mu\text{A} )</td>
</tr>
<tr>
<td>( I_{QCC} )</td>
<td>High-side quiescent current</td>
<td>—</td>
<td>—</td>
<td>1</td>
<td>mA</td>
<td>( V_{IN}+V_{CC} ), ( I_{IN}=0 \text{ A} )</td>
</tr>
<tr>
<td>( I_{QCC} )</td>
<td>Low-side quiescent current</td>
<td>—</td>
<td>—</td>
<td>4</td>
<td>mA</td>
<td>( V_{IN}+V_{CC} ), ( I_{IN}=0 \text{ A} )</td>
</tr>
<tr>
<td>( I_{Q} )</td>
<td>High-to-low-side leakage current</td>
<td>—</td>
<td>—</td>
<td>50</td>
<td>mA</td>
<td>( V_{IN}=3.3 \text{ V} ), ( I_{IN}=0 \text{ A} )</td>
</tr>
<tr>
<td>( I_{IN} )</td>
<td>Logic “1” input bias current</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>—</td>
<td>( V_{IN}=3.3 \text{ V} ), ( I_{IN}=0 \text{ A} )</td>
</tr>
<tr>
<td>( I_{I} )</td>
<td>Logic “0” input bias current</td>
<td>—</td>
<td>0</td>
<td>1.0</td>
<td>—</td>
<td>( V_{IN}=0 \text{ V} ), ( I_{IN}=0 \text{ A} )</td>
</tr>
<tr>
<td>( I_{PH} )</td>
<td>Output high short circuit current (source)</td>
<td>1.0</td>
<td>1.0</td>
<td>—</td>
<td>A</td>
<td>( V_{IN}=0 \text{ V} ), ( I_{IN}=10 \mu\text{A} )</td>
</tr>
<tr>
<td>( I_{PL} )</td>
<td>Output low short circuit current (sink)</td>
<td>1.2</td>
<td>1.2</td>
<td>—</td>
<td>A</td>
<td>( V_{IN}=15 \text{ V} ), ( I_{IN}=10 \mu\text{A} )</td>
</tr>
</tbody>
</table>

\[ \begin{align*}
V_{GT1} & \leq 0.8(V_{CC}) \quad 0.9(V_{CC}) \quad 0.97(V_{CC}) \\
V_{GT2} & \leq 0.51(V_{CC}) \quad 0.57(V_{CC}) \quad 0.63(V_{CC}) \\
V_{GT3} & \leq 0.32(V_{CC}) \quad 0.36(V_{CC}) \quad 0.40(V_{CC}) \\
V_{GT4} & \leq 0.21(V_{CC}) \quad 0.29(V_{CC}) \quad 0.35(V_{CC}) \\
V_{ICOC+} & \leq 0.76 \quad 1.0 \quad 1.25 \\
V_{ICOC} & \leq -1.25 \quad -1.0 \quad -0.75
\end{align*} \]
# Lead Definitions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Low-side logic supply voltage</td>
</tr>
<tr>
<td>VB</td>
<td>High-side floating supply</td>
</tr>
<tr>
<td>HO</td>
<td>High-side output</td>
</tr>
<tr>
<td>VS</td>
<td>High-side floating supply return</td>
</tr>
<tr>
<td>IN</td>
<td>Logic input for high-side and low-side gate driver outputs (HO and LO), in phase with HO</td>
</tr>
<tr>
<td>DT/SD</td>
<td>Input for programmable deadtime, referenced to COM. shutdown LO and HO when tied to COM</td>
</tr>
<tr>
<td>COM</td>
<td>Low-side supply return</td>
</tr>
<tr>
<td>LO</td>
<td>Low-side output</td>
</tr>
<tr>
<td>OC</td>
<td>Over-current output (negative logic)</td>
</tr>
<tr>
<td>OCSET1</td>
<td>Input for setting negative over current threshold</td>
</tr>
<tr>
<td>OCSET2</td>
<td>Input for setting positive over current threshold</td>
</tr>
</tbody>
</table>

![IR20124S 14 Lead SOIC (narrow body)](image-url)
Figure 1. Switching Time Waveform Definitions

Figure 2. Shutdown Waveform Definitions
IRS20124S(PbF)

Figure 10A, Logic "1" Input Voltage vs. Temperature

Figure 10B, Logic "1" Input Voltage vs. Supply Voltage

Figure 11A, Logic "0" Input Voltage vs. Temperature

Figure 11B, Logic "0" Input Voltage vs. Supply Voltage
Figure 21: $V_{\text{DS(th)}}$ Undervoltage Threshold (+) vs. Temperature

Figure 22: $V_{\text{DS(th)}}$ Undervoltage Threshold (−) vs. Temperature

Figure 23: Output Source Current vs. Supply Voltage

Figure 24: Output Sink Current vs. Supply Voltage
Figure 25. Maximum Vg Negative Offset vs. Supply Voltage

Figure 26. DT Mode Select Threshold (1) vs. Temperature

Figure 27. DT Mode Select Threshold (2) vs. Temperature

Figure 28. DT Mode Select Threshold (3) vs. Temperature
Functional description

Programmable Dead-time

The IRS20124 has an internal deadtime generation block to reduce the number of external components in the output stage of a Class D audio amplifier. Selectable deadtime through the DT/SD pin voltage is an easy and reliable function, which requires only two external resistors. The deadtime generation block is also designed to provide a constant deadtime interval, independent of $V_{oc}$ fluctuations. Since the timings are critical to the audio performance of a Class D audio amplifier, the unique internal deadtime generation block is designed to be immune to noise on the DT/SD pin and the $V_{oc}$ pin. Noise-free programmable deadtime function is available by selecting deadtime from four preset values, which are optimized and compensated.

How to Determine Optimal Deadtime

Please note that the effective deadtime in an actual application differs from the deadtime specified in this datasheet due to finite fall time, $t_f$. The deadtime value in this datasheet is defined as the time period from the starting point of turn-off on one side of the switching stage to the starting point of turn-on on the other side as shown in Fig. 2. The fall time of MOSFET gate voltage must be subtracted from the deadtime value in the datasheet to determine the effective deadtime of a Class D audio amplifier.

\[
\text{(Effective deadtime)} = (\text{Deadtime in datasheet}) - (\text{fall time, } t_f)
\]

A longer deadtime period is required for a MOSFET with a larger gate charge value because of the longer $t_f$. A shorter effective deadtime setting is always beneficial to achieve better linearity in the Class D switching stage. However, the likelihood of shoot-through current increases with narrower deadtime settings in mass production. Negative values of effective deadtime may cause excessive heat dissipation in the MOSFETs, potentially leading to their serious damage. To calculate the optimal deadtime in a given application, the fall time $t_f$ for both output voltages, HO and LO, in the actual circuit needs to be measured. In addition, the effective deadtime can also vary with temperature and device parameter variations. Therefore, a minimum effective deadtime of 10 ns is recommended to avoid shoot-through current over the range of operating temperatures and supply voltages.
DT/SD pin

The DT/SD pin provides two functions: 1) setting dead-time and 2) shutdown. The IRS20124 determines its operation mode based on the voltage applied to the DT/SD pin. An internal comparator translates which mode is being used by comparing internal reference voltages. Threshold voltages for each mode are set internally by a resistive voltage divider off $V_{CC}$, negating the need of using a precise absolute voltage to set the mode.

![Deadtime Settings vs $V_{DD}$ Voltage](image)

**Design Example**

Table 1 shows suggested values of resistance for setting the deadtime. Resistors with up to 5% tolerance can be used if these listed values are followed.

![External Resistor](image)

<table>
<thead>
<tr>
<th>Deadtime mode</th>
<th>R1 (Ω)</th>
<th>R2 (Ω)</th>
<th>DT/SD (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DT1</td>
<td>&lt;10k</td>
<td>Open</td>
<td>1.00 (Vcc)</td>
</tr>
<tr>
<td>DT2</td>
<td>3.3k</td>
<td>8.2k</td>
<td>0.71 (Vcc)</td>
</tr>
<tr>
<td>DT3</td>
<td>6.6k</td>
<td>4.7k</td>
<td>0.46 (Vcc)</td>
</tr>
<tr>
<td>DT4</td>
<td>8.2k</td>
<td>3.3k</td>
<td>0.29 (Vcc)</td>
</tr>
</tbody>
</table>

**Shutdown**

Since IRS20124 has internal deadtime generation, independent inputs for HO and LO are no longer provided. Shutdown mode is the only way to turn off both MOSFETs simultaneously to protect them from over current conditions. If the DT/SD pin detects an input voltage below the threshold, $V_{DD}$, the IRS20124 will output 0 V at both HO and LO outputs, forcing the switching output node to go into a high impedance state.

**Over Current Sensing**

In order to protect the power MOSFET, IRS20124 has a feature to detect over current conditions, which can occur when speaker wires are shorted together. The over-current shutdown feature can be configured by combining the current sensing function with the shutdown mode via the DT/SD pin.

**Load Current Direction in Class D Audio Application**

In a Class D audio amplifier, the direction of the load current alternates according to the audio input signal. An over current condition can therefore happen during either a positive current cycle or a negative current cycle. It should be noted that...
each MOSFET carries a part of the load current in an audio cycle. Bi-directional current sensing offers over current detection capabilities in both cases by monitoring only the low side MOSFET.

Direction in MOSFET Current and Load Current

Bi-Directional Current Sensing

IRS20124 has an over-current detection function utilizing RSHDN of the low side switch as a current sensing shunt resistor. Due to the proprietary HVIC process, the IRS20124 is able to sense negative as well as positive current flow, enabling bi-directional load current sensing without the need for any additional external passive components.

IRS20124 measures the current during the period when the low side MOSFET is turned on. Under normal operating conditions, Vsd voltage for the low side switch is well within the trip threshold boundaries, VTHS+ and VTHS-. In the case of Fig. 9(b) which demonstrates the amplifier sourcing too much current to the load, the Vsd node is found below the trip level, VTHS-. In Fig. 9(c) with opposite current direction, the amplifier sinks too much current from the load, positioning Vsd well above trip level, VTHS+.

Once the voltage in Vsd exceeds the preset threshold, the OC pin pulls down to COM to detect an over-current condition.

Since the switching waveform usually contains overshoot and associated oscillatory artifacts on their transient edges, a 200 ns blanking interval is inserted in the Vsd voltage sensing block at the instant the low side switch is engaged. Because of this blanking interval, the OC function will be unable to detect over current conditions if the low side ON duration less than 200 ns.

Simplified Functional Block Diagram of Bi-Directional Current Sensing

The bi-directional current sensing block has an internal V level shifter feeding the signal to the comparator, OCSET. sets the threshold, and is given a trip level at VTHS-, which is \( \text{OCSET} \cdot -V \). In the same way, for a given \( \text{OCSET} \cdot V \text{\text{\_\_\_\_}} \) is set at \( \text{OCSET} \cdot V \).

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How to set OC Threshold

The positive and negative trip thresholds for bidirectional current sensing are set by the voltages at OCSET1 and OCSET2.

The trip threshold voltages, \( V_{\text{OCSET1}} \) and \( V_{\text{OCSET2}} \), are determined by the required trip current levels, \( I_{\text{trip}} \), in the low side MOSFET.

The sensed voltage of \( V_\text{S} \) is shifted up by 2.21 V internally and compared with the voltages fed to the OCSET1 and OCSET2 pins. The required value of OCSET with respect to COM is

\[
V_{\text{OCSET1}} = V_{\text{OCSET2}} + 2.21 \text{ V} = I \times R_{\text{RDS(ON)}} + 2.21 \text{ V}
\]

The same relation holds between OCSET1 and OCSET2.

In general, \( R_{\text{RDS(ON)}} \) has a positive temperature coefficient that needs to be considered when the threshold level is being set. Please also note that, in the negative load current direction, the sensing voltage at the \( V_\text{S} \) node is limited by the body diode of the low side MOSFET as explained later.

Design Example

This example demonstrates how to use the external resistor network to set \( I_{\text{trip}} \) and \( I_{\text{ltol}} \) to be \( \pm 11 \text{ A} \) using a MOSFET that has \( R_{\text{RDS(ON)}} = 90 \text{ \mu} \Omega \).

\[
\begin{align*}
V_{\text{SET1}} &= V_{\text{OCSET1}} + 2.21 \text{ V} = I_{\text{RDL}} \times R_{\text{RDS(ON)}} + 2.21 \text{ V} = 11 \times 60 \text{ \mu} \Omega + 2.21 \text{ V} = 2.87 \text{ V} \\
V_{\text{SET2}} &= V_{\text{OCSET2}} + 2.21 \text{ V} = I_{\text{RDL}} \times R_{\text{RDS(ON)}} + 2.21 \text{ V} = (-11) \times 60 \text{ \mu} \Omega + 2.21 \text{ V} = 1.55 \text{ V}
\end{align*}
\]

The total resistance of the resistor network is based on the voltage at the \( V_{\text{CC}} \) and required bias current in this resistor network.

\[
R_{\text{tot}} = R_3 + R_4 + R_5 = V_{\text{CC}} \div I_{\text{bias}} = 12 \text{ V} \div 1 \text{ mA} = 12 \text{ k} \Omega
\]

The expected voltage across R3 is \( V_{\text{CC}} - V_{\text{SET1}} = 12 \text{ V} - 2.87 \text{ V} = 9.13 \text{ V} \). Similarly, the voltages across R4 is \( V_{\text{OCSET2}} - V_{\text{CC}} = 2.87 \text{ V} - 1.55 \text{ V} = 1.32 \text{ V} \), and the voltage across R5 is \( V_{\text{SET2}} = 1.55 \text{ V} \) respectively.

\[
\begin{align*}
R_3 &= 9.13 \text{ V} \div 9.13 \text{ k} \Omega = 1 \text{ k} \Omega \\
R_4 &= 1.32 \text{ V} \div 1.32 \text{ k} \Omega = 1 \text{ k} \Omega \\
R_5 &= 1.55 \text{ V} \div 1.55 \text{ k} \Omega = 1 \text{ k} \Omega
\end{align*}
\]

Choose \( R_3 = 9.09 \text{ k} \Omega, R_4 = 1.33 \text{ k} \Omega, R_5 = 1.54 \text{ k} \Omega \) from E-9 series.

Consequently, actual threshold levels are

\[
\begin{align*}
V_{\text{OCSET1}} &= 2.88 \text{ V} \text{ gives } I_{\text{trip}} = 11.2 \text{ A} \\
V_{\text{OCSET2}} &= 1.56 \text{ V} \text{ gives } I_{\text{ltol}} = 11.0 \text{ A}
\end{align*}
\]

Resistors with 1% tolerances are recommended.
OC Output Signal

The OC pin is a 20 V open drain output. The OC pin is pulled down to ground when an over current condition is detected. A single external pull-up resistor can be shared by multiple IRS20124 OC pins to form the ORing logic. In order for a microprocessor to read the OC signal, this information is buffered with a mono stable multi vibrator to ensure 100 ns minimum pulse width. Because of unpredictable logic status of the OC pin, the OC signal should be ignored during power up/down.

Limitation from Body Diode in MOSFET

When a Class D stage outputs a positive current, flowing from the Class D amp to the load, the body diode of the MOSFET will turn on when the drain to source voltage of the MOSFET become larger than the diode forward drop voltage. In such a case, the sensing voltage at the V_D pin of the IRS20124 is clamped by the body diode. This means that the effective R DS(on) is now much lower than expected from R DS(on) of the MOSFET, and the Vs node my not able to reach the threshold to turn the OC output on before the MOSFET fails. Therefore, the region where body diode clamping takes a place should be avoided when setting V OC.
LEADFREE PART MARKING INFORMATION

ORDER INFORMATION
14-Lead SOIC IRS20124SPbF
14-Lead SOIC Tape & Reel IRS20124STRPbF
Appendix C

MOSFET Datasheet

**Features**
- Key parameters optimized for Class-D audio amplifier applications
- Low Rds(on) for improved efficiency
- Low Qfs for better THD and improved efficiency
- Low Qgs for better THD and lower EMI
- Low package stray inductance for reduced ringing and lower EMI
- Can deliver up to 100W per channel into 8Ω with no heatsink
- Dual sided cooling compatible
- Compatible with existing surface mount technologies
- RoHS compliant containing no lead or bromide
- Lead-Free (Qualified up to 260°C Reflow)
- Industrial Qualified

**Key Parameters**

<table>
<thead>
<tr>
<th>Vgs</th>
<th>100 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rds(on) typ. @ Vgs = 10V</td>
<td>51 mΩ</td>
</tr>
<tr>
<td>Qg typ.</td>
<td>8.3 nC</td>
</tr>
<tr>
<td>Rdeff typ.</td>
<td>3.5 Ω</td>
</tr>
</tbody>
</table>

**Description**

This Digital Audio MOSFET is specifically designed for Class-D audio amplifier applications. This MOSFET utilizes the latest processing techniques to achieve low on-resistance per silicon area. Furthermore, gate charge, body-diode reverse recovery and internal gate resistance are optimized to improve key Class-D audio amplifier performance factors such as efficiency, THD, and EMI.

The IRF7665S2TRPbF device utilizes DirectFET™ packaging technology. DirectFET™ packaging technology offers lower parasitic inductance and resistance when compared to conventional wirebonded SOIC packaging. Lower inductance improves EMI performance by reducing the voltage ringing that accompanies fast current transients. The DirectFET™ package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques, when application note AN-1005 is followed regarding the manufacturing method and processes. The DirectFET™ package also allows dual sided cooling to maximize thermal transfer in power systems, improving thermal resistance and power dissipation. These features combine to make this MOSFET a highly efficient, robust and reliable device for Class-D audio amplifier applications.

**Absolute Maximum Ratings**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vgs</td>
<td>100 V</td>
<td></td>
</tr>
<tr>
<td>Vds</td>
<td>± 20 A</td>
<td></td>
</tr>
<tr>
<td>Is @ Tj = 25°C, Continuous Drain Current, Vgs = 10V</td>
<td>14.4 A</td>
<td></td>
</tr>
<tr>
<td>Is @ Tj = 100°C, Continuous Drain Current, Vgs = 10V</td>
<td>19.2 A</td>
<td></td>
</tr>
<tr>
<td>Is @ Tj = 25°C, Pulsed Drain Current</td>
<td>4.1 A</td>
<td></td>
</tr>
<tr>
<td>Pd @ Tj = 25°C, Maximum Power Dissipation</td>
<td>30 W</td>
<td></td>
</tr>
<tr>
<td>Pd @ Tj = 100°C, Power Dissipation</td>
<td>15 W</td>
<td></td>
</tr>
<tr>
<td>Pd @ Tj = 25°C, Power Dissipation</td>
<td>2.4 W</td>
<td></td>
</tr>
<tr>
<td>Tj Linear Operating Junction and Storage Temperature Range</td>
<td>-55 to 175 °C</td>
<td></td>
</tr>
</tbody>
</table>

**Thermal Resistance**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>RthJA</td>
<td>83 °C/W</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RthJA</td>
<td>125 °C/W</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RthJA</td>
<td>20 °C/W</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RthJA</td>
<td>5.0 °C/W</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RthJC</td>
<td>1.4 °C/W</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Notes: © through ® are on page 2
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07/02/09
## Static @ $T_J = 25^\circ$C (unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{BDM}$-Drain-Source Breakdown Voltage</td>
<td>100</td>
<td>9.19</td>
<td></td>
<td>V</td>
<td>$V_{DD} = DV$, $I_D = 256\mu A$</td>
</tr>
<tr>
<td>$AV_{BDM}$-Drain-Source Breakdown Voltage</td>
<td>51</td>
<td>62</td>
<td></td>
<td>mΩ</td>
<td>$V_{DD} = 10V$, $I_D = 8.6\mu A$</td>
</tr>
<tr>
<td>$V_{GDM}$-Gate Threshold Voltage</td>
<td>8.0</td>
<td>4.2</td>
<td>6.2</td>
<td>V</td>
<td>$V_{GD} = V_{DD}$</td>
</tr>
<tr>
<td>$I_{DSS}$-Drain-Source Leakage Current</td>
<td></td>
<td>20</td>
<td></td>
<td>µA</td>
<td>$V_{DD} = 100V$, $V_{DS} = 6V$</td>
</tr>
<tr>
<td>$I_{GSS}$-Gate-to-Source Leakage Current</td>
<td></td>
<td>280</td>
<td></td>
<td>µA</td>
<td>$V_{DD} = 80V$, $V_{DS} = DV$, $T_J = 125^\circ$C</td>
</tr>
<tr>
<td>$G_{MAX}$-Gate-to-Source Forward Leakage</td>
<td></td>
<td>100</td>
<td></td>
<td>nA</td>
<td>$V_{DD} = 20V$</td>
</tr>
<tr>
<td>$R_{GSS}$-Gate-to-Source Reverse Leakage</td>
<td></td>
<td></td>
<td>-100</td>
<td>Ω</td>
<td>$V_{DD} = 20V$</td>
</tr>
</tbody>
</table>

## Dynamic @ $T_J = 25^\circ$C (unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$g_{ds}$-Total Gate Charge</td>
<td>6.3</td>
<td>13</td>
<td></td>
<td>mS</td>
<td>$V_{DD} = 50V$</td>
</tr>
<tr>
<td>$C_{gss}$-Gate-to-Source Charge</td>
<td>1.8</td>
<td></td>
<td></td>
<td>µF</td>
<td>$V_{DD} = 10V$</td>
</tr>
<tr>
<td>$C_{gss}$-Gate-to-Source Charge</td>
<td>0.77</td>
<td></td>
<td></td>
<td>µF</td>
<td>$V_{DD} = 20V$</td>
</tr>
<tr>
<td>$R_{gs}$-Gate-to-Drain Charge</td>
<td>3.2</td>
<td></td>
<td></td>
<td>mΩ</td>
<td>$V_{DD} = 20V$</td>
</tr>
<tr>
<td>$R_{gd}$-Gate Output Resistance</td>
<td>2.8</td>
<td></td>
<td></td>
<td>Ω</td>
<td>$V_{DD} = 20V$</td>
</tr>
<tr>
<td>$D_{on}$-Switch Delay (on $Q_{uk}$)</td>
<td></td>
<td>6.0</td>
<td></td>
<td>mΩ</td>
<td>$V_{DD} = 20V$</td>
</tr>
<tr>
<td>$r_{on}$-Turn-OFF Delay Time</td>
<td>3.3</td>
<td></td>
<td></td>
<td>mΩ</td>
<td>$V_{DD} = 20V$</td>
</tr>
<tr>
<td>$t_{on}$-Turn-On Delay Time</td>
<td>9.8</td>
<td></td>
<td></td>
<td>ns</td>
<td>$V_{DD} = 20V$</td>
</tr>
<tr>
<td>$t_{off}$-Fall Time</td>
<td>3.1</td>
<td></td>
<td></td>
<td>ns</td>
<td>$V_{DD} = 20V$</td>
</tr>
<tr>
<td>$C_{in}$-Input capacitance</td>
<td></td>
<td>515</td>
<td></td>
<td>nF</td>
<td>$V_{DD} = 20V$</td>
</tr>
<tr>
<td>$C_{out}$-Output capacitance</td>
<td>122</td>
<td></td>
<td></td>
<td>nF</td>
<td>$V_{DD} = 20V$</td>
</tr>
<tr>
<td>$C_{rec}$-Reverse Transfer Capacitance</td>
<td>35</td>
<td></td>
<td></td>
<td>nF</td>
<td>$f = 1MHz$</td>
</tr>
<tr>
<td>$C_{max}$-Output Capacitance</td>
<td>333</td>
<td></td>
<td></td>
<td>nF</td>
<td>$V_{DD} = 20V$, $V_{DS} = 16V$, $f = 1MHz$</td>
</tr>
<tr>
<td>$C_{out}$-Output Capacitance</td>
<td>87</td>
<td></td>
<td></td>
<td>nF</td>
<td>$V_{DD} = 20V$, $V_{DS} = 40V$, $f = 1MHz$</td>
</tr>
<tr>
<td>$C_{eff}$-Effective Output Capacitance</td>
<td>115</td>
<td></td>
<td></td>
<td>nF</td>
<td>$V_{DD} = 20V$, $V_{DS} = 40V$, $f = 100KHz$</td>
</tr>
</tbody>
</table>

### Avalanche Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_{PE}$-Single Pulse Avalanche Energy</td>
<td></td>
<td>27</td>
<td></td>
<td>µJ</td>
</tr>
<tr>
<td>$I_{A}$-Avalanche Current</td>
<td></td>
<td>6.8</td>
<td></td>
<td>A</td>
</tr>
</tbody>
</table>

### Diode Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{D}$-Continuous Drain Current</td>
<td></td>
<td>16.6</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{DM}$-Pulsed Drain Current (Body Diode)</td>
<td></td>
<td>569</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>$V_{f}$-Diode Forward Voltage</td>
<td></td>
<td>1.0</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$t_{f}$-Reverse Recovery Time</td>
<td></td>
<td>32</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{o}$-Reverse Recovery Time</td>
<td></td>
<td>36</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

**Notes:**
- ①: Positive gate voltage, pulse with limited by max. junction temperature.
- ②: Drain $V_{DD} = 25V$, $I_D = 0.4mA$, $R_D = 250\Omega$, $I_{DD} = 8.6\mu A$.
- ③: Suffix mounted on 1 in. square Du bond.
- ④: Pulse width ≤ $400\mu s$, duty cycle ≤ 2%.
- ⑤: $C_{gss}$-eff is a fixed capacitance that gives the same charging time as $C_{gss}$ while $V_{DD}$ is rising from 0 to $8.6\mu A$, $V_{DD}$.
- ⑥: Used double sided copper, mounting pad.
- ⑦: Mounted on minimum footprint fixture board with metalized bond and with small strip bonding.
- ⑧: $T_{Q}$ measured with thermal couple mounted to top (Drain) pad.
- ⑨: $T_{f}$ measured at $T_{Q}$ of approximately $90^\circ$C.
- ⑩: Based on testing done using a typical device and evaluation board at $V_{DD}=12V$, $f=400KHz$, and $T_{Q}=25^\circ$C. The delta base temperature $\Delta T_{B} = 55^\circ$C.

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Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance vs. Temperature

Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

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Fig 7. Typical Source-Drain Diode Forward Voltage

Fig 8. Maximum Drain Current vs. Case Temperature

Fig 9. Threshold Voltage vs. Temperature

Fig 10. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient
Fig 17a. Gate Charge Test Circuit

Fig 17b. Gate Charge Waveform

Fig 18. Diode Reverse Recovery Test Circuit for N-Channel HEXFET® Power MOSFETs
DirectFET Auto™ Board Footprint, SB (Small Size Can).

Please see AN-1036 for DirectFET assembly details and stencil and substrate design recommendations.
DirectFET™ Outline Dimension, SB Outline (Small Size Can).

Please see AN-1035 for DirectFET assembly details and stencil and substrate design recommendations.

<table>
<thead>
<tr>
<th>CODE</th>
<th>MIN</th>
<th>MAX</th>
<th>MIN</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>4.75</td>
<td>4.85</td>
<td>0.105</td>
<td>0.115</td>
</tr>
<tr>
<td>B</td>
<td>3.70</td>
<td>3.85</td>
<td>0.154</td>
<td>0.165</td>
</tr>
<tr>
<td>C</td>
<td>2.75</td>
<td>2.85</td>
<td>0.105</td>
<td>0.115</td>
</tr>
<tr>
<td>D</td>
<td>0.25</td>
<td>0.40</td>
<td>0.014</td>
<td>0.016</td>
</tr>
<tr>
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DirectFET™ Part Marking

GATE MARKING
LOGO
PART NUMBER
BATCH NUMBER
DATE CODE
Line above the first 3 characters of the date code indicates "Lead-Free"
DirectFET™ Tape & Reel Dimension (Showing component orientation).

NOTE: Controlling dimensions in mm
Default quantity is 4400 pcs/pkg

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<th>IMPERIAL</th>
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Data and specifications subject to change without notice.
This product has been designed and qualified to MCL1 rating for the industrial market.
Additional storage requirement details for DirectFET products can be found in application note AN1035 on IR's Web site.
Qualification Standards can be found on IR's Web site.

International Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.
Appendix D

Speaker Datasheet

FEATURES:
- Outdoor design, suited for out-door and in-door use;
- Small volume, 700 x 610 x 1040 mm³;
- Weight 45kg, equipped with bracket for hanging from three points;
- Dispersion 40° X 60°, the 130 meter from the loudspeaker sound level still attain 91dB;
- Wide frequency, sound clear and sonorously.

FREQ. RESPONSE

INPUT VOLTAGE: 70V/140V
RATED POWER: 100W/200W
FREQUENCY RESPONSE: 70Hz-18kHz
SENSITIVITY: 108dB
MAX SOUND LEVEL: 131dB
DISPERSION(H°V°): 40° X 60°
( 50Hz-4kHz, -10dB )

DSPPAACOUSTIC TECHNOLOGY CO., LTD.
Appendix E

Improved Version Schematics
## Appendix F

### Soundpressure Measurements

**Soundpressure vs input voltage (Music)**

<table>
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<tr>
<th>$V_i$ (mV)</th>
<th>$p_{SPL}$ (dB)</th>
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**Soundpressure vs input voltage (Helicopter)**

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**Soundpressure vs input voltage (Gunshot)**

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## Appendix G

### Powerconsumption Measurements Improved Version

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