TrACS: Transceiver Architecture and Wireless Channel Simulator

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ABSTRACT

This paper presents the design of a system-level simulator for radio receivers, including receiver circuits, in Matlab. The system level outlook offers a better characterization of circuit design, as the signal processing in the digital receiver is asymmetric across topologies. Also, circuit models in the simulator make it more precise and realistic compared to baseband models, which assume a single-step error-free down conversion. This interpretation is especially relevant in the design of energy-constrained wireless sensor network solutions. The simulator results for binary FSK in AWGN confirm the importance of system level simulation.

Categories and Subject Descriptors

B.4.4 [**Input/Output and Data Communications**]: Performance Analysis and Design Aids – *Formal models, Simulation, Verification.* B.7.2 [**Integrated Circuits**]: Design Aids – V*erification.*

General Terms

Performance, Design, Theory, Verification.

Keywords

Wireless sensor node design, receiver, simulator, transceiver circuits, system-level design and performance verification.

1. INTRODUCTION

Wireless sensor node design has become synonymous with energy- constrained solutions, as energy in the sensor node is a scarce resource. The emphasis on low power design extends to both the circuit and the signal processing in the receiver of the sensor node [14]. Low power circuit design is an active area of research, with a few circuit architectures well identified for their performance [5], [10]. Circuit architectures down-convert signals received by the antenna and digitize it. While doing so, they corrupt signals with additive noise and scaling. In addition, circuits are non-linear, though constrained to operate in linear mode. Some of these impairments are compensated after the signal is digitized. Also, the low power constraint pushes more of the receiver functionality into the digital domain. These factors alone make it difficult to characterize the performance of the circuit in isolation.

The baseband equivalent model, often used to describe a communication link, assumes that the down-conversion is a single step error free process. Circuit-induced impairments are not included on the grounds that they can be neglected, especially in spread spectrum systems. These impairments, though small, gain importance in the context of low power design.

The scarce energy resource has motivated many cross layer optimization algorithms in the digital receiver [8], [9], [15]. This simulator is a combined model of the analog circuit and the digital receiver in Matlab, providing a platform for a cross-domain study of circuit design and wireless communications. The implicit assumption that the signal processing acts uniformly across all topologies is investigated in this paper. Previous work includes [15], which makes the point that the impact of different types of hardware models is mostly not considered in such studies. The WINS [3] and PicoRadio [12] are involved in the design of a wireless sensor node on an integrated chip. Thoonen looks at a few system level considerations for low-power wireless networks [18]. ADS Ptolemy provides a simulation of the total communications system path, but not in Matlab [1]. This is a disadvantage to engineers from outside the circuit domain who stand to benefit from cross-domain studies. TrACS (**Tr**ansceiver **A**rchitecture and Wireless **C**hannel **S**imulator) presents a unique platform to test energy conservation schemes – both circuit and signal processing – and study the system level performance.

2. SIMULATOR CONCEPT

The simulator models the communication link shown in Fig. 1. The transmitter and receiver circuit are modeled in Matlab along with the wireless channel, to account for all the signal modifications between the digital transmitter and receiver. The simulator consists of five modifiable blocks, each chosen from options based on constraints and the wireless scenario.

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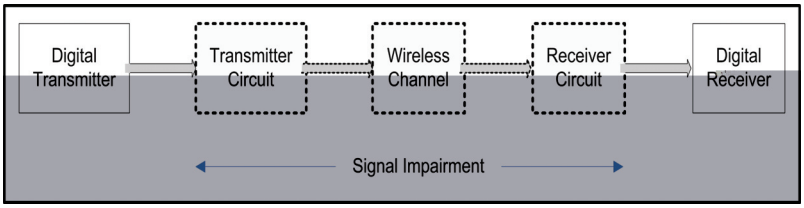

Figure 1. Block Diagram of a Communication Link.

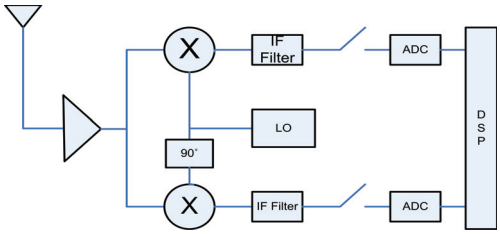

Figure 2. Block Diagram of the Low IF Architecture.

The transmitter and receiver circuits are implemented through various topologies. This paper presents the modeling of receiver low-power topologies. Low-IF and Direct Conversion receivers are often the only alternatives considered, but the class of sub-sampling receivers is an active area of research and is included in the simulator. Each of these topologies affects the signal in different ways, which are identified and modeled as described in Section III.

The digital transmitter and receiver along with the wireless channel are modeled in Matlab. Only the physical (PHY) layer is implemented – this includes pulse shaping, spread spectrum and modulation. The wireless channel models include AWGN (Additive White Gaussian Noise) and fading channels.

The digital transceiver uses the baseband model, where the complex equivalent is used to represent the RF signal. This amounts to removing the frequency content of the signal and modeling the complex envelope to quicken the simulations. But, circuit models are passband and need to be translated to the baseband.

The simulator provides a cohesive platform for system-level verification of RF circuit design. Along with the circuit design, digital receiver algorithms for power conservation and signal compensation can be tested simultaneously to determine the effect on the BER (Bit Error Rate) of the system. The simulator aids the circuit designer in choosing the receiver architecture given the PHY layer and the wireless scenario. Finally, this simulator could help identify optimal solutions in a test bed for wireless sensor networks.

3. SIMULATOR DESIGN

The design of the simulator is covered under three sections. The baseband equivalent model is used to represent the signal.

3.1 Modeling Receiver Topologies

Three widely used topologies are modeled in the simulator. The up-conversion and down-conversion are not performed; the signal remains in the baseband throughout the simulation. But, each block of the receiver affects the signal in a unique manner, and this is translated to the baseband for the purpose of modeling.

3.1.1 Low IF Architecture

This is the super-heterodyne architecture with a low IF (1-10 MHz). The low IF simplifies filter design, but the image filter requirements become steep. This requires the use of a quadrature receiver, which permits image cancellation. The block diagram of a typical low IF receiver is shown in Fig. 2.

The received signal is down-converted, sampled and digitized. These are implied in the baseband representation and not done explicitly. Only the signal impairments are modeled to simulate the topology. The signal is amplified by the LNA (Low Noise Amplifier) gain factor. Non-linearities in the circuit introduce inter-modulation products, which may saturate the circuit. Only the third order products form a part of the filtered signal and cause interference. The inter-modulation signal amplitude is calculated as $A_{IM3} = \alpha A_{in}^3 / A_{IP3}^2$; where, A_{in} is the input amplitude of the desired signal, α is the LNA Gain and A_{IP3} is the input IP3 of the circuit. [13]. This is a bandpass signal, which is modeled in baseband after down-conversion and low pass filtering.

$$A_{IM3}\left[e^{j2\pi f_{IM}t} + e^{-j2\pi f_{IM}t}\right] \times 2e^{-j2\pi f_c t} = 2A_{IM3}e^{j2\pi(f_{IM}-f_c)t} \qquad (1)$$

where, f_{IM} is the inter-modulation product frequency and f_c is the carrier frequency. Thus, a complex signal at the difference frequency is added as the inter-modulation signal.

The local oscillator introduces some errors. Reciprocal mixing refers to the mismatch of the LO center frequency and is modeled as white noise of power $S_0.\Delta B$. [13]. The phase angle may vary, causing a distortion, which is modeled by multiplying the signal with a random phase φ. Both these errors occur after the down-conversion, when the signal is at the IF frequency. Translating to baseband, this results in a power of 4 ($S_0.\Delta B$).

The mixer causes an image frequency to also down-convert to the same IF. Though image cancellation is employed, this is never perfect because of imbalances in the quadrature arms. The diminished image is modeled by adding a low-power baseband signal to the desired signal.

Sampling jitter corrupts the signal, and this distortion is modeled with white noise. The variance is taken to be $P_j = 2\pi^2 f_{in}^2 A^2 \sigma_j^2$; where f_{in} is the maximum frequency of the sampled signal (f_{IF}), A is the input signal amplitude and σ_j is the square root of the variance of the sample and hold circuit. [16]. Finally, the ADC introduces a quantization error, which lies uniformly between [-Δ/2, Δ/2]. Δ is the step-size of the quantizer. The impairments added to model the Low IF architecture are summarized in Fig. 3.

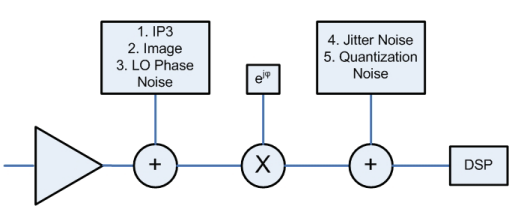

Figure 3. Model of the Low IF Architecture.

3.1.2 *Direct Conversion Architecture*

This is the homodyne or zero-IF architecture where the signal is directly down-converted to the base band. Simplicity of design and the lack of need for an image-reject filter are some of the advantages of this topology. But, the signal is its own image here, and there is interference between the upper and lower side bands. To cancel the interference, a quadrature receiver is required. The block diagram for this architecture is shown in Fig. 4.

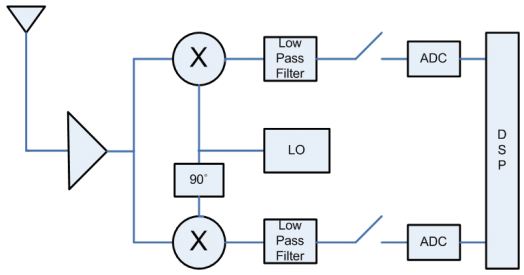

Figure 4. Block Diagram of the DC Architecture.

The signal impairments are translated to the baseband as before. The signal is amplified by the LNA gain. Non-linearities are of concern here as well, but only the second order inter-modulation products. The low pass filter removes the third order interference. The inter-modulation signal amplitude is calculated as $A_{IM2} = \alpha A_{in}^2 / A_{IP2}$; where, A_{in} is the input amplitude of the desired signal, α is the LNA Gain and A_{IP2} is the input IP2 of the circuit. [13]. This is a baseband signal, appearing at the frequency f_{IM}.

The local oscillator errors are modeled as before, with the exception that the translation to baseband is not required. Image cancellation is imperfect due to imbalances in the quadrature branches. This is modeled as –

$$\begin{aligned} Real\{rx\} &= Real\{rx\}\cdot\left(1+\varepsilon/2\right)\cdot\cos\left(\theta/2\right) - Imag\{rx\}\cdot\left(1+\varepsilon/2\right)\cdot\sin\left(\theta/2\right) \\ Imag\{rx\} &= -Real\{rx\}\cdot\left(1-\varepsilon/2\right)\cdot\sin\left(\theta/2\right) + Imag\{rx\}\cdot\left(1-\varepsilon/2\right)\cdot\cos\left(\theta/2\right) \end{aligned} \quad (2)$$

where, ε is the imbalance in amplitude and θ is the phase difference between the two branches. [13].

The signal is in the baseband and stray DC offsets in the circuit add to the desired signal. DC offset from three main sources is modeled. a) Self-mixing of local oscillator signals leaking into the RF port of the mixer and the input port of the LNA. This is modeled as K_1+A.K_2; where K_1 is the attenuation of the LO signal leaking into the mixer, K_2 is the attenuation of the LO signal leaking into the LNA and A is the LNA gain factor. b) Self-mixing of LO signals leaking into, radiated from and reflected back to the antenna. This is modeled with a complex sinusoid at the Doppler shifted frequency (f_{DS}; near baseband) of amplitude A.K_3; where K_3 is the attenuation of the LO signal leaking into the antenna. c) Self-mixing of strong in-band interferers leaking into the LO port of the mixer from the output of the LNA. This is modeled with a complex sinusoid at the difference frequency (between in-band interferer and carrier frequency: f_O) of amplitude A.K_4; where K_4 is the attenuation of interfering signal leaking into the LO port of the mixer from the output of the LNA. [11].

The circuit exhibits a low-frequency noise known as flicker noise or 1/f noise. This is represented as random white noise of a user-input power level in the baseband. The sampling jitter and quantization error are modeled as before. The impairments added to model the Direct Conversion architecture are summarized in Fig. 5.

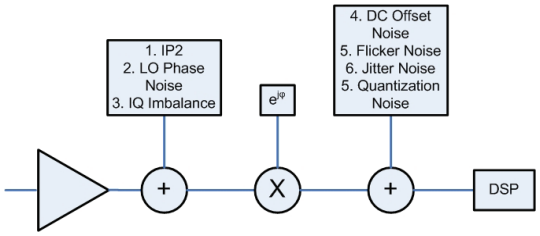

Figure 5. Model of the DC Architecture.

3.1.3 *IF Sub-sampling Architecture*

The intermediate frequency in the low IF architecture is sometimes too high for the ADC. The signal is bandpass and can be down-sampled. But, the reduction in sampling frequency comes at the cost of aliasing noise. The block diagram for this topology is shown in Fig. 6.

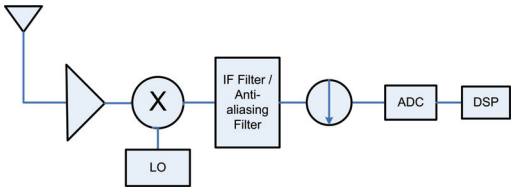

Figure 6. Block Diagram of the IF-SS Architecture.

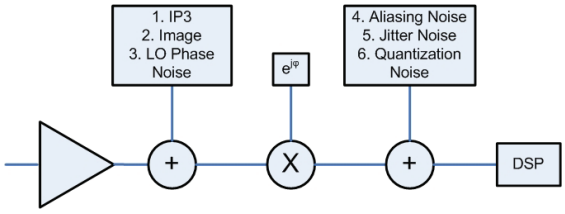

Figure 7. Model of the IF-SS Architecture.

The error sources in this model are the same as for the Low-IF architecture, with the addition of aliasing noise due to inadequate anti-alias filtering. To model the aliasing noise, we look at down sampling in detail – assume the bandpass signal bandwidth is B, the anti-aliasing filter bandwidth is B_f and the sampling frequency is F_s. The unfiltered noise is folded over at the folding frequency given by f_{fold}.

$$f_{fold} = f_c + B/2 - F_s/4 + B/2; f_{fold} = \begin{cases} f_c - F_s/4 + B; \ldots F_s > 2B \\ f_c + B/2; \ldots F_s = 2B \end{cases} \quad (3)$$

The total noise is the noise floor of the un-sampled signal multiplied by the number of times the noise is folded over. Let this number be n_{fold}.

$$n_{fold} = \frac{\left(f_c + B_f/2\right) - \left(f_{fold}\right)}{F_s/2} + 1; n_{fold} = \begin{cases} \frac{B_f}{F_s} - \frac{2B}{F_s} + \frac{3}{2}; \ldots F_s > 2B \\ \frac{B_f}{F_s} + \frac{1}{2}; \ldots F_s = 2B \end{cases} \quad (4)$$

The final model is given in Fig. 7.

3.2 Digital Transceiver Design

The digital transceiver consists of the network software layers, but this simulator implements only the PHY layer - including modulation schemes, pulse shaping and spread spectrum.

The modulation schemes implemented in the simulator are the popular options for wireless sensor networks. The low power constraint necessitates simple receiver circuits, and limits us to the basic modulation techniques. DPSK (Differential Phase Shift Keying) and O-QPSK (Offset Quadrature Phase Shift Keying) are the formats used in the ZigBee standard. BPSK (Binary Phase Shift Keying) and QPSK (Quadrature Phase Shift Keying) are the simplest modulation schemes used in fading channels and BFSK (Binary Frequency Shift Keying) is a well-researched technique for low power receiver circuits.

The rectangular pulse shape has been provided as a default option, along with the raised cosine pulse and half-sine pulse. Direct Sequence spread spectrum is included in the model.

3.3 Wireless Channel Model

Wireless sensor networks can be used in a staggering number of wireless scenarios. For the purpose of simulation, only the simplest AWGN and fading channels are modeled. Fading channels include flat and frequency selective fading, with Rayleigh and Rician models. Doppler fading is also included as an option in the model.

4. CASE STUDY

The simulation results for BFSK in an AWGN channel are compared for the three topologies and the system level perspective is investigated. This simple case study has been provided to demonstrate the use of a system simulator.

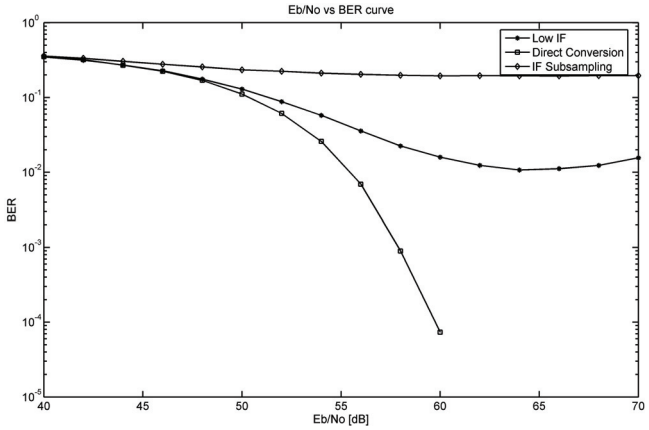

Figure 8. Chip Error Rate versus Eb/No.

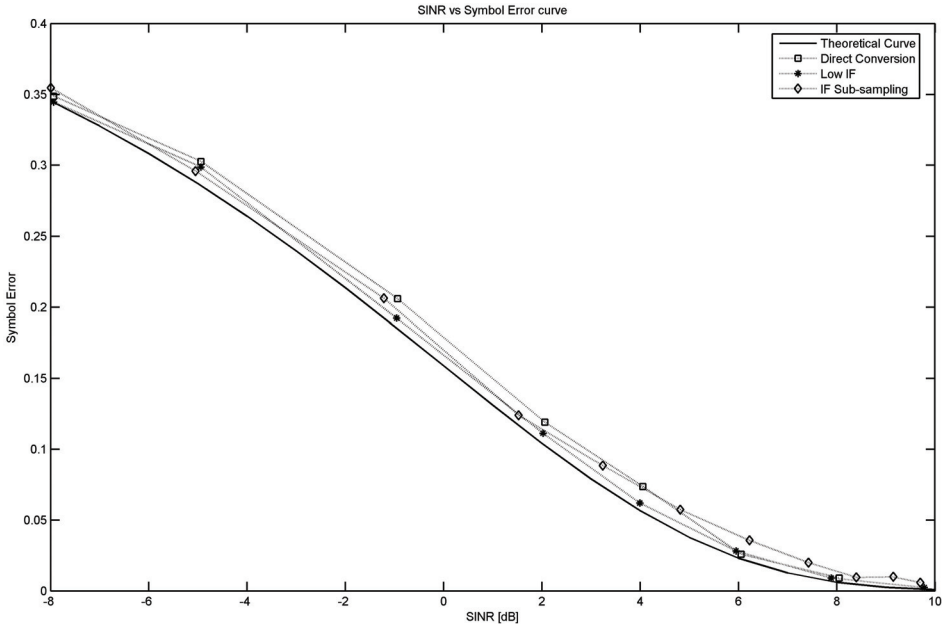

Figure 9. Symbol Error Rate versus Signal to Interference and Noise Ratio (SINR).

4.1 Binary FSK

Binary FSK has the advantage of zero power at DC. A simple logical analysis can lead to the conclusion that the Direct Conversion architecture provides the best results as most of the interference is at DC. But, these conclusions are supported by studies based on circuit simulation results alone.

4.2 Simulation Results

The results can be computed at two points in the system. Conventionally, circuit performance is measured at the ADC. This results in a Chip Error Rate versus Eb/No. But, the system performance is better estimated at the end of the digital receiver to give a Bit Error Rate versus SINR (Signal to Interference and Noise Ratio).

A comparison of the Chip Error Rate curves for the three topologies is presented in Fig. 8. The Direct Conversion topology indeed seems to perform better.

A comparison of the Bit Error Rate curves for the architectures is presented in Figure 9. These curves are similar for all three architectures, within reasonable limits. The interference signals are attenuated by the processing gain of the spread spectrum system. However, the processing gain is not equal across the topologies as the errors (narrowband interference and white Gaussian noise) introduced by each topology are not the same. The equalization in performance can be attributed to this.

The Bit Error Rate is a system level performance indicator as against the Chip Error Rate, which is more directly a circuit performance indicator as it measures the SNR (Signal to Noise Ratio) at the ADC. Thus, the simulation results at the system level indicate an almost equal performance for all three architectures. Now, digital compensation techniques for each of the architectures can be rated against their computational complexity and the optimum solution can be chosen taking the hardware or signal processing constraints into account.

5. CONCLUSION

The simulator presented in this paper provides a shared platform for circuit and signal processing techniques in low power receivers. The advantage offered to circuit designers is system level performance verification along with digital compensation and power-conservation algorithms. The simulator provides a novel interpretation of the communication link, treating the receiver circuit as part of the channel.

The simulator performance was tested against well-known results for binary FSK. The results matched the previously known conclusions, while offering a new and useful perspective at the system level.

6. ACKNOWLEDGMENTS

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