Exploration of Target Architecture for a Wireless Camera Based Sensor Node

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Abstract. The challenges associated with wireless vision sensor networks are low energy consumption, less bandwidth and limited processing capabilities. In order to meet these challenges different approaches are proposed. Research in wireless vision sensor networks has been focused on two different assumptions, first is sending all data to the central base station without local processing, second approach is based on conducting all processing locally at the sensor node and transmitting only the final results. Our research is focused on partitioning the vision processing tasks between Senor node and central base station. In this paper we have added the exploration dimension to perform some of the vision tasks such as image capturing, background subtraction, segmentation and Tiff Group4 compression on FPGA while communication on microcontroller. The remaining vision processing tasks i.e. morphology, labeling, bubble remover and classification are processed on central base station. Our results show that the introduction of FPGA for some of the visual tasks will result in a longer life time for the visual sensor node while the architecture is still programmable.

I. INTRODUCTION

Typically Vision Sensor Nodes (VSN) in Wireless Vision Sensor Networks (WVSN) consists of a camera for acquiring images, a processor for local image processing and a transceiver for communicating the results to the central base station. Due to the technological development in image sensors, sensor networking, distributed processing, low power processing and embedded systems smart camera networks can perform complex tasks using limited resources such as batteries, a wireless link and with a limited storage facility. Such camera based networks could easily be installed in out-doors areas where there is a limited availability of power, where access is difficult and it is inconvenient to modify the locations of the nodes or frequently change the batteries. VSN have been designed and implemented on microcontroller and microprocessor [1,4]. Often these solutions have high power consumption and moderate processing capabilities. Due to rapid development in the semiconductor technology, the single chip capacity of Field Programmable Gate Array (FPGA) increases greatly while its power consumption decreases tremendously [15]. Presently FPGA chips consist of many cores which makes it ideal candidate for the designing of VSN. As VSN needs to be capable of performing complex image processing such as image compression, which needs a lot of processing. High processing requirement is increased for an increased image size. Attention must be paid to the hardware/software co-design strategy to meet both processing and power requirements of VSN [8]. In [9] the authors designed a novel VSN based on a low cost, low power FPGA plus microcontroller System on Programmable Chip (SOPC). The authors in [10] have implemented a computer vision algorithm in hardware. They have provided a comparison of hardware and software implemented system using the same algorithm. It is concluded that hardware implemented system achieved a superior performance. A vision based sensor network for health care hygiene was implemented in [11]. The system consisted of a low resolution CMOS image sensor and FPGA processor which were integrated with a microcontroller and a ZigBee standard wireless transceiver. A design methodology for mapping computer vision algorithm onto an FPGA through the use of coarse grain reconfigurable data flow graph was discussed in detail in [5] and [13]. The pros and cons of FPGA technology and its suitability for computer vision task were discussed in detail in [3] and its optimization in [12] and [14]. The large amount of data generated by a vision sensor node requires a great deal of energy for processing and transmission bandwidth compared to other types of sensor networks. Both on board processing and communication influence energy consumption of sensor node and that more on board processing reduces the energy consumption due to communication and vice versa [1]. Different software and hardware approaches are proposed in order to minimize the energy consumption in wireless sensor networks [1,4,6]. FireFly Mosaic [4] wireless camera consists of a wireless sensor platform which uses a real-time distributed image processing infrastructure with a collision free TDMA based communication protocol. The FireFly is a low-cost, low power sensor platform that uses a real time operating system and an expansion board. SensEye [6] is a multi-tier

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of heterogeneous wireless nodes and cameras which aims at low power, low latency detection and low latency wakeup. In this low power elements are used to wakeup high power elements. Partitioning a task in hardware and software parts has significant effects on the system costs and performance. FPGA can be configured to perform specific task with better performance metric than certain embedded platforms. In our work we perform vision tasks i.e. image capturing, subtraction, segmentation and Tiff Group4 compression on FPGA, communication on SENTIO32 [2] platform while some vision processing tasks i.e. morphology, labeling, bubble remover and classification on central base station. Our results show that using FPGA for vision processing, microcontroller for communication and central base station for particular vision tasks result in a longer life time for the Visual Sensor Node. Following introduction, Section II recapitulates the test system, Section III considers target architecture, Section IV and V show results and conclusion respectively.

II. TEST SYSTEM

The application for our work is the detection of magnetic particles in a flowing liquid. The particles are classified both by their size and number and this system is used for failure detection in machinery. The flowing liquid in the system might contain air bubbles which can be identified and removed. The following are the main stages of our algorithm.

Pre-Processing: In this step the image is captured using CMOS camera. The captured image is then subtracted from the background image which is stored in Flash memory followed by segmentation.

Image Compression: Tiff Group4 compression is performed after segmentation shown in Fig.2 which reduced the data from 300x800 bytes to 500 bytes. This improved the results because few hundred bytes of data is sent over wireless link which lead to minimum energy consumption.

Bubble Remover: Bubbles can be identified as moving objects, so if an object changes its location in two consecutive frames, it is identified as a bubble. In the pixel based method [7] the bubbles are removed after the morphological operations shown in Fig.2 at point A, while in the object based method the bubbles are removed after classification as shown at point B in Fig.2.

Morphology, Labeling and Classification: Morphological operations are performed to remove one to two pixel false objects. Each object is assigned a unique label. Following this, the area and location of each object is determined.

In Fig.1, images are taken from a setup of the system in which A is the image when current image is subtracted from the background image, B is the image after segmentation and C is the result after the morphological operation while D is the final results when bubbles are removed.

III. TARGET ARCHITECTURE

Based on results of our research work [7] it was concluded that, if a compressed binary image after segmentation is sent from sensor node to server over the wireless link, it will result in a longer life time for the sensor node. Reason is that, at this stage the energy consumption due to the processing and communication are in such a proportion that it will result in the minimum energy consumption. Performing the same vision tasks on FPGA would further improve the results. Communication portion is handled on SENTIO32 platform [2], while other vision processing tasks such as morphology, labeling, classification and bubbles remover are shifted to the central base station. The target architecture for our current research is presented in Fig.2 which includes FPGA, SENTIO32 and central base station. A suitable FPGA architecture is very important as the leakage current in FPGA significantly affects the results. For analysis purpose we used Xilinx Spartan 6 Low Power FPGA and Actel IGLOO Low-Power Flash FPGA. SENTIO32 is a platform for wireless sensor networks developed at Mid Sweden University and has a high performance, low power AVR32 32bit RISC MCU running at 60MHz for only 23.5mA. It has a CC2520 RF transceiver with 2.4 GHz IEEE 802.15.4 and on-board antenna. It has 256KB flash, 32KB SRAM and a low sleep current of 60μA. CMOS image sensor is used for image capturing. The central base station will perform other vision processing tasks such as morphology, labeling, bubble remover and classification.

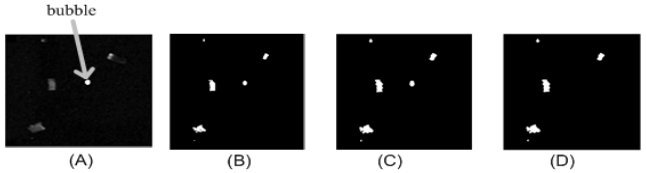

Figure 1.Background subtraction (A), Segmentation (B), Morphology (C), and Bubble Remover (D)

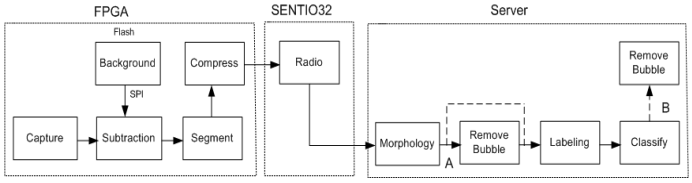

Figure 2.Target Architecture

IV. RESULTS

The execution time of vision tasks i.e. image capturing, background subtraction, segmentation and Tiff Group4

compression is calculated and compared for both SENTIO32 and FPGA platforms. While calculating time on SENTIO32 a high signal was sent on one of the output pins of the SENTIO32 when vision processing get started and then made it low when the task finished. During this operation time stamp was recorded using logic analyzer. The execution time on FPGA is determined by the camera speed at which it is capturing images because all other modules are running at the camera clock speed. The execution time for same vision processing tasks is calculated on FPGA, embedded with a CMOS camera of 300x800 resolutions and a frequency of 10 MHz. It must be noted that there are 32 black pixels after each row and each vision task has a latency of 1 clock cycle, so the execution time for four tasks i.e. image capturing, background subtraction, segmentation and Tiff group4 compression is calculated as

$$T = (300 \times (800 + 32) + 4) \times 10^{-7}$$

Time spent on communication is calculated as

$$T\_IEEE = (X + 19) \cdot 0.000032 + 0.000192$$

where X is the number of bytes transmitted.

Table 1 shows the energy consumption of individual components in the sensor node. The total energy spent on sending compressed data (500 bytes) over wireless link will be combination of IEEE 802.15.4 and SENTIO32 platform energy consumption.

TABLE 1. ENERGY CONSUMPTION OF INDIVIDUAL COMPONENTS

Component	I (mA)	V (v)	T (ms)	E (mJ)
Light	15	3.3	1.484	0.0734
Camera	35	3.3	9.2857	1.1
IEEE 802.15.4	40	3.3	16.8	2.2176
SENTIO32	23.5	3.3	16.8	1.302
FPGA	6,81 mW		24.960	0.169

Table 2 shows a comparison of the energy consumption when compression after segmentation is processed on FPGA (Xilinux Spartan 6) and SENTIO32 (AVR32) separately. During processing, SENTIO32 consumes 74.642 mJ energy while same vision processing tasks on FPGA consume 0.169 mJ energy. In Table 2 E_TARGET and T_TARGET are the energies consumed and the time spent on the computation of the operations respectively.

TABLE 2. ENERGY OF PROCESSING FOR BEST CASE: COMPRESSION AFTER SEGMENTATION ON TWO DIFFERENT PLATFORMS

Processing Platform	No.of bytes produced	T_TARGET (ms)	E_TARGET (mJ)
SENTIO32	500	951.49	74.642
FPGA	500	24.960	0.169

Fig.3 shows the absolute energy consumption due to processing and communication on software and hardware implemented platforms for different partition strategies. It can be observed that compression after segmentation (COMPRESS_AF_SEG_SOFTWARE) has minimum energy consumption compared to other strategies such as when all processing is done at a local node and only features are sent to server shown by FEATURES_SOFTWARE bar. The energy consumption is further reduced when the same vision tasks are performed on FPGA with small leakage current, evident from the bar COMPRESS_AF_SEG_FPGA. Fig.4 shows relative energy consumption for the same data. We can observe that communication energy is dominant over the processing energy.

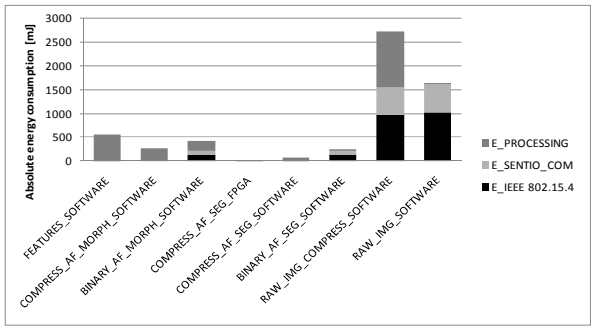

Figure 3. Absolute energy consumption for each partition strategy

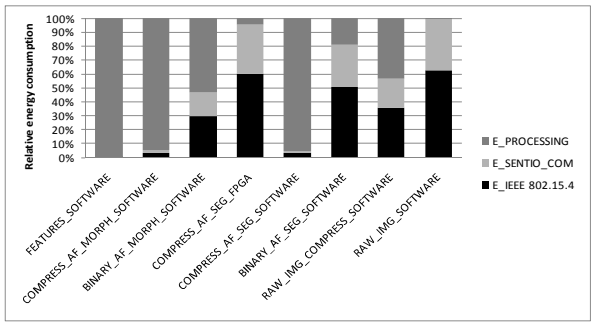

Figure 4. Relative energy for each partition Strategy

As discussed previously, the leakage current significantly affects the result. Fig.5 shows this fact when the sample period is increasing the sleep energy is dominating and with a sample period of 480 minutes it is completely prevailing.

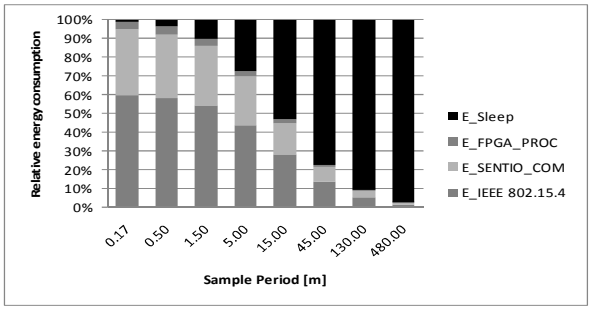

Figure 5. Energy consumption showing sleep energy dominancy

The life time of the vision sensor node is predicted on SENTIO32 and FPGA platforms using 4 AA batteries

shown in Fig.6 for different partition strategies. When compressed images after segmentation are sent from sensor node, the maximum life time of 1.04 years can be achieved with a sample period of 1.5 minutes for a full software solution, shown in Fig.6. This optimal case is evaluated for a solution implemented on FPGA with a small and large static current. The life time has dramatically increased when the same vision tasks were performed on FPGA with a static power consumption of 5µW (FPGA1), the life time is increased to 5.04 years while it results in 1.16 months (0.097 year) with high static power of 12.44 mW (FPGA2). Thus, the selection of suitable FPGA architecture is very important as the leakage current has profound impact on the results.

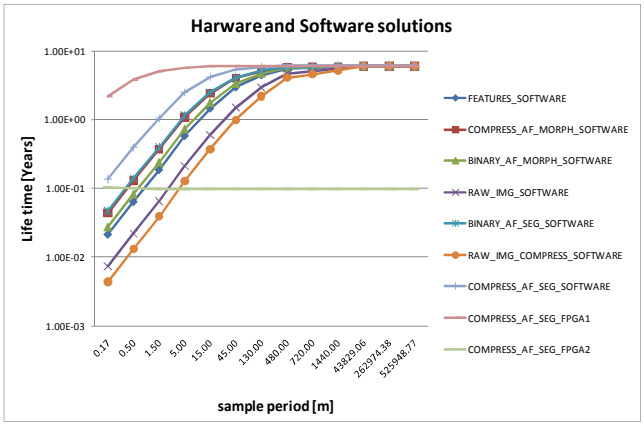

Figure 6.Life time of sensor node for different partition strategies

V. CONCLUSION

We have shown that partitioning between local and central computation and portioning tasks on particular platform affects the energy consumption in visual sensor nodes. The sensor node with software implementation results in minimum life time when compressed raw data was sent over wireless link. This was the worst case in software implemented sensor node. The best case in software solution was when compressed images after segmentation were sent over wireless link and it results in maximum life time of the sensor node. A life time of 1.04 years was predicted with a sample period of 1.5 minutes using 4 AA batteries. We have shown that if the local processing is performed on an FPGA having small static current, life time of 5.04 years can be achieved. By employing FPGA for the local vision tasks the energy consumption can be reduced by over 400 times and it increases the system life time upto 4.8 times. Most importantly life time is still 2.19 years with increased sampling period of 10 sec in case of FPGA while in case of software solution sensor node has only 1.6 months life time.

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