Wideband Sigma-Delta Modulators

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Abstract

Sigma-delta modulators (SDM) have come up as an attractive candidate for analog-to-digital conversion in single chip front ends thanks to the continuous improving performance. The major disadvantage is the limited bandwidth due to the need of oversampling. Therefore, extending these converters to broadband applications requires lowering the oversampling ratio (OSR) in order. The aim of this thesis is the investigation on the topology and structure of sigma-delta modulators suitable for wideband applications, e.g. wireline or wireless communication system applications having a digital baseband about one to ten MHz.

It has recently become very popular to feedforward the input signal in wideband sigma-delta modulators, so that the integrators only process quantization errors. The advantage being that the actual signal is not distorted by opamp and integrator nonlinearities. An improved feedforward 2-2 cascaded structure is presented based on unity-gain signal transfer function (STF). The improved signal-to-noise-ratio (SNR) is obtained by optimizing zero placement of the noise transfer function (NTF) and adopting multi-bit quantizer. The proposed structure has low distortion across the entire input range.

In high order single loop continuous-time (CT) sigma-delta modulator, excess loop delay may cause instability. Previous techniques in compensation of internal quantizer and feedback DAC delay are studied especially for the feedforward structure. Two alternative low power feedforward continuous-time sigma-delta modulators with excess loop delay compensation are proposed. Simulation based CT modulator synthesis from discrete time topologies is adopted to obtain the loop filter coefficients. Design examples are given to illustrate the proposed structure and synthesis methodology.

Continuous time quadrature bandpass sigma-delta modulators (QBSDM) efficiently realize asymmetric noise-shaping due to its complex filtering embedded in the loops. The effect of different feedback waveforms inside the modulator on the NTF of quadrature sigma-delta modulators is presented. An observation is made that a complex NTF can be realized by implementing the loop as a cascade of complex integrators with a SCR feedback digital-to-analog converter (DAC), which is desirable for its lower sensitivity to loop mismatch. The QBSDM design for different bandpass center frequencies relative to the sampling frequency is illustrated.

The last part of the thesis is devoted to the design of a wideband reconfigurable sigma-delta pipelined modulator, which consists of a 2-1-1 cascaded modulator and a pipelined analog-to-digital convertor (ADC) as a multi-bit quantizer in the last stage. It is scalable for different bandwidth/resolution application. The detail design is presented from system to circuit level. The prototype chip is fabricated in TSMC 0.25um process and measured on the test bench. The measurement results show that a SNR over 60dB is obtained with a sampling frequency of 70 MHz and an OSR of ten.

Keywords: sigma-delta modulator, feedforward, reconfigurable, quadrature bandpass filtering.
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Chapter 1

Introduction

1.1 Background

Nowadays the world is becoming more and more digital due to the development of digital computing and signal processing. Digital circuits are less sensitive to the disturbances and more robust compared to the analog counterparts. In addition, the digital circuits are easier to integrate on a chip to realize complicated functions. Nevertheless, the signals we are dealing with naturally are analog: voice, image, etc. As a consequence, an interface between analog and digital world is a must to convert an analog signal into a digital signal which we usually refer as analog-to-digital convert (ADC).

The development of ADCs, however, lags far behind the fast development of digital circuit since analog designs gets less benefits from the continuous scaling down of complementary metal-oxide-semiconductor (CMOS) technology due to the reducing voltage headroom. Therefore the ADCs become increasingly the bottleneck in many signal processing systems. Any improvement in the field of the ADCs always leads to system improvements.

There are mainly two classes of ADCs, distinguished according to the ratio of the sampling frequency $f_s$ and the signal bandwidth $f_B$

- Nyquist rate ADCs: $f_s = 2f_B$; the flash, the interpolating, the folding, the algorithmic, the successive approximation register (SAR), the pipelined ADCs belong to Nyquist rate ADC.

- Oversampling ADCs: $f_s$ equals multiple ($> 2$) $f_B$; The sigma-delta, error-feedback ADC belong to this class.

Different types of converters require vastly different architectures, design techniques, and therefore has different performance metrics. As illustrated in Fig. 1.1, every type of ADC architecture shows its optimum performance range in terms of resolution and bandwidth requirements.
ADCs are widely used in the application fields such as audio, video, sensor, instrumentation, and digital communication. In Fig. 1.2, we show an overview of applications vs. their requirements on bandwidth and resolution.

Corresponding to the Fig. 1.1, oversampling ADC is the best candidate for audio applications (the generally accepted standard range of audible frequencies is 20 to 20k hertz) since it can achieve over 16 bits resolution. The major disadvantage is the limited bandwidth due to the need of oversampling. So in Video applications that require a higher bandwidth, pipelined ADC is more favorable due to its high speed while medium resolution. Sensor converters are very application specific and they have wide range of resolution and frequency bandwidth requirements.

### 1.2 Motivation

In wireline communications, the digital subscriber line (DSL) standards allow very high transmission rates over ordinary telephone lines. ADCs used in these appli-
applications need to satisfy bandwidth requirements ranging from 2.5MS/s to 25MS/s, with typical resolutions on the order of 13 to 14 bits.

In modern wireless communication system design, the current trend is to move the analog-to-digital interface as far forward in the signal path as possible. Also, the emerging trend in 4th generation cellular system is to integrate cellular and wireless local area networks (WLANs) into the same handheld mobile phone. To allow multi-standard operation, the ADCs have to meet the needs of large signal bandwidth and high dynamic range. Shown in Table 1.1 are some specifications for different standards. The WCDMA standard requires a high-speed medium resolution converter while GSM requires a high resolution and medium speed converter. For WLAN even higher converter speeds than for WCDMA are needed. This imposes a challenging task on ADC design.

In communication system applications, pipelined ADCs and sigma-delta ADCs attract more research efforts. However, the former should be extended to high resolution and the latter to higher bandwidth. In this thesis, we will focus on the

![Figure 1.2. Application areas of ADCs](image)
new structure of sigma-delta ADCs, which is suitable for high bandwidth operation while still with a high resolution.

1.3 Outline and Contributions

In this thesis, we aim at exploring sigma-delta structures suitable for wideband applications. Both discrete-time and continuous-time modulators are considered and some novel structures are proposed. Possible solutions to non-ideal effects in sigma-delta modulators are presented. This thesis is organized into seven chapters.

- **Chapter 2** Fundamentals of ADCs are described and the concept of the sigma-delta converter is introduced, as well as some design issues related to modulator design. Also presented are the state-of-the-art performance published during recent years.

- **Chapter 3** In this chapter, a low distortion sigma-delta modulator is introduced. Based on that, an improved wideband low distortion cascaded sigma-delta structure is presented. Most of the material was published in:
  X. Yuan, A. Gothenberg and X. Wu, "Improved Wideband Low Distortion Cascaded Delta-Sigma Modulator," -In proceedings of The 5th Int. Workshop of SoC for Real-Time Applications (ISWOC’05), Alberta, Canada, July, 2005.

- **Chapter 4** In this chapter, a feedforward continuous time sigma-delta modulator structure with new loop delay compensation scheme is presented. Some of the content appear in:

- **Chapter 5** In this chapter, the effect of different feedback DAC schemes on the design of continuous time quadrature bandpass sigma-delta modulators is compared. The results appear at:

- **Chapter 6** In this chapter, the design of a wideband reconfigurable sigma-delta pipelined modulator is presented, which consists of a 2-1-1 cascaded modulator and a pipelined ADC as a multi-bit quantizer in the last stage.

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Chapter 7 Finally, the results of this dissertation are summarized and some future work are proposed.

Other Publications


2. X. Yuan, and S. Signell, "Hybrid CT DT Sigma-Delta Modulator with 1.5b Quantizer," -In proceedings of SSoCC’07, Sweden, May, 2007.
Chapter 2

Overview of Sigma-Delta Modulators

2.1 ADC Fundamentals

An ideal model of an ideal analog-to-digital convertor (ADC) consists of two parts: sampling and quantization, as shown in Fig. 2.1.

![Figure 2.1. Ideal ADC concept](image)

2.1.1 Ideal Sampling and Aliasing

The discrete-time representation is typically obtained through periodic sampling, $x[n] = x[nT_s]$, where $T_s = 1/f_s$ is the uniform sampling time and $f_s$ the sampling frequency. In order to fully reconstruct the signal, $f_s$ has to fulfil the sampling theorem:

$$f_s > 2f_B,$$

(2.1)

where $f_B$ is the signal bandwidth. Usually an anti-alias-filter (AAF) must precede the ADC.

2.1.2 Quantization Noise

The input-output characteristic of an ADC is shown in Fig. 2.2 (a). The ADC takes an analog input and converts it into discrete levels, resulting in an offset.
digital output code from 0...0 to 1...1. The number of code bits, N, represents the resolution of an ADC. Notice that the ADC output saturates for large input values. The conversion range without overloading is referred as the full scale (FS) range of the converter and the step size is defined as $\Delta = FS/2^N$. Due to the limited number to represent the input value, there is an error between input and output, $q(n) = y(n) - x(n)$, except for few points. This error is referred as the quantization error, as shown in Fig. 2.2 (b). As long as the input signal remains between $-FS/2$ and $FS/2$, the quantization error is bounded between $-\Delta/2$ and $\Delta/2$. Under certain circumstances - for example, the resolution of the converter is high and the ADC remains in the non-overload region - the quantization error is assumed to be uncorrelated white noise with a uniformly distributed amplitude of $\Delta/2$. The probability density function (PDF) is shown in Fig. 2.3. The total quantization noise power can be calculated as

$$
\sigma_q^2 = \int_{-\infty}^{\infty} q^2 \cdot PDF(q) \cdot dq = \frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} q^2 \cdot dq = \frac{\Delta^2}{12}.
$$

(2.2)

The quantization noise is a fundamental limitation in data converters that can be used to represent the basic performance of the ADC.

### 2.1.3 ADC Performance Metrics

In order to better understand the performance limitations in data converter, some parameters are used to specify the behavior of an ADC. A sinusoidal signal is often used to characterize a data converter.
2.1. ADC FUNDAMENTALS

- **Signal to Noise Ratio (SNR):** The ratio between the power of the sinusoidal signal and the total noise power excluding harmonics within the maximum signal bandwidth. For an ideal ADC with a full scale sine wave input \( A = FS/2 \) without causing saturation, the maximum SNR is given by:

\[
SNR = \frac{A^2}{\sigma_q^2} = 3 \cdot 2^{2N-1}
\]  

Expressed in dB:

\[
SNR[dB] = 10 \log_{10}(SNR) = 6.02N + 1.76(dB)
\]  

Hence the \( SNR[dB] \) is increased by 6 dB for every additional bit in a data converter.

- **Signal to Noise and Distortion Ratio (SNDR):** The SNDR is defined as the ratio of the fundamental frequency of the signal and the total noise power including distortion within the maximum signal bandwidth.

- **Effective Number of Bits (ENOB):** The effective resolution of the converter is derived from above equation with distortion included:

\[
ENOB = \frac{SNDR[dB] - 1.76}{6.02}
\]

- **Dynamic Range (DR):** The ratio between the power of the full scale (FS) input signal and the power of the smallest detectable input signal (usually \( SNDR=0 \)).
• **Spurious Free Dynamic Range (SFDR):** The ratio of the power of the input signal to the power of the highest harmonic or spurious noise component.

Fig. 2.4 shows the typical characteristic of an ADC: the SNR increases when the input power increases, but to a certain level the performance degrades due to the larger harmonic distortion.

### 2.2 Sigma-Delta Modulator Basic Theory

Sigma-Delta ADCs or ΣΔ ADCs are based on the principle that the input signal is oversampled and the quantization noise is shaped and later removed by digital filters.

#### 2.2.1 Oversampling

In Nyquist ADC, the sampling frequency is twice of the maximum signal bandwidth, i.e. $f_s = 2f_B$. If an ADC operates at a sampling frequency much higher than the Nyquist rate ($f_s \geq 2f_B$), the in-band noise power will be reduced. The oversampling ratio (OSR) is defined as the ratio between the sampling frequency and the Nyquist
rate:

\[ OSR = \frac{f_s}{2f_B}. \] (2.6)

The power of the quantization noise can be calculated with equation

\[ N_q^2 = \frac{1}{f_s} \int_{-f_B}^{f_B} \sigma_q^2 df = \frac{\sigma_q^2}{OSR}. \] (2.7)

Compared to a Nyquist converter, the noise power is reduced by OSR.

Since the signal bandwidth is much smaller than \( f_s/2 \), the requirements on the anti-alias filter can be relaxed.

**2.2.2 Sigma-Delta Concept**

Although the quantization noise is reduced by 3dB per octave of oversampling according to equation 2.6, the improvement is fairly small. A more efficient way is to shape the quantization noise up to higher frequency, i.e. less quantization noise remains in the band of interest while higher at the out of band. Therefore, the number of bits in the loop can be less than that in a Nyquist ADC. A system that can do this is known as a sigma-delta modulator.

A sigma-delta modulator has three important components, depicted in Fig. 2.5(a).

- A loop filter \( H(z) \)
- An internal quantizer
- A feedback digital-to-analog converter (DAC)

The quantizer can be single-bit or multi-bit. It is a strongly nonlinear component especially in the single-bit case, which makes exact modeling very complicated analytically. A linearized model is shown in Figure 2.5(b), where the quantizer is replaced by an adder with additive quantization noise. The output is the function of the input and quantization noise:

\[
Y(z) = \frac{H(z)}{1 + H(z)} \cdot X(z) + \frac{1}{1 + H(z)} \cdot Q(z)
= STF(z) \cdot X(z) + NTF(z) \cdot Q(z),
\] (2.8)

where \( STF(z) \) and \( NTF(z) \) is the signal transfer function (STF) and noise transfer function (NTF), respectively.

**2.2.3 Low Order Sigma-Delta Modulator**

Fig. 2.6 shows the first and second order sigma-delta modulators. For the first-order modulator, the loop filter is a simple forward-Euler integrator, with the transfer function:

\[ H(z) = \frac{z^{-1}}{1 - z^{-1}}. \] (2.9)
Figure 2.5. Sigma-delta modulator (a) structure (b) linearized model
Two respective transfer functions can be calculated using equation 2.8:

\[ STF(z) = \frac{H(z)}{1 + H(z)} = z^{-1}. \]  

(2.10)

and

\[ NTF(z) = \frac{1}{1 + H(z)} = 1 - z^{-1}. \]  

(2.11)

For the \( STF(z) \), it is a single clock period delay. The \( NTF(z) \) is a first-order high pass transfer function. This means that the quantization noise is first-order shaped, as shown in Fig. 2.7. The total noise in-band of interest is:

\[ N_q^2 = \frac{\sigma_q^2}{f_s} \int_{-f_s}^{f_s} |1 - e^{-j2\pi f/f_s}|^2 \ df \approx \frac{\sigma_q^2 \cdot \pi^2}{3 \cdot OSR^3}. \]  

(2.12)

Each doubling of the OSR reduces the noise by 9dB.
In the second-order case, the transfer functions are as following:

\[ STF(z) = z^{-2} \]  \hspace{1cm} (2.13)

and

\[ NTF(z) = (1 - z^{-1})^2. \]  \hspace{1cm} (2.14)

The inband noise is:

\[ N_q^2 \approx \frac{\sigma_q^2}{f_s} \int_{f_B}^{f_s/2} | (1 - e^{-j2\pi f/f_s})^4 | df \approx \frac{\sigma_q^2 \pi^4}{5OSR^5}. \]  \hspace{1cm} (2.15)

The PSD is also shown in Fig. 2.7. Compared to a first-order modulator, a second-order modulator has SNR improvements of 15 dB per octave of oversampling.

### 2.2.4 Higher Order Sigma-Delta Modulator

The order of the modulator can be even higher, resulting in further improvements. A general NTF with order of \( L \) is:

\[ N_q(z) = (1 - z^{-1})^L \cdot Q(z). \]  \hspace{1cm} (2.16)

Therefore, the power of the quantization error can be calculated as

\[ N_q^2 \approx \frac{\sigma_q^2 \pi^{2L}}{2L + 1} \cdot \frac{1}{OSR^{2L+1}}. \]  \hspace{1cm} (2.17)
If the internal quantizer of the modulator is $N$ bits, the step size equals $FS/2^N$ and the maximum amplitude of the sinusoidal input signal can be $FS/2$. The ideal obtainable dynamic-range is:

$$DR = \frac{3 \cdot 2L + 1}{\pi 2^L} OSR^{2L+1} (2^N - 1)^2.$$  (2.18)

Equation 2.18 clearly shows the influence of the sigma-delta modulator parameters: the order of the loop filter $L$, the number of quantization bits $N$ and the oversampling ratio $OSR$. The ideal $SNR$ improvements with $OSR$ is shown in Fig. 2.8, for the different $L$ and $N$. Some basic observations can be made based on the equation and figure. The $SNR$ increases with oversampling ratio, order or the number of quantization bits. However, if the oversampling ratio is increased, the sampling frequency should also be increased if the bandwidth is kept same which consumes more power. Increasing the order may cause stability problem and multi-bit quantization has nonlinearity issues.
2.2.5 Stability

Although a high-order modulator can be used to efficiently shape the quantization noise out of the band, simulations reveal that modulators employing high-order NTF are often unstable. The stability of a single-bit sigma-delta modulator is difficult to analyze, because of the nonlinearity involved. The most popular technique is to model the quantizer as a block with a varying gain $\lambda$ [3]. The pole locations of the NTF are then analyzed as a function of the quantizer gain. Some methods use numerical computer-aided optimizers to find NTF poles and zeros locations for minimizing in-band quantization noise subjected to some design constraints such as [4]

$$A_{OL} = 1 - \frac{\|ntf\|_1 - 2}{2^N - 1},$$  \hspace{1cm} (2.19)

where $\|ntf\|_1$ is the 1-norm of the impulse response $ntf(n)$ for the noise transfer function $NTF(z)$. Lee [5] argues that $\|ntf\|_{\infty} < 2$ whereas Agrawal [6] proposed the criterion $\|ntf\|_{\infty}^2 < 3$.

Other methods focus on designing the NTF for a sigma-delta modulator such that its SNR can be maximized when an OSR and an order are given. For example, a Butterworth or an inverse-Chebyshev function is used for the NTF denominator design and then proper zeros are added to its numerator [7].

2.2.6 Single Loop Topologies

To realize a stable high order modulator, poles are introduced into its $NTF$, as shown below:

$$NTF = \frac{(1-z^{-1})^L}{D(z)}.$$ \hspace{1cm} (2.20)

The purpose of adding the polynomial $D(z)$ is to flatten the high frequency portion of $NTF$. Different topologies exist to implement the same $NTF$. These topologies can be roughly divided into two classes: multiple feedback (FB) and feedforward (FF). If a chain of integrators are used, two main types of topology result [7]:

1. Chain of integrators with distributed feedback, distributed feedforward, and local resonator feedbacks, referred as CIFB

2. Chain of integrators with weighted feedforward summation and local resonator feedbacks, referred as CIFF

The advantages and disadvantages for each type are compared below:

- **CIFB**: For the CIFB topology shown in Fig. 2.9, the loop filter transfer function:

$$H(z) = \frac{f_1}{(z-1)^n} + \frac{f_2}{(z-1)^{n-1}} + \frac{f_3}{(z-1)^{n-2}} \cdots$$ \hspace{1cm} (2.21)
A small negative feedback term $g_i$ around pairs of integrators in the loop filter is used to shift zeros from DC to some in-band frequency in the NTF. The in-band quantization noise power can be further reduced [8].

- **CIFF**: The CIFF topology is shown in Fig. 2.10.

In CIFF topology, only the error signal is fed into the loop filter. This signal consists primarily of quantization noise. The first integrator can have large gain to suppress the subsequent stage’s noise and distortion. While in CIFB topology, the entire output signal, including the input signal and the quantization noise, is fed back to every internal node of the filter and each integrator has larger swing compared with that in the CIFF topology.

The NTFs are the same in the two figures, however, their STF are different. The STF of the CIFF topology features first-order filtering beyond the unity-gain frequency $f_u$ of the loop while the CIFB topology has $L$-order filtering.
2.2.7 MASH Topologies

Due to the stability problem of the single-loop single-bit oversampling modulators of high order (more than 2), multi-stage architecture (MASH) is developed to implement higher order loops without stability problems. Stages are cascaded and each of them can be first order or second order. The quantization noise in each stage is acquired and digitized by a subsequent stage, then it is canceled out through the digital error-cancellation-logic.

Shown in Figure 2.11 is a 2-1 cascaded sigma-delta modulator, which consists of a second-order modulator ($\Sigma\Delta_1$) and a first-order one ($\Sigma\Delta_2$). The output of the first stage modulator ($\Sigma\Delta_1$) is given by

$$Y_1(z) = z^{-2}X(z) + (1 - z^{-1})^2 Q_1(z).$$  \hfill (2.22)

And the output of the second stage ($\Sigma\Delta_2$) can be written as

$$Y_2(z) = z^{-1} \cdot g_1 \cdot Q_1(z) + (1 - z^{-1})Q_2(z),$$  \hfill (2.23)

where $\lambda_1$ is assumed to be 1, and can be adjusted to achieve better performance based on simulation, and $g_1$ is the inter-stage gain to scale the quantization noise.
2.2. SIGMA-DELTA MODULATOR BASIC THEORY

The final output is obtained by cancelling out the quantization noise, $Q_1(z)$, of the first stage via an error-cancellation-logic (ECL):

$$Y(z) = Y_1(z)H_1(z) + Y_2(z)H_2(z).$$

(2.24)

To have a third-order noise shaping, i.e. $(1 - z^{-1})^3$, the ECL should be

$$H_1(z) = z^{-1}$$
$$H_2(z) = \frac{1}{g_1}(1 - z^{-1})^2.$$  

(2.25)

By substituting them into equation 2.24, we get the ideal output

$$Y(z) = z^{-3}X(z) + \frac{1}{g_1}(1 - z^{-1})^3Q_2(z),$$

(2.26)

which indicates that the quantization noise is shaped by the NTF of both modulators.

The main drawback of the MASH topologies is their sensitivity to circuit parameter variations and component mismatch. The cancellation of the first stage noise is based on the match of analog NTF of the first stage and the digital error-cancellation-logic of the second stage. The deviation from ideal characteristics of the first stage NTF results in incomplete noise cancellation and leakage of the first stage noise to the output.

2.2.8 Non-Idealities

Equation 2.18 indicates the ideal performance of the sigma-delta modulator, which only takes into account the white quantization noise. However, in practice there are several non-idealities to be considered.

**Thermal Noise**

The noise associated with a sampling switch is the sampled noise, which is aliased in the sampling process if the switch and capacitance time constant is much smaller than the sampling period [9]. Due to the folding effect, the spectrum of the sampled noise will be very nearly white and the total noise power within $f_s/2$ is given by

$$\overline{V_{n,s}^2} = \frac{KT}{C_s},$$

(2.27)

where $K$ is the Boltzman constant, $T$ is the absolute temperature, and $C_s$ is the sampling capacitance.

**Operation Amplifiers (OPAMPS)**

Opamps are main building blocks of sigma-delta modulators if the opamp-based switched-capacitor integrator is used. The opamp performance causes various non-linearities in the modulator.
• **Finite opamp gain** The z-domain transfer function of an SC integrator with finite opamp DC gain is given by

\[ H(z) = \frac{z^{-1}}{1 - \alpha z^{-1}}. \]  

(2.28)

where \( \alpha \) is a parameter associated with DC gain and causes the NTF zeros shifted from unit circle, which results in a lossy integrator and leads quantization noise leakage.

• **Finite bandwidth** For a single-pole system with unit-gain bandwidth (UGB), the time constant is \( \tau = 1/(2\pi \cdot UGB) \), and the linear settling is given by

\[ v(t) = 1 - e^{-\frac{t}{\tau}}. \]  

(2.29)

If there is no enough time allocated for settling, the in-band quantization noise will increase. Given an error tolerance, the requirements on \( \tau \) can be calculated based on equation 2.29. In the sigma-delta modulator case, a minimum condition that does not degrade noise performance too much is \( \tau < T_s/2 \).

• **Finite slew rate (SR)** The effect of the finite bandwidth and the slew rate are related to each other, since they reflect the effect of how much the output close to the settling value. However, slewing is a nonlinear settling process and it usually produce harmonic distortion at the output.

• **Limited range** Opamps always have a limited swing due to the limited supply voltage. If the swing of the opamp is less than the maximum signal at the integrator’s output, clipping will occur, which results in harmonic distortion and noise. Proper scaling should be adopted to avoid clipping. On the other hand, large efforts need to be paid on large swing opamp design.

**Switch Resistance**

The nonzero resistance of the switch in the SC circuit results in the degradation of linear settling while relaxing the requirement on SR.

**Multi-Bit Feedback DAC**

Equation 2.18 shows that a sigma-delta modulator with multi-bit internal quantizer can offer 6VdB SNR better than their single-bit counterparts. In addition, increasing the number of bits improves the stability of the modulator, which allows more aggressive noise shaping of the NTF.

In the multi-bit modulator, a multi-bit DAC is needed in the feedback loop to translate the digital signal back to an analog. In general, the N-bit DAC is composed of \( 2^N - 1 \) unit elements. The linearity depends on the matching of these unit elements.
Although multi-bit is more favorable, the non-linearities introduced by the DAC in the feedback loop are directly input-referred, i.e., the transfer function from DAC non-linearities to the output approximately equals one. For example, to implement a 14 bit sigma-delta ADC, a corresponding 14 bit matching of unit elements is required which is hard to achieve without calibration technique.

To overcome this disadvantage, some techniques called dynamic element matching (DEM) are developed where mismatched DAC elements are shuffled so that the distortion is somehow whitened. Data Weighted Averaging (DWA) is the most popular DEM technique, due to its simple implementation and efficiency. The basic idea of DWA is use all DAC elements equally over the time, which is realized by using them rotationally. Figure 2.12 shows the PSD of a third-order, 4 bits internal quantizer, sigma-delta modulator output. To see the effect of DAC non-linearities, random mismatching between unit elements is introduced and large distortion can be observed if using thermometer coding. While by rotationally selecting the unit elements, the distortion is suppressed a lot compared to thermometer coding.
2.3 Advanced Topics

2.3.1 Continuous-Time Sigma-Delta Modulator

Recently, continuous-time (CT) sigma-delta converters have attracted more interest. The loop filters are implemented as continuous-time circuits (active RC, Gm-C, LC filters) rather than discrete-time circuits. As shown in Figure 2.13, the sampling operation is usually done before the internal quantizer, which offers some advantage [10]:

- Relaxed sampler
- Intrinsic anti-aliasing
- Relaxed slew rate and bandwidth requirement imposed on opamp, thus lower power

2.3.2 Bandpass Sigma-Delta Modulator

In the lowpass sigma-delta modulator, the loop filter $H(z)$ is low pass filter with poles at DC and the NTF has a high pass shape. If we embed a bandpass filter or a resonator into the loop, the quantization noise is shaped away from the resonant frequency. A common type of bandpass converter can be derived from a low pass filter $H(z)$ by performing the interpolation $z^{-1} \rightarrow z^{-2}$. The resulting modulator inherits the stability properties and the dynamics of the low pass counterparts with noise shaped away from central frequency $f_s/4$.

A typical application of such a converter is the conversion of a radio frequency (RF) or intermediate frequency (IF) signal to baseband, which now becomes a very attractive trend. However, in practice such implementation tend to have worse performance since it is difficult to design a good resonator. Fig 2.14 shows a general continuous time bandpass sigma-delta modulator.
### 2.3.3 Complex Sigma-Delta Modulator

If complex or quadrature filtering is embedded in the loop of sigma-delta modulators, the NTF can have an asymmetric noise-shaping, which is usually referred as complex or quadrature sigma-delta modulators. Such kind of modulator is desirable in radio communication and often implemented with two quadrature channels I and Q (in-phase and quadrature phase).

### 2.4 Reported Performance

As mentioned previously, the trend is using sigma-delta modulator for wideband applications, as also the work presented in this thesis focuses on. In order to give an overview of recent performances that have been published, a selection of sigma-delta modulator/ADC presented at International Solid-State Circuit Conference (ISSCC) or Journal of Solid-State Circuit (JSSC) is listed in Tables 2.1-2.3: Table 2.1 lists the SNR versus bandwidth for discrete-time implementation, Table 2.2 for continuous-time implementation and Table 2.3 for bandpass sigma-delta modulator. In the tables, the column ‘Type’ indicates whether the single loop or cascaded structure is used in the sigma-delta modulator. For example, ‘2-2’ means the modulator is two second-order modulators cascaded, while ‘3rd’ means it is a third-order single loop sigma-delta modulator. In the Table 2.3, ‘CT Quad’ means it is a continuous-time quadrature sigma-delta modulator.
## Table 2.1. Reported discrete-time sigma-delta results

<table>
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<tr>
<th>Reference</th>
<th>Type</th>
<th>OSR</th>
<th>BW (MHz)</th>
<th>SNDR/DR (dB)</th>
<th>Power (mW)@5V</th>
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## Table 2.2. Reported continuous-time sigma-delta results

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Table 2.3. Reported bandpass sigma-delta results

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Chapter 3

Feedforward Sigma-Delta Modulators

3.1 Introduction

The advantage of the cascaded sigma-delta modulators is that it realizes high-order noise shaping by cascading second order stages (or lower) to avoid instability [43], and it is an attractive candidate for high-speed ADCs with low oversampling ratio (OSR) applications [44][45].

In this chapter, a modified feedforward structure is proposed. It is based on the architecture presented in the paper [46], with the optimization of the NTF in the second stage.

3.2 Advantage of Unity-Gain STF

It is well known that harmonic distortion, due to the opamp’s limited and non-linear DC gain, finite bandwidth, and slew rate, will be created at the outputs of

Figure 3.1. A traditional second-order feedforward sigma-delta modulator
CHAPTER 3. FEEDFORWARD SIGMA-DELTA MODULATORS

Figure 3.2. Low distortion second-order feedforward sigma-delta modulator

Figure 3.3. The 1st and 2nd integrator’s output swing
the switched-capacitor integrators [47]. The attenuation by the sigma-delta loop is inadequate in low oversampling applications [46]. Fig. 3.1 shows a 2nd order feedforward sigma-delta modulator, which has noise transfer function:

\[
NTF(z) = (1 - z^{-1})^2,
\]

(3.1)

and signal transfer function:

\[
STF(z) = z^{-2}.
\]

(3.2)

If the STF equal to one instead \(z^{-2}\), the integrators will only process quantization noise, no input signal is processed by the integrators and no input signal harmonics will be generated. This unity-gain STF can be achieved by adding a feedforward input path into the modulator, as shown in Fig. 3.2. This structure has reduced sensitivity to opamp nonlinearity and exhibits lower distortion. Hence, such a design can achieve less power and save area due to relaxed requirements on the integrator and opamp [48],[49].

Fig. 3.3 shows the 1st and 2nd integrator output swing respectively. The integrator’s gain can be scaled less than those of a traditional topology [50]. For the same sampling capacitor, the integrating capacitor can be smaller hence resulting in lower area. Also, lower output swing reduces the requirements on the slew rate of the opamp, thus resulting in lower power consumption.

3.3 Multi-Bit Quantization in Feedforward Modulators

Multi-bit sigma-delta modulators relax the instability problem and can achieve high SNR even in low OSR situation, but they have nonlinearity problems due to mismatch of their internal multi-bit DAC [44]. Since the error of the internal DAC, \(d(n)\), resides in the feedback path and is added directly to the input signal, it is not shaped by the sigma-delta loop. Techniques have been introduced to shape the spectrum of DAC mismatch error out of the baseband. Among them, data-weighted-average (DWA) [51] is the most popular one, in which DAC units are selected by code-dependent shifting, and the result is that the DAC distortion spectrum has been flattened [52].

3.4 Optimizing the NTF Zeros

We do not have to locate the zeros of the NTF necessarily at DC. By spreading the zeros across the band of interest, the in-band noise power can be reduced, so aggressive (more quantization noise is shaped out of the bandwidth) NTFs can be designed. For a second-order sigma-delta modulator, the optimal placement of the complex-conjugate zeros of NTF is at approximately [53],[49],

\[
f_0 = \sqrt{\frac{1}{3}} \cdot f_B,
\]

(3.3)
Figure 3.4. Normalized in-band noise power versus zero placement

Figure 3.5. Modulator with optimized zero placement
where $f_B$ is the Nyquist bandwidth, as depicted in Fig. 3.4.

Based on realizing STF=1 and optimizing NTF zeros, a suitable architecture is shown in Fig. 3.5[53]. A local feedback branch is added between the two integrators to realize the optimizing zeros, with the gain of $g$ as:

$$g = 2 - 2 \cdot \cos \left(2\pi f_0 / f_s\right),$$

(3.4)

where $f_s$ means sampling frequency and $f_0$ equals to equation 3.3.

If the feedback coefficient $g$ is inaccurate, the NTF zeros and poles will shift slightly away from the ideal one, whereas, simulation has indicated that the SNR is not sensitive to the exact location of the optimal $f_0$. If multi-bit quantizer is used, this effect can be minimized [53].

### 3.5 Traditional 2-2 MASH Architecture

The multi-stage architecture (MASH) was developed to offer higher order loops without stability problems. In addition, it can operate at high-speed with a low
OSR [44]. Shown in Fig. 3.6 is a 2-2 cascaded sigma-delta modulator, which consists of two second-order modulators. The output of the first stage modulator is given by

\[ Y_1(z) = z^{-2}X(z) + (1 - z^{-1})^2Q_1(z), \]  
(3.5)

and the output of the second stage can be written

\[ Y_2(z) = z^{-2}c_1Q_1(z) + (1 - z^{-1})Q_2(z), \]  
(3.6)

where \( \lambda_1 \) is assumed to be 1, which can be adjusted to achieve better performance based on simulation. \( c_1 \) is the inter-stage gain used to scale the input to the second stage. The final output is obtained by cancelling out the quantization noise of the first stage via error-cancelling-logic:

\[ Y(z) = Y_1(z)H_1(z) + Y_2(z)H_2(z). \]  
(3.7)

To have a fourth-order noise shaping, i.e. \((1-z^{-1})^4\), the error-cancelling-logic (ECL) should be

\[ H_1(z) = z^{-2}, \]
\[ H_2(z) = \frac{1}{c_1}(1 - z^{-1})^2. \]  
(3.8)
3.6 IMPROVED ARCHITECTURE

By substituting them into equation 3.7, we can get the ideal output

\[ Y(z) = z^{-4}X(z) + \frac{1}{c_1}(1 - z^{-1})^4Q_2(z). \] (3.9)

3.6 Improved Architecture

To improve the cascaded sigma-delta noise shaper regarding its sensitivity to circuit non-idealities, a feedforward cascaded topology is presented in [46], as shown in Fig. 3.7. A single-bit quantizer (ADC1) has been used in the first stage and a 4-bit quantizer (ADC2) in the second stage. By properly combining the outputs of both stages, it is possible to cancel out the quantization error in the first stage and have the modulator output attenuated by a 4th order noise shaping function. With the feedforward technique in both stages, a better signal-to-noise-and-distortion ratio (SNDR) is obtained in the desired baseband.

Based on this structure and discussion in previous section, we now propose an improved topology, shown in Fig. 3.8, by introducing the zero-optimized structure at the second stage while keeping the first stage unchanged and not introducing unnecessary distortion in the signal path, i.e. the first stage. In addition, this makes
the error-cancellation-logic quite simple and no extra mismatch error is generated. In the second stage, we relocate the zeros of the NTF by using the structure in Fig. 3.5. Ideally, the following is obtained for the $z$ domain output

$$Y(z) = X(z) + \frac{1}{c_1} \cdot (1 - z^{-1})^2 (1 - 2 \cos \alpha \cdot z^{-1} + z^{-2}) \cdot Q_2(z), \quad (3.10)$$

where $1/c_1$ is a digital multiplier which compensates for the scaling factor $c_1$ in the inter-stage gain, preventing the input to the second stage to overload. Its value is a trade-off between SNR and the dynamic range of second stage. The product $Q_2(z)$ represents the second stage quantization error. With this structure, a better SNR is obtained while maintaining the reduced sensitivity to the integrator nonlinearity. The ECL still remains simple:

$$H_1(z) = 1 \quad H_2(z) = \frac{1}{c_1} (1 - z^{-1})^2. \quad (3.11)$$

### 3.7 Simulation Results

To illustrate the advantages of the proposed new architecture, two topologies, in Fig 3.8 and Fig. 3.7, were modelled and simulated in MATLAB. Both architectures were modelled as having an integrator nonlinearity in both stages. The nonlinearities are described by a polynomial [54],[55], assuming single-end case,

$$G(t) = b_1 \cdot u(t) + b_2 \cdot u(t)^2 + b_3 \cdot u(t)^3 + \ldots. \quad (3.12)$$

Here $u(t)$ is the input signal to the nonlinear circuit block, $G(t)$ is the output and $b_n$ are coefficients. The input signal has an amplitude of 0.1FS and a frequency of 1MHz. The sampling frequency is 96MHz and an oversampling ratio of 16 was used. The ideal simulation result is shown in Fig. 3.9(a), compared with the feedforward cascaded structure in Fig. 3.7. On the right side of Fig. 3.9(a), the shifted zeros result in the high-pass NTF characteristic having a notch at frequency $f_0$. Comparing with the left figure, where no zero-optimization is used, we can see that about 4 dB SNR advantage is achieved. Another simulation result is shown in Fig. 3.9(b) with the amplitude of 0.8FS, and nonlinearity. We can see the 3rd harmonic distortion power, in the power-spectrum-density (PSD) plot, are almost equal.

Fig. 3.10 shows the SNR versus the input amplitude curves for both topologies. As shown in the figure, the SNR of the two structures does not degrade until the input power of -1 dBFS, and the proposed one can achieve a maximum SNR of 83.8 dB while the feedforward cascaded structure [46] achieves 79 dB.
3.7. SIMULATION RESULTS

Figure 3.9. Power spectrum density of the modulators

(a) Amp=0.1FS, without nonlinearity

(b) Amp=0.8FS, with nonlinearity

SNR = 59.7dB

Feedforward Cascaded

SNR = 64.4dB

Improved Structure

SNR = 76.0dB

Improved Structure

SNR = 79.9dB

Feedforward Cascaded
3.8 Conclusion

In this chapter, we have proposed an improved feedforward cascaded sigma-delta modulator with reduced sensitivity to opamp nonlinearities and reduced in-band noise, based on unity-gain STF and optimized NTF zeros placement. It achieves higher SNR across the entire input range. In practice, internal DAC non-linearities cancelling technique such as data weighted averaging (DWA) can be used to further enhance the overall performance.
Chapter 4

Continuous-Time Sigma-Delta Modulators

4.1 Introduction

In modern wireless receiver designs, the desire for direct digitization at high intermediate frequency (IF) with high resolution has led to the development of high-sample-rate sigma-delta modulators, which has recently come up as an attractive candidate for analog-to-digital (A/D) conversion in single chip radio frequency (RF) front ends[56]. By using a continuous-time (CT) circuit for the loop filter, modulators can potentially operate at higher clock frequencies and/or with less power consumption than their discrete-time (DT) counterparts [1], [2]. Other benefits of continuous-time modulators are intrinsic anti-alias filtering and much-relaxed sampling circuit requirements [10].

A non return to zero (NRZ) DAC scheme in continuous-time sigma-delta modulators design is often used to relax the clock jitter requirement. The main drawback of NRZ DAC is that instability may result if the excess loop delay is too large [57]. The loop delay is mainly due to nonzero switching time of the transistors in the feedback path. The order of modulator’s noise transfer function (NTF) may increase by one that alters the equivalence between the CT and DT representations of the loop filter. One or one half clock delay is usually explicitly introduced before the DAC to absorb the loop delay [1], [31]. To keep the loop filter unchanged at the sampling instants, an additional feedback DAC is required to compensate for this delay. In this chapter, we will study some popular architectures and their compensation schemes. Based on this we will propose two alternative low power feedforward continuous-time sigma-delta modulators with compensation of the internal quantizer and feedback DAC delay.

4.2 Equivalence Between CT and DT Sigma-Delta Modulators

Usually, there are two main ways to synthesize loop filters in continuous-time modulator: 1) synthesize CT loop filters in the frequency domain directly 2) first design
a DT modulator then transform it to a CT modulator [57]. Since sigma-delta modulator is essentially a nonlinear system, unlike a linear filter, the approximation in quantizer and feedback DAC may result in an unstable system. The later design method, taking advantage of the large existing research on DT sigma-delta modulators design, is therefore more popular. Fig. 4.1 and Fig. 4.2 show a general DT and a CT modulator, respectively. For a CT modulator, the sample values of the CT waveform at the input of the quantizer at each sampling instance define an exact DT impulse response. To make the DT and CT loops equivalent, the open loop impulse responses of the discrete-time loop filters, from quantizer outputs to the input of quantizer, should match the samples of the impulse response of the continuous time modulator loops, as shown in Fig. 4.3. This means

$$h_d(n) = [h_{DAC}(t) * h_c(t)]_{t=nT_s} ,$$ \hspace{1cm} (4.1)

where $h_d(n)$ is the DT counterpart loop response and $T_s$ is the sampling period.

The Laplace domain to the $z$ domain mapping is established through the following
The transformation is called impulse-invariant transformation (IIT).

As seen in the equation, the feedback pulse shape has to be taken into account. Fig. 4.4 shows commonly used rectangular DAC feedback waveforms: non return to zero (NRZ), return to zero (RZ) and half delay return to zero (HRZ). The s domain transfer function can be described by the equation:

$$H_{NRZ/RZ}(s) = e^{-s\beta} - e^{-s\alpha},$$

where $\alpha = 0, \beta = 1$ leads to NRZ DAC, $\alpha = 0, \beta = 0.5$ to RZ DAC, and $\alpha = 0.5, \beta = 1$ to HRZ DAC.

To illustrate this method, let us take a second-order sigma-delta modulator as an example with the NTF of $(1 - z^{-1})^2$. Its loop filter is:

$$H_d(z) = \frac{2z^{-1} - z^{-2}}{(1 - z^{-1})^2}.$$  

By applying IIT, we can get a corresponding $s$ domain loop transfer function with a NRZ DAC:

$$H_e(s) = \frac{1 + 1.5sT}{(sT)^2}.$$  

4.3 Inherent Anti-Aliasing Filtering

One of the major advantages of the CT modulator is its inherent anti-aliasing filtering. To illustrate this characteristic, a more general CT modulator diagram...
is shown in Fig. 4.5(a) in which $G_c(s)$ and $H_c(s)$ represent feedforward and loop transfer function respectively. Normally, $G_c(s)$ is obtained based on $H_c(s)$ to meet the signal transfer function (STF) specifications. By arranging the structure, an equivalent representation of the CT modulator is shown in Fig. 4.5(b), with $G_d$ and $H_d$ being IIT transform of $G_c(s)$ and $H_c(s) \cdot H_{DAC}(s)$ respectively. The STF can be expressed as:

$$STF_c(w) = \frac{G_c(jw)}{G_d(e^{jwT})} \frac{G_d(e^{jwT})}{1 + H_d(e^{jwT})},$$  \hspace{1cm} (4.6)

where the first part of the equation representing the anti-alias filtering:

$$F_{aa}(w) = \frac{G_c(jw)}{G_d(e^{jwT})}. \hspace{1cm} (4.7)$$

### 4.4 Modulators with Excess Loop Delay Compensation

Most recently published continuous-time sigma-delta modulator designs use feedforward topologies because of its reduced sensitivity to opamp harmonic distortion and also reduced swing $[1][2][31][34][58]$. Based on their designs, two new feedforward structures are proposed.
4.4. MODULATORS WITH EXCESS LOOP DELAY COMPENSATION

(a)

\[ X(s) \rightarrow G_c(s) \rightarrow U(z) \rightarrow Y(z) \]

\[ H_c(s) \rightarrow H_{DAC}(s) \]

(b)

\[ X(s) \rightarrow G_c(s) \rightarrow \frac{1}{G_d(z)} \rightarrow X(z) \rightarrow \frac{G_d(z)}{1+H_d(z)} \rightarrow Y(z) \]

\[ F_{na}(j\omega) \]

Figure 4.5. Inherent anti-aliasing filtering model

Figure 4.6. CT sigma-delta modulator structure [1]
4.4.1 Reported Feedforward Continuous-Time Structures

A popular feedforward CT sigma-delta modulator is shown in Fig. 4.6 [1], [31], [58]. It is generalized into $L$th order with feedforward coefficients $f_1 - f_L$. It has the advantage of requiring only one DAC, compared to multiple feedback topology. The DAC2 with gain of $f_c$ is used to compensate the one clock delay in the main feedback path, which is used to relax the timing requirements imposed on the quantizer and dynamic element matching (DEM) of a multi-bit DAC design. The main drawback of such kind of architecture is that an adder is needed to sum all feedforward branches and the additional feedback DAC before the quantizer. A passive or an active adder can fulfill the task, however, a passive adder is sensitive to parasitic capacitance while an active adder consumes more power.

A lower power consumption structure was proposed in [2] as shown in Fig. 4.7. The feedforward branches are summed before the last integrator instead of in front of the quantizer. To realize the same NTF, an additional feedback DAC2 branch is added to replace the first order feedforward path. Also, one clock delay is embedded to alleviate excess loop delay requirements. Its compensation is moved before the last integrator too by digitally differentiating the feedback DAC3. Since the summing circuit before the quantizer, which consumes a lot of power, is totally eliminated, this leads to a low power design.

4.4.2 Proposed Low Power Feedforward CT Structure

An alternative way to compensate for excess loop delay is to use an additional feedback with a different kind of DAC pulse [59]. Instead of using two DACs to realize the transfer function, $1 - z^{-1/2}$, as the excess loop delay compensation, we can simply use either RZ or HRZ DAC to compensate the NRZ DAC path delay. Different types of feedback DACs were introduced in bandpass sigma-delta...
Fig. 4.8. The first proposed CT sigma-delta modulator structure

modulators [60] to achieve the controllability of tunable parameters.

Our first proposed feedforward CT structure is shown in Fig. 4.8. This structure is quite similar with that of [2] except that there the HRZ DAC3 is used for compensation. The advantages of using the HRZ DAC are: first, the HRZ DAC is not sensitive to the DAC loop delay itself; second, only one DAC is required in the compensation feedback path while in [2] two DACs are needed to realize $(1 - z^{-1/2})$. The HRZ DAC compensation scheme is illustrated in Fig. 4.9. The signal goes through the last $1/sT_s$ integrator, and make contribution not only to the first sample at $T_s$, but also to the later impulse response sample value. This compensation leads to a smaller $f_L$ coefficient in the feedback DAC2 path.

Fig. 4.10 shows the second proposed feedforward CT structure. There is no feedback path, i.e. DAC2 is eliminated. The feedforward paths are divided into two parts: before last integrator and quantizer respectively. The loading of last integrator is reduced. The adder in front of the quantizer can be implemented by switched-capacitor (SC) without much loading since such kind of circuit is often needed to do offset cancellation in the quantizer.

4.5 Simulation Based Impulse Invariant Transformation

Synthesis of the CT sigma-delta modulator is usually done by discretizing its loop filter and equating it with the loop filter of a DT sigma-delta modulator. The Laplace domain to the $z$ domain mapping is established through equation 4.1. $H_d(z)$ is the equivalent DT loop filter which is easily synthesized from the toolbox [61]. Given the DAC transfer function, we can get the coefficients of the loop filter $H_c(s)$. This approach seems a little bit complex mathematically, especially when a loop delay is included.

Another approach of determining the coefficients is directly equating the impulse
Figure 4.9. Impulse response of HRZ DAC compensation

Figure 4.10. The second proposed CT sigma-delta modulator structure
Table 4.1. Coefficients of loop filter, $H_{inf} = 6$

<table>
<thead>
<tr>
<th></th>
<th>$f_1$</th>
<th>$f_2$</th>
<th>$f_3$</th>
<th>$f_4$</th>
<th>$f_c$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Yan04</td>
<td>0.517</td>
<td>2.028</td>
<td>3.868</td>
<td>4.733</td>
<td>3.115</td>
</tr>
<tr>
<td>Mitter06</td>
<td>0.517</td>
<td>2.028</td>
<td>3.868</td>
<td>4.733</td>
<td>1.497</td>
</tr>
<tr>
<td>Proposed 1</td>
<td>0.517</td>
<td>2.028</td>
<td>3.868</td>
<td>3.235</td>
<td>2.995</td>
</tr>
<tr>
<td>Proposed 2</td>
<td>0.517</td>
<td>2.028</td>
<td>3.868</td>
<td>1.618</td>
<td>6.231</td>
</tr>
</tbody>
</table>

Table 4.2. Coefficients of loop filter, $H_{inf} = 2$

<table>
<thead>
<tr>
<th></th>
<th>$f_1$</th>
<th>$f_2$</th>
<th>$f_3$</th>
<th>$f_4$</th>
<th>$f_c$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Yan04</td>
<td>0.038</td>
<td>0.257</td>
<td>0.844</td>
<td>1.739</td>
<td>1.359</td>
</tr>
<tr>
<td>Mitter06</td>
<td>0.038</td>
<td>0.257</td>
<td>0.844</td>
<td>1.739</td>
<td>0.978</td>
</tr>
<tr>
<td>Proposed 1</td>
<td>0.038</td>
<td>0.257</td>
<td>0.844</td>
<td>0.761</td>
<td>1.997</td>
</tr>
<tr>
<td>Proposed 2</td>
<td>0.038</td>
<td>0.257</td>
<td>0.844</td>
<td>0.380</td>
<td>2.718</td>
</tr>
</tbody>
</table>

The response in the time domain based on the fact that the total impulse response $h_d(k)$ at the $k$th sampling instant is the sum of each branch’s impulse response $h_i(k)$ [59] [62]. The impulse response $h_i(k)$ could be obtained through a simulation tool. Here we extend the equation by taking the excess loop delay compensation into consideration:

$$h_d(k) = \sum_{i=1}^{L} f_i h_i(k) + f_c h_{ldc}(k),$$

(4.8)

where, $L$ is the modulator order, $f_i, f_c$ are loop coefficients and compensation factor, respectively and $h_{ldc}(k)$ is impulse response of the loop delay compensation path. The above equations can be re-written in matrix form:

$$
\begin{bmatrix}
    h_1(1) & \cdots & h_L(1) & h_{ldc}(1) \\
    h_1(2) & \cdots & h_L(2) & h_{ldc}(2) \\
    \vdots & \ddots & \vdots & \vdots \\
    h_1(t+1) & \cdots & h_L(t+1) & h_{ldc}(t+1)
\end{bmatrix}
\begin{bmatrix}
    f_1 \\
    f_L
\end{bmatrix}
= \begin{bmatrix}
    h_d(1) \\
    \vdots \\
    h_d(t)
\end{bmatrix}
\begin{bmatrix}
    h_{ldc}(1) \\
    \vdots \\
    h_{ldc}(t+1)
\end{bmatrix}

(4.9)

By solving these equations, we can get the corresponding loop filter coefficients.

### 4.6 Design Examples

To illustrate the proposed structure and synthesis approach, two 4th-order multi-bit sigma-delta modulators are designed and simulated in Matlab. The target bandwidth is several MHz and the dynamic range above 70 dB. For simplicity, a zero frequency notch in the NTF is not introduced, which can be realized by add local feedback between two integrators. Due to the high bandwidth and low oversampling ratio, a 17 level internal quantizer is used. The synthesized loop
Figure 4.11. Power spectrum density of the (a) proposed 1 and (b) proposed 2 modulator.
Figure 4.12. SNR versus excess loop delay for case (a) $H_{inf} = 2$ and (b) $H_{inf} = 6$
coefficients are listed in Table 4.1 with the maximum NTF gain $H_{\inf} = 6$. For comparison, loop coefficients for $H_{\inf} = 2$ case are also listed in Table 4.1.

Fig. 4.11(a) and Fig. 4.11(b) show the power spectrum density (PSD) of the proposed sigma-delta modulators respectively. The input signal has an amplitude of -6 dBFS and a frequency of about 55KHz. The sampling frequency is 100MHz and an OSR of 10 is used. About 76 dB SNR is achieved over 5 MHz bandwidth. A jitter noise, modelled in the proposed structures, with a constant standard deviation of $\sigma_{\text{jitter}} = 0.05\%T_s$ is allowed without beginning to degrade the SNR.

The SNR versus the extra excess loop delay (caused by nonzero switching time of the circuit, not including one explicit clock delay) is shown in Fig. 4.12. For illustration purposes, only $H_{\inf} = 2$ and $H_{\inf} = 6$ are simulated and compared. In the figures, the steep decrease of the SNR indicates the modulators become unstable when the excess loop delay increases to a certain level. It is obvious to see the trade-off between maximum achievable SNR and maximum tolerated excess loop delay with different noise gains. Higher maximum NTF gain means higher quantization noise suppression, i.e. higher SNR, but less stability [8]. Since excess loop delay causes stability problems, the decrease of NTF’s out-of-band gain make
4.7. CONCLUSION

the modulator more tolerating to the excess loop delay. In our example, the extra excess loop delay in $H_{inf} = 2$ case is up to $0.4T_s$ at the cost of about $20dB$ SNR loss. In both cases, our proposed structures achieve as good loop delay performance as that of Fig. 4.7 while better than that of Fig. 4.6. The SNR versus input signal level is shown in Fig. 4.13.

In terms of power, the first proposed structure has less feedback DAC current since the value of $f_4$ is less than that of Fig. 4.6 while other coefficients and the voltage swing of the integrators are almost the same (two DACs are needed to implement the digital differential feedback branch $f_c$).

4.7 Conclusion

Feedforward continuous-time sigma-delta modulators have an advantage over its multi-feedback counterpart. However, to save power, we usually need totally or partly get rid of the adder before the quantizer. When designing a CT sigma-delta modulator, we also should take feedback excess loop delay into consideration. In this chapter, previous feedforward CT structures with excess loop delay compensation are studied. Two new feedforward continuous-time sigma-delta modulators with loop delay compensation are proposed. Simulation based synthesis from discrete time topologies is extended to obtain the loop filter coefficients with excess loop delay. Simulation results show that they achieve the same performance, with expected reduced power consumption which is implicitly seen from the reduced number of the DAC or reduced requirements on the quantizer.
Chapter 5

Quadrature Sigma-Delta Modulators

5.1 Introduction

In modern wireless receiver designs, the current trend is to move the analog-to-digital interface as far forward in the signal path as possible toward the antenna or sensor. Digitizing the received signal at the intermediate frequency (IF) or higher permits the signal processing mostly performed in the digital domain, resulting in a more robust and flexible system.

The receiver architecture shown in Fig. 5.1 converts the received radio frequency (RF) signal into an IF in-phase (I) and a quadrature phase (Q) signal [63]. The analog-to-digital (A/D) conversion is usually performed by two real bandpass ADCs, or by one quadrature bandpass ADC.

Quadrature bandpass sigma-delta modulator (QBSDM) is an attractive candidate for such applications since it directly converts complex input signals into digital ones [38][40][42][56][64][65][66]. The distinguishing feature is that its quantization noise stop-band needs only exist for positive frequencies. It is more efficient than two real bandpass converters because no power is wasted digitizing the negative frequency content of the input.

By using a continuous-time circuit for implementing the loop filter, modulators can potentially operate at higher clock frequencies and with less power consumption than their discrete-time (DT) counterparts [59]. Other benefits of CT modulators are intrinsic anti-alias filtering and much-relaxed sampling circuit requirements [59] which are especially desired in wide-band wireless receiver design.

In this chapter, we will discuss the effect of different feedback digital-to-analog waveforms inside the modulator on the design of complex NTFs.

5.2 Quadrature Bandpass Sigma-Delta Modulators

In the implementation sense, a complex signal is nothing more than two real signals carried by two separate wires or bit-streams. The concept is commonly used in
communication signal processing to model a bandpass system.

### 5.2.1 Complex Signal Processing

A quadrature bandpass signal, \( x(t) \), may be represented by combination of real and imaginary parts as: \( x(t) = x_{re}(t) + j x_{im}(t) \), where \( x_{re}(t) \) is a real bandpass signal and \( x_{im}(t) \) its Hilbert transform. The Fourier transform is

\[
X(w) = X_{re}(w) + jX_{im}(w),
\]

where

\[
X_{im}(w) = \begin{cases} 
-jX_{re}(w) & w > 0, \\
 jX_{re}(w) & w < 0.
\end{cases}
\]

It only has single side band of \( x_{re}(t) \). Similarly, the complex filter has impulse response: \( h(t) = h_{re}(t) + j h_{im}(t) \). We can get the filter outputs:

\[
Y(s) = H(s)X(s) = Y_{re}(s) + j Y_{im}(s),
\]

with

\[
Y_{re}(s) = H_{re}(s)X_{re}(s) - H_{im}(s)X_{im}(s)
\]

\[
Y_{im}(s) = H_{re}(s)X_{im}(s) + H_{im}(s)X_{re}(s).
\]

The complex NTF can be designed to have non-conjugate poles and zeros which realize asymmetric noise-shaped spectra as shown in Fig. 5.2. The poles and zeros are shifted from DC to the positive (or negative) frequency [56]. Fig. 5.3 shows such complex NTF that only has noise shaping at positive frequency.

### 5.2.2 Design Methods

As indicated by equation 4.1, the synthesis of continuous-time sigma-delta modulators is usually done by discretizing the loop filter and equating.
Figure 5.2. Poles and zeros of complex sigma-delta modulator

Figure 5.3. Complex NTF
Generally complex coefficients are needed to realize a complex loop filter [56], [38]. This means that cross-couplings are needed between real and imaginary paths. In general, the number of cross-couplings is up to four times the order of the modulator. However, the more couplings there are, the more mismatch results. Due to the mismatch, the image signal will leak into the passband and degrade the effective signal to noise ratio (SNR) [56]. To reduce the number of couplings, a quadrature loop filter can be approximately implemented as a cascade of complex integrators with only real coefficients, i.e. shifting the pole $s = 0$ of the integrator $1/s$ to a complex pole, $1/(s - jw_c)$, and shifting a low pass real filter $H_{lp}$ to a bandpass filter, $H_{lp}(s - jw_c)$ [64][66][42]. Fig. 5.4 shows such a generalized $L$th order CT QBSDM with real feedforward coefficients $f_1, ..., f_L$ and complex integrators as the example in Fig. 5.5. However, at higher center frequency $f_c$, such approximation may not be valid anymore and lead to instability due to [67]:

$$Z^{-1}\{H_{qbp}(z)\} = L^{-1}\{H_{DAC}(s - jw)H_{lp}(s - jw)\}|_{nT},$$

where $H_{DAC}(s)$ is the feedback DAC transfer function and $H_{qbp}(z)$ is the equivalent DT quadrature bandpass loop filter. The method proposed in [67] is trying to realize a complex DAC with $H_{DAC}(s)$ which fulfils the condition:

$$\lim_{s \rightarrow p_i} \{H_{DAC}(s - jw)\} = \lim_{s \rightarrow p_i} \{H_{DAC}(s)\},$$

where $p_i$ are the poles of $H_{DAC}(s - jw)H_{lp}(s - jw)$. However, this method needs cross-couplings between the $I$ and $Q$ path of the feedback DAC.
If we can find a DAC with its $H_{DAC}(s) \approx H_{DAC}(s - jw)$ in the frequency range of interest, we may get rid of the cross-couplings between $I$ and $Q$ path in the feedback DAC. Let us study some feedback waveforms first:

- Non return to zero (NRZ) DAC
- Return to zero (RZ) DAC
- Switched-capacitor resistor (SCR) DAC [68].

The first two are well known, and the $s$ domain transfer function can be described as:

$$H_{NRZ/RZ}(s) = \frac{e^{-s\beta} - e^{-s\alpha}}{s}$$

where $\alpha = 0, \beta = 1$ leads to a NRZ DAC, and $0 < \alpha < \beta < 1$ leads to a RZ DAC.

While the SCR DAC is recently proposed in [68] to relax the jitter requirement imposed on the CT sigma-delta modulator with the following form:

$$p_{(\tau,\alpha,\beta)}(t) = \begin{cases} 
e^{-s\alpha} \frac{\alpha T_s - t}{\tau} & \alpha T_s \leq t < \beta T_s \\ 0 & otherwise \end{cases}$$
with $0 \leq \alpha < \beta < 1$, and $\tau$ corresponding to a decaying RC time constant. The DAC pulse shapes are drawn in Fig. 5.6. By applying the Fourier transform on them, we can get the corresponding $s$ domain transfer function:

$$H_{SCR}(s) = \frac{\tau \left( 1 - e^{-\beta \tau s} - \beta + \alpha \right)}{(s \tau + 1)} e^{-\alpha \tau}.$$  

(5.8)

Figure 5.6. Waveforms of (a) NRZ (b) RZ (c) SCR DAC

From the frequency response plot in Fig. 5.7, we can see that SCR feedback DAC, with $\tau = 0.1$ used, has lowest magnitude attenuation when the centre frequency moves towards the sampling frequency. The RZ DAC is 50% duty cycle in the figure which has first zero at $2f_s$. The smaller duty cycle it has, the higher frequency its first zero is located at. When the frequency response is flat, i.e., the magnitude is less decreasing with relative to the frequency, in the interesting frequency range, the condition $H_{DAC}(s) \approx H_{DAC}(s - jw)$ is fulfilled. In such case, no complex DAC is needed. Our observation is coincident with the results in [67] where the cross-coupling coefficients are implicitly related to the duty cycle of RZ DAC. Actually when the duty cycle is small, the coupling coefficients between $I$ and $Q$ path in the feedback DAC will be approximately zero. Since SCR feedback DAC has flattest response, it will remain stable at highest center frequency without introducing cross-coupling. RZ DAC can achieve higher stable center frequency than NRZ DAC, however it has more jitter noise degradation.
5.4 JITTER NOISE ANALYSIS

In practice, the sampling clock usually has uncertainties in the rising and falling edge, commonly referred to as clock jitter. Suppose the sampling times for \( n \)th output is given by

\[
t(n) = nT_s + \Delta t(n), \quad n = 0, 1, ..., 
\]

where \( \Delta t(n) \) is the white jitter noise with variance \( \sigma_{\Delta t} \). For discrete sigma-delta modulators, the error in sampling a sinusoidal signal \( v_{in}(t) = A\sin(2\pi f_{in}t + w_t) \) due to clock jitter is:

\[
\Delta v_{in}(t) = \frac{dv_{in}(t)}{dt} \cdot \Delta t = 2\pi f_{in}A \cdot \Delta t \cdot \cos(2\pi f_{in}t + w_t). 
\]

The corresponding error variance can be calculated as:

\[
\sigma_{ej}^2 = (2\pi f_{in}A\sigma_{\Delta t})^2/2. 
\]

In CT modulators, as shown in Fig. 5.8, there are two points in the CT sigma-delta modulator that suffer from clock jitter degradation: the sampler before the
quantizer and the DAC in the feedback path. From the transfer function point of view, the transfer function from sampling error, $\Delta t_q(n)$, to the out equals the NTF of the modulator, therefore this error is shaped by the modulator loop. Its influence is much smaller than the error introduced by the feedback DAC, $\Delta t_{DAC}(n)$. Therefore we will only consider SNR degradation in the feedback path.

Fig. 5.9 shows the three used feedback waveforms with clock sampling uncer-
In the case of RZ feedback waveform, the output error due to jitter is proportional to the DAC output instead of the adjacent output difference, i.e.

\[ e_j(n) = y(n) \cdot \frac{\Delta t_{DAC}(n)}{(\beta - \alpha)T_s}. \]  

(5.15)

Since the RZ feedback waveform is affected by jitter both on the rising and falling edge of each clock cycle, its error variance is two times larger:

\[ \sigma^2_{e_j} = 2\sigma^2_y \cdot \frac{\sigma^2_{\Delta t_{DAC}}}{(\beta - \alpha)^2T_s^2}. \]  

(5.16)

Generally, \( \sigma^2_y \) is larger than \( \sigma^2_{\Delta y} \), therefore NRZ DACs are less sensitive to clock jitter compared to RZ DACs.

The fundamental idea of using SCR feedback DACs to reduce the jitter effect is to make amplitude small near the edge of the clock so that the clock sampling variations have less effect. As shown in Fig. 5.8(c), the amplitude of the SCR feedback signal is exponentially reduced at the switching instant, \( \beta T_s \), with a settling time constant \( \tau \). The jitter noise error approximately equals:

\[ \sigma^2_{e_j} = \sigma^2_y (e^{-(\beta - \alpha)T_s/\tau})^2 \cdot \frac{\sigma^2_{\Delta t_{DAC}}}{T_s^2}. \]  

(5.17)

In a switched-capacitor DAC design, \( \tau \) is normally less than \( T_s \) to ensure small settling error. Equation 5.16 shows that the jitter error in a SCR DAC will be less than that of a NRZ DAC.
Figure 5.10. PSD of a CT QBPSDM with NRZ DAC for (a) $f_c/f_s = 0.05$, and (b) $f_c/f_s = 0.15$

Figure 5.11. PSD of a CT QBPSDM with RZ DAC for (a) $f_c/f_s = 0.05$, and (b) $f_c/f_s = 0.15$
5.5 Simulation Results

To illustrate this observation, a second-order multi-bits CT QBPSDM is simulated in Matlab. Fig. 5.10 shows the power spectrum density (PSD) of the CT QBPSDM with NRZ feedback DAC, where Fig. 5.10(a), 5.10(b) represent different center frequencies, \( f_c = \omega_c / 2 \cdot \pi \), normalized to the sampling frequency, \( f_s \) respectively. It is obvious that when \( f_c / f_s \) equals 0.15 the performance and stability are starting to degrade. When increasing \( f_c \), the QBSDM may be totally unstable. The PSD of QBSDM with RZ DAC and SCR DAC are shown in Fig. 5.11 and 5.12, respectively. Even when the center frequency is close to 0.25\( f_s \), the noise shaping remains almost unchanged.

The SNR versus center frequency for the second-order multi-bit CT QBPSDM with different feedback waveforms is illustrated in Fig. 5.13(a). The steep degradation of the SNR in the figures indicates the modulators become unstable or the approximation, \( H_{DAC}(s) \approx H_{DAC}(s - j\omega) \), does not hold anymore when the center frequencies, \( f_c \), increased. The modulator with NRZ DAC becomes unstable when \( f_c / f_s > 0.2 \). To see the effect of different orders, a fifth-order single bit CT QBPSDM with maximum NTF gain \([8] H_{nf} = 1.6 \) is simulated. As shown in Fig. 5.13(a), the NRZ DAC tends to be unstable even at lower center frequency. While the CT QBSDM with SCR DAC remains stable even when \( f_c / f_s > 0.25 \), which is enough for most applications such as \( f_s / 4 \) quadrature bandpass signal.

Figure 5.12. PSD of a CT QBPSDM with SCR DAC for (a) \( f_c / f_s = 0.05 \), and (b) \( f_c / f_s = 0.25 \).
Figure 5.13. SNR versus $f_c$ for (a)second-order (b)fifth-order CT QBPSDM

processing. Although low duty cycle RZ DAC can achieve flat frequency response also, it suffers more jitter degradation. While another advantage of using a SCR DAC feedback is its less sensitive to clock jitter.

5.6 Conclusion

In this chapter, we present the design of continuous time quadrature bandpass sigma-delta modulators which are more favorable than two real bandpass modulators. The effect of different feedback DAC waveforms on the design of QBPSDM is discussed. The simulation results reveal that CT QBPSDM can be archived by cascading complex integrators with only real coefficients if the feedback waveform has a flat frequency response. With SCR feedback, the QBPSDM is easy to reconfigure to zero-IF or IF architectures since its NTF is less sensitive to the centre frequency.
Chapter 6

A Sigma-Delta Pipelined Modulator

6.1 Introduction

Sigma-delta modulators are well suited for high performance applications. The need of digital signal processing circuits is hardly a drawback when the modulators are implemented in fine-geometry CMOS processes. The major disadvantage is the limited bandwidth due to the need of over-sampling. One way to extend the signal bandwidth is to employ a multi-bit quantizer in the modulator loop and/or increase the order of the modulator [19]. Both techniques have advantages and disadvantages.

The goal of this chapter is to find a robust architecture that can deliver over 12-bit performance with an OSR of 8 to 12. At the same time, this architecture should be scalable such that for lower bandwidth applications (with an OSR over 24), the architecture is capable of over 14 bits with minimum risk and power consumption.

There are quite a few architectures that can deliver over 14 bits performance with an OSR of 24. The best candidate for this kind of performance is the 4th order three-stage 2-1-1 MASH modulator [69]. It has been proven in silicon [12][13]. Therefore, we choose the architecture based on this one.

To further reduce the OSR to around 10 while achieving more than 12 bits resolution, we can either employ a multi-bit quantizer or add more stages. With only a 4th order modulator, the multi-bit quantizer has to have at least 5 bits to achieve 12 bits resolution with an OSR of 10. Putting a multi-bit quantizer inside a loop severely limits the options of multi-bit quantizer type. We can usually only use a flash-type ADC for the multi-bit quantizer. Also adding a multi-bit quantizer in the last stage of the 2-1-1 architecture destroys the scalability goal. Reconfiguring a multi-bit quantizer (more than 5-bit) to a single-bit quantizer on the fly could be messy. The more sensible option is to add more stages.

Adding more stages however will increase the modulator order. If only 1-bit quantizer is employed, the order of the modulator could be too high. Another disadvantage of high order single-bit modulators is the increased out-of-the-band
Figure 6.1. The proposed reconfigurable sigma-delta modulator
6.2. SYSTEM LEVEL DESIGN

6.2.1 Architectures

The proposed modulator architecture is shown in the Fig. 6.1. It is based on the classic 2-1-1 MASH architecture [12], in that a difference of the input and output of the previous stage quantizer, weighted by $\lambda_i$ and $g_i$ respectively, is used as the input to the next stage. A multi-bit ADC is used to quantize the quantization noise of the last stage. This ADC can be of any type, e.g., pipelined ADC. If we assume $\lambda_i = 1$, the final output is obtained by canceling out the quantization noise of the 2-1-1 MASH architecture:

$$Y(z) = z^{-4}X(z) + \frac{1}{g_1g_2g_3}(1 - z^{-1})^4Q_4(z),$$  \hspace{1cm} (6.1)
where $g_i$ is the inter-stage gain and $Q_4(z)$ is the quantization error in the last stage. To cancel out the MASH quantization noise, the error-cancelation-logic (ECL) should be

$$H_1(z) = z^{-2}$$
$$H_2(z) = \frac{1}{g_1}z^{-1}(1 - z^{-1})^2$$
$$H_3(z) = \frac{1}{g_1g_2}(1 - z^{-1})^3$$
$$H_4(z) = \frac{1}{g_1g_2g_3}(1 - z^{-1})^4. \quad (6.2)$$

Since we only add an extra stage to the 2-1-1 architecture, the reconfiguration to the 2-1-1 architecture on the fly is almost risk free. Since the added stage is a multi-bit ADC without noise shaping loop, we have the choice to use whatever ADC architecture we prefer. Pipelined ADC can offer high degree of concurrence and approximately linear hardware cost with resolution, and it is easy to be reconfigured to different resolution by adopting different stages. Thus Pipelined ADC is a good candidate for the last stage conversion. Since we have not increased the noise shaping order, the decimator filter can be the same as for the 2-1-1 architecture. As a matter of fact, due to the reduced total out-of-the-band noise power, the decimation filter could be made simpler if we wish to.

The pipelined ADC is shown in the Fig. 6.2, which consists of a cascade of K stages. Each pipeline stage comprises a sample-and-hold amplifier (SHA), a low resolution coarse ADC, a DAC, and a subtracter. In operation, each stage initially samples and holds the output from the previous stage and is then converted into a digital code by the ADC, which is converted back into an analog representation by the DAC. Finally, the difference between the held analog signal and the output of the DAC is amplified to give the residue for the next stage. The final output is the combination of each stage through a digital correction circuit. The primary advantage of pipelined ADCs is that they provide high throughput rates and occupy small die areas.

### 6.2.2 Signal Scaling

Besides the transfer function, the signal scaling is very important in an oversampling sigma-delta modulator design because of the limited supply voltage and the integrator output swing. Fig. 6.3 shows the 2-1-1 architecture implementation with scaling coefficients. It produces outputs $y_i$ that are identical to those in the 2-1-1
architecture in Fig. 6.1, given that

\[
\begin{align*}
b &= \frac{a_{f2}}{a_{f1}a_{i2}} \\
\lambda_1 &= \frac{a_{i3}}{a_{f1}a_{i3}a_{u3}} \\
g_1 &= \frac{a_{f3}}{a_{i5}} \\
\lambda_2 &= \frac{a_{f3}a_{i4}a_{u5}}{a_{f3}a_{i4}a_{u5}} \\
g_2 &= \frac{g_3}{a_{f3}} \\
g_3 &= \frac{a_{f1}a_{i2}a_{u3}}{a_{f3}}
\end{align*}
\]  

(6.3)

The scale coefficients used in this design are summarized in Table 6.1. The scaling in the 2nd integrator of the first stage is different from what was used in [12][13].
The more aggressive scaling used here (1/6 instead of 1/5) makes the capacitance spread of the following stage smaller. This improves matching without calling for large capacitance. Another difference between the 2-1-1 used here and the one used in [12][13] is how much of the 1st stage output is fed to the 2nd stage. Simulations and analytical modeling of the 2-1-1 architecture indicate that for different values of $\lambda$, $b$, and $g$, there is a tradeoff between quantization noise and the input level at which the modulator overloads. Fig. 6.4 shows the histogram of the four integrators outputs of the architecture in Fig. 6.1 based on $2^{14}$ consecutive samples. It is important to keep the outputs inside the linear range, one in this case, so that there is no distortion caused by the limited headroom of the opamps. In the simulations, the sampling frequency is 70MHz and the signal frequency is 170KHz. The input signal power is -4.4 dBFS (0.6 relative to 1).

6.2.3 Performance

The fast Fourier transform (FFT) plots of the second and fourth order modulator outputs are shown in Fig. 6.5 under the same simulation condition. It is obvious
Table 6.1. The scaling coefficients

<table>
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<th>Gain</th>
<th>$a_1$</th>
<th>$a_{i2}$</th>
<th>$a_{f1}$</th>
<th>$a_{f2}$</th>
<th>$a_{i3}$</th>
<th>$a_{i4}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>1/3</td>
<td>1/6</td>
<td>1/3</td>
<td>1/3</td>
<td>1/3</td>
<td>1/3</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Gain</th>
<th>$a_5$</th>
<th>$a_{f3}$</th>
<th>$a_{f4}$</th>
<th>$a_{u3}$</th>
<th>$a_{u4}$</th>
<th>$a_{u5}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
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<td>1/3</td>
<td>1/3</td>
<td>1</td>
<td>1</td>
<td>3</td>
</tr>
</tbody>
</table>

Figure 6.5. PSD of the proposed modulator
that both outputs of 4th order and the proposed one have a 4th order noise shaping. Due to the use of the extra stage, the noise of the proposed is reduced by 36 dB (6 bits). The SNR vs different OSR is shown in Fig. 6.6. The signal amplitude is -4.4 dBFS and random noise is introduced to model thermal noise of the real circuits. At low OSR (high bandwidth), the SNR difference between the 2-1-1 MASH and the final output is equivalent about to the added extra bits. While at high OSR, since the modulator performance is limited by thermal noise, the adding of an extra stage shows no advantage.

6.3 Design Consideration

A differential switched-capacitor (SC) integrator is shown in Fig. 6.7. In the real circuit designs, several non-idealities need to be taken into account, such as thermal noise, opamp bandwidth, slew rate and so on. Based on these considerations, we will select proper specifications for the circuit components, which would not impose too much power requirement while at the same time not degrade the SNR too much.
6.3. DESIGN CONSIDERATION

6.3.1 Thermal Noise

Besides quantization noise, there are various types of circuit noise present in a switched-capacitor sigma-delta modulator, including switch, opmap, DAC noise and other noise sources. The in-band noise power of a modulator can be expressed as:

\[ P = P_Q + P_{cn}, \]

where \( P_Q \) stands for the quantization noise and \( P_{cn} \) for circuit noise. Generally, the circuit noise dominates in low frequency since the quantization noise is shaped away from DC. Given a noise power target, a balance between each noise contribution should be made to optimize power consumptions and areas.

The noise associated with a sampling switch is the thermal noise, i.e. \( KT/C \) noise. The noise associated with an operational amplifier (opamp) is the thermal noise and flicker noise. In wide-band application, the flicker noise is small with relative to thermal noise. We only consider thermal noise here. Fig. 6.8 shows the noise representation of a switched-capacitor integrator, where \( V_{ni}^2 \) represents the noise power associated with switches and \( V_{no}^2 \) represents the noise power of the opamp. Since one of the capacitor plates is connected to the input of the opamp, the noise bandwidth of Fig. 6.8 is related with both the capacitor and opamp [70], given by

\[ \tau_n = (2R_{on} + 1/g_m)C. \]
The input referred thermal noise is contributed by switches and the opamp [70]:

\[ \overline{V_{n,\text{int}}} = \overline{V_{n1}} + \overline{V_{n2}} = \frac{KT}{C_s(1 + 1/x)} + \frac{4KT}{3C_s(1 + x)}, \]  
(6.6)

where \( x = 2R_{\text{on}}g_m \) includes the reduction effect caused by the finite on resistance of switches. Hence, the total noise power is

\[ \overline{V_n} = 1 + \frac{KT}{C_s(1 + 1/x)} + \frac{4KT}{3C_s(1 + x)} = \frac{KT}{C_s} \left( \frac{7/3 + 2x}{1 + x} \right), \]  
(6.7)

The total input referred thermal noise of a modulator is a function of the input referred noise of each integrator. Since the circuit noise of the later stage is shaped by the loop, the noise power of the first integrator dominates.

### 6.3.2 Settling and Slewing

In a sigma-delta modulator, opamp is the key component which limits the overall modulator dynamic range, speed and power. It may raise the quantization noise floor or introduce distortion if the settling is not accurate or nonlinear. It is important to find out the specification of the opamp to achieve the targeted performance while keeping power consumption as low as possible.

As shown in Fig. 6.7 the amplifier in a SC integrator is working in two different configurations at different phase. During \( \phi_1 \), \( C_s \) is sampling the input and the opamp is in hold mode. During \( \phi_2 \), the opamp is in integration mode and starts to settle to a new value. The integration mode specify the power and speed requirements on the opamp since the sampling capacitor \( C_s \) is connected to the input of
6.3. DESIGN CONSIDERATION

the opamp, which increases the load. In the hold mode, the stability of the opamp need to be tested since it has lower loading.

In integration mode, the transient response of the OTA output can be separated into two steps: linear settling and slewing, which specify the small signal and large signal speed performance respectively.

Assuming a single-pole model for the opamp, the output voltages of the integrator is given by:

\[
V_o(t) = \begin{cases} 
V_o(nT_s - T_s) + SR \cdot t & t \leq t_0, \\
V_o(t_0) + (G_i V_i - SR \cdot t_0)(1 - e^{-(t-t_0)/\tau}) & t > t_0.
\end{cases}
\]  

(6.8)

\[
V_o(t) = V_o(nT_s - T_s) + G_i V_i - sgn(V_i)SR \cdot \tau \cdot e^{-(1+\frac{T_s}{\tau} - \frac{G_i}{SR})}.
\]  

(6.9)

In a sigma-delta modulator, a linear settling error can be considered as quantization noise leakage, which gives rise only to noise floor. While slewing results in harmonic distortion since the trans-conductance of an opamp is not constant for large input voltages [71].

It is difficult to determine bandwidth and slew rate specification analytically. System level simulation is usually employed to specify the requirement, by embedding the non-ideal settling effects into the modulator [72]. A practical design need leave significant margin from simulations to ensure good performance.

6.3.3 DC Gain

If the DC gain of the opamp in a SC integrator is not high enough, the pole of the integrator will shift slightly off the unit circle:

\[
Int(z) = \frac{C_s}{C_i} \frac{z^{-1}}{1 - \gamma z^{-1}}.
\]  

(6.10)

This is known as quantization noise leakage too. In a single-loop modulator, this leakage has negligible effect as long as the dc gain is on the order of the oversampling ratio [73]. However in a cascade modulator, the quantization noise will not be canceled exactly by the error-cancellation-logic if the the integrator pole is not at unit circle. The leakage noise will degrade significantly the modulator performance.

6.3.4 Bandwidth and Slew Rate

The closed loop single-pole transfer function can be expressed as

\[
\frac{v_o}{v_i} = -\frac{C_s}{C_i} \cdot \frac{1}{1 + \frac{1}{w_0}}.
\]  

(6.11)
where \( w_0 \) is the dominant pole in feedback. If the amplifier is an operational transconductance amplifier (OTA) with trans-conductance \( g_m \), the pole is given by:

\[
\omega_0 = f \cdot GBW = f \frac{g_m}{C_{\text{leff}}},
\]

where \( GBW \) is the open loop gain bandwidth, \( C_{\text{leff}} \) is the effective load of OTA, and \( f \) is the feedback factor.

\[
C_{\text{leff}} = C_i + C_s \cdot (1 - f)
\]

\[
f = \frac{C_i}{C_s + C_i + C_p},
\]

where \( C_i \) is output capacitance and \( C_p \) is the parasitic input capacitance. Substituting above equations into \( w_0 \), we can get the dominant pole of the transfer function as

\[
\omega_0 = \frac{g_m}{C_{\text{eq}}} = \frac{g_m}{C_i + (C_s + C_p) + \frac{C_i(C_s + C_p)}{C_p}}.
\]

Usually, \( C_i \) is small compared with \( C_p \) and \( C_s \) is large compared with \( C_s \). The effective closed-loop load capacitance becomes:

\[
C_{\text{eq}} \approx C_i + C_s + C_p.
\]

The sampling capacitor \( C_s \) is determined by noise considerations. While the parasitic capacitance \( C_p \) is related to the dimensions of the differential input transistors. If a simple CMOS square law is assumed, the trans-conductance \( g_m \) is proportional to the square root of the transistor width given a fixed bias current. Hence, the bandwidth can be increased by increasing the width \( W \) of the input transistors. However, if \( W \) becomes too large, the increasing of bandwidth is slower since the parasitic capacitance begins to dominate \( C_{\text{eq}} \). A proper width should be chosen to achieve high power efficiency.

For a single-stage amplifier based SC integrators, e.g. with a telescopic amplifier, the slew rate is given by,

\[
SR = \frac{I_B}{C_{\text{leff}}},
\]

where \( I_B \) is the input transistors bias current.

### 6.4 Circuit Design

Fig. 6.9 depicts a switched capacitor implementation of the first stage of the 2-1-1 modulator. It consists of a sampling switch, two integrators and a comparator. In the following section, the design detail will be presented.
Figure 6.9. The SC implementation of the second-order modulator
6.4.1 Sampling Capacitance

The capacitance in a switched capacitor circuit usually determines the maximum speed, area, power dissipation, and design difficulties. Minimizing the capacitance improves the speed and reduces the power dissipation. However, the thermal noise power is inversely proportional to the capacitance and the matching is inversely proportional to the square root of the capacitance area. Another subtle issue is the influence of parasitic capacitance when the sampling capacitor is minimized.

In this design, we select the sampling capacitance in the first stage integrator to be 2.4 pF. The KT/C noise would be well below -80dB level assuming the peak-to-peak signal swing is 2.6V and the OSR is 10. Thanks to the noise shaping, we can scale the capacitance more aggressively than that in a pipelined ADC. We scale the sampling capacitance by a factor of 2 in the second integrator, another factor of 1.5 for the third integrator. Further scaling of the capacitance would have larger impact on the matching.

6.4.2 Bootstrap Switches

As supply voltage goes down, there is less gate-source voltage headroom to turn on the switches, which results in increased on resistance of the switches. To overcome the problems, a dynamic clock voltage doubler is adopted in the design of first
6.4. CIRCUIT DESIGN

Figure 6.11. Fully differential telescopic OTA with gain-boosting

integrator in the first stage. Fig. 6.10 shows the well known gate-source bootstrapping circuit [74]. During $\phi_2$, switches MN3 and MP4 charge the capacitor $C_{boost}$ to VDD. And during $\phi_1$, switches MN1 and MP2 add the pre-charged capacitor $C_{boost}$ in series with the input $V_{in}$ such that the gate-source voltage of the signal switch MNSW is equal to the voltage across the capacitor. Additional transistors MP6, MN6 and MN6s are used to extend all switch operations from rail-to-rail while limiting all gate-source voltages to VDD.

6.4.3 OTA Design

To meet the high DC gain specifications imposed on OTA in MASH structure, a proper OTA topology should be chosen to have optimized performance. Normally multi-stage amplifiers are used if high gain and high swing are required. However, an additional frequency compensation circuit are needed to make multi-stage design stable. Another topology is a single-stage OTA with gain-boosting technique [75], which allows high DC gain while remains high speed. A fully differential telescopic OTA with gain-boosting has been been used in this design. The schematic is shown in Fig. 6.11.

The additional gain-boosting amplifiers, NBOOST and PBOOST outlined in the figure, are implemented with two fully differential, folded cascode OTA with PMOS and NMOS transistor as input differential pairs, as shown in Fig. 6.12. Since the amplifiers have local unit-gain feedback configuration in the main amplifier, setting
Figure 6.12. Schematic of the gain-boosters (a) NBOOST (b) PBOOST
6.4. Circuit Design

6.4.1 Common-Mode Feedback Circuit (CMFB)

The common-mode levels in the full differential OTA are set by the common-mode feedback circuit shown in Fig. 6.14. $V_{cm}$ is the desired common-mode level and $V_b$ is connected to a replica of biasing network so as to establish the desired quiescent currents. The difference between them is sampled onto the $C_a$ to provide a constant voltage on the feedback capacitor $C_b$. The output common-mode level is sensed and refreshed every clock cycle across the common feedback capacitor $C_b$. The

The input common mode level is equivalent to setting the output common mode level [76]. So the common mode feedback is simply achieved only by adding two extra transistors, $MPC$ and $MNC$.

Although gain-boosting technique is able to achieve high DC gain, it introduces pole-zero doubllets that might result in slow settling behavior. The following criterion is proposed so as not to degrade the settling performance[75]:

$$w_0 = f \cdot GBW < w_{booster} < w_{p2}, \quad (6.17)$$

where $w_{booster}$ is the unit-gain frequency of the boosting amplifier and $w_{p2}$ is the 2nd pole frequency of the main amplifier. Fig. 6.13 shows the simulation results of the designed OTA, which has over 100 dB gain and 1.5 GHz unit-gain bandwidth.

![Figure 6.13. The gain and phase plot of the OTA](image)

The gain and phase plot of the OTA.
feedback voltage $V_{cm,fb}$ is used to control the common-mode biasing circuit of the differential opamp, i.e. $VPN$ in Fig. 6.11.

To ensure the stability of the output common-mode voltage or adequate phase margin, the unit-gain frequency of the common-mode closed loop circuit is less than that of the differential-mode closed loop circuit.

6.4.5 Comparator

Since the non-ideality of the single-bit quantizer in each 2-1-1 stages are suppressed by the loop filter, the offset specification is much relaxed. A semi-dynamic comparator is used as a quantizer since it can achieve high speed with a low offset, hysteresis and kick-back noise, while consuming low power. The comparator circuit is shown
in Fig. 6.14, which consists of a differential input pair (M1-M2), a CMOS latch circuit (M4-M7), and an S-R latch [77]. During $\phi_2$, the top (M4-M5) and bottom (M6-M7) regeneration loop are reset. The differential input stage injects a current proportional to the input voltage difference flowing through the resetting switch M12, which generates an initial voltage imbalance between nodes a and b. This imbalance is then amplified in the two regeneration steps. Between $\phi_2$ going down and $\phi_1$ getting high, the initial voltage is first regenerated by the M4-M5. Then after $\phi_1$ goes high, M8-M9 are closed and p-channel flip-flop, M4-M5, starts to regenerate so that the voltage difference between O1 and O2 is amplified to a voltage swing nearly equal to the power supply voltages. The S-R latch is brought to the logic state during regeneration phase and keeps the last output state in the resetting mode.

6.4.6 Clock Generator

Switched capacitor circuits require two non-overlapping clock phases to control the switches. To avoid signal-dependent charge injection, bottom plate sampling is commonly used in which two slightly delayed waveforms are needed. In actual design, to extend the settling time, only the falling clock edges need to be delayed, as shown in Fig. 6.16(b). The circuit designed to implement such clock scheme is shown in Fig. 6.16(a).

6.4.7 Inter-Gain Stage and Pipelined ADC

The inter-gain stage between the 2-1-1 MASH and the extra pipelined ADC is shown in Fig. 6.17. The gain is programmable by 3 or 1.5 due to the SC circuit speed consideration. The speed of an SC circuit does not only depend on the opamp speed but also the feedback factor. As the equation 6.12 indicates, the smaller the feedback factor (the higher the closed-loop gain), the lower the speed. The feedback factor is related to the gain as following

$$f = \frac{1}{1 + (a - 1) + \delta}, \quad (6.18)$$

where $a$ is the gain and $\delta$ is the ratio of the input stray capacitance of the opamp and the sampling cap. Notice that the term $(a - 1)$ is due to the use of the feedback capacitor as one of the sampling capacitor. This improve the speed. Otherwise, the term $(a - 1)$ becomes only $a$.

To achieve a settling error of 0.01%, the -3 dB bandwidth has to be 3-4 times the clock frequency. With a gain of 3, the opamp has to be have a unit-gain bandwidth of 1 GHz within all the corners. It is not a simple task. With a gain of 1.5, the opamp only needs to have a unit-gain bandwidth in the neighborhood of 500 MHz. It is much easier task. The drawback of having a gain of 1.5 is the attenuation of the quantization noises of the previous stage and therefore one more bit is needed
in the following Nyquist ADC. Since we use a pipelined ADC, the cost of adding one extra bit is negligible.

6.4.8 Voltage Reference Buffer

In ADCs, a stable voltage reference is required as the basis of the conversion. In a switched capacitor circuit, a voltage reference buffer is usually needed to provide current to the capacitor. It must have low impedance enough to ensure complete settling within every clock period. There are two ways to implement the voltage reference buffer. One is using an on chip high speed negative feedback opamp as buffer, as shown in Fig. 6.18(a), which results in high power consumption. Another way is employing a large external capacitor to provide low impedance to over wide
Figure 6.17. Switched-capacitor circuit of inter-gain stage
bandwidth as shown in Fig. 6.18(b). This approach has better noise performance but requires additional pins. Also a large trans-conductance $G_m$ is required to provide dc current since the SC circuit has an equivalent resistor of $1/(f_sC)$. In high speed application, it is hard to settle completely due to the resonant tank formed by pad-bonding and the external capacitor. So we adopt the former approach in this design.

6.5 Expermental Results

The modulator of Fig. 6.1 has been implemented in a $0.25\mu m$, 3.3 V CMOS technology with metal-insulator-metal (MIM) cap. The power supply voltage for the analog circuit is 3.3V and 2.5V for the digital circuit. Fig. 6.19 shows the photo of the prototype chip. Bench test board are made to evaluate the performance of the prototype chip. The input signal is generated by SGS DS360, and is converted to differential signal on the board. The sampling clock is produced by Agilent 33250A. In the measurement, the sampling frequency is 70MHz and the input sinusoid signal frequency is 170KHz. Different signal amplitudes are applied to the chip. The modulator digital output data are captured through Logic Analyzer TLA614 and stored in a PC. The FFT analysis of the data is then performed in Matlab as shown in Fig. 6.20 and Fig. 6.21. In the figures, the top line is the FFT of the first stage's second-order modulator output, which exactly shows the second-order characteristic: the quantization noise increases by $20dB/decade$; the middle one is the FFT of 2-1-1 cascaded modulator output, and the bottom line is the FFT of the whole
6.6. CONCLUSION

In this chapter, we propose a new reconfigurable sigma-delta pipelined modulator. The measurement results show that it achieves 65 dB SNR over 7 MHz bandwidth and be scalable for different bandwidth/resolution application.

modulator output. Thanks to the extra ADC stage added in the last stage, it is obviously seen that the quantization noise is lower for the modulator although it still presents a fourth-order characteristic performance.

Figure 6.22 plots the measured SNDR versus input amplitude at the sampling frequency of 70MHz and the OSR of 10. The highest SNDR is around 67dB. Compared to the ideal system level simulation, the white noise floor is higher than the ideal case. Also the distortion when the large input signal applied is higher than the simulation. The reason for this could be: 1) The input signal to the chip is not a pure high quality sinusoidal waveform. 2) The test PCB will introduce some noise and distortion. 3) Some parts of the circuit are not well designed. In the later work, we will focus on the above items and improve the chip’s performance.

6.6 Conclusion

In this chapter, we propose a new reconfigurable sigma-delta pipelined modulator. The measurement results show that it achieves 65 dB SNR over 7 MHz bandwidth and be scalable for different bandwidth/resolution application.

Figure 6.19. Die micrograph of the proposed modulator
Figure 6.20. FFT of the measured output data without input

Figure 6.21. FFT of the measured output data with -4 dbFS input
Figure 6.22. SNDR versus input power


Chapter 7

Conclusions and Future Work

7.1 Conclusions

In this thesis, we investigated the new topology and structure of sigma-delta modulator suitable for wideband applications, e.g., wireline or wireless communication system applications. The following topics associated with the design of high speed high resolution sigma-delta modulator were studied in detail:

- The low distortion sigma-delta modulator is introduced. Based on that, an improved wideband low distortion cascaded sigma-delta structure is presented.
- A feedforward continuous-time sigma-delta modulator with new loop delay compensation scheme is proposed.
- The effect of different feedback DAC scheme on the design of continuous-time quadrature bandpass sigma-delta modulator is compared.
- The design of a new reconfigurable sigma-delta pipelined modulator is presented. The measurements results shows that it achieves a high SNR over a wideband and be scalable for different bandwidth/resolution application

7.2 Future Work

Some of the new structures described in this thesis are based on the MATLAB simulation. It would be good to implement them to prove the theory. Besides, a lot of real implementation issue related the circuit design should be taken into consideration, e.g., high performance integrator or resonator design, dynamic element matching (DEM) techniques in multi-bit feedback DAC.

In the last chapter, the function of proposed reconfigurable sigma delta pipelined modulator is verified, but its performance is somehow not good enough as we expected. In the future, more work will be put on to improve its performance.
Also, the design and implementation of the proposed SCR feedback continuous-time quadrature bandpass sigma-delta modulator will be continued.
Bibliography


