Design of a Direct-conversion Radio Receiver Front-end in CMOS Technology

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The front-end comprises a low-noise amplifier (LNA) and a mixer. Different LNA and mixer architectures has been studied and from the mentioned inherited problems with direct conversion, one proposal for a solution is a differential source degenerated LNA and a differential harmonic mixer, which has been designed and simulated.

The LNA has a gain of 12dB, a noise figure of 3.6dB and provides a return loss better than -15dB. The overall noise figure of the signal path is 8dB and the overall IIP3 and IIP2 is -12dBm and 31dBm, respectively.

Keyword
Direct-conversion, Radio receiver, Front-end, CMOS, LNA, Mixer, Low-noise amplifier, Harmonic mixer.
Abstract

In this Master’s thesis, a direct-conversion receiver front-end has been designed in a 0.18 \( \mu m \) CMOS technology.

Direct-conversion receivers (DCR) have obvious advantages over the heterodyne counterpart. Since the intermediate frequency (IF) is zero, the problem of image is circumvented. As a result, no front-end image reject filter is required and the channel selection requires only a low-pass filter which makes it easy to integrate directly on chip. However, the DCR also suffers from several drawbacks such as extreme sensitivity to DC offsets, 1/f noise, local oscillator (LO) leakage/radiation, front-end nonlinearity and I/Q mismatch. This implies very high demands on the DCR front-end.

The front-end comprises a low-noise amplifier (LNA) and a mixer. Different LNA and mixer architectures has been studied and from the mentioned inherited problems with direct conversion, one proposal for a solution is a differential source degenerated LNA and a differential harmonic mixer, which has been designed and simulated.

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1 Terminology

CMOS - Complementary Metal Oxide Semiconductor

DC - Direct Current

DCR - Direct Conversion Receiver

DSB - Double Sideband

IF - Intermediate Frequency

IIP2 - Second order Input Interceptpoint

IIP3 - Third order Input Interceptpoint

IM - Intermodulation

LAN - Local Area Network

LNA - Low Noise Amplifier

LO - Local Oscillator

MOSFET - Metal Oxide Semiconductor Field Effect Transistor

NF - Noise Figure

RF - Radio Frequency

SAW - Surface Acoustic Wave

SNR - Signal to Noise Ratio

SSB - Single Sideband

TDMA - Time Division Multiple Access

TSMC - Taiwan Semiconductor Manufacturing Company

VCO - Voltage Controlled Oscillator

W-LAN - Wireless Local Area Network
2 Introduction

2.1 Background

The growing popularity of notebook computers has lead to a demand for high data-rate wireless local area network (LAN) systems. The superheterodyne architecture is the most widely used architecture for wireless receivers. But since the development goes towards greater miniaturization and more cost efficient manufacturing, the direct-conversion architecture becomes more and more interesting.

Radio receivers with a direct-conversion, also known as Zero-IF or homodyne, architecture are suitable for integration due to the absence of highly selective filters at radio- and intermediate frequencies, which have to be implemented off-chip. The direct-conversion architecture however has some inherent drawbacks, e.g. sensitivity to DC-offsets and local oscillator leakage which are issues that need to be addressed in the design of front-ends for such receivers.

2.2 Task

To study different direct-conversion receiver front-end circuit topologies consisting of a low noise amplifier and a quadrature mixer. Find and design one CMOS front-end showing promise for low local oscillator leakage, low inherent DC-offset, good amplitude and phase balance and sufficient dynamic range for IEEE Std 802.11a 5 GHz W-LAN applications. The process used was TSMC 0.18 μm mixed signal 1P6M+ salicide 1.8V / 3.3V, and the software tool and simulator was Cadence RF Spectre togheter with foundry-provided component libraries.

2.3 Outline of the report

The first part of the report, section 1 to section 5, is a introduction to direct-conversion receivers, different low-noise amplifiers and mixers. Section 6, covers the design and simulations of the chosen LNA and mixer. In section 7 to 9, the results are presented and discussed.
3 Direct Conversion Receivers

Direct-conversion receivers (DCR), differs from the more commonly used heterodyne receiver in such way that there is only one downconversion stage, and it converts the RF signal all the way down to zero frequency. The DCR uses the fact that a signal and its image is separated by twice the intermediate frequency (IF). Thus a downconversion architecture with zero IF, produces an image at zero frequency, i.e. the desired signal is its own image. This is an important advantage over the heterodyne architecture since no image filter is required, and the low-noise amplifier (LNA) need not drive a 50-Ω load which is common when an off-chip image filter is used. Furthermore the IF SAW filter and subsequent downconversion stages in the heterodyne receiver can be replaced with low-pass filters and baseband amplifiers that can be integrated directly on the chip. However, the DCR suffers from several serious drawbacks.

3.1 DC Offsets

One of the most severe problem in a DCR is the extreme sensitivity to DC offsets. DC offsets mainly arises from so-called local oscillator (LO) leakage or another phenomenon called interferer leakage.

![Diagram of DCR](image)

Figure 1: Self mixing of (a) LO signal, (b) a strong interferer. [5]

The isolation between the LO port and the inputs of the mixer and the LNA is not infinite. This means that a finite amount of feedthrough exists from the LO port of the mixer to the input port of the LNA and RF port of the mixer. This leakage is due to capacitive and substrate coupling. If the LO signal leaks to the inputs of the LNA or mixer, it will be mixed with the “real” LO signal and then produce a DC component. This is called “self mixing”. Similarly, if a
large interferer leaks from the LNA or mixer input to the LO port. It will be
multiplied by itself and thus also produce a DC component, figure 1.

The DC offset problem can be even worsened if the LO leaks to the antenna
and radiates. Then, the LO signal might reflect from moving objects back to the
receiver. This will cause a time varying offset which may be difficult to distinguish
from the actual signal. The radiated signal can also interfere with other receivers.

The offset problem can be somewhat mitigated by the use of offset cancel-
lation. For example in TDMA systems, the idle time can be used to perform
offset cancellation with sufficient frequency to take into account variations due to
moving objects. When designing the DCR front end, great care must be taken
in the choice of LNA and mixer architecture to minimize LO leakage. [3] [5]

3.2 1/f Noise

Since the downconverted spectrum extends to zero frequency, the 1/f noise of
devices will corrupt the signal, especially in CMOS implementations. This sets
high demands on the LNA and mixer to provide a high gain at the RF frequency.
As the stages following the mixer operate at low frequencies, these devices can
be made large to minimize the magnitude of the 1/f noise. [3] [5]

3.3 I/Q Mismatch

For phase and frequency modulated signals the DCR must perform quadrature
mixing. This can be done by shifting either the RF signal or the LO output by
90°. Since shifting the RF signal involves severe noise-power-gain tradeoffs, it is
preferable to shift the LO signal. In either case, the errors in phase and amplitude
between the I and Q signals corrupt the downconverted signal constellation and
raises the bit error rate.

Typically it is desirable to maintain the amplitude mismatch below 1 dB and
phase error below 5°. But it is the type of modulation that sets the bounds for
the I/Q mismatch. [5]

3.4 Even-Order Distortion

When using a DCR architecture, even-order distortion also becomes a problem-
atic issue. For example, if two strong interferers close to the channel experience
a nonlinearity in the LNA. The result could be that the two interferers generate
a low-frequency beat in the presence of even-order distortion. If the mixer were
ideal, this would not be any problem since such a term would be translated to
high frequency. However, in the non ideal world, the mixer exhibit some finite
direct feedthrough from the RF input to the IF output. This makes it possible
for a low frequency interferer to pass through the mixer and corrupt the signal.
One approach to this problem is to use a differential LNA which by symmetry reduces the even-order distortion. [5]

4 Low Noise Amplifier LNA

The main function of the LNA is to provide enough gain to overcome the noise of the following stages. Since the LNA is the first gain stage in the receive path, its noise figure directly adds to that of the system. The LNA must also present a specific impedance to the input source, usually 50 Ω. Another important parameter for the LNA is the reverse isolation. It is the reverse isolation that determines the amount of LO signal that leaks to the antenna. The leakage stems from capacitive paths, substrate coupling, and bond wire coupling.

Linearity also is an important consideration since the LNA must do more than just amplify the signal without adding noise. It is important that the LNA remains linear when strong signals are being received and even more when weak signals, in the presence of a strong interferer are received. Otherwise, problems like blocking and cross-modulation can occur. The most common measure of linearity is the third-order intercept (IP3) and 1-dB compression point ($P_{1dB}$), figure 2. In the case when DCRs are used it is the second-order intercept (IP2) that is more important. Where it is desirable to achieve as high IP2 and $P_{1dB}$ as possible.

![Figure 2: LNA linearity parameters.](image-url)
4.1 LNA Design Strategies

In an MOSFET device, the input impedance is capacitive. But we want to present a specific impedance to the source so that we match the input impedance of the LNA to the preceding elements output impedance. Otherwise unwanted reflection of the signal takes place.

One way is simply to put a resistor across the input terminals of a common-source amplifier. This is not a particularly good solution since the resistor adds thermal noise and attenuates the signal ahead of the transistor. A better way is to use inductive source degeneration where an inductance is coupled to the source of the transistor, figure 3. The advantage is that one can control the real part of the impedance through choice of inductance, and a pure reactance is noiseless. However with inductive source degeneration the impedance is only resistive at resonance, so this can only provide a narrowband impedance match, which in some cases might be preferable. But the inductors usually needs to be quite large, occupying a lot of die area and can easily pick up noise. Although, since the frequency is quite high in this application, inductive source degeneration would be a good choice since the inductances would become rather small due to the high frequency.

![Source degeneration diagram](image)

**Figure 3: Source degeneration.**

Another interesting approach is an inductorless cascoded differential LNA, Figure 4, where a mixture of resistive and capacitive feedback is used to achieve a resistive input impedance. This architecture prevents inductive crosstalk and reduces size. [3] [1]

A differential LNA is a good choice for the DCR since it reduces the effect of even order distortion and improves the dynamic range. Although a differential solution requires twice as much current to maintain the same NF as a single ended LNA. It also requires a balun since the antenna interface is single-ended.
5 Mixers

All present mixers in use today perform an indirect multiplication operation between two signals in the time domain, and thereby converts the signal to the desired frequency. The result from the multiplication is output signals at the sum and difference frequencies of the input. The amplitudes of the output signals are proportional to the product of the LO and RF amplitudes. Since the LO amplitude is constant, any amplitude modulation of the RF signal is transferred to the IF signal. An unwanted transfer of modulation can also occur through nonlinear interaction in both mixers and amplifiers, so called cross-modulation. So a high linearity is also an important factor in mixer design. Another important mixer characteristic is conversion gain, which is defined as the ratio of the desired IF output to the value of the RF input. A conversion gain is more preferable than conversion loss, since the mixer then provides amplification along with the frequency translation. [3]

The noise figure of the mixer is also important. The definition of NF is the signal to noise ratio (SNR) at the RF input port, divided by the SNR at the IF output port. Usually, when desired signal only exists at one frequency, the noise figure of interest is the single-sideband noise figure (SSB NF). But in the case when a DCR architecture is used, it is the double-sideband noise figure (DSB NF) that is of interest. This is because it is both the “main” RF and image signals that contains useful information.

Isolation is another parameter of importance in a mixer. Since the LO signal power is generally higher than the RF signal power, any leakage to the RF or IF port is unfortunate, causing DC offsets. Especially in the DCR case when the
LO signal is at the same frequency as the RF signal.

5.1 Double-Balanced Mixers

Since direct conversion receivers suffers greatly from LO leakage to the RF and IF paths, some means must be taken to mitigate this problem. One approach is to use double-balanced mixers. Such mixers exploit symmetry to remove the undesired output LO component through cancellation. [3]

5.1.1 Active Double-Balanced Mixer

In an active double-balanced mixer, the LO drive must be large enough to make the differential pairs act like current-steering switches, Figure 5. The RF signal is converted into a current and the multiplication takes place in the current domain. The mixer provides good LO-IF isolation, but the dynamic range is limited by the linearity of the V-I converter in the RF port of the mixer.

![Active Double-Balanced Mixer](image)

Figure 5: Active double-balanced mixer. [3]

5.1.2 Passive Double-Balanced Mixer

An alternative that avoids the V-I conversion problem is to switch the RF signal directly in the voltage domain. Since CMOS technology offers good switches, an interesting mixer would be a passive double-balanced mixer. Such a mixer consists of four switches in a bridge configuration, Figure 6. The absence of DC bias current in such mixers implies the absence of 1/f noise which is particularly valuable in DCR:s, where such noise often is dominant. The switches can be implemented with complementary transmission gates, and ideally cancel out the LO feed-through due to capacitive and substrate coupling, if the signal paths are made equal and symmetric in the layout [4]. The drawback to this mixer is that the LO drive must be high enough so that the switches can change their states fast. Then, any leakage of the LO signal creates a strong interferer which can corrupt the signal.
5.2 Harmonic Mixers

Since DC offset is the major problem in DCR:s, a balanced harmonic mixer would be an interesting alternative. In the harmonic mixer, the LO frequency is half the RF frequency and it is the second harmonic of the LO signal that takes part in the mixing process. As a result, the LO leakage generates no DC component but an output situated at the LO frequency which easily can be filtered out, Figure 7.

The LO stage of the mixer converts the differential LO voltage into a time-varying current which contains the second harmonic. In principle, the fundamental and all odd harmonics of the LO cancels out at the connected drain terminals and the DC offset problem will be mitigated. The injected current I0, Figure 8, reduce the current through the upper transistors driven by the RF signal. This reduces the 1/f noise of the upper transistor pair, which is the main noise contributor. [8]
Figure 8: Harmonic mixer with current injection. [8]
6 Front End Design

The receiver front-end is intended for the IEEE Std 802.11a 5 GHz W-LAN. The standard covers 300 MHz divided into three frequency bands. The lower band 5.15 - 5.25 GHz, the middle band 5.25 - 5.35 GHz and the upper band 5.725 - 5.825 GHz.

6.1 LNA Design

The LNA architecture was chosen to be a differential source degenerated LNA, figure 9. The differential structure has obvious advantages over the single ended counterpart. The incremental ground located at the symmetrical point of a differential structure removes the sensitivity to parasitic ground inductance. This makes the real part of the input impedance controlled only by the source degeneration inductor (Ls), and unaffected by parasitics in the current source’s ground return path. Another advantage is the ability to reject common-mode disturbances.

![Differential source degenerated LNA](image)

Figure 9: Differential source degenerated LNA.
6.1.1 Circuit Design

The first parameter calculated for the LNA is the optimum width of the input MOSFETs. An expression for the width of the optimum device with respect to noise and power optimization can be derived from the MOSFET noise parameters [3]

\[ W_{\text{opt}} \approx \frac{1}{3\omega LC_{\text{ac}} R_s} \]  

(1)

Where in this case:

\[ \omega = 2\pi f = 2\pi \times 5.5 \times 10^9 \approx 34.6 \text{Grad/s} \]

\[ L = 0.18 \mu m \]

\[ C_{\text{ac}} \approx 8.46 \text{mF/m}^2 \]

\[ R_s = 50\Omega \text{ Differentially} \]

This gives the optimum width of the input transistors as approximately 250\mu m. The next step in the design process is to determine the source inductance. First \( f_T \) needs to be calculated. The frequency capability of an MOSFET is usually specified by finding the transition frequency \( f_T \). For an MOS transistor, \( f_T \) is defined as the frequency where the magnitude of the short-circuit, common-source current gain falls to unity. In the short-channel regime [7]

\[ \omega_T = \frac{v_{\text{sat}}}{L} \]  

(2)

Where:

\( v_{\text{sat}} \) is the velocity saturation of carriers in the channel and expressed as \( f_T \):

\[ f_T = \frac{v_{\text{sat}}}{2\pi L} \]  

(3)

One can see that \( f_T \) is independent of width and gate overdrive when we take the short-channel effects into account. In this design with \( v_{\text{sat}} = 84292.05 \text{ m/s} \), specified in the TSMC transistor model, gives an \( f_T \) of 74 GHz. Now, the source inductance \( L_s \) can be calculated.

\[ L_s = \frac{Z_{\text{in}}}{\omega_T} \]  

(4)

To generate a real part of 25\Omega, the source inductance should be approximately 50pH. However, a somewhat larger value should be chosen to compensate for the cascoding transistors effect on the overlapping gate-drain capacitance \( (C_{gd}) \) of the input transistors.

To calculate the total inductance of the input stage, the gate-source capacitance of the input transistor must be calculated.
\[ C_{gs} = C_{ox} W (L - 2\delta L) \] (5)

In this process, \( \delta L = 1 \times 10^{-8} \). This results in a \( C_{gs} \) of 340 fF. To resonate this capacitance at 5.5 GHz, the total inductance can be calculated from:

\[ X_C = \frac{1}{\omega C} \] (6)
\[ X_L = \omega L \] (7)

For resonance, \( X_C = X_L \Rightarrow \)

\[ L_{tot} = \frac{1}{\omega^2 C_{gs}} \] (8)

This gives the total inductance to be approximately 2.4 nH. So the gate inductance \( L_g \) should be 2.35 nH.

The cascoding transistors main tasks is to provide gain and reverse isolation between the output and the input of the LNA. Otherwise any leaking LO signal could find its way through the LNA and radiate out from the antenna, and thus interfere with other devices. The transistors are chosen to have the same width as the input transistors. This is a common choice but not necessarily ideal. The size of the cascoding transistors is constrained by two competing considerations. To reduce the consequences of the Miller effect (unwanted capacitive feedback from output to input), a large cascoding device would be preferable. However with a large device, the parasitic source capacitance effectively increases the amplification of the cascoding device’s own internal noise at high frequencies. [3]

The LC network on the output forms an L-matching network for optimal power transfer to the mixers.

6.1.2 Simulations

The simulations of the circuit resulted in somewhat different dimensions of the input-matching network. In order to achieve a good matching with low noise and high gain, the gate inductors were modified. The result with \( L_g = 1.7 \) nH and \( L_s = 50 \) pH is shown in figure 10.

The S-parameter or scattering-parameter representation is common figures of merit when describing RF circuits. S-parameters are power-wave descriptors that define the input-output relations of a network in terms of incident and reflected power waves. S11 is the input reflection coefficient, i.e. how much of the incident power wave is reflected back at the input. Of course, one would want this to be as little as possible. In this case, S11 is \( < -14 \) dB over the frequency range 5.15 - 5.825 GHz. In the same way, S22 = \( < -11 \) dB and is the output reflection coefficient. S21 describes the forward gain of the circuit which in this case is 20
Figure 10: Simulated LNA S-parameters.

dB. The isolation from the output to the input is described by S12 which is the reverse gain, in this case < -35.5 dB.

One of the most important characteristics of an amplifier is its gain. The LNA must provide enough gain to overcome the noise of the subsequent stages. As already mentioned, S21 described the forward gain. In this case when the input and output impedances differ, S21 is the forward power gain. In figure 11, the simulated voltage gain is shown. The voltage gain at 5.5 GHz is 29 dB, and the 3-dB bandwidth is 1.3 GHz.

The noise figure of the LNA is also of great importance. Since the LNA is the first gain stage of the receiver, its noise figure directly adds to that of the system. In most analog circuits, the signal-to-noise ratio (SNR), defined as the ratio of the signal power to the total noise power is the important parameter. In RF design on the other hand, most of the front-end receiver blocks are characterized in terms of their noise figure rather than the SNR. The definition of the noise figure differs somewhat in the literature but a common definition is:

\[
\text{Noise Figure} = 10 \log_{10} F \tag{9}
\]

Where F is the noise factor:

\[
F \equiv \frac{\text{total output noise power}}{\text{output noise due to input source}} \tag{10}
\]

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The noise figure is a measure of the degeneration in SNR that a system introduces. A large degeneration results in a large noise figure. If a system adds no noise of its own, then the total output noise is completely due to the source, and the noise figure is zero since the noise factor is unity. The simulated noise figure of the LNA at 5.5 GHz is 2.44 dB, figure 12.
Receivers for the wireless-LAN standard must have a wide dynamic range. The transmitter and receiver can be very close to each other, and then the receiver must handle signal strengths up to -20 dBm. On the other hand, the signal can be quite weak due to fading. So the receiver must be sensitive enough to detect signals down to -82 dBm. A highly linear receiver is needed to accommodate such strong signals in the presence of very weak signals. One common linearity measure is the 1-dB compression point \( P_{1dB} \). The 1-dB compression point is the point where an increase in the RF input amplitude results in a conversion gain that is 1 dB lower than that observed at lower input amplitudes. The 1-dB compression point for the LNA is -20.7 dBm, figure 13.

![1-dB Compression Point](image)

**Figure 13: Simulated LNA 1-dB compression point.**

Another linearity measure is the third-order input intercept point (IIP3). This parameter is measured by a two-tone test with two signals close to each other in frequency. When two signals with different frequencies are applied to a nonlinear system, so called intermodulation occurs. This arises from mixing of the two signals when their sum is raised to a power greater than unity. Suppose the signal \( V_p \cos(\omega_1 t) + V_p \cos(\omega_2 t) \) passes through a non linear system, then the resulting output signal would be:

\[
\Rightarrow a_1 (V_p \cos(\omega_1 t) + V_p \cos(\omega_2 t)) + a_2 (V_p \cos(\omega_1 t) + V_p \cos(\omega_2 t))^2 +
\underbrace{a_3 (V_p \cos(\omega_1 t) + V_p \cos(\omega_2 t))^3 + \ldots}_{(11)}
\]
Where (a) is the second-order intermodulation:

\[
(a) = a_2 V_p^2 \left( \frac{1 + \cos(2\omega_1 t)}{2} \right) + a_2 V_p^2 \left( \frac{1 + \cos(2\omega_2 t)}{2} \right) + 2a_2 V_p^2 \left( \frac{\cos([\omega_1 + \omega_2] t) + \cos([\omega_1 - \omega_2] t)}{2} \right) \quad (12)
\]

And (b) is the third-order intermodulation:

\[
(b) = a_3 V_p^3 \left( \frac{\cos(3\omega_1 t) + 3 \cos(\omega_1 t)}{4} \right) + a_3 V_p^3 \left( \frac{\cos(3\omega_2 t) + 3 \cos(\omega_2 t)}{4} \right) + 3a_3 V_p^3 \left( \frac{\cos(\omega_1 t) + 0.5 \cos([2\omega_1 - \omega_2] t) + 0.5 \cos([2\omega_1 + \omega_2] t)}{2} \right) + 3a_3 V_p^3 \left( \frac{\cos(\omega_2 t) + 0.5 \cos([2\omega_2 - \omega_1] t) + 0.5 \cos([2\omega_2 + \omega_1] t)}{2} \right) \quad (13)
\]

Usually, it is only the third-order intermodulation products \(2\omega_1 - \omega_2\) and \(2\omega_2 - \omega_1\) that are of interest since they can fall in the desired band. However, one can see that the second-order IM product \(\omega_1 - \omega_2\) becomes important when direct conversion is used. If the two signals are very close together, they will produce a component very close to DC. So the second-order intercept point (IIP2) is an even more important parameter for the direct conversion receiver than the IIP3. The IIP2 and IIP3 are unique quantities that can serve as a means when comparing the linearity of different circuits. The simulated IIP3 is shown in figure 14.

![Simulated LNA third-order interceptpoint](image)

Figure 14: Simulated LNA third-order interceptpoint.
6.1.3 Simulations With RF-models

When the thesis work started, the TSMC process was not completely functioning. As a result, the former design and simulations were carried out with non RF transistor models and ideal passive components, although with added resistive parasitics to the inductors and an estimated Q-value of 6.

When the complete process design kit were installed, some new problems occurred. The TSMC RF-models for the inductors does not support inductances less than 2.37 nH. This is somewhat problematic since at this frequency, 5 - 6 GHz, the source inductors must be much smaller if a good match to 50Ω is to be accomplished. This meant that a redesign was needed. Since the LNA must be preceded by a balun to differentiate the single ended signal from the antenna. An impedance conversion from 50Ω to 100Ω should not be a problem. After this change, a reasonable impedance match with all the inductors set to 2.37 nH were accomplished, figure 15.

![Figure 15: Simulated LNA S-parameters with RF-models.](image)

A negative effect, caused by the large source inductors is that the power gain has dropped significantly, S21 in figure 15. This is since the source inductors provides a resistive impedance at this frequency, and thus acts like a negative feedback that lowers the gain. As a result, the voltage gain at 5.5 GHz is now just over 12 dB, figure 16.

The noise figure is also deteriorated. Mostly as a result of the increased resistive losses due to the larger inductances. But probably also since the RF-transistor models predicts the noise better in the high frequency range than the
ordinary models. Now, the worst-case noise figure is just above 3.6 dB at 5.825 GHz, figure 17.

Figure 17: Simulated LNA noise figure with RF-models.

As one could expect, improved linearity is a consequence of the lowered gain of the LNA and the fact that the negative feedback from the large source inductors has a linearizing effect. The simulated 1-dB compression point is shown in figure 18, the compression point now occurs at -1.6 dBm. The input referred IP3 has also moved up to around 10 dBm, figure 19
Figure 18: Simulated LNA 1-dB compression point with RF-models.

Figure 19: Simulated LNA IIP3 with RF-models.

6.1.4 Bias and Stability

The DC biasing of the LNA is done with simple current mirrors. This is mainly due to the limited time frame of this thesis work. An more advantageous solution would be to use a constant-$g_m$ bias source to stabilize gain and input impedance over temperature and supply variations [3]. In this design however, the current is mirrored by a transistor through a high value resistor to set the DC-bias level at the gate of the input transistor. A decoupling capacitor is also added to prevent
any RF signal leakage to the supply, figure 20. [6]

The stability must also be considered when designing amplifiers. The first step is to determine whether the amplifier is unconditionally stable or not. This can easily be done using Rollet’s K stability factor and Δ. The amplifier will be unconditionally stable if K > 1 and |Δ| < 1. [4] [6]

\[
K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|}
\] (14)

Where Δ = S_{11}S_{22} - S_{12}S_{21}.

In figure 21, the K-factor and |Δ| is plotted from 0 to 60 GHz. Since K > 1 and |Δ| < 1, the LNA is unconditionally stable, at least up to 60 GHz. However, one must remember that the stability is not only affected by frequency, but also the bias conditions. So the stability can change if the biasing, or even the temperature changes.

![Figure 21: LNA K-factor and |Δ|](image-url)
6.1.5 LNA Performance Summary

The simulated performance of the LNA, both with the non RF transistor models and small source inductances. And with the RF-models and TSMC provided inductors is presented in table 1.

<table>
<thead>
<tr>
<th></th>
<th>“Ideal”-Models</th>
<th>RF-Models</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply</td>
<td>1.8 V</td>
<td>1.8 V</td>
</tr>
<tr>
<td>Voltage gain</td>
<td>29 dB</td>
<td>12 dB</td>
</tr>
<tr>
<td>S11</td>
<td>&lt; -14 dB</td>
<td>&lt; -15 dB</td>
</tr>
<tr>
<td>S21</td>
<td>&gt; 20 dB</td>
<td>&gt; 6.35 dB</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>2.48 dB</td>
<td>3.6 dB</td>
</tr>
<tr>
<td>1-dB Compression point</td>
<td>-20.7 dBm</td>
<td>-1.6 dBm</td>
</tr>
<tr>
<td>IIIP3</td>
<td>-6.8 dBm</td>
<td>10 dBm</td>
</tr>
<tr>
<td>IIIP2</td>
<td>20 dBm</td>
<td>51 dBm</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>31 mW</td>
<td>27 mW</td>
</tr>
</tbody>
</table>

Table 1: LNA performance parameters.

6.2 Mixer Design

The mixer structure is chosen to be a differential double balanced harmonic mixer for its inherited insensitivity to LO leakage and self-mixing. Recall that the harmonic mixer is fed with an LO frequency that is half the RF frequency, and it is the second harmonic of the LO that is used for the mixing. Therefore, any LO leakage from the LO port to the RF port is not a problem since it won’t be mixed down to DC.

The differential structure is used to suppress common-mode substrate noise and interference. To improve linearity and provide constant impedance to the LNA, a double balanced structure is also used.

6.2.1 Circuit Design

The LO stage of the mixer consists of the four transistors M1 - M4 at the bottom of figure 22. They are put up in pairs where each pair acts like a squaring cell that converts the differential LO voltage to the time-varying current, which contains the second harmonic. The right pair is driven by the same LO signal as the left, although shifted 90° in phase. The result is a differential signal at twice the LO frequency at point A in figure 22. To obtain as large current as possible, the LO-transistors are made wide, 300 um, and biased very close to their threshold voltage since it is the non-linearity of the MOSFET and the switching operation that is used to obtain the second harmonic. The RF transistors, M5 - M8, are
also dimensioned to be quite wide, 250 um. This is to provide a large \( \text{gm} \) and a lower thermal noise. The two output resistors are set to place the output signal in the middle of the remaining voltage room to allow a large swing of the output signal.

### 6.2.2 Simulations

In figure 23, the LO signal is at 2.5 GHz and the resulting second harmonic at point A in figure 22 is at 5 GHz. The simulations give that the optimum LO amplitude for this design is 200mV with the present bias conditions.

The gain of the mixer is expressed as conversion gain (or loss), which is defined as the ratio of the desired IF output to the value of the RF input. An active mixer can have a conversion gain, which is desirable since the mixer then provide amplification along with the frequency translation. In this design, the voltage conversion gain is >5 dB in the lower frequency range (5.15 - 5.35 GHz). And >3 dB in the upper frequency range (5.725 - 5.825 GHz), figure 24. The gain difference between the two bands stem from the input matching difference.

The noise figure of the mixer is defined as in the case with the LNA. There is a difference though, in a mixer there are two input frequencies that will generate a given intermediate frequency. One is the desired RF signal, and the other is the image signal. Usually it is only the single sideband (SSB) noise figure that is correct since there is no desired signal in the image. In the case with direct conversion however, both the RF signal and it’s image contains useful information. So, then the double sideband (DSB) noise figure is of interest. The DSB noise figure is usually 3 dB lower than the SSB noise figure if the conversion
gain is equal in the two sidebands. In figure 25, the SSB noise figure is 30 dB at 312.5 kHz, which is the distance from DC to the first subcarrier frequency in the W-LAN standard.

In 802.11a W-LAN, each channel is 20 MHz wide and consists of 64 subcarriers. However, there are 48 subcarriers used for data and 4 is pilots, the remaining 12 subcarriers are set to zero. One zero is set to DC and the remaining 11 zeros are set around the edges of the band. So, the distance from DC to the first data subcarrier is \(20M/64 = 312.5kHz\). [2]
Figure 25: Simulated mixer SSB noise figure.

In figure 25, one can see that it is the 1/f noise that dominates as the frequency moves towards zero. The noise figure is very high, the DSB noise figure is approximately 27 dB. The 1/f noise rapidly drops down as the frequency increases. The average noise effect on the whole signal channel can be calculated by integrating the noise figure over the desired frequency range. This yield in an average DSB noise figure of 19 dB. There is however some questions regarding the noise modeling in the TSMC transistor models. So, the mixer should be implemented and measured before any final conclusions can be drawn.

The linearity of the mixer in terms of the 1-dB compression point is -13.4 dBm and shown in figure 26.

The IIP3 and IIP2 curves are shown in figure 27. To be able to see the second intermodulation products, the mixer was modified so it was not completely symmetric. This was made by changing the width of one of the RF-input transistors. The IIP3 point occurs at -6.6 dBm and the IIP2 point is outside the plot, but occurs at 8 dBm.

As mentioned before, the noise figure of the mixer is quite high. One way to lower the noise figure is to inject a current, Inj in figure 28, to the symmetrical point of the RF transistor pairs. Since the 1/f noise in the RF transistors contribute with 95% of the total noise in the mixer, lowering of the current through these transistors will help reduce the 1/f noise.

The injected current itself will not introduce noise in this balanced structure. Unlike the normal Gilbert-type mixer, the four RF transistors change their currents simultaneously and any noise at their common source node will be completely cancelled out at the differential output [9]. The amount of noise reduction is determined by the injected current. In figure 29, the noise figure is plotted with
Figure 26: Simulated mixer 1-dB compression point.

Figure 27: Simulated mixer IIP2 and IIP3 curves.

a swept injected current from 0 to 2 mA.

The noise reduction is approximately 7 dB at 312 kHz with a injected current of 2 mA. This is however not so good since then the injected current drives the RF transistors into the weak inversion region. So, in order not to lose gain and too much linearity, the injected current is set to 1.5 mA. Then the SSB noise figure is 24.8 dB and the DSB noise figure approximately 3 dB lower, a reduction with 5.3 dB compared with no current injection at all.

As one could expect, the linearity is somewhat degraded due to the fact that the injected current drives the RF transistors towards the weak inversion region.
Figure 28: Mixer with injected current Iinj.

Figure 29: Mixer noise figure with swept injected current.

So, there is a trade off between noise reduction and linearity degradation. Another effect is that the conversion gain and bandwidth increases somewhat up to a certain level of the injected current before the current drives the transistors too far into the weak inversion region.

6.2.3 Mixer Performance Summary

As with the LNA, simulations has been carried out both with non RF models and RF-models. The result is shown in table 2, the last column presents the results with an injected current of 1.5 mA. The parameter "average DSB noise figure", presents the average noise figure of the whole channel signal frequency band.
<table>
<thead>
<tr>
<th>Parameter</th>
<th>&quot;Ideal&quot;-Models</th>
<th>RF-Models</th>
<th>RF-Models, 1.5mA Tiny</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply</td>
<td>1.8 V</td>
<td>1.8 V</td>
<td>1.8 V</td>
</tr>
<tr>
<td>Conversion gain (lower band)</td>
<td>6.5 dB</td>
<td>5 dB</td>
<td>7.3 dB</td>
</tr>
<tr>
<td>Conversion gain (upper band)</td>
<td>5 dB</td>
<td>3 dB</td>
<td>4.1 dB</td>
</tr>
<tr>
<td>DSB Noise figure @ 312 kHz</td>
<td>23 dB</td>
<td>27 dB</td>
<td>21.8 dB</td>
</tr>
<tr>
<td>Average DSB noise figure</td>
<td>15.4</td>
<td>19 dB</td>
<td>14.2 dB</td>
</tr>
<tr>
<td>1-dB Compression point</td>
<td>-17 dBm</td>
<td>-13.4 dBm</td>
<td>-17.3 dBm</td>
</tr>
<tr>
<td>IIP3</td>
<td>-8.3 dBm</td>
<td>-6.6 dBm</td>
<td>-9.1 dBm</td>
</tr>
<tr>
<td>IIP2</td>
<td>12 dBm</td>
<td>8 dBm</td>
<td>30 dBm</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>8 mW</td>
<td>10.1 mW</td>
<td>10.8 mW</td>
</tr>
</tbody>
</table>

Table 2: Mixer performance parameters.

6.3 Front End Performance

The complete front-end with the LNA and mixer connected has also been simulated. The mixer used was the one with the injected current of 1.5 mA. The result is shown in table 3.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply</td>
<td>1.8 V</td>
</tr>
<tr>
<td>Voltage gain (lower band)</td>
<td>20 dB</td>
</tr>
<tr>
<td>Voltage gain (upper band)</td>
<td>18 dB</td>
</tr>
<tr>
<td>DSB Noise figure @ 312 kHz</td>
<td>12.2 dB</td>
</tr>
<tr>
<td>Average DSB noise figure</td>
<td>8 dB</td>
</tr>
<tr>
<td>1-dB Compression point</td>
<td>-24.3 dBm</td>
</tr>
<tr>
<td>IIP3</td>
<td>-12.1 dBm</td>
</tr>
<tr>
<td>IIP2</td>
<td>31 dBm</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>38 mW</td>
</tr>
</tbody>
</table>

Table 3: The complete front-end performance parameters.

The front-end gain differs somewhat from the expected, the gain is slightly higher than the sum of the gain when the LNA and the mixer is simulated separately. This is the consequence of better matching between the LNA and mixer.

The total noise of the front-end can be calculated from Friis equation, [5]:

\[ F = F_1 + \frac{F_2 - 1}{G_1} + \cdots + \frac{F_m - 1}{G_1 \cdots G_{m-1}} \quad (15) \]

Where F is the noise factor and G is the power gain. Friis equation gives the total noise figure of the front-end to approximately 9 dB and the simulations yields a noise figure of 8 dB. This is also a consequence of the matching between...
the LNA and mixer. When the mixer was simulated as stand alone, the source impedance was estimated to a real resistance. But the output impedance of the LNA is complex, so a small imaginary part of the impedance has changed the matching slightly.

6.4 Layout

A layout has been made of the LNA. One would want to achieve a good matching between the differential pair, this is however not so easy in this design due to the six inductors, which dominates the layout. So, in order to keep the wire lines short, the layout of one side of the LNA were completed first and then mirrored to complete the layout and achieve symmetry. Some means were taken to match the RF and cascode transistors. The transistors were split into four parallel segments each and then symmetrically coupled together, figure 30. This is also known as common centroid layout.

![Diagram](image)

Figure 30: Layout of one RF and cascode transistor.

The corresponding schematic view of the RF and cascode transistor is shown in figure 31.

As mentioned before, one side of the LNA were completed first and then mirrored to the other side, this makes the LNA totally symmetric. However, the differential transistor pair is not matched together. This is mainly because of the sizes of the inductors. In figure 32, the complete LNA layout is presented. One can see that there is a lot of free space in the middle of the layout. The chip area inside the rectangle is approximately 1.9 $mm^2$. 

31
6.4.1 LNA Simulations With Extracted Parasitics

The resistive and capacitive parasitics has been extracted from the layout and simulations on the extracted view shows small changes. The S-parameters has changed slightly due to differences in the impedance matching, figure 33.

The voltage gain is more or less unchanged, 12.8 dB which is just slightly higher than before due to better matching. The noise figure is also lowered to 3.2 dB, this also stems from the fact that the impedance matching has changed and that the optimum noise reflection coefficient (Gmin) has moved closer to S11 and S22, figure 34.
Figure 33: LNA S-parameters with extracted parasitics.

Figure 34: S11, S22 and Gmin, (a) with parasitics, (b) without parasitics.

In figure 34, the leftmost curve in (a) and (b) is S22, the next curve is S11 and the short curve to the right is Gmin.

Also, the linearity is somewhat deteriorated. The 1-dB compression point now occurs at -3.7 dBm and the IIP3 at 7.8 dBm. The IIP2 could not be simulated since the LNA is almost perfectly symmetric and the differential symmetry
suppresses the even order harmonics.

The performance of the LNA with extracted parasitics is presented in table 4.

<table>
<thead>
<tr>
<th></th>
<th>W/O Parasitics</th>
<th>With Parasitics</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage gain</td>
<td>12 dB</td>
<td>12.8 dB</td>
</tr>
<tr>
<td>S11</td>
<td>&lt; -15 dB</td>
<td>&lt; -12 dB</td>
</tr>
<tr>
<td>S21</td>
<td>&gt; 6.35 dB</td>
<td>&gt; 6.7 dB</td>
</tr>
<tr>
<td>Noise figure</td>
<td>3.6 dB</td>
<td>3.2 dB</td>
</tr>
<tr>
<td>1-dB Compression point</td>
<td>-1.6 dBm</td>
<td>-3.7 dBm</td>
</tr>
<tr>
<td>IIP3</td>
<td>10 dBm</td>
<td>7.8 dBm</td>
</tr>
<tr>
<td>IIP2</td>
<td>51 dBm</td>
<td>-</td>
</tr>
</tbody>
</table>

Table 4: Summary of the LNA performance with extracted parasitics.
7 Results

A differential source degenerated LNA, and a differential double balanced harmonic mixer has been presented. The simulated performance without the extracted parasitics in the LNA is summarized in table 5.

<table>
<thead>
<tr>
<th></th>
<th>LNA</th>
<th>Mixer</th>
<th>Front-end</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply</td>
<td>1.8 V</td>
<td>1.8 V</td>
<td>1.8 V</td>
</tr>
<tr>
<td>Voltage gain</td>
<td>12 dB</td>
<td>4.1 dB</td>
<td>18 dB</td>
</tr>
<tr>
<td>Noise figure</td>
<td>3.6 dB</td>
<td>14.2 dB</td>
<td>8 dB</td>
</tr>
<tr>
<td>1-dB Compression point</td>
<td>-1.6 dBm</td>
<td>-17.3 dBm</td>
<td>-24.3 dBm</td>
</tr>
<tr>
<td>IIP3</td>
<td>10 dBm</td>
<td>-9.1 dBm</td>
<td>-12.1 dBm</td>
</tr>
<tr>
<td>IIP2</td>
<td>51 dBm</td>
<td>30 dBm</td>
<td>31 dBm</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>27 mW</td>
<td>10.8 mW</td>
<td>38 mW</td>
</tr>
</tbody>
</table>

Table 5: Front-end summary.

7.1 Discussion

The voltage gain presented in table 5, refers to the upper frequency band and is a few dB lower than the gain of the lower band. It is however too low, especially in the LNA which suffers from large source degenerating inductors which lowers the gain. The calculated values for these inductors with a 50Ω input impedance was as low as 50 pH. This is a unrealizable low value but a quick simulation with Asitic shows that the wire alone from the source will present a parasitic inductance just under 200 pH. So, if accurate modeling could be done with for example Asitic, the source degenerating inductors could be removed and instead realized with only the wires. This would boost up the gain and lower the noise of the front-end.

The low gain in the LNA causes the noise figure of the complete front end to be quite high since the LNA gain is critical for suppressing the noise of the mixer. The noise of the mixer is problematic since it is dominated by 1/f noise which is a well known problem in CMOS direct conversion implementations. Some improvement has been achieved with the introduction of the injected current described on page 27 in section 6.2.2. There is however some questions regarding the noise modeling in the TSMC transistor models. So, the mixer should be implemented and measured before any final conclusions can be drawn.

The linearity could be a problem for W-LAN applications if the gain in the LNA is increased. Then the mixer linearity probably must be improved in order to meet the specifications of the 802.11a Std.

The DC-offset is not relevant to simulate since it arises from transistor mismatch in the signal path. One can however, draw the conclusion that this front-
end will be self mixing free since the LO frequency not equals the RF frequency. This is desirable since the static DC-offset caused by device mismatch is not as problematic as the self mixing induced offset which can change with operating conditions and incoming signals.

The I/Q mismatch of the front-end will also be determined by the transistor matching, but also by the accuracy of the VCO. The VCO will need to produce four accurate phases, 0°, 45°, 90° and 135° to the mixers which might be somewhat difficult. One solution could be to implement a 4-stage ring oscillator. [9]

The simulations of the LNA and mixer has been performed with simple bias circuits described on page 22 in section 6.1.4 and constant supply and temperature. These are factors that certainly can degrade the performance of the design.

8 Conclusions

The purpose of this Master’s thesis was to design a direct conversion receiver front-end for the IEEE 802.11a Std. Different LNA and mixer topologies has been studied and one solution designed and simulated. At this stage, the proposed front-end does not show good enough performance. However, with the suggested improvements of the LNA, this front-end could mitigate the inherent DCR problems and prove to be a good solution in many applications.

9 Recommendations

Recommendations for future work on this design would be to improve the bias circuitry with respect to power supply and temperature variations. Also to investigate the possibilities to implement the source inductors in the LNA with the parasitic inductance in the wires instead. This would increase gain and reduce the chip area consumed. Further improvements of the noise and linearity in the mixer should also be investigated, a suggestion would be to find a optimum injected current with respect to noise and linearity. Also to implement the current injection in the mixer with for example P-type transistors instead of the ideal current sources used here..
Acknowledgments

I wish to thank Lars-Olof Eriksson and Joacim Olsson, my supervisors at Acreo, for technical discussions and support to this thesis. At Acreo, I would also like to thank Andreas Dreyfert, David Åström, Henrik Johansson and Ulf Lindgren for putting up with my various questions and invaluable help with Unix/LaTeX.
References


Appendix A

A Schematics

A.1 LNA

Figure 35: LNA schematic.
A.2 Mixer

Figure 36: Mixer schematic.