Integrating InP MMICs and Silicon Micromachined Waveguides for sub-THz Systems

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***Abstract*—A novel co-designed transition from InP monolithic microwave integrated circuits to silicon micromachined waveguides is presented. The transition couples a microstrip line to a substrate waveguide sitting on top of a vertical waveguide. The silicon part of the transition consists of a top and a bottom chip, fabricated in a very low-loss silicon micromachined waveguide technology using silicon on insulator wafers. The transition has been designed, fabricated and characterized for 220–330 GHz in a back-to-back configuration. Measured insertion loss is 3–6 dB at 250–300 GHz, and return loss is in excess of 5 dB.**

***Index Terms*—InP, MMIC, silicon micromachining, submillimeter wave, terahertz, transition, waveguide**

I. Introduction

In recent years the terahertz (THz) frequency range has gained an increased interest for use in applications such as high-speed wireless data links, vehicular and aircraft safety systems, high-resolution security imaging, medical sensors and space communication [1], [2].

Although complete single-chip receiver and transmitter front-end monolithic microwave integrated circuits (MMICs) with integrated on-chip antennas have been presented [3], waveguides are the transmission medium of choice for sub-THz and THz systems due to their low-loss characteristics [4]. Waveguides at terahertz frequencies are typically manufactured by computer numerical control (CNC) milling utilizing a split block design. The serial nature of the CNC milling process result in high manufacturing costs and prevents scaling to high volumes, which limits the wide-spread exploitation of THz technology [5] making them suitable only for low volume high-end scientific instrumentation. Moreover, the fabrication of components at THz frequencies becomes challenging and, in some cases, extremely complicated with CNC milling due to small waveguide dimensions and the requirement of complex geometries [6]. Silicon micromachining is currently the most appealing alternative to make THz waveguides and waveguide components with unparalleled performance due to their micrometer-scale manufacturing uniformity, precision and nanometer surface roughness [7]. The authors have developed a silicon micromachined waveguide platform and within this technology, components with outstanding performance have already been reported [6], [8]–[10].

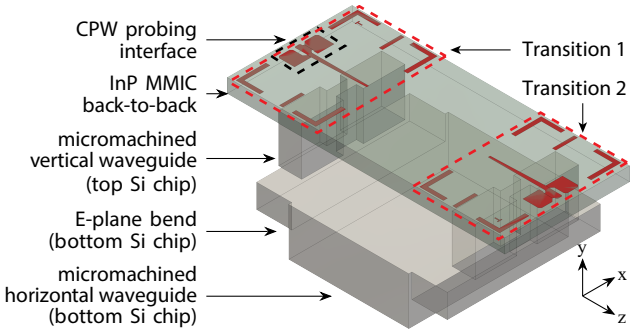

Fig. 1. Three-dimensional model of the proposed transition. Two transitions are implemented in a back-to back configuration for characterization purpose. The InP MMIC with two microstrip to vertical waveguide transitions is placed on top of a two-silicon-chip stack. The InP MMIC has CPW interfaces for probing. In the top silicon chip the vertical micromachined waveguide is realized. The bottom silicon chip consists of the E-plane bend and the horizontal micromachined waveguide.

Low-loss MMIC to silicon micromachined waveguide transitions are crucial for the industrial exploitation of the THz domain [11]. Numerous transitions from MMIC microstrip line (MSL) to waveguide have been presented of which the E-plane probe transition is the most well-known and used [12]–[15]. Such a probe transition is implemented on an MMIC substrate and the chip is partially placed inside the waveguide. Alternatively, to avoid design constraints on the MMIC and to lower assembly and integration complexity, the entire MMIC must be placed outside the waveguide. One such alternative approach is based on slot coupling in the ground plane of MSL followed by placing a dielectric quarter wave transformer of high dielectric constant [16]–[18]. Such solutions either require the waveguide part being manufactured using Rogers substrate [18] or using low temperature co-fired ceramic (LTCC) [16], [17] located under the MMIC. Hence, the performance is reported only for low millimeter wave frequencies. For THz and sub-THz systems, the transition has to be co-designed depending on the specific layer stack-up and design rules for the chosen MMIC and silicon processes.

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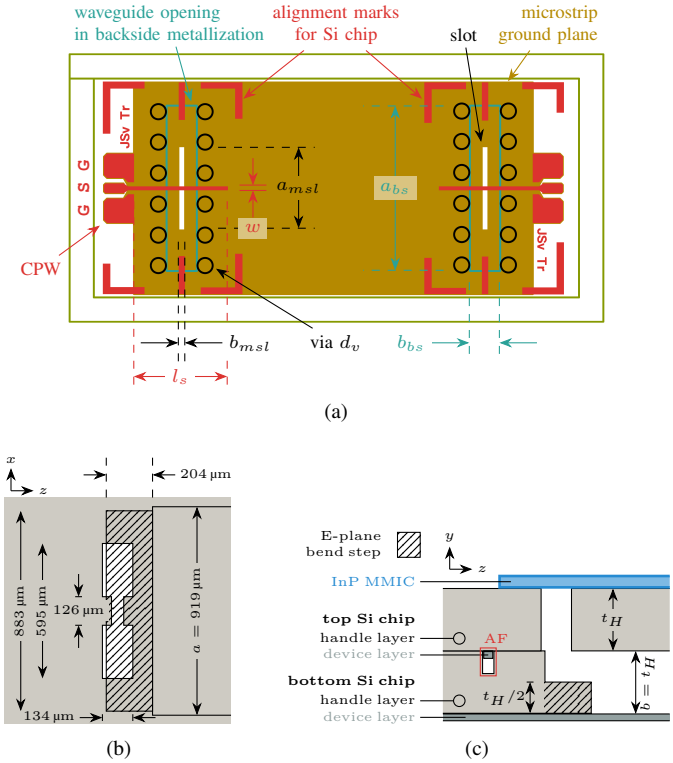


Fig. 2. (a) Top view of the InP back-to-back transition MMIC, with $l_s = 330\,\mu\text{m}$, $w = 12\,\mu\text{m}$, $a_{msl} = 277\,\mu\text{m}$, $b_{msl} = 22\,\mu\text{m}$, $a_{bs} = 544\,\mu\text{m}$, $b_{bs} = 100\,\mu\text{m}$ and $d_v = 50\,\mu\text{m}$. (b) Top and (c) side view of the silicon micromachined part of the transition. Top and bottom Si chips are joined by thermocompression bonding. Alignment features (AF) in the device and handle layer of the top and bottom Si chip, respectively. SOI handle layer thickness $t_H = 275\,\mu\text{m}$.

The authors have previously shown in their silicon micromachined waveguide platform, the integration of silicon micromachined E- and H-plane rectangular waveguide components [19] and an axial waveguide integration platform enabling direct integration of micromachined chips with in-plane silicon micromachined waveguide components [20]. However, a direct transition from MMIC MSL to the silicon micromachined waveguide platform have not been shown. In this paper we present a low-loss transition design intended for the Teledyne TSC250 InP DHBT process [21] and the double H-split silicon micromachined waveguide process presented in [7]. We report on design details and simulation results and discuss measurement data for a back-to-back transition test circuit obtained from a first manufacturing run.

II. Design

The transition couples a MSL on top of an InP MMIC to a horizontal (in-plane) micromachined hollow waveguide located below the MMIC. A three-dimensional representation of two such transitions implemented for characterization purpose in a back-to-back configuration are shown in Fig. 1. The layout of the InP MMIC with the proposed transitions in a back-to-back configuration is shown in Fig. 2a. For practical implementation, the active circuit will be placed in between the GSG probe pads and the MSL transition. The transition uses a single MSL of width $w = 12\,\mu\text{m}$ and open stub length $l_s = 330\,\mu\text{m}$ coupling energy through a slot in the MSL ground plane with dimensions $(a_{msl} = 277\,\mu\text{m}) \times (b_{msl} = 22\,\mu\text{m})$. The ground plane also acts as a backshort for a vertical dielectric waveguide that is designed inside the MMIC substrate acting as a quarter-wave transformer to achieve impedance matching between the high impedance of the hollow waveguide and the much lower impedance of the MSL slot feed [18]. The dielectric waveguide is formed by substrate vias with diameter $d_v = 50\,\mu\text{m}$. An opening in the backside metallization of the MMIC with dimensions $(a_{bs} = 544\,\mu\text{m}) \times (b_{bs} = 100\,\mu\text{m})$ couples the dielectric waveguide to a vertical hollow micromachined waveguide section. Due to size limitations of the MMIC and the reduced width of the opening in the backside metallization, the vertical waveguide is implemented as a ridge waveguide in the top silicon chip. A single-stepped E-plane bend is implemented in a bottom silicon chip, interfacing to the horizontal, in-plane waveguide. Dimensions for the silicon chips are given in Fig. 2b and (c). The transition is compatible with industrial assembly equipment and can be integrated with a range of passive waveguide components in the silicon micromachined waveguide technology.

III. Fabrication

The silicon micromachined waveguide part of the transition consists of a top and a bottom chip fabricated in the double H-plane split waveguide technology using silicon on insulator (SOI) wafers presented in [7] (Fig. 3).

Alignment of the chips is facilitated by complementing alignment features etched in the device layer of the top chip and the handle layer of the bottom chip, respectively (see Fig. 2c and 3e). Such features would make the alignment and subsequent bonding of the silicon micromachined chips easier and increase the yield of assembled chips. Both the vertical waveguide in the top chip and the horizontal in-plane waveguide in the bottom chip are etched in the handle layer of the SOI wafer using deep reactive-ion etching (DRIE). In the case of the bottom chip a two-mask etch is used in order to etch down the step of the E-plane bend to half of the handle layer thickness. Corresponding Vernier scales in the top and bottom chip facilitate good alignment before thermocompression bonding at 200 °C.

The MMIC was fabricated in the Teledyne InP HBT 250 nm process [21]. The design rules for the waveguide opening in the backside metallization were incorrect when the transition was designed. Due to this process limitation, the waveguide opening between the vias in the backside metallization of the MMIC were fabricated in a post-processing step where the metallization at the waveguide openings was removed by laser ablation (image of the backside of the MMIC seen in Fig. 4a). The design rules were later investigated by Teledyne and more correct design rules were derived for future fabrication.

IV. RF Characterization

The measurement setup consists of a Rohde & Schwarz ZVA 24 Vector Network Analyzer with two Rohde & Schwarz ZC330 TxRx extension heads and GGB

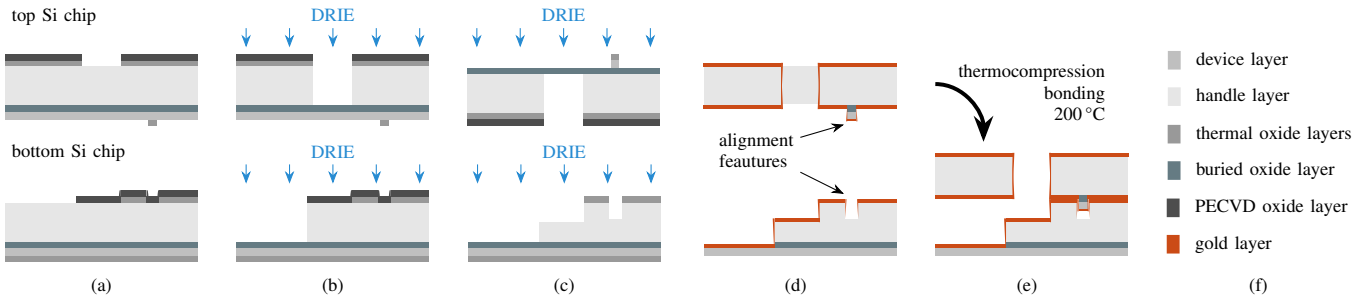
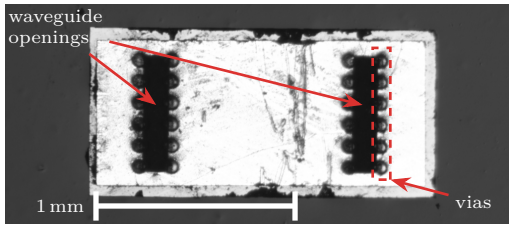
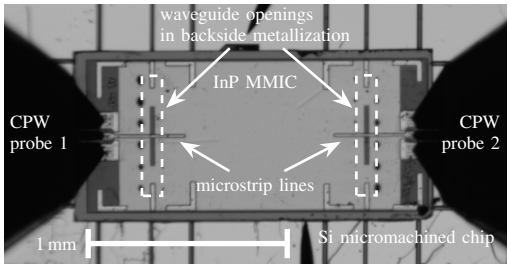


Fig. 3. Silicon top and bottom chips fabrication process: SOI wafer dimensions are device layer thickness $t_D = 30\,\mu\text{m}$, handle layer thickness $t_H = 275\,\mu\text{m}$ and buried oxide layer thickness $t_B = 3\,\mu\text{m}$.(a) Masks in the oxide layers on top of device and handle layers; (b) DRIE of handle layers for waveguide cavities; (c) DRIE of top chip device layer and DRIE to reduce height of step in E-plane bend after removal of top oxide mask; (d) removal of exposed oxide layers, sputtering of 2 µm of gold; (e) thermocompression bonding of top on bottom chip at 200 °C; (f) legend for the figure.



(a)



(b)

Fig. 4. Microscopic pictures of the back-to-back transition InP MMIC: (a) backside, visible are the waveguide openings in the backside metallization created by laser ablation and (b) topside, with both CPW interfaces probed by GGB Model 325B CPW probes.

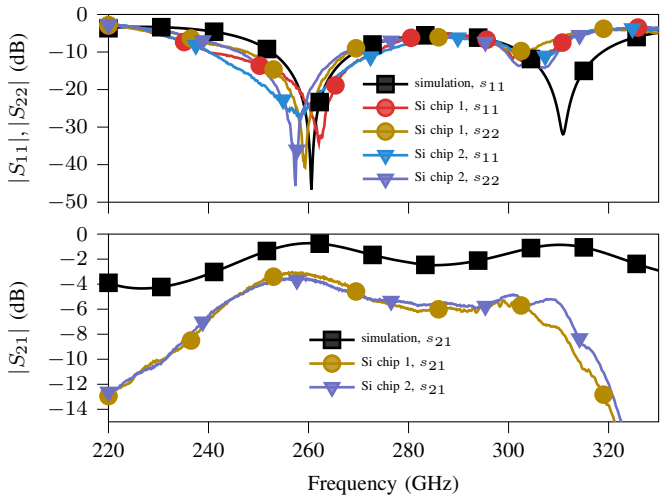


Fig. 5. Reflection and transmission coefficient of the measured back-to-back transition compared to simulation results. The MMIC chip was placed on three different silicon micromachined waveguides chips (Si chip 1–3).

Model 325B ground-signal-ground (GSG) microwave probes for the frequency band of 220–330 GHz. A microscopic image of two CPW probes in contact with the CPW interfaces of the back-to-back transition is shown in Fig. 4b.

Fig. 5 shows the measurement and simulation results. The InP MMIC chip with back-to-back MSL to silicon micromachined waveguide transition has been placed on two different silicon micromachined waveguide chips (Si chip 1–2) for characterization. An insertion loss (IL) of 3–6 dB in the frequency range of 250–300 GHz was observed for the entire stack of two MSL to silicon micromachiend waveguide transitions and a 1.5 mm silicon micromachined waveguide. This is 2–3.5 dB higher than the simulation results for the stack. The higher IL is attributed to the laser post-processing to remove the backside metallization for the waveguide openings. The laser ablation procedure resulted in position, alignment and dimensional inaccuracies causing dimensional variation along all axes in the waveguide opening compared to the design dimensions. Moreover, the re-deposition of the ablated material on the edges of the ablated region resulted in a gap between the INP MMIC and the silicon micromachined waveguide chips during measurements. This resulted is higher IL which was confirmed by CST simulations. The return loss was better than 5 dB in the frequency band of interest. There is a minimal shift in the frequency between simulation and measurements due to the dimensional inaccuracies of the ablated metal and the ablation of the InP layer underneath the metal layer. The 1.5 mm silicon micromachined horizontal waveguide connecting the two transitions has an IL of 0.09 dB [7]. This results in the calculated IL for each transition being 1.05–2.55 dB.

V. Conclusion

A novel transition to integrate MMICs with silicon micromachined waveguide components for sub-terahertz systems was presented. The transition was co-designed at 220–330 GHz for an InP MMIC and a silicon micromachined waveguide technology using SOI wafers. Fabricated and characterized in a back-to-back configuration, insertion loss is 3–6 dB. Despite the higher than simulated insertion loss attributed to the post-processing step to remove backside metallization, the transition promises highly compact and integrated terahertz and sub-terahertz systems.

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