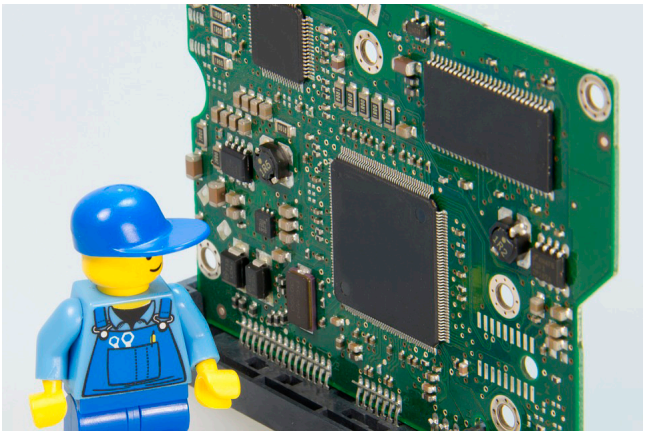
LICENTIATE THESIS

An SBU fully additive production approach for Board-level Electronics Packaging (SBU-CBM Method)



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To Mama-Papa & Appy

Abstract

The worldwide electronics market is focusing on developing innovative technologies that can lead to denser, more resilient, and tighter board-level integration. The consumer electronics market is trending toward miniaturization, with HDI-PCBs dominating. Electronics shrinking and scaling technology is the prime concern of all manufacturers. The PCBA industry is transforming its production practices which can reduce the solder joints, limit the usage of discrete and bulky components, reduce the packaging factor of printed boards by accommodating the maximum number of ICs, minimize the assembly span, optimize the latency, and so on. However, developments in production processes in the PCB manufacturing industry need more attention than those in Silicon-based (ICs) fabrications. One of the issues in PCB fabrication is utilizing conventional metallization approaches. The majority of manufacturers continue to use standard Copper(Cu) laminates on the base substrate and lithography methods to shape the structures.In recent manufacturing technologies, semi-Additive process (SAP) or modified-SAP (mSAP) methods are being adopted to replace traditional subtractive print-and-etch procedures. To scale down the Lines and Spaces (L&S) on PCBs comparable to that of IC-level, most smartphone makers use Substrate-like PCB (SLP) using mSAP methods. However, subtractive patterning has been used in the intermediate stages of fabrication in those methods. This thesis demonstrates a fully additive selective metallization-based production approach to bridge this technology gap between IC-level and board-level fabrications. The fabrication process has given the name 'Sequential Build-Up Covalent Bonded Metallisation' (SBU-CBM) method.

This dissertation presents a new approach to Cu metallization using a significant step reducing-pattern-transfer process. The patterning method activates a seed layer of CBM polymer chains on a polymer surface with optimal UV-Laser settings. This surface modification enables a strong Copper (Cu) bonding onto the modified surface by Cu-plating. The suggested approach generated a 2.5D surface pattern using a micrometer via laser ablation and subsequent sub-micrometer laser lithography. Furthermore, the surface characterization of each step involved in the fabrication process is analysed and presented to show the sequential growth of layers on top of each other. To investigate the mechanism of the process at the interfaces, characterizations such as EDS, SEM, and XRD characterizations were performed. This PCB manufacturing method can selectively add metallic layers to the finest feature sizes at considerably lower temperatures. Overall, the thesis has addressed two critical aspects i.e. miniaturization of interconnects at board-level and the feasibility of a fully-additive production approach for electronics packaging.

First, a subtractive method is shown to achieve Copper interconnects with feature

size 3.0μm. This miniaturization corresponds to 70% reduction in the feature size from 20 μm to 3 μm. Next, the proposed additive production process has produced Cu interconnects with feature sizes of 2.5 μm L&S and via of diameter 10 μm. The scaling of the interconnects was achieved by optimizing the process parameters involved in the proposed fabrication recipe.

Second, the sequential build-up (SBU) procedure is adopted to realize the embedded passives with the minimum possible feature size (< 10 μm). An embedded capacitor and a planar inductor were fabricated. The proposed method can be employed to achieve any desirable pattern on FR-4, and a few of them are shown in the thesis. This additive technique can further be investigated through electrical and reliability assessment to make it an industrially accepted method.

Contents

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List of Abbreviations

PCB Printed Circuit Board

SBU Sequential Build-Up

CAD Computer Aided Design

CBM Covalent Bonded Metallisation

CCL Copper Clad Laminates

SOP System on Package

HDIs High Density Interconnects

RoHS Restriction of Hazardous Substances Directive

IC Integrated Circuit

PU Poly-Urethane

UV Ultra-Violet

SEM Scanning Electron Microscopy

EDS Energy Dispersive Spectroscopy

XRD X-ray Diffraction

HAST Highly Accelerated Stress Test

DFT Density Function Theory

ITRS International Technology Roadmap for Semiconductors

IPC Institute for Printed Circuits

NEMA National Electrical Manufacturers Association

FR Flame Retardant

Cu Copper

ETS Embedded Trace Substrate

ATP Advanced Tenting Processing

PE Printed Electronics

LDW Laser Direct Write

Part I

Chapter 1

Introduction

"There is plenty of room at the bottom."

Richard P. Feynman

The electrical product is analogous to the human body. Electronic items have "brains" or microprocessors, and their packaging contains "nervous" and "skeletal" systems. As a result, an electronic system is worthless unless it is packaged. It requires its packaging to be networked, powered or "fed", cooled by its "circulatory" system and protected by its "skeletal" system. This is precisely what packaging is all about.

1.1 Introduction to Electronics System Packaging

Electronics system packaging is defined as 'every technology required between a single wafer preparation to the whole system deployment'. It is the process of assembling a group of electronics components into a properly assembled device that can perform reliably over a period of time. Fabrication techniques are one of the most crucial interlinking steps between a known good die and a complete system realization in this cross-disciplinary field [35]. The electronics packaging hierarchy has broadly categorised into five levels as follows in [2]:

Level 0: Interconnection on a monolithic silicon die.
Level 1: Several silicon dies into a single chip module.
Level 2: Multi-chip module.
Level 3: Interconnection of discrete components on board.
Level 4: Complete electronic system.

However, as indicated in figure 1.1, the aforementioned categorization may be divided into three major categories: chip-level, board-level, and system-level. Levels 0, 1, and 2 are implemented on the silicon substrate and hence combine to form the chip-level. Level 3 is board-level, which might be a single board or a collection of printed circuit boards (PCBs) integrated into a motherboard. The last one is the system-level, which represents the complete system [35].

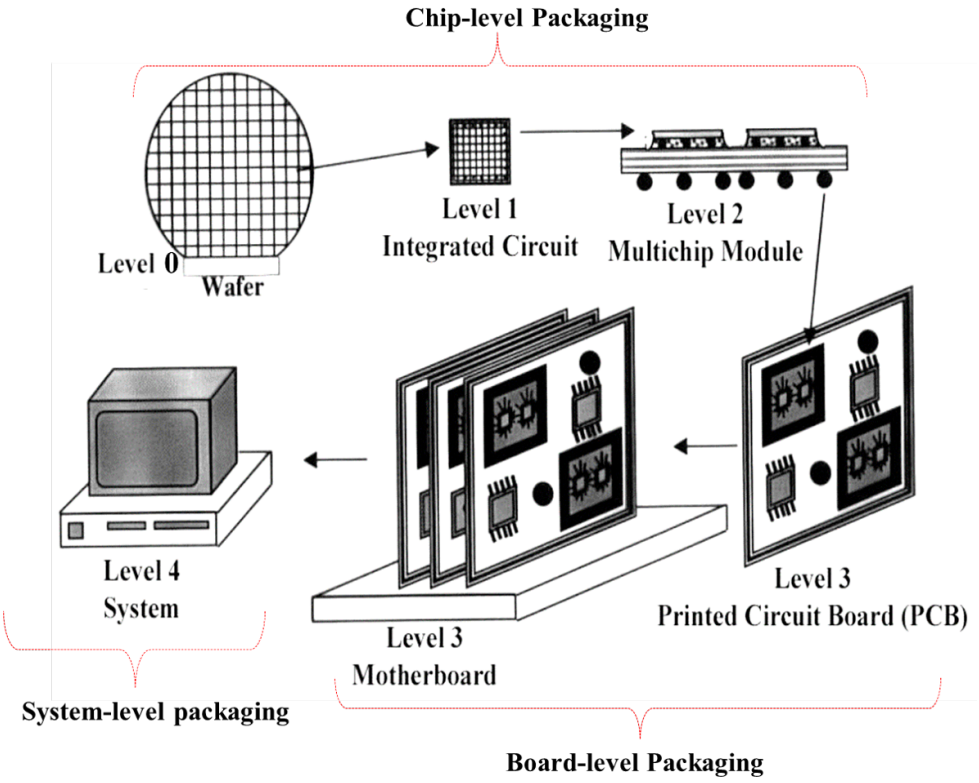


Figure 1.1: An overview of different levels in Electronics Packaging.

1.2 Gap Analysis in Fabrication methods

The fourth industrial revolution (industry 4.0) has also accelerated the scaling and miniaturization processes in electronics manufacturing. The demand for lighter, smarter, and more compact hardware has prompted device manufacturers such as TSMC, IBM, AMD, Globalfoundries, and others to move to a 2nm process node at the chip-level [29]. The focus of high-speed electronics is more on communication and computing capabilities, and not just switching and control functions. However, chip-level implementations still have challenges like nano-scale patterning using extreme ultraviolet (EUV) lithography processes, integration of poly-gate, reliability testing strategies for miniaturised devices, thermal noise cancellation, realization of inductors on a single chip, and so on. Similarly, some of the extant system-level gaps include system-on-Package (SOP) implementations, electrical and reliability testing of SOP modules, multi-layer architecture for mixed-signal applications, etc [36].

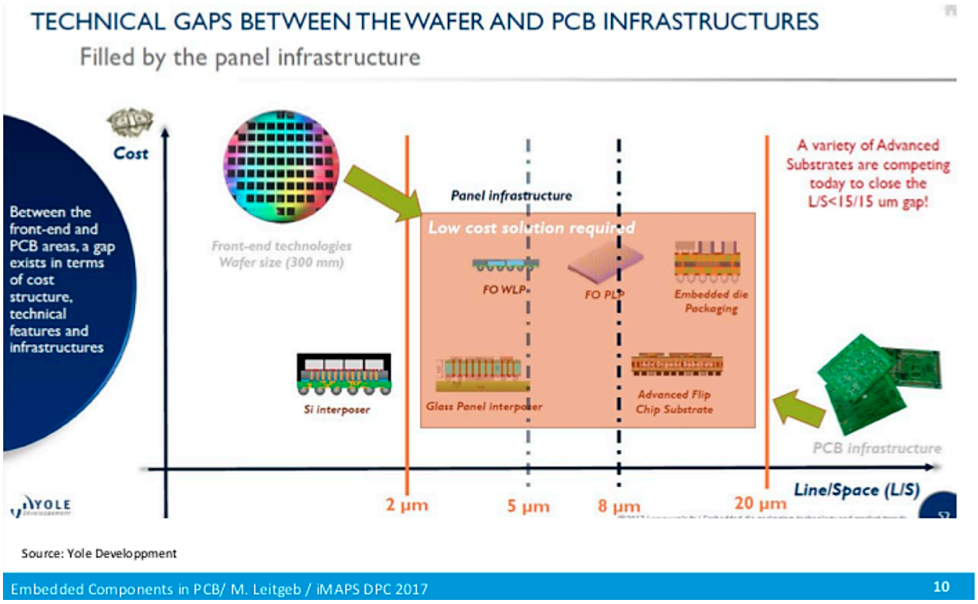


Figure 1.2: Miniaturisation gaps between chip-level and board-level fabrication due to the lack of PCB infrastructures as shown in Leitgeb et al [16]

PCBs are one of the essential components of electrical appliances at the board level. It connects several integrated circuits (ICs), discrete components, and other devices to form a functional system, similar to how the human body's backbone works. Although the fabrication techniques used in chip-level and board-level manufacturing processes are almost identical. However, the geometric scaling of board-level compared to silicon-based fabrications is still at an infancy stage. Therefore, while building up a product, the aggressive scaling in IC level is getting sacrificed because of the lower scaling factors at the board-level. Thus, resulting in large packaging volume, higher form factor, and heavier product than those of the original ICs [10]. As shown in figure 1.2, the existing infrastructure and technical features related to PCB production are lagging in terms of scalability.

Based on the latest roadmaps on the board-level production requirements, shown in figure 1.3, the expected line width of copper (Cu) interconnects, and micro vias are roughly around 20μm and 40μm respectively, which is significantly behind the 2nm feature sizes at the wafer level. The majority of production methods are subtractive etch-print, semi-additive productions (SAPs), and advanced modified SAPs (amSAPs) as shown in figure 1.3(a). The expected feature sizes are shown in figure 1.3(b). The term '6+N+6' represents the multi-layer structure of the board, where 'N' is the core layer and 12 (6+6) sequential layers can be build up on either sides of the core. The estimated numbers in the roadmap is another indication of gaps in the production approaches at

the board-level.

(a)

	2015	2016	2017	2018	2019	2020
µVia Diameter (µm)	70		50		40	
µVia Diameter Aspect Ratio	0.8			0.9	1.0	
µVia Pad Diameter (µm)	200	140	140	130	120	100
Min L/S (µm)	35/35		25/25		20/20	
Cu Thickness (µm)	15	12	10			8
BGA Pitch (µm)	350	300		250	200	
Technology	Subtractive		m-SAP		am-SAP	

(b)

Category	Item	Current Capability	By 2022 H1	By 2022 H2	By 2023 H1
Structure	Stagger Via	6+N+6	6+N+6	7+N+7	7+N+7
	Stacked Via	6+N+6	6+N+6	7+N+7	7+N+7
	All Stacked Via	12 Layers	12 Layers	14 Layers	14 Layers
Routing Density	Line Width/Space	40/40 µm	35/35 µm	35/35 µm	30/30 µm
	Laser Via/Pad	70/150 µm	70/150 µm	60/115 µm	60/100 µm
	Router Tolerance	+/- 50µm	+/- 50µm	+/- 50µm	+/- 50µm
Material		High Tg, Low CTE, Low Dk/Df, Halogen Free			

Figure 1.3: (a) Roadmap of the board-level Fabrication approaches released by Atotech Gmbh [3].(b) The future roadmap estimation by one of the leading manufacturers of PCBs, NAN YA PCB Corporation [25].

Summing up the gap analysis on the fabrication methods, it can be inferred that the PCBs, which hold the miniaturised ICs continue to struggle to find a production process in terms of flexibility and scalability. As the intermediary platform for connecting ICs into a system, the board-level requires efficient infrastructure and manufacturing techniques. Therefore, one of the motivations of this research is to investigate a production method that can minimize feature sizes at the board level. Another motivation for this study is to examine a fully additive production recipe that can meet the requirements of the present roadmap while reducing the number of fabrication steps and being environmentally benign.

1.3 Research Questions and Applied Methodologies

This study has focused on board-level fabrication gaps. Firstly, how the feature size of the Cu interconnects can be scaled through existing production approaches? Secondly, is a fully additive production approach feasible at the board level? To achieve the first objective, a laser-assisted subtractive technique and a fully additive approach have been tested to scale the on-board Cu interconnects.

For the second objective, the fully additive manufacturing recipe with a comprehensive surface mechanism has been demonstrated.

RQ-1 ***What feature sized Cu interconnects are possible through different board-level fabrication methods?***

Current board-level manufacturing methods are challenged by the miniaturization of line widths of Cu interconnects. The PCB technology gap for metal patterning with lines and spaces (L/S) dimensions required improved infrastructures and new manufacturing procedures to scale them down further, contributing to 2D integration at the board level. Our research aims to scale down the Cu interconnects using laser-assisted lithography. Two different laser-assisted methods have been used, one is a subtractive etch-print method, and other one is an additive method.

RQ-2 ***How will be a fully additive method for selective metallisation at the board-level and what will the state-of-the-art contribution of such approach?***

In order to comply with RoHS regulations, industrial board-level manufacturing processes are using additive technologies such as SAPs and amSAPs. Such methods are useful for selective metallization on circuit boards. However, metal removal techniques are still included within the fabrication strategy. Our research intends to demonstrate a fully additive manufacturing recipe for selective metallisation with fewer stages than existing methods.

1.4 Thesis Scope

Electronics system packaging is a transdisciplinary area that incorporates expertise from the domains of electronics, material science, and chemical engineering. Design, verification, manufacturing, testing, reliability measurements, validation, and other aspects are all part of electronics packaging. This thesis has centered on the manufacturing or fabrication side of it. Industrial PCB production lines are transitioning from the traditional etch-print method to semi-additive and modified-semi additive methodologies to procure board-level miniaturization.

The goal of this research is to demonstrate a fully additive manufacturing technique for board-level applications. The Sequential Build-Up Covalent Bonded Metallisation (SBU-CBM) method is the name given to this manufacturing approach. To illustrate the method, industrial standard substrates and proprietary materials were employed.

The outcomes of this research work is based on iterative experiments and scientific analysis aiming to demonstrate a fully additive technique. All the fabrication works were conducted in the cleanroom at Luleå Tekniska Universitet (LTU), Sweden.

The scope of this research is focused on achieving a stable manufacturing recipe for the board-level fabrication. Initial fabrication such as geometries, embedded passives, lines & spaces with a state-of-the-art feature size on board level, and micro-vias were achieved and demonstrated using the proposed technique. Surface mechanism involved in each fabrication steps were investigated using various material characterizations.

Thermal testing, reliability testing, and electrical characterization of the manufacturing strategy are significant fields to analyse a production method. However, those are out of the scope of this thesis.

1.5 Structure of the Thesis

This thesis is of composite type and divided into two main sections. Part I outlines the research theme and develops the research questions and methodology. Part II comprises five append papers which make up this thesis's contribution. All of the articles have been published, accepted, or are in the process of being published in peer-reviewed journals and international conferences (IMAPs).

Six chapters comprise Part I. The first chapter includes a brief introduction to the research topic, motivation, research questions, applied methodology, and the thesis's scope. The second chapter presents a comprehensive review of standard electronics production techniques for board-level and outlines the comparison among them. The Sequential Build-Up Covalent Bonded Metallisation (SBU-CBM) process, which is fully additive, is proposed in the third chapter. It outlines the resources and materials utilized, the workflow of the fabrication scheme, and the surface mechanism involved. The fourth chapter demonstrates the experimental outcomes of the proposed fabrication scheme and its potential for different utilities connected with cutting-edge manufacturing trends. This chapter also delves into the various process parameters and how to optimize them during the fabrication. The scientific contributions of this thesis with attached publications are summarized in the fifth chapter. Finally, the sixth chapter concludes the findings and future research possibilities.

Chapter 2

Industrial Practices of Electronics Fabrication

Building of a complete electronic system from a single wafer, has to pass through various levels as indicated in the first chapter. However, the chip-level and board-level packaging has three steps in common, which are designing, manufacturing and testing. The design steps in both the levels include computer-aided-design (CAD) softwares to pattern and layout. Manufacturing stages in the industries include conveyorised automated systems with fixed recipe for different products. Whereas the research institutes use simple prototyping processes as used in this thesis work. There after, the manufactured products are tested and characterised using different setups before their release to consumer markets. All the three steps in both the levels are evolving and adapting new technologies to withstand the aggressive miniaturization since a few decades. Nevertheless, the production approaches at the board-level is still at developing stages compared to the chip-level manufacturing. Especially, the feature size of the geometries at chip-level is around 4nm [39], where as in the board level, it is around 30-40 μm.

Therefore, this thesis has focused on the fabrication approach at PCB segment. In this chapter, various approaches used for board-level fabrication are discussed. Each manufacturer uses their own techniques to form Cu interconnects on the board. Some of the well-known methods are outlined below.

2.1 Subtractive Etch & Print Method

It is one of the traditional production approach. This method uses photosensitive resist materials and etching solutions to transfer the pattern on the board. The process flow of this technique is to deposit a positive (or) negative resist layer on bulk Cu laminate and then print the pattern on to it using UV radiation. The alkaline/ acidic etchants remove the extra Cu and the developer solutions procure the desired interconnects on the board [14]. Such fabrication processes are cost-efficient and have shorter process flow. However, this produces a large amount of metallic wastes and are inefficient for

thick Cu layer patterning [13]. Considering the rapid scaling at the board-level, most of the industrial production approaches are shifting towards additive methods from this conventional technique. In this thesis, a laser assisted subtractive etch-print method is proposed in paper A. This work shows the possibility of scaling the Cu interconnects down to 3 μm by a subtractive method.

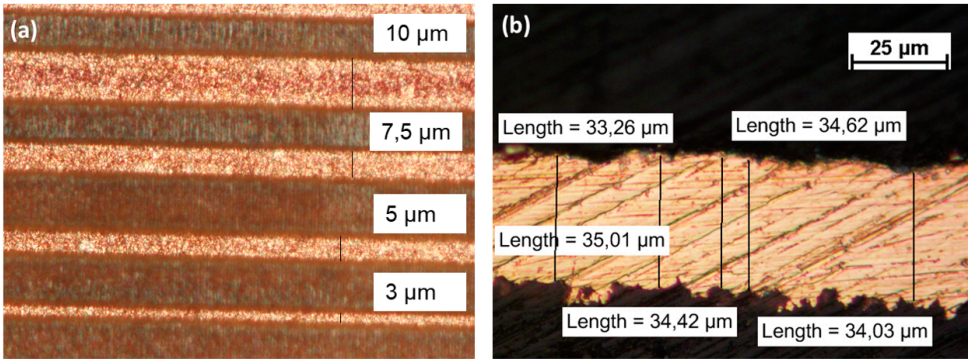


Figure 2.1: Optical Microscopic image of :(a) lines with different widths ; (b) Cross-sectional view of the thickness of the Cu.

2.2 Semi Additive Productions (SAPs)

This type of production processes are heavily in use for IC-level fabrication since decades and now are emerging in PCB fabrication as well. The process flow of this technique is to grow a seed layer of Cu using electroless plating or sputtering. Next, a liquid type resist material is used for selective patterning of Cu. However, the etching is inevitable in this technique [21]. This method produces finer tracks and lesser wastes compared to the subtractive methods. The process flow of such techniques follow sequential building of layers (SBU methods). Damascene and Dual Damascene processes are the examples of such techniques used in wafer-level production. In recent years, these SAP methods further categorised into modified and advanced modified methods with the advancement in fabrication steps.

2.2.1 modified-SAPs (m-SAPs)

This variant of SAPs has more additive steps compared to SAPs. The process flow is similar to the process flow of SAP. The key difference is the initial Cu layer. In m-SAPs, a laminated Cu foil (CCL) is used instead of the seed layer [8]. The primary metallisation process in m-SAPs techniques use either electroless Cu (or) carbon direct metallisation. The carbon technology has proven to be simpler, reduced number of steps

and cost-friendly than the horizontal electroless Cu processes.

2.2.2 advanced modified-SAPs (am-SAPs)

It is the advanced variant of m-SAP methods. Such production techniques are common with IC-level fabrication. Therefore, these are also called substrate like PCBs (SLP) [23], as the feature sizes are comparable to IC packages. The electroless Cu plating is an integral part of these approaches to achieve fine traces/spaces at the board-level. However, both m-SAPs and am-SAPs approaches still use anisotropic etching to remove the extra Cu during patterning [20].

2.3 Comparison among Methods

This section outlines the technical distinctions between the manufacturing methods as mentioned. In figure 2.2, the board-level production technologies were compared based on 9 aspects and reported in [3]. The electroplating stage distinguishes the subtractive and semi-additive techniques (m-SAPs and am-SAPs). Panel plating occurs in subtractive techniques, which deposits excess Cu and removes it during patterning. In contrast, pattern plating occurs in SAPs, which deposits Cu selectively on the traces and pads. The process flow of m-SAP and am-SAP methods has combined additive (deposition of materials) and subtractive (etching) steps. Nevertheless, am-SAP methods employ more additive steps than m-SAP methods. As seen in the figure 2.2, the finest lines and spaces (L/S) and smallest vias are possible through am-SAP methods. Additive techniques are environmentally friendly and produce lesser amount of metallic wastes compared to the subtractive etch-and-print methods as shown in the figure 2.2. Another

	Subtractive	**m-SAP**	**am-SAP**
Cu clad thickness (µm)	2-9	2-5	< 3
Eless Cu thickness (µm)	0.35-0.5	0.35-0.5	1
Flash Cu thickness (µm)	2-5	1-3	----
Panel plating thickness (µm)	15-20	----	----
Pattern plating required	No	Yes	Yes
Etch resist	Dry film or LER	----	
Cu to be etched (µm)	17-29	4-10	< 3
Achievable L/S (µm)	> 35	> 30	> 20
µVia Diameter (µm)	70	50	40

Figure 2.2: Technical comparison among the board-level fabrication methods presented by Atotech Gmbh in [3].

comparison among the board-level production methods with respect to the lines/spaces and the thickness of the starting Cu layer is shown in figure 2.3. The feature sizes achieved by different metallisation techniques such as embedded trace sustrate (ETS), advanced tenting processing (ATP) and substrate-like-PCBs (SLPs) are illustrated. This indicates how the production approaches are shifting towards additive methods from conventional subtractive ones.

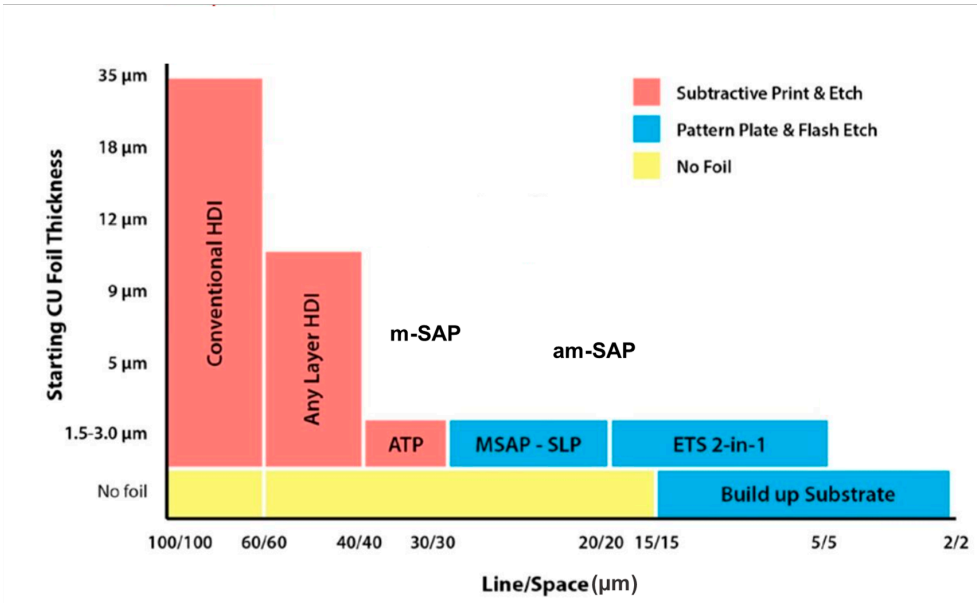


Figure 2.3: Starting copper foil thickness vs. line/space dimensions for various advanced PCB manufacturing applications and commercial metallization processes associated with them reported by MacDermid Alpha electronics solutions in [1].

2.4 Printed Electronics in Electronics Production

Over a few decades, electronics manufacturing technologies have transformed worldwide by generating smart, ultra-cost-effective, and miniaturized products. Silicon-based electronics and printed electronics (PE) are two significant contributors to these manufacturing techniques [19]. PE is a hybrid technology incorporating innovative additive manufacturing processes with emerging functional nano-materials. This combination of methods and materials yields thin, light-weight, wearable, flexible, economical, and ecologically friendly electronics [30]. Applications of PE technologies are most common in four areas:

radio frequency identification tags (RFID), printed circuit boards (PCBs), flexible display devices, and sensors [38]. In PE, the additive material deposition techniques, to form conductive traces, are classified as parallel methods or sequential methods [31]. The parallel methods are contact techniques in which the substrate and the printing plate directly contact each other. Screen printing, flexography, micro-stamping, gravure printing, soft lithography, and stencil printing are some of the parallel methods used in industry [6, 7]. The sequential methods are non-contact approaches where the substrate only gets in contact with deposition materials. Here are several examples:aerosol printing [9], spray coating [26, 27], inkjet printing [28, 40] and laser direct writing (LDW) [4, 18].

Because of the additive nature of the process, LDW technologies have lately gained widespread acceptance for device manufacturing, and packaging [31]. Current board-level feature size expectations for interconnects and patterns are in the mesoscale (1-100 μm), while chip-level demands are in the nano-scale. Therefore, there is a clear necessity for such fabrication procedures at the board level, which may minimize the dimensions of Cu interconnects, the number of fabrication steps, the cost, and metallic wastes. In an attempt, a fully additive production approach has been proposed in this thesis. This process employs the LDW method and electroless Cu plating for metallisation at the board level. A detailed description of the method is presented in the next chapter.

Chapter 3

A fully Additive Fabrication Method

'Additive manufacturing (AM), also known as 3D printing, is a transformative approach to industrial production that enables the creation of lighter, stronger parts and systems.'- General Electric

3.1 SBU-CBM Approach

The fabrication process illustrated in this thesis has named 'Sequential Build Up-Covalent Bonded Metallization' (SBU-CBM), falls under fully additive production category. In this technique, the layers were gradually created on top of one other, with covalent bonding between the layers to generate a metallic coating on non-conductive polymers.

Figure 3.1 depicts the key steps of this pattern-transferring approach. In figure 3.1(a), a conventional etch-and-print method is shown where the Cu foil has been laminated onto an FR-4 substrate and with the use of a mask, any designed structure can be made. A considerable portion of the undesired Cu (besides the pattern) is drained during the etching stage. This waste is magnified when dealing with smaller feature size patterns. Meanwhile, in figure 3.1 (b), an additive process additive technique that supports selective metallization is shown. Metallization of the desired pattern is regulated throughout the laser exposure and pattern transfer stages. Because the metal will only be deposited in the desired places, such procedures in mass production will reduce the amount of metallic waste and the cost of manufacturing.

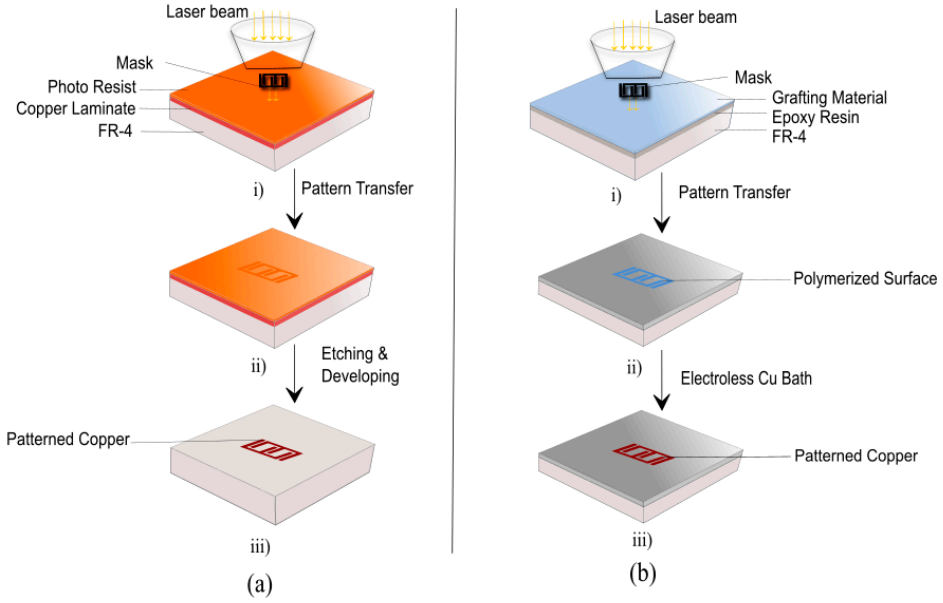


Figure 3.1: Main Patterning and Metallization steps in the PCB fabrication (**a**) A conventional Subtractive etch-and-print Technology. (**b**) A fully additive Technology named SBU-CBM approach with selective metallization.

In this work, a recipe of the fully additive fabrication technique has been demonstrated. The main highlights of this work are:

- To show a completely additive approach for obtaining any desired geometries on the FR-4 substrate utilizing exopy resins and polymer-based CBM technology at relatively lower temperature (20-45 °C).
- To demonstrate the selective metallization feature of the process by eliminating the etching process significantly (especially during the metallization), i.e., adapting an environmentally friendlier manufacturing strategy.
- To understand the surface modification and mechanism of metallization (of fabrication steps) using various material characterization methods.
- To demonstrate the feasibility of a manufacturing method for the PCB fabrication segment of the industry in the direction of miniaturization.

3.2 Machines & Materials Specifications

All the experimental works related to the fabrication reported in this thesis are carried out in a particle-free environment. Two laser devices utilized in this study are installed in a sophisticated cleanroom to ensure that no contamination occurs. One of the laser

instruments used in producing the horizontal 2D constructions is LW405 by Microtech [22]. This machine was being used for both the subtractive method shown in paper A and the additive SBU-CBM approach in rest of the papers. Another laser machine, the PL2210, has been used to create micro vias. List of machines used throughout this research work are as follows:

- LW405 laser writer machine.
- PL2210 laser machine.
- Spin coater.
- Ultra-sonic cleaner.
- UV curing equipment.

The materials used in this production process meet IPC standards and are NEMA grade compatible. Industrial standard FR-4 is selected as the base material; however, the recipe is flexible enough to use FR-2, SU-8, FR-3, XPC, CEM-3, etc. Polyurethane (PU) is used as the epoxy prepreg for the fabrication. CBM solutions are the core of this fabrication technique. Because the composition of each CBM solution differs, the activation energy of the chemical constituents necessitates a correct laser exposure setting. The chemical ingredients (monomers, initiators, solvents, and spacers) and their stoichiometry ratios are the main variants in CBM solutions. Therefore, the selection of process parameters is the most crucial part of this manufacturing approach. Both the PU and CBM solutions are patented materials obtained from Cuptronic Technology AB, Stockholm, Sweden [32]. Jkem ltd, Stockholm, Sweden, has provided the proprietary electroless Cu kit for the metallisation [11]. The following materials were used during this work :

- FR-4 as base substrate.
- Polyurethane as epoxy resin.
- HP-14 as CBM solution.
- PEC-660 series electroless plating kit.

3.3 Process Flow of the fabrication

The process flow of the SBU-CBM method is shown in figure 3.2 and 3.4. Figure 3.2 is showing the steps for the bulk Cu deposition on FR-4, whereas figure 3.4 is demonstrating the selective metallisation steps. The only difference is the computer-aided (CAD) mask file used in the latter one.

The fabrication recipe of the proposed additive technique has the following steps :

Step 1: Ultrasonic cleaning of the FR-4 substrate using de-ionized water (DIW).
Step 2: Drying of the FR-4 substrate at room temperature.
Step 3: Spin coating of the PU layer on top of FR-4.
Step 4: UV soft baking for 1 minute followed by surface hardening at room temperature.
Step 5: Spin coating of HP-14 on PU.
Step 6: Polymerization of the surface using actinic radiation and pattern file (optional in case of bulk Cu deposition)

Step 7: Proper cleaning using DIW of the sample to remove the unexposed HP-14 solution from the sample surface before the Cu bath.
Step 8: Electroless Cu bath (Predip, Activator, Reducer and Cu bath).
Step 9: Final cleaning of the surface and characterization.

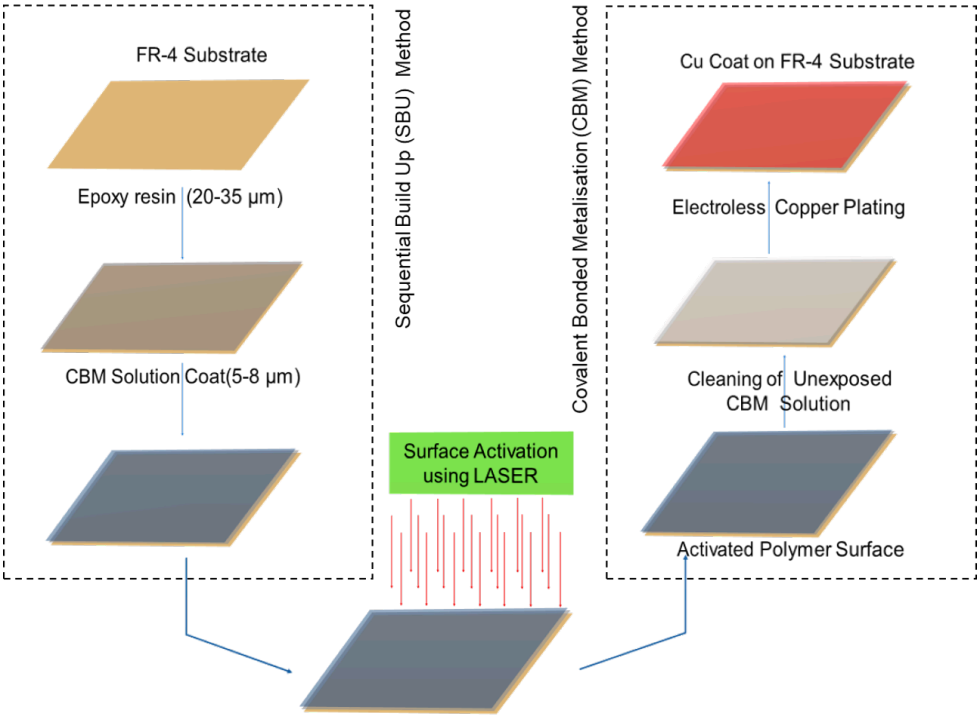


Figure 3.2: The Process flow diagram of the SBU-CBM method for bulk Cu Metalisation.

3.4 Surface Modification Mechanism

In this section, a thorough investigation of the surface mechanism of the fabrication steps is presented. The samples of each fabrication step shown in the process flow diagram were tested with different characterization techniques to understand the surface modification phenomena. Both experimental and computational methods were employed to identify the critical steps in this production approach as presented in paper E. The two main steps identified are i) polymerization of CBM seed layer using laser and ii) electroless Cu plating through different baths.

3.4.1 Bulk Metallisation

The first step of the SBU-CBM process is a uniform coating of PU over the FR-4 substrate and adequately curing it to ensure the adhesion of the CBM solution on top of it. This procedure is adaptable enough to utilize any other epoxy resin instead. The seed layer of the CBM solution was then evenly spin-coated. In this case, HP-14 is used, which has acrylic acid as an active monomer, ester of acrylic acid, and amide of acrylic acid as spacers and initiators respectively. When the polymerizable units of the acrylic acid (C=C) are appropriately exposed to the UV laser, they perform a chemical reaction with the unsaturated groups of polyurethane and produce covalent bonding at the interface. The tasks of the initiators and spacers are to start the polymerization reaction and control the optical properties of the active monomers.

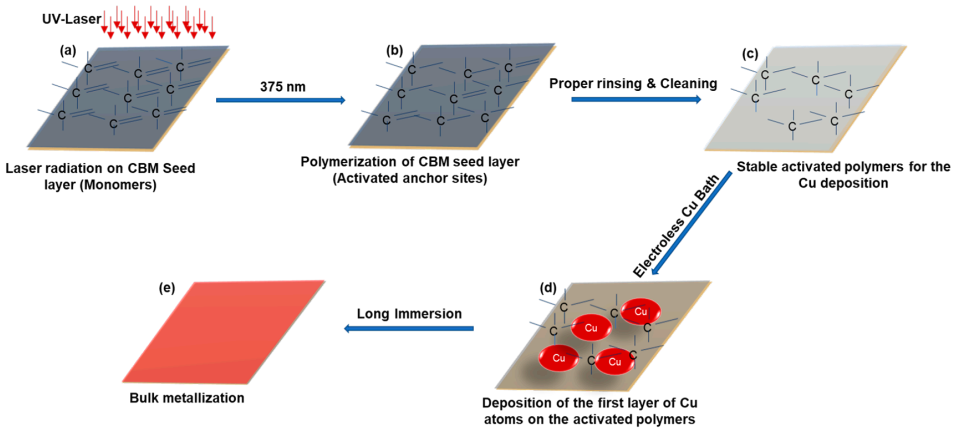


Figure 3.3: Surface modification steps in the SBU-CBM method with bulk metallisation,(a) Showing the carbon double bonds in acrylic acid (the primary constituent of the CBM solution seed layer) ; (b) Partial activation of the double bonds by the actinic radiation and polymerization on Polyurethane surface; (c) Stable activated polymers on the sample's surface after proper cleaning and rinsing; (d) First layer of Cu deposited on the activated polymers; (e) Formation of a uniform layer of Cu at the final step of the SBU-CBM process.

In figure 3.3, steps (a), (b) and (c) are showing the aforementioned mechanism. Double bonds of carbon in the acrylic acid get unsaturated upon receiving activation energy from UV radiation as shown in figure 3.3(a). Meanwhile, some of the double bonds remain as it is and are removed from the surface by proper cleaning and rinsing as shown in figure 3.3(c). The polymerized surface then undergoes an electroless bath to adhere metal ions onto it as shown in figure 3.3(d) and (e). In the case of bulk metallisation, the surface activation is pretty straightforward as it doesn't have a pattern file as shown

in figure 3.2. The only crucial step is to provide an actinic radiation on the seed layer to undergo bulk polymerisation. This surface activation can be done through UV-laser (or) UV-optical sources. The surface phenomenon of creating covalent bonding between the CBM solution and epoxy resin is easy to manage on the bulk surface. In contrast, many accuracies are needed to confine this polymerisation reaction with specific patterns.

3.4.2 Selective Metallisation

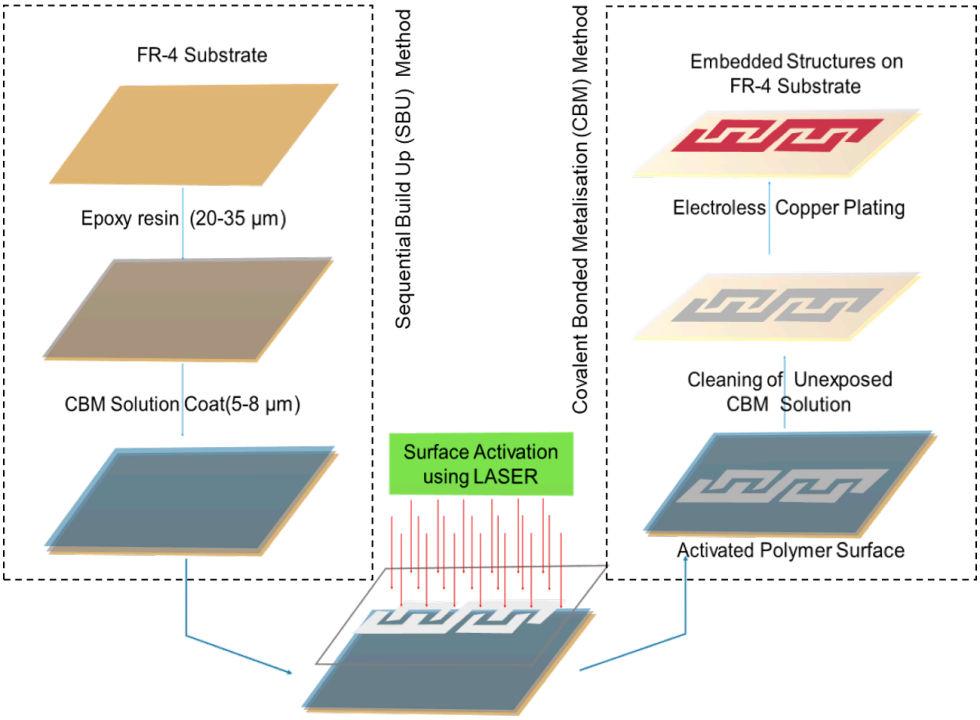


Figure 3.4: The Process flow diagram of the SBU-CBM method for selective metallisation.

In the case of selective metallisation, a UV-laser source is used to activate the surface. Due to the presence of pattern-mask file, only selective regions of the seed layer undergo polymerisation, as shown in figure 3.4. The surface phenomena are the same as shown in figure 3.3. The selection of process parameters is critical in achieving an excellent selective polymerised pattern. In this case, the surface cleaning and metallisation part become extremely important, especially for designs with small feature sizes. More about the process parameters is outlined in chapter 4.

3.4.3 Electroless Metallization

Once the surface gets polymerized (with or without pattern), the next step is electroless plating. The electroless Cu kit, used in this work, consists of four different baths. The information about the baths is as follows:

1. Predip (Bath-I): This is the initial bath containing Ammonium hydroxide solution which has two main advantages. One, it ensures good coverage with a Palladium (Pd) based activator. Second, it also acts as a physical buffer to the activator bath.
2. Activator (Bath-II): This bath contains Pd as a catalyst which acts as an activator, used after bath-I.
3. Reducer (Bath-III): This bath contains boric acid and a proprietary reducing agent (ACS-2075) which reduces the Pd ion and forms the nucleation site for the Cu atoms.
4. Cu Bath (Bath-IV): This is the last bath containing Copper sulphate and formaldehyde solution received as PEC-A, PEC-M, and PEC-B.

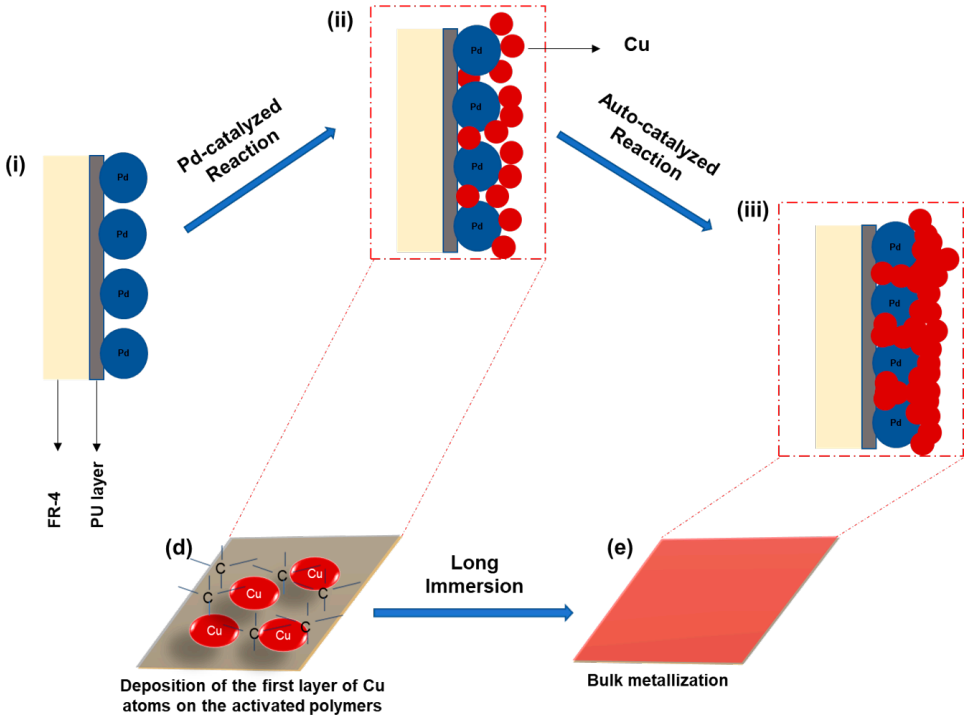


Figure 3.5: Elaboration of the step (d) & (e) of figure 3.3 :(i) Deposition of Pd atom on the surface during bath-II; (ii) Deposition of the first Cu layer through Pd-catalytic reduction; (iii) Bulk metallisation through auto-catalytic deposition (achieved by long immersion in bath-IV).

After the completion of the above baths, a bulk layer of Cu is deposited on the surface. Selective metallisation can be observed in case of patterns. A detailed mechanism of these baths is shown in figure 3.5. The steps (d) and (e) in figure 3.3 undergoes two major catalytic reaction as shown in figure 3.5.

Catalytic behaviour of *Pd* ion: Bath-II activates the nucleation site for the absorption of Cu atoms. This bath contains colloidal palladium (Pd) as a catalyst, which enhances the metallisation process. Whereas, bath-III is the reducer bath, the Pd atoms catalyze the copper-reduction and creates an initial layer of Cu at the nucleation sites around Pd atom as shown in figure 3.5(ii). It is a very crucial step in the case of selective metallisation of patterns which is dependent on surface activation step.

Auto-catalytic Copper deposition: The last step of the SBU-CBM method is Cu bath i.e. bath-IV. Each 'nascent' Cu atom acts as a catalyst in itself and the reaction continues as shown in figure 3.5(iii), hence it is called 'auto-catalytic deposition'.The metallisation of the surface has a great influence from bath-II and bath-III. To successfully pattern the finest feature sizes, process parameters of the baths need to be well-controlled and optimised.

3.5 Surface Characterizations

A few material characterizations were performed to investigate the surface modification mechanism of the proposed fabrication technique. A set of seven samples were used for the examination, which is prepared based on the process flow shown in figure 3.2. The investigation includes optical microscopy, scanning electron microscopy (SEM), energy-dispersive X-ray spectroscopy (EDS), and X-ray diffraction (XRD). Finally, a complementary density functional theory (DFT) computation was performed to validate the surface analysis.

SEM-EDS Analysis

The use of scanning electron microscopy (SEM) with energy-dispersive X-ray spectroscopy (EDS) allows for the focused examination of sample surfaces. These techniques are commonly used for material surface examination, product failure investigation, reverse engineering, contaminant detection, solder joint study, and other purposes. Because of the non-conductive surface, the samples were sputtered with platinum (Pt) so that the focused electron beam could penetrate the sample's surface. The SEM images of the crucial steps are shown in figure 3.6. The surface of the PU and polymerized seed layer of the CBM solution are shown in figure 3.6(a) and (b), respectively. The corresponding EDS report of the polymerized CBM layer is shown in figure 3.7 (a).The result shows the surface is completely polymerised with carbon chains, as expected. In figure 3.6 (c), (d), (e), and (f), the surface of the test specimen after bath-I, II, III, and IV are shown,

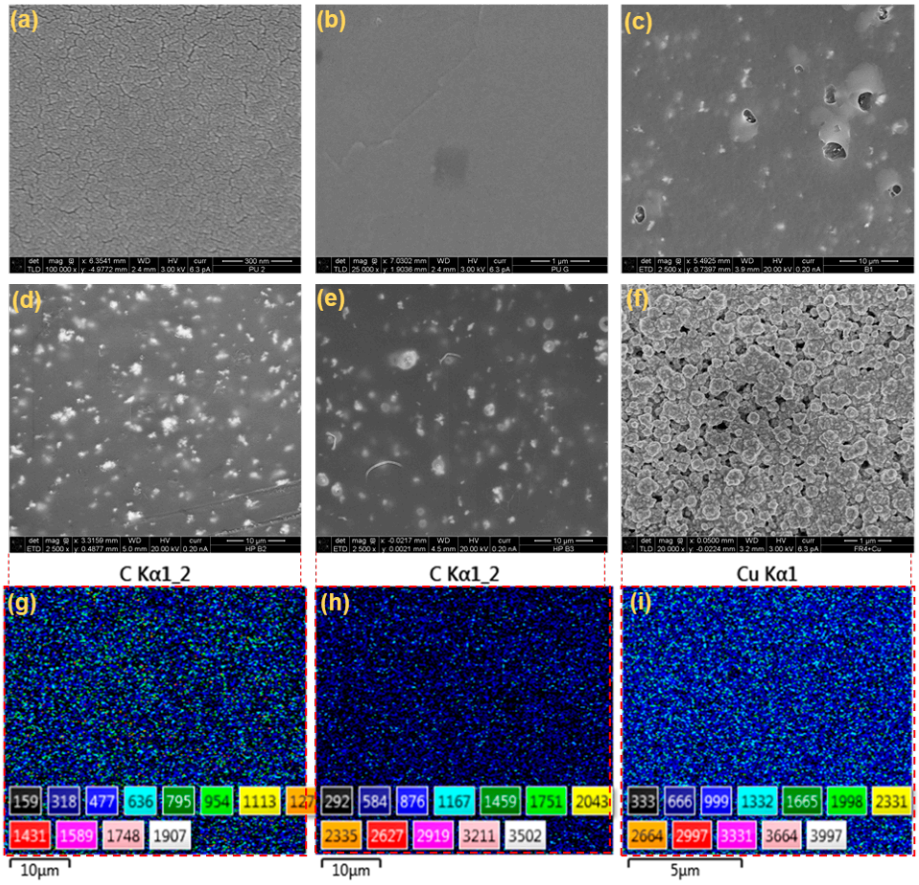


Figure 3.6: SEM-EDS analysis of the SBU-CBM method: (a) SEM image of the PU surface ; (b) SEM image of the polymerized CBM solution's surface; (c) SEM image of the surface after electroless plating bath-I; (d) SEM image of the surface after bath-II; (e) SEM image of the surface after bath-III ; (f) SEM image of the final Cu metalised surface; (g) EDS analysis of the surface after bath-II; (h) EDS analysis of the surface after bath-III; (i) EDS analysis of the surface after bath-IV.

respectively. Figures 3.6 (g), (h) and (i) show the EDS mapping of the sample's surface after bath-II, III, and IV, respectively.

In figure 3.7 (b), the EDS report of the sample's surface after bath-II is shown. The result is confirming the presence of 'Pd' atoms on the surface. Whereas in bath-III, after the reduction bath, same amount of Pd present on the surface but in a dispersed manner as shown in the EDS report in figure 3.7 (c). The EDS report of the last step, shown in 3.7 (d), is showing the presence of Cu atoms in abundant on the sample's surface.

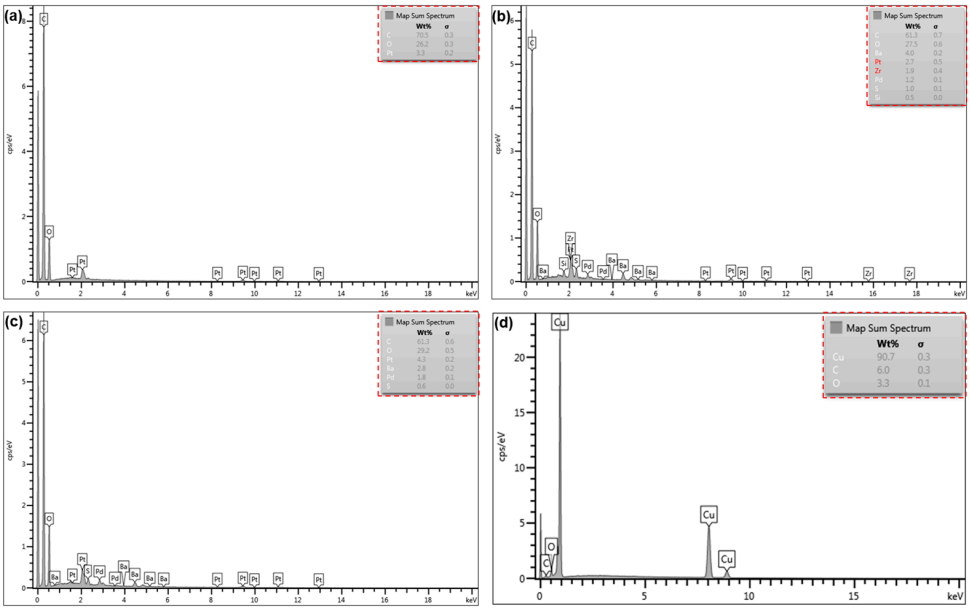
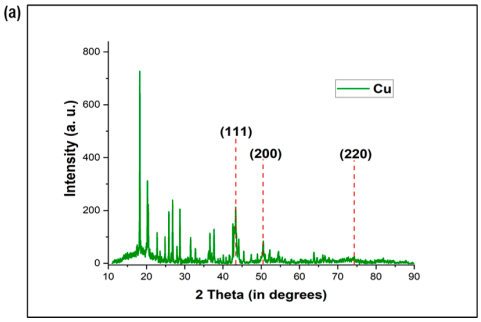


Figure 3.7: EDS report of crucial steps of the fabrication: (a) Polymerized CBM layer surface; (b) Surface after bath-II; (c) Surface after bath-III; (d) Surface after bath-IV.

The above analysis indicates that polyurethane (PU) and CBM solution sequentially create carbon bonds on FR-4. Then, bath-II adds palladium (Pd) to the polymerised surface via a catalytic process. This also provides nucleation sites for the copper (Cu) atom to adhere to the surface in bath-IV. After bath-IV, the final surface only has Cu on it, confirming that the bulk Cu metallisation has occurred.

XRD Analysis

In solid-state chemistry and materials research, XRD is one of the principal characterisation methods used to investigate the physicochemical make-up of unknown materials. It helps to determine the size and form of the unit cell for qualitative (Phase Identification) and quantitative (Lattice parameter determination and analysis of Phase fraction) analysis. XRD Peaks provide information on translational symmetry - the size and shape of the unit cell. The peak intensities provide information on electron density inside the unit cell, essentially where the atoms are placed. In the present study, XRD analysis has been done for all the samples, however, only the final Cu metalised sample is shown in figure 3.8(a). The diffraction peaks on the Cu deposited sample are located : (111) at 43.38, (200) at 50.524 and (220) at 74.24 respectively. Figure 3.8(b) shows the crystallographic information about the deposited Cu with cubical crystal structure.



Crystallographic parameters		Peak List						
Crystal System:	Cubic	No.	h	k	l	d[Å]	2θ [°]	I[%]
Space group:	Fm-3m	1	1	1	1	2.08420	43.381	100.0
Space group number:	225	2	2	0	0	1.80500	50.524	42.6
		3	2	2	0	1.27630	74.248	17.4
a(Å)	3.6100	4	3	1	1	1.08850	90.091	15.9
b(Å)	3.6100	5	2	2	2	1.04210	95.323	4.4
C(Å)	3.6100	6	4	0	0	0.90250	117.193	1.9
Alpha (°)	90.0000	7	3	3	1	0.82820	136.897	5.9
Beta (°)	90.0000	8	4	2	0	0.80720	145.217	5.6
Gamma (°)	90.0000							
Volume of cell ((10^6 pm^3)	47.05							
Z:	4.00							
RIR:	8.85							

Figure 3.8: XRD analysis of the SBU-CBM Fabrication method, (a) XRD plot of the Cu deposited sample with the main diffraction peaks.; (b) Crystallographic Information about the Cu peaks used for DFT modelling of the process.

This analysis shows the deposited Cu through the SBU-CBM method has cubic crystal structure. Based on literature [33,34], this Cu deposition is perfect for its usage in printed electronics applications. Furthermore, this crystallographic information has been utilized for computation simulation (DFT) of the fabrication process.

DFT Analysis

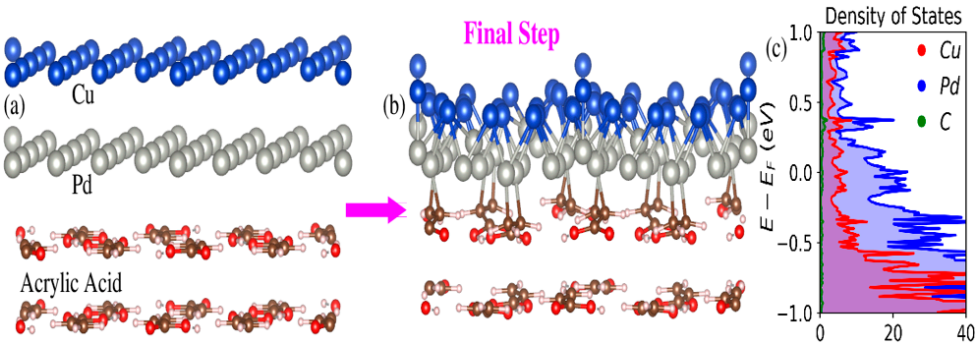


Figure 3.9: DFT analysis of the SBU-CBM Fabrication method,(a) shows schematic view of the molecular structure of acrylic acid (an active monomer in HP-14 samples) having Pd and Cu atomic layers deposited on top to mimic the experimental setup; (b) displays the Pd atoms tend to form covalent bonds with unsaturated C atoms as well as Cu atoms implanted on its surface; (c) Calculation of element-projected density of states (DOS) to confirm the characteristic nature of inter atomic interactions. The presence of orbital hybridization between Cu and Pd d-orbitals close to the Fermi level support the experimental observations.

This computation has been done in collaboration with one of the colleagues in the Department of Physics at LTU, to elucidate the underlying mechanism of the SBU-CBM method. The first-principle calculations based on density functional theory (DFT) were performed using the projector augmented wave method as implemented in the Vienna Ab-initio Simulation Package (VASP) [12]. The outcomes of this analysis are shown in figure 3.9. A detailed description of this analysis is reported in E.

Chapter 4

Experimental Outcomes of SBU-CBM Method

'A lot is also happening beyond conventional PCB production. Digital and additive manufacturing technologies such as laser direct exposure and soldermask inkjeting are fundamentally changing the technical basis of PCB manufacturers. In addition, the latest developments in the field of additive manufacturing technologies with 3D printing show new opportunities and possibilities for the additive fully digitalised production of a PCB outside the known standard processes. This requires printable materials that have comparable or better final properties as well as machines and systems to bring the process costs into an economic corridor'.- PCB Roadmap Blog

4.1 Fabrication of feature sized Interconnects

In this section, the experimental results are presented. The proposed fabrication recipe has been used to achieve the following outcomes.

4.1.1 Lines and Spaces (L/S)

The L/S requirement of the Cu interconnects at the board-level, to assemble the state-of-the art ICs, are around 20μm. So far, this production technique has achieved 2.5 μm width of copper tracks and 2.65 μm of least spacing between the tracks as shown in figure 4.1 (b) and (d) respectively. Whereas in figure 4.1(a) and (c), the SEM image of different Cu track ranging between 5 to 8 μm and a spacing of 5.5 μm between the lines, is shown. The spot between the metallic tracks, in 4.1(a), is due to the high beam of EDS. However, this production approach has the potential to reach further finest feature sizes by optimizing the current process parameters.

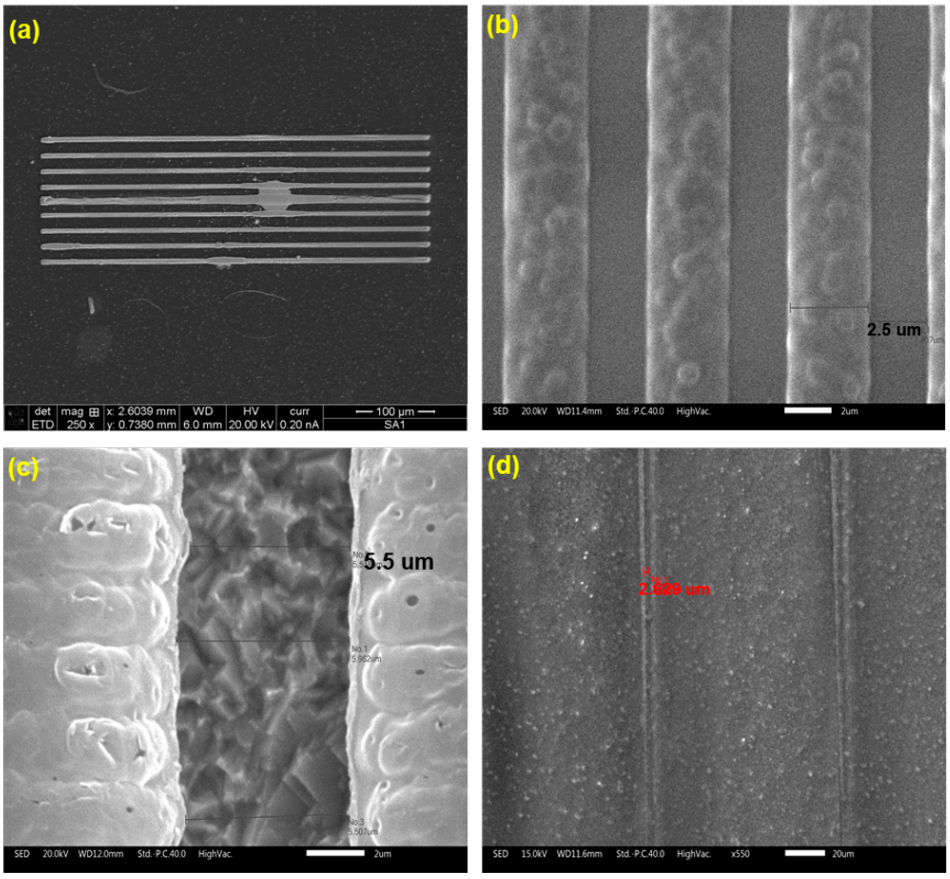


Figure 4.1: L/S fabriacted using the proposed SBU-CBM method (a) SEM image of several Cu lines of dimension ranging between 5 to 8 μm (the bright spot in the image is formed due to high beam of EDS spectrum); (b) SEM image of the Cu tracks with 2.5 μm width; (c) SEM image of the spacing of width 5.5 μm; (d) SEM image of the minimum spacing between two Cu tracks (reported so far) i.e. 2.629 μm .

4.1.2 Microvias

In electronics production, microvia technology is one of the important manufacturing processes for obtaining high-density circuitry [17]. This uses SBU technique to form multi-layer boards to support SOP packaging [37]. Microvias are broadly classified into three types : blind via, buried via and through-hole via. According to the IPC standards, there are five major processes to form microvias and laser ablation is the most used technique in recent years [15]. This SBU-CBM method has used laser cold ablation to form a microvia of minimum radius of 10 μm shown in figure 4.2 (b). In figure 4.2 (a), a

square shaped via without metal plating is shown. Some of the work related to microvia with metal plating is shown in figure 4.2 (c) and (d), which illustrates the potential of this fabrication method to procure high-density interconnects [24].

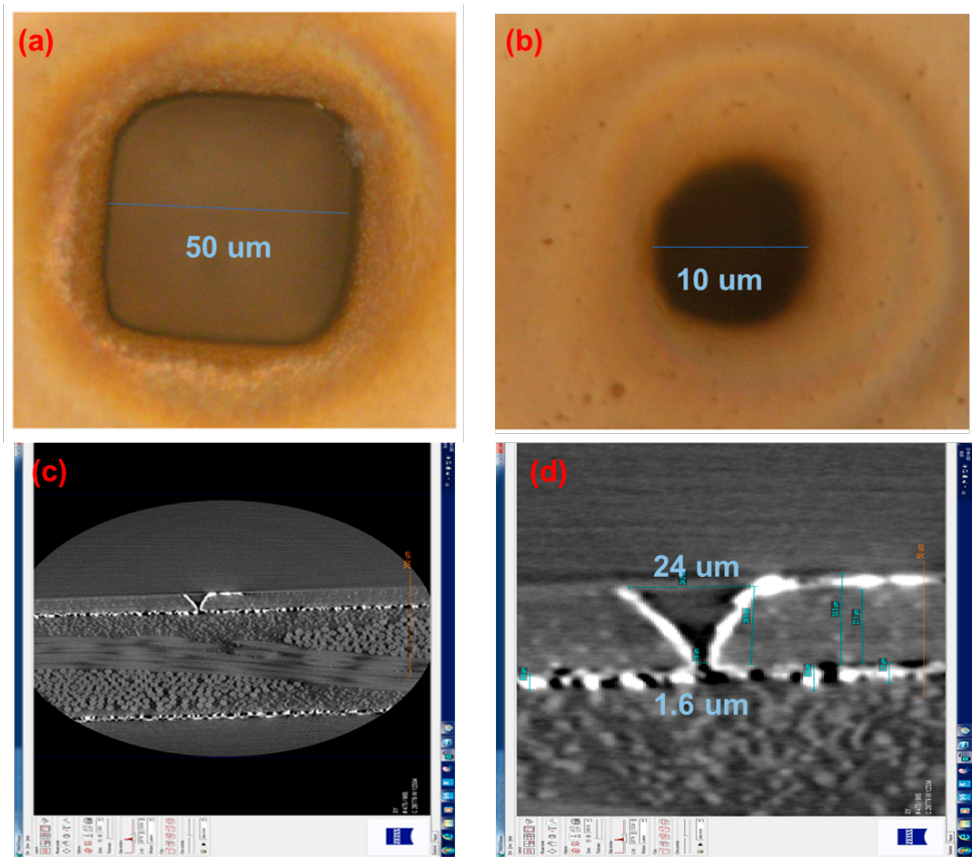


Figure 4.2: Microvias fabriacted using the proposed SBU-CBM method (a) Optical microscopic image of a via without metallization Cu of dimension 50X50 μm ; (b) A circular via with 10 μm radius; (c) X-ray tomographic image of a via (Previous work in EISLAB by Abdelghani et al. [24]); (d)Tomographic image of the via made using SBU-CBM method with feature size dimensions [24]

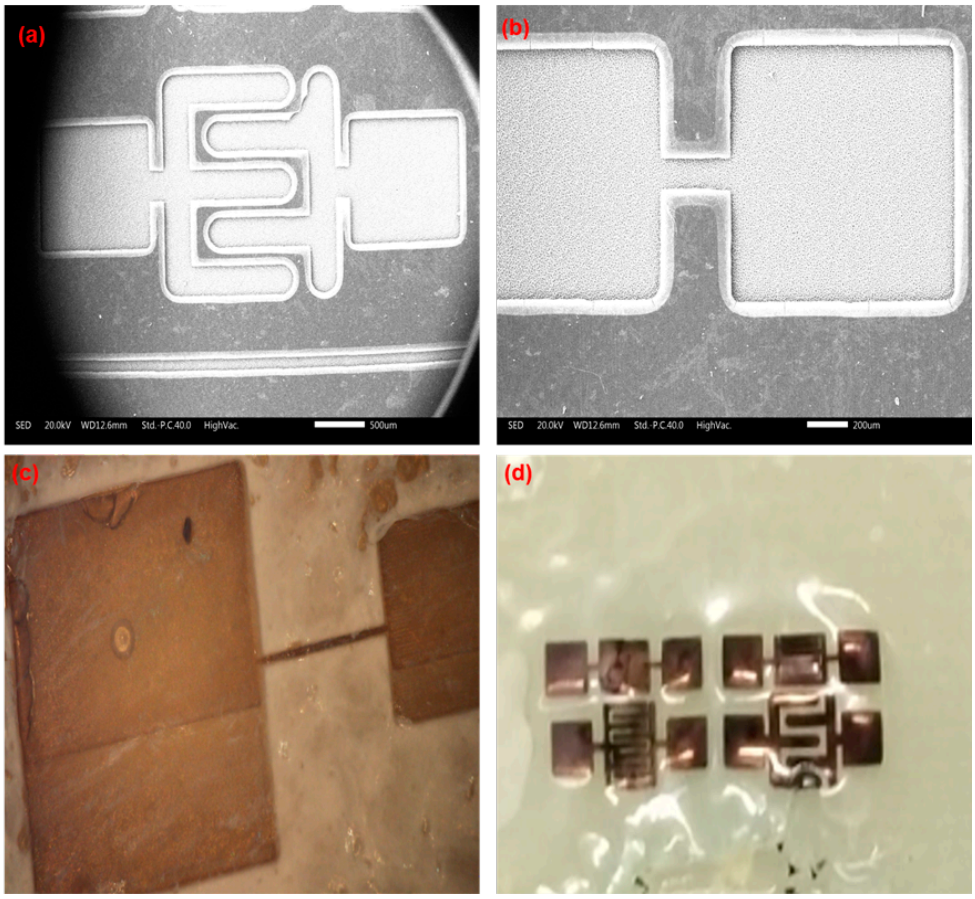


Figure 4.3: Different on-board geometries drawn using SBU-CBM mthod: (a) SEM image of a capacitive structure connected with pads; (b) SEM image of two same-sized connecting pads; (C) Optical microscopic view of two different pads using 2.5 μm line width; (d) Overview of a SBU-CBM fabricated sample with complex geometrical structures.

4.2 Fabrication of on-board Patterns

The potential of this fully additive fabrication approach is demonstrated by patterning desired geometries on a 2D surface. Experimental evidence of a successful 2D fabrication is presented in paper D. The view of an actual sample made by this production approach is shown in figure 4.3(d). Other examples of the geometries are shown 4.3(a), (b) and (c).

4.3 Embedded Passives

Miniaturization in electronics packaging is the call of the day. The use of bulky passive components in PCBs, such as resistors, capacitors, and inductors, results in an area penalty, limiting the overall packaging density of the system. In a typical PCB, more than 80 % of components are passives, which take more than 40 % of the area [5].

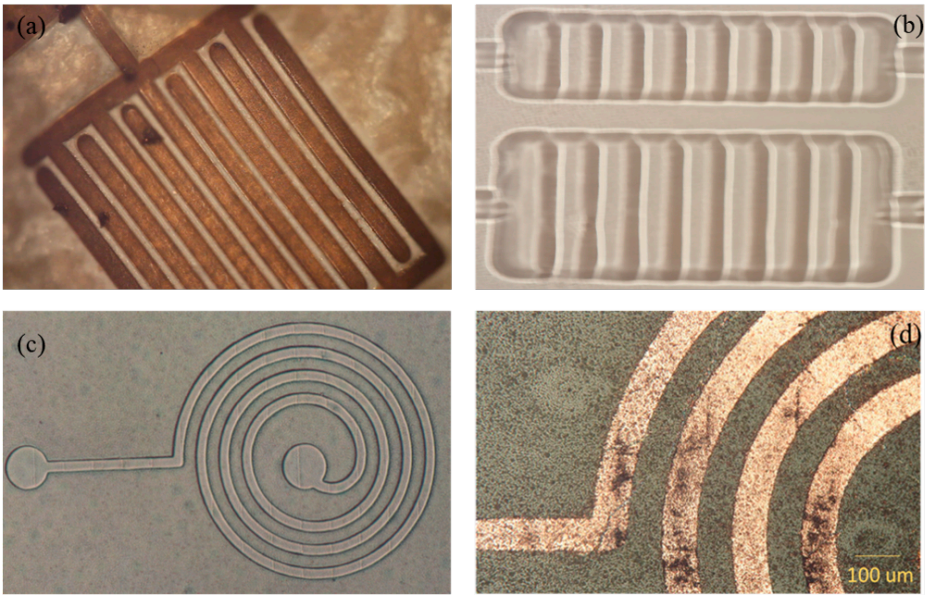


Figure 4.4: Surface engineering of the SBU-CBM method,(a) Showing the carbon double bonds in acrylic acid (the primary constituent of the CBM solution seed layer) ; (b) Partial activation of the double bonds by the actinic radiation and polymerization on Polyurethane surface; (c) Stable activated polymers on the sample's surface after proper cleaning and rinsing; (d) First layer of Cu deposited on the activated polymer.

As a result, embedded passives are widely employed in current packaging to fit many components in a small amount of space. Embedded passives are made on PCB base substrates utilizing dielectric materials and metallic layer patterning are presented in paper B and D. These methods are in high demand because they eliminate solder connections and minimize parasitic. Using the SBU-CBM method, embedded capacitors were fabricated with the value ranging from 0.3 to 8 pF, as shown in figure 4.4 (a) and (b). While, a planar circular-spiral inductor is fabricated with a feature size of 75 μm as shown in figure 4.4 (c) and (d).

4.4 Challenges in Fabrication

In this section, a few challenges observed during the experiments related to the fabrication methodology are presented.

4.4.1 Inadequate Surface Activation

The CBM solution on the PU surface requires an adequate amount of actinic radiation to polymerize and form bonds. Hence, the appropriate selection of laser parameters plays a crucial role in patterning the structures. Table 4.2 shows some of the parameters adjusted with respect to HP-14. A few shortcomings witnessed during the surface activation were due to the formation of cross-linked or branched polymerization while drawing complex patterns. High laser gain and an excessive number of repetitions are the principal causes of such effects, which result in structural widening.

4.4.2 Surface Cleansing

Cleaning the surface of substrate is another critical stage in this production approach. Specifically, following laser exposure with an active polymerized unit, the samples must be carefully cleaned to avoid excessive metallisation on the surface. Because the bonds are covalent in nature, proper washing of the surface doesn't affect the polymerized units. Furthermore, it has been observed that, washing the substrate with de-ionised water (DIW) in between the electroless baths, improves metallisation outcomes.

4.4.3 Improper Metallization

Poor metallization is another factor to consider in this production approach. Due to the selection of odd parameters, the polymer chains remain under metalised or sometimes over metalised for different patterns. Hence, two related issues observed during the experimentation are over-and under-metallization. Sometimes, the reason behind the poor Cu plating is sub-standard laser modification. The challenges outlined were due to inappropriate selection of process parameters; therefore, optimisation of parameters is one of the crucial steps in this proposed technique. Optimised parameters for the electroless plating is presented in table 4.1.

4.5 Process Parameter Optimisation

Because of the experimental nature of the study and the involvement of several parameters, each specimen is exposed to a visual inspection following every parametric sweep. The values of the parameters vary for different CBM solutions. In this scenario, parameters for HP-14 were examined. This manufacturing process included two critical stages that controlled the formation of structures on the FR-4 substrate: laser exposure and electroless Cu bath. The former features three control parameters: power gain, No.

Table 4.1: Process parameter of the electroless Cu Bath for perfect metallisation

Electroless Copper Bath Parameters					
	Type	Name	Concentration	Time (in Minutes)	Temperature (°C)
I	Predip	Precup-128	55.5 ml in 200 ml of DIW	1	25
II	Activator	Catcup-207	55.5 ml in 200 ml of DIW	6	42
III	Reducer	Boric acid + ACS-2075	2.4 gm in 100 ml of DIW + 1.5 ml of ACS-2075	6	27
IV	Cu Bath	PEC-660 (A/M/B)	9.25 ml of PEC-A + 6.75 ml of PEC-M + 9.75 ml of PEC-B in 100 ml of DIW	4-6	25

of repetition (exposure time), and D-step (rate of scan). The latter incorporates three parameters: bath time, concentration, and temperature of the bath. The electroless bath also requires optimal bath time, concentration, and temperature to achieve proper Cu deposition, and these parameters vary for CBM solutions as well. The optimised parameters for HP-14 is presented in table 4.2.

The important process parameters involved in this production technique are:

A. Laser Gain
B. Exposure time (no. of repetition)
C. Scanning rate (D-step)
D. Concentration of electroless bath
E. Immersion time

A, B, and C are the parameters associated to Laser whereas; D and E are associated with Cu bath.

Table 4.2: Laser Parameters optimized for HP-14

Feature size in the Pattern (in μm)	laser Gain (mW)	D-step (80 μm/sec)	No. of Repetition
30 and above	6.6	4.0	6.0
10	6.5	4.0	6.0
7.5	6.4	4.0	5.0
5	6.5	2.0	3.0
2.5	6.5	2.0	3.0

Statistical Analysis: During the design of any experiment, the process parameters need systematic evaluation and analysis to get a proper outcome. To observe the significance of different parameters, a statistical analysis of the parameters was performed using Design-Exert Version 12 ®. In this investigation, five factors were taken into account concerning the minimum feature size in a pattern with 32 distinct samples. A 2^k factorial design was used for the analysis as shown in figure 4.5. The analysis was done with 32 different samples with different feature sizes of 10, 7.5, 5 and 2.5 μm in the pattern. Where 'Y' was the response variable i.e. the minimum feature size patterned in each sample. All 5 process parameters were altered and analyzed by 2^k factorial design method (k = 5), where k is the number of parameters.

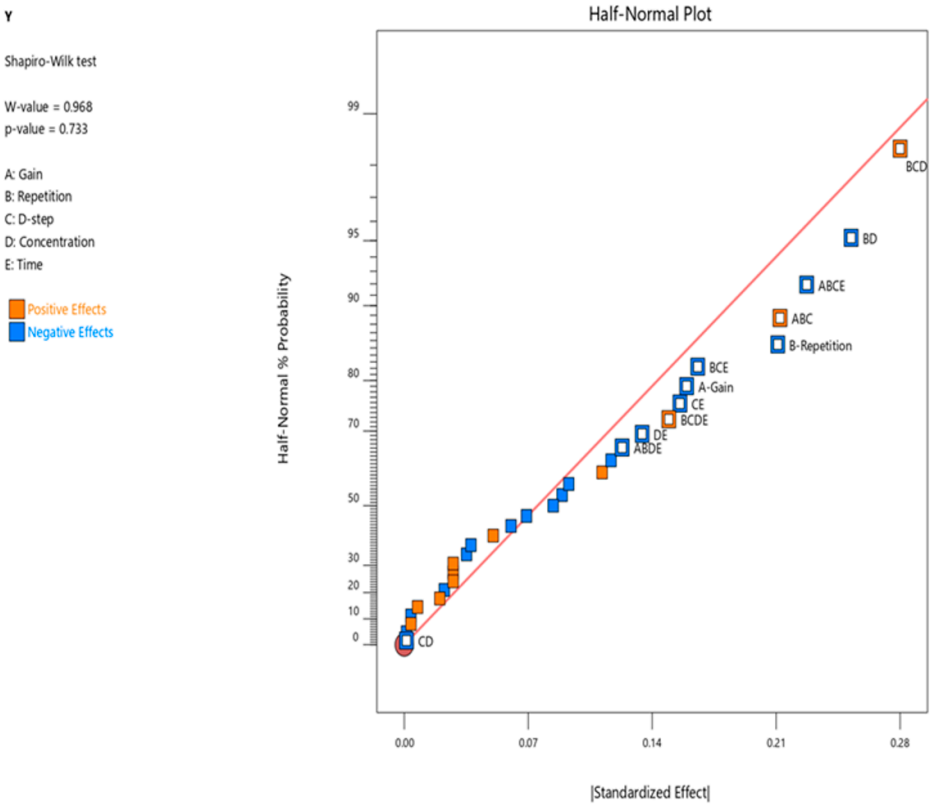


Figure 4.5: Parameter Optimization using the statistical analysis by the software Design-Exert ®Version12.

	Subtractive	m-SAP	am-SAP	Fully additive (SBU-CBM)
Cu clad thickness (µm)	2-9	2-5	< 3	**None**
Eless Cu thickness (µm)	0.35-0.5	0.35-0.5	1	**0.5-3**
Flash Cu thickness (µm)	2-5	1-3	----	**None**
Panel plating thickness (µm)	15-20	----	----	**No**
Pattern plating required	No	Yes	Yes	**Yes**
Etch resist	Dry film or LER	----		**No**
Cu to be etched (µm)	17-29	4-10	< 3	**None**
Achievable L/S (µm)	> 35	> 30	> 20	**2.5/2.65**
µVia Diameter (µm)	70	50	40	**10**

Figure 4.6: Experimental outcomes of the SBU-CBM method mapped to the other industrial production approaches

4.6 Result Mapping to the Roadmaps

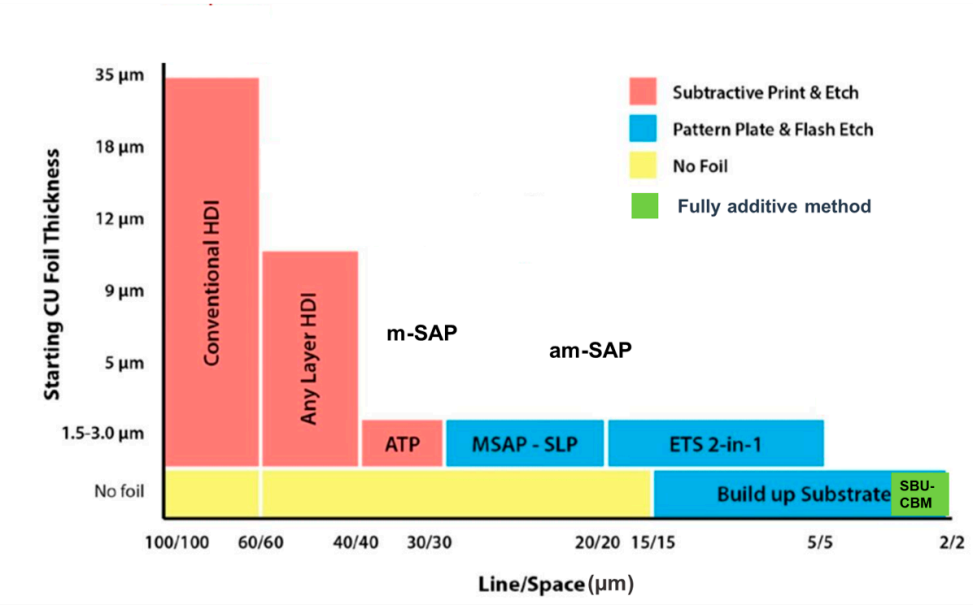


Figure 4.7: Positioning of the SBU-CBM method in existing production practices at board-level.

As mentioned in chapter 2, the current requirements of the international roadmap is to build multi-functional system boards. To achieve that a new production approach has been demonstrated in this thesis. The obtained experimental outcomes using the proposed SBU-CBM method are mapped to the roadmap shown in figure 2.2 and presented in figure 4.6. There is no etching steps involved in the proposed technique. Similarly in figure 4.7, an overview of the SBU-CBM method in the existing industrial manufacturing practices is shown.

Chapter 5

Summary of Contributions

The appended publications are presented in chronological order. This section presents a summary of the papers and the contributions made by the author.

5.1 Summary of Appended Papers

Paper A: Scalability of Copper-Interconnects down to 3μm on Printed Boards by Laser-assisted-subtractive process.
Authors: Sarthak Acharya, Shailesh Singh Chouhan, Jerker Delsing.
Published in: IEEE Nordic Conference on Microelectronics Packaging (IMAPs-NordPac), 2019.
Summary: This paper shows a cost-efficient way to use laser-assisted writing and wet chemical etching to achieve the lowest possible line resolution on a conventional photo-sensitive material-coated PCB. The existing board-level lines and spaces dimensions are around 20μm and the achieved feature size in this paper is 3μm. This technique contributes to the achievement of metallic connecting lines on PCBs, which are decreased by 70%.

Contribution: The author has conceptualised the work, performed the experiment, analysed the results and wrote the paper.

Paper B: Realization of Embedded Passives using an additive Covalent bonded metallization approach.
Authors: Sarthak Acharya, Shailesh Singh Chouhan, Jerker Delsing.
Published in: The 22nd IEEE European Microelectronics and Packaging Conference (IMAPs-EMPC), 2019.
Summary: This paper has focused on developing a new cost-efficient fabrication method for realization of embedded passives using an additive Laser assisted production method.

Electrical characterization of the embedded passives was done.

Contribution: The author performed the study concerning the embedded passives, and designed the experiments. In addition, the author analysed the results and wrote the paper.

Paper C: An Additive Production approach for Microvias and Multilayered polymer substrate patterning of 2.5μm feature sizes
Authors: Sarthak Acharya, Shailesh Singh Chouhan, Jerker Delsing.
Published in: The 70$^{\text{th}}$ IEEE Electronic Components and Technology Conference (IMAPs-ECTC), 2020.
Summary: This paper presents the scalability potential of the proposed production technique. The L&S of 2.5/2.65 μm and microvias of 10 μm, were obtained with this technique, which is meeting the expectations of the roadmap.Therefore, this fully additive production approach has all the potential to become a standardized solution for WLPs.

Contribution: The author has done the state-of-the-art literature review and performed the experiment accordingly. The author is also responsible for analysis of the results and writing of the paper.

Paper D: Fabrication Process for On-Board Geometries Using a Polymer Composite-Based Selective Metallization for Next-Generation Electronics Packaging.
Authors: Sarthak Acharya, Shailesh Singh Chouhan, Jerker Delsing.
Published in: Recent Advances in Printed Electronics and Flexible Electronics: Materials and Applications, Processes journal, MDPI, 2021.
Summary: This paper presents the usage of the fully additive fabrication technique by creating different geometries using exopy resins and polymer-based CBM technology, generally used in electronics packaging. Selective metallisation with optimisation of process parameters were discussed.

Contribution: The author has conceptualised and designed the experiments. The author performed the experiments, analysed the data and wrote the paper.

Paper E: Detailed Characterization of a Fully-Additive Covalent Bonded PCB Manufacturing Process (SBU-CBM Method).
Authors: Sarthak Acharya, Shahid sattar, Shailesh Singh Chouhan, Jerker Delsing.
Published in: Submitted for publication in Recent Advances in Printed Electronics and Flexible Electronics: Materials and Applications, Processes journal, MDPI, 2021.
Summary: This paper demonstrates the fabrication steps in detail, involved in the

SBU-CBM technique. The surface mechanism at the interfaces were outlined. It combines the analysis from experimental and simulation results of the fabrication steps for further optimisation of the process parameters.

Contribution: The author in collaboration with the other authors discussed and designed the experiments. The author investigated different characterisations for revealing the surface modification phenomena, and wrote the paper.

Chapter 6

Conclusions and Future Work

This thesis presents the results related to an additive production approach for board-level manufacturing. The experimental outcomes using the proposed fully additive recipe were outlined. Various material characterization techniques were used to explore the surface mechanism involved.

The next section summarizes the research contributions and conclusions in addition to the future research directions.

6.1 Conclusions

In terms of this licentiate thesis, the primary contribution of this study is to identify state-of-the-art production gaps, provide a completely additive metallisation approach, and lastly demonstrate the potential of the process for its acceptance in industrial manufacturing techniques to effectively answer future requirements of the electronics packaging roadmap.

The research questions of this thesis were answered based on the obtained experimental data and published contributions as follows:

Q1 *What feature sized Cu interconnects are possible through different board-level fabrication methods?*

The results of the scaling of Cu interconnects are demonstrated in the thesis using both the subtractive and additive methods. In Paper A, a cost-effective laser aided subtractive process is shown, and copper interconnects with feature sizes of 3.0 μm have been accomplished at the board-level, corresponding to a 70% decrease in the present feature sizes Whereas in paper C, Cu interconnects using a fully additive technique is investigated.

Q2 *How will be a fully additive method for selective metallisation at the board-level and what will the state-of-the-art contribution of such approach?*

The thesis has demonstrated the fabrication recipe for a fully additive board-level manufacturing technique. Selective metallisation is shown in paper C for fabricating Cu interconnects. In paper B and paper D, the embedded passives and fabrication of desirable geometries were illustrated. In paper E, a detailed mechanism of the surface phenomena involved in the production stages was shown. In this thesis, HP-14 was employed as a CBM solution in the experiments, and optimized process parameters (for HP-14) were established.

In conclusion, Cu interconnects of L&S of 2.5/2.65 μm and micro vias of 10 μm, were obtained using a two-dimensional (2D) fully additive technique, which is meeting the expectations of future roadmap. A brief summary of the contribution is shown in figure 6.1.

	Paper-A	**Paper-B**	**Paper-C**	**Paper-D**	**Paper-E**
RQ-1	Cu interconnects of 3.0 µm have been demonstrated.		Cu L&S of 2.5/2.65 µm and micro vias of 10 µm, were obtained using a fully additive technique.		
RQ-2		Embedded Passives	Selective Metallization	• Fabrication of geometries. • Embedded passives.	Detailed Surface mechanism of the SBU-CBM Method.

Figure 6.1: Summary of the Contributions in this Thesis.

6.2 Future Work

Possible future extension of this work will focus on the followings:

Investigation on further scaling of Cu interconnects and metallisation of microvias: The proposed technique has the potential of further scaling down the dimensions of the lines/spaces (L/S) and microvias, at the board-level. This may be accomplished by utilizing different epoxy resins and CBM solutions. In epoxy resin, polyamide can be a good alternative. The composition change in electroless baths could be another critical factor for scaling as observed during the experiments. The fabrication recipe, on the other hand, will be the same and could be used for any different chemistry (epoxy materials and CBM solutions). The future work also be focused on metalising the vias and their electrical characterizations.

Reliability assessment of the production approach: The reliability evaluations of the samples (produced by the proposed approach) are crucial for analyzing the stability of the metallisation for its applications. Based on literature, tests such as thermal cycle testing, high-temperature humidity tests, highly accelerated stress tests (HAST), and bending tests are recommended. Different test structures are required to carry out these tests, which can be accomplished using the proposed fabrication recipe.

Electrical characterizations of the process: Similarly, electrical tests are also essential to examine the performance of the metallisation. To measure the electrical data, investigations such as sheet resistance, leakage current, evaluation of embedded passives, and radio-frequency tests (RF) are suggested in studies.

Realisation of a 2.5D structure combining the horizontal patterning with metal filled vias A 2D patterning was presented in this thesis. The next goal must be to connect two (or more) metallic layers via conductive vias. As a result, the board will have a 2.5D structure to support the high density interconnects (HDIs). In addition, embedded passives and other discrete components on top & bottom layer can be added to realise heterogeneous integration using the SBU-CBM technique.

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