

Spatiotemporal Spike-Pattern Selectivity in Single Mixed-Signal Neurons with Balanced Synapses

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Abstract—Realizing the potential of mixed-signal neuromorphic processors for ultra-low-power inference and learning requires efficient use of their inhomogeneous analog circuitry as well as sparse, time-based information encoding and processing. Here, we investigate spike-timing-based spatiotemporal receptive fields of output-neurons in the Spatiotemporal Correlator (STC) network, for which we used excitatory–inhibitory balanced disynaptic inputs instead of dedicated axonal or neuronal delays. We present hardware-in-the-loop experiments with a mixed-signal DYNAP-SE neuromorphic processor, in which five-dimensional receptive fields of hardware neurons were mapped by randomly sampling input spike-patterns from a uniform distribution. We find that, when the balanced disynaptic elements are randomly programmed, some of the neurons display distinct receptive fields. Furthermore, we demonstrate how a neuron was tuned to detect a particular spatiotemporal feature, to which it initially was non-selective, by activating a different subset of the inhomogeneous analog synaptic circuits. The energy dissipation of the balanced synaptic elements is one order of magnitude lower per lateral connection (0.65 nJ vs 9.3 nJ per spike) than former delay-based neuromorphic hardware implementations. Thus, we show how the inhomogeneous synaptic circuits could be utilized for resource-efficient implementation of STC network layers, in a way that enables synapse-address reprogramming as a discrete mechanism for feature tuning.

Index Terms—Neuromorphic, Spatiotemporal, Spike timing, Excitatory–inhibitory balance, Ultra-low-power

I. INTRODUCTION

Neuromorphic Engineering [1], [2] deals with creating physical substrates for information processing and sensing by imitating mechanisms and structures observed in the brain. Following that approach, mixed-signal neuromorphic processors emulate the biophysical dynamics of neurons and synapses [3] in event-driven Spiking Neural Networks (SNNs) and have high potential for ultra-low-power pattern recognition and learning [4]—for instance close to sensors, such as in wearable biomedical devices [5]. However, such mixed-signal systems are subject to device mismatch in the analog nanoscale circuits, resulting in distributions of inhomogeneous neuronal and synaptic dynamics, which need to be utilized appropriately for SNN implementations to be efficient. Furthermore, the dynamic real-time operation of the neuronal–synaptic computational elements of these processing systems needs to be employed in a way that results in sparse temporal processing of information [6] with spike-time based encoding [7]–[10].

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Learning and recognition of spatiotemporal patterns—in contrast to static spatial patterns, or even sequences of such—is a central conceptual problem to neuromorphic and event-based processing [11], and has been addressed, for instance, with SNNs that incorporate neural signal-propagation delays [11]–[15]. Some current approaches to spatiotemporal pattern recognition with inhomogeneous neuromorphic hardware use neural processing frameworks that actually *rely* on variability in the processing elements [13], [16]–[21]—such as reservoir computing, liquid state machines, and ensemble learning. Another relevant concept is that of the Spiking Time-Difference Encoder (sTDE) [22], which provides a general neurocomputational primitive for temporal encoding but requires specialized hardware for its implementation.

In addition to neuromorphic hardware design, biological nervous systems can provide inspiration for architectural principles for efficient neural processing [23]. One biologically inspired SNN for spatiotemporal pattern recognition and learning in neuromorphic hardware is the Spatiotemporal Correlator (STC) neural network, which was derived from a biophysically plausible model of thalamocortical auditory processing [24] and implemented in real-time mixed-signal neuromorphic hardware [13], [25]. The robustness of the STC to variability in stimulus patterns was further demonstrated in [26], which is a prerequisite of most real-world sensing applications.

Here, we investigate spike-timing-based spatiotemporal pattern recognition with inhomogeneous, low-power neuromorphic hardware. To that end, we selected the STC neural network as a starting point based on its relative simplicity and intelligibility, compatibility with general-purpose neuromorphic hardware, and potential to form layers in deep SNNs for processing of increasingly complex spatiotemporal patterns. We propose a modified STC network—the Synaptic Spatiotemporal Correlator (sSTC)—which uses Excitatory–Inhibitory (E–I) balanced disynaptic delay elements [15] as a less resource-intensive alternative to the dedicated delay neurons of the original model [13], and hardware emulation of dendritic dynamics [27], [28].

To investigate the feasibility and effectiveness of implementing the sSTC in mixed-signal neuromorphic hardware, we characterize the spike-timing-based spatiotemporal receptive fields that form in its feature-detection neurons when implemented in a DYNAP-SE neuromorphic processor [29].

Furthermore, we investigate how such a feature-detection neuron can be tuned to a specific, prescribed spatiotemporal spike pattern by using synapse-address reprogramming and the inherent synapse efficacy distributions. Finally, we present an estimate of the difference in power requirement for hardware implementations of the sSTC and STC neural networks.

In summary, we present how inhomogeneous synaptic dynamics in neuromorphic processors like the DYNAP-SE can be efficiently used for spatiotemporal pattern recognition, in a way that enables synapse-address reprogramming as a discrete mechanism for feature tuning. This approach may serve as a complement to more accurate but resource-intensive delay-based coincidence detection or dendritic integration.

II. MATERIALS AND METHODS

The experiments presented in this work were conducted with a DYNAP-SE—a Dynamic Neuromorphic Asynchronous Processor (DYNAP) [29] from SynSense¹—in a closed loop with a PC, interfaced using the software *Legacy Samna*² (formerly *ctxctl*). All input stimuli were generated using the built-in spike-generator in the Field-Programmable Gate Array (FPGA) of the DYNAP-SE, which generates spike-events according to assigned temporal Interspike Intervals (ISIs) and virtual source-neuron addresses.

A. Neuromorphic Processor

The DYNAP-SE is a reconfigurable, general-purpose, mixed-signal SNN processor, which uses subthreshold analog circuits to emulate the biophysical dynamics of neurons and synapses in real time, and asynchronous digital circuits for spike-event transmission according to the Address-Event Representation (AER) protocol. One DYNAP-SE unit comprises four four-core neuromorphic chips—each of which comprises 256 Adaptive Exponential Integrate-and-Fire (AdEx) [30] neuron-circuits. Each neuron has a Content-Addressable Memory (CAM) block that can contain up to 64 different addresses, each representing a presynaptic neuronal connection³—see **Fig. 1**. For each connection, dynamic synapses in the form of Differential Pair Integrator (DPI) circuits [31] are available in four different synaptic types: fast and slow excitatory, and subtractive and shunting inhibitory. The dynamic behaviors of the neuronal and synaptic circuits of the DYNAP-SE are governed by analog circuit parameters that are set by on-chip programmable bias generators, which provide 25 bias parameters independently for each core.

B. Spiking Neural Network Architecture

The Spatiotemporal Correlator (STC) neural network—originally proposed in [13] and further described in [25]—is a Spiking Neural Network (SNN) for spatiotemporal pattern recognition and learning that builds on the mechanism

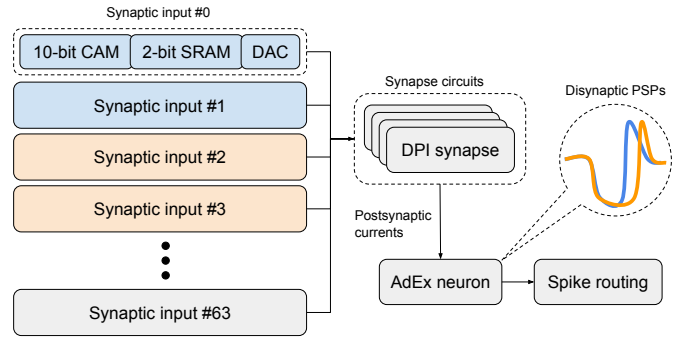


Fig. 1: Neuronal-synaptic mixed-signal computational node of the DYNAP-SE neuromorphic processor, adapted and simplified from [29]. Each node contains 64 mixed-signal synapses—with a CAM cell for the presynaptic neuron address, an SRAM cell for the synapse-type information, and digital-to-analog signal-converting circuitry (DAC)—four analog synaptic DPI circuits of different types, and one analog AdEx-neuron circuit. The coloring indicates the use of two synaptic inputs for each excitatory-inhibitory disynaptic delay element, with an illustrated example of the resulting inhomogeneous postsynaptic potentials (PSPs).

of coincidence detection of temporally delayed, lateral neuronal projections. The original network design (**Fig. 2A**) consists of the following qualitative neuronal populations:

- **A**: Input neurons
- **B1**: Secondary input neurons
- **B2**: Coincidence-detection neurons
- **C**: Delay neurons

The STC network is structured in columns—not to be confused with cortical columns—each of which consists of one A, B1, and B2 neuron. Within each column, the input neuron, A, receives a signal from an input channel—for instance spatial or spectral—which it then projects to both the B1 and B2 neurons via excitatory synapses. B1 then generates a one-to-one mapping of its input from A, which is projected by inhibition to the B2 neuron of the same column, and by excitation to the B2 neurons of some number of adjacent columns. Each lateral B1-B2 excitation is projected via a neuron from the C population, thereby inducing a temporal signal-propagation delay. The A-B2 excitation is slightly faster than the B1-B2 inhibition, thus creating a time-window during which B2 is primed to spike in response to coincident lateral projections from adjacent columns. Hence, each B2 neuron constitutes a coincidence detector sensitive to some particular set of spatiotemporal spike-patterns in a local receptive region, which forms a subfeature of the pattern recognized by the STC network as a whole.

1) *The Synaptic STC Neural Network*: Here, we propose a modified version of the STC—the Synaptic Spatiotemporal Correlator (sSTC) (**Fig. 2B**). In the sSTC, the delay neurons of the STC are replaced with E-I balanced disynaptic delay elements [15]—thereby, in principle, substantially reducing the amount of resources required to implement the network. In the sSTC architecture, the differences in temporal delay of the different lateral connections to one B2 neuron arise from the internal inhomogeneity of the synaptic circuitry—see

¹<https://www.synsense-neuromorphic.com/technology>

²<https://pypi.org/project/samna/>

³Each CAM address can match the same local neuron-ID on different cores, enabling multiple presynaptic connections per input circuit.

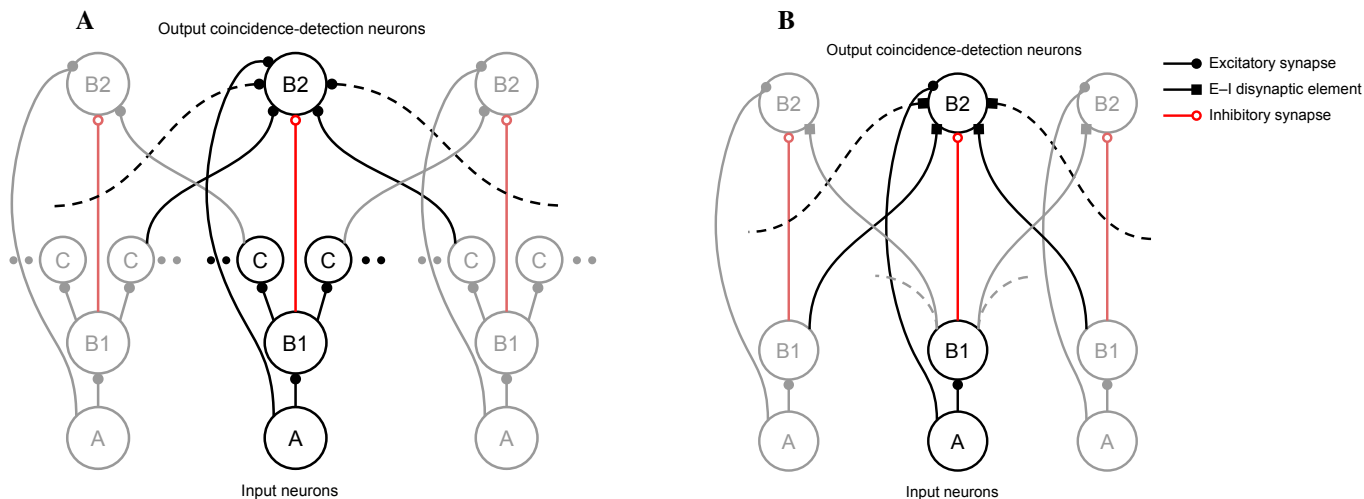


Fig. 2: **Spatiotemporal Correlator (STC) neural network architectures.** For each architecture, one column is highlighted, and the two closest neighboring columns within the layer are included shaded to illustrate lateral connections. Circles represent single neurons from populations A, B1, B2, and C. **A:** Original STC network, adapted from [25]. **B:** Synaptic STC (sSTC) network, which uses excitatory–inhibitory (E–I) disynaptic delay elements [15], [20].

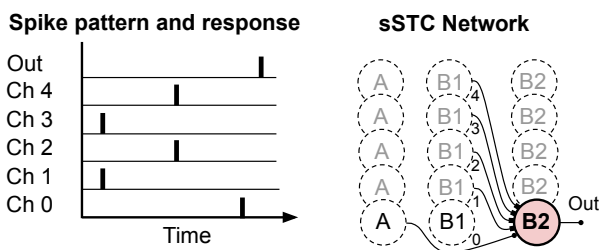


Fig. 3: **Experimentally investigated feature-detection neurons of the Synaptic Spatiotemporal Correlator network and an example spike-pattern.** The B2 neurons are stimulated with spatiotemporal spike patterns on five input channels, of which four channels (Chs 1–4) are lateral, delayed connections via balanced disynaptic elements.

Fig. 1. This gives rise to partially random, device-mismatch dependent spatiotemporal subfeatures—or receptive fields—to which each B2 neuron is sensitive. In this manner, the sSTC performs coincidence-based spatiotemporal feature detection by synaptic integration as described in [20].

We investigated such receptive fields of B2 neurons having four lateral connections each (see **Fig. 3**)—similar to the original STC [13] after training—by implementing a population of B2 neurons in one core of the DYNAP-SE neuromorphic processor. We focused on the forward and lateral connections and omitted the B1–B2 inhibition, since its function is to regulate spike-timing-dependent plasticity and to prevent sensitivity to excessive stimulation, and is therefore not required to investigate the receptive fields.

C. Mapping of Receptive Fields

The spatiotemporal receptive fields were mapped by stimulating a population of B2 neurons—independently from each other—with randomized spike-patterns ($N = 10,000$), each consisting of one spike per input channel, as illustrated by the sample pattern in **Fig. 3**. The spike-times of each of the lateral, delayed projections were independently drawn from a uniform

TABLE I: **DYNAP-SE circuit IDs used to obtain the different receptive fields.** The neuron IDs are local to the processor core, and the input-circuit IDs are local to each neuron. The input-circuit IDs used for each disynaptic connection are grouped inside parentheses.

Receptive field	Neuron ID $\in [0,255]$	Input-circuit IDs $\in [0,63]$
Fig. 4A	74	0–8
Fig. 4B	129	0–8
Fig. 4C	222	0–8
Fig. 4D	248	0–8
Fig. 5B	248	56, (2, 30), (54, 15), (46, 6), (4, 51)
Fig. 5C	248	24, (25, 2), (45, 42), (28, 57), (16, 50)

random distribution ranging from 1–50 ms before the direct forward excitation from A to B2, which defines the reference time ($t = 0$) of the pattern. All spike-patterns for which a given B2 neuron generated one or more postsynaptic spikes in response were accumulated to approximate the receptive field of that neuron.

D. Feature Tuning by Synapse Sampling

Based on the results in [20], we further investigated whether replacing the specific input circuits—see **Fig. 1**—used for each synaptic connection of a B2 neuron could affect the coincidence detection enough to make the neuron distinguish between two different prescribed patterns (**Fig. 5A**), which the neuron initially could not. The synaptic reconfigurations were made by assigning to each of the synapses a random, unique input circuit drawn from the set of all the 64 input circuits of the neuron. Following each subsequent synaptic reconfiguration, the neuron was presented with both of the different patterns, separately, ten times—and its response in terms of the number of postsynaptic spikes was recorded.

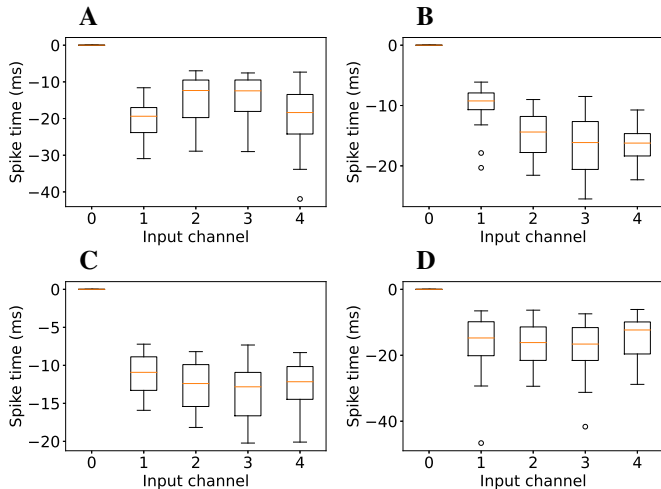


Fig. 4: **Spatiotemporal receptive fields of four different coincidence detecting B2 neurons**, sampled with random stimuli ($N = 10,000$). Each B2 neuron has a feed-forward input (Channel 0) at reference-time $t = 0$, and four lateral inputs (Channels 1–4) that are stimulated with spikes at random points in time. Boxes extend from lower to upper quartiles, with lines at median presynaptic spike times. Whiskers and flier points denote the range of data.

III. RESULTS

A. Receptive Fields

Fig. 4 illustrates the receptive fields of four different B2 neurons, in the form of box plots, accumulated from presynaptic stimulation with different randomized input patterns ($N = 10,000$). The box plots consists of all the stimulus patterns—that is, channel–spike-time combinations—that made the B2 neuron in question generate at least one spike in response. **Table I** presents the hardware neuron IDs—local to the DYNAP-SE core used—for which the receptive fields in **Fig. 4** were observed.

B. Feature Tuning

The B2 neuron with the receptive field of **Fig. 4D** was successfully reconfigured by input-circuit sampling to distinguish between Pattern A and Pattern B in **Fig. 5A** with a spiking and non-spiking response, respectively. Prior to reconfiguration, the receptive field was fairly uniform, with the inputs on Channels 1–4 being practically interchangeable. This feature tuning was accomplished by randomly replacing the input circuits used for the presynaptic connections—see **Table I**. Out of 200 randomized configurations, four resulted in accurate discrimination between the two patterns. **Fig. 5B–C** shows the receptive fields of two of these configurations.

C. Energy Usage

Based on Table III in [29], which presents the energy dissipation for the main operations of a DYNAP-SE neuromorphic processor, we present an estimate of the energy usage per laterally projected spike-event in **Table II**, suggesting an improvement of one order of magnitude for the sSTC model—from 9.3 nJ to 0.65 nJ.

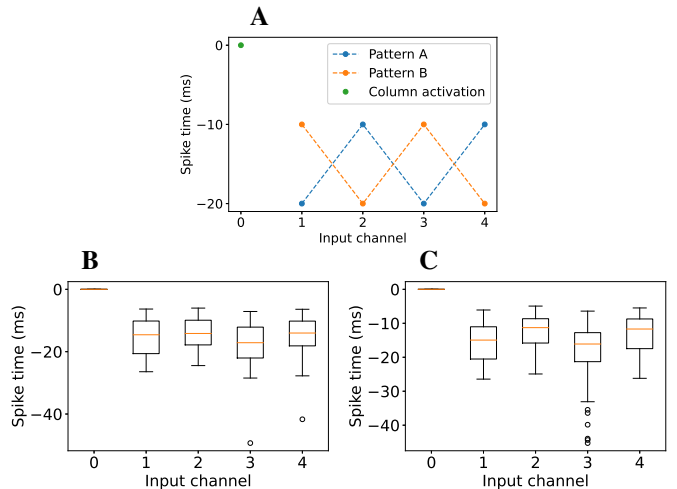


Fig. 5: **Feature tuning by synapse sampling**. **A**: Spatiotemporal stimulus spike-patterns. Each pattern consists of one spike per input channel, including the feed-forward input at reference time $t = 0$, resulting in five spikes per pattern. **B–C**: Receptive fields of successfully pattern-detecting synapse configurations.

IV. DISCUSSION

We have investigated spike-timing-based spatiotemporal receptive fields of single mixed-signal spiking neurons utilizing inhomogeneous synaptic dynamics [31] in the DYNAP-SE neuromorphic processor, and the possibility of feature tuning of such receptive fields. The neurons were configured with a particular kind of excitatory–inhibitory balanced synaptic dynamics [15], [20] and four lateral connections per neuron, like for example the neurons in the output layer of an STC network [13], [25].

In contrast to the former work on STC networks, no neuronal or axonal delays are required since the dynamics of the postsynaptic currents contribute, in effect, a delayed excitation that is unique and tunable for each lateral input connection. Comparison with an STC network with dedicated delay neurons, as in [13], shows a reduction of energy usage per lateral connection by about one order of magnitude—see **Table II**. In fact, the original implementation of the STC used *three* multiple synapses per lateral, delayed B2-input, to mitigate device mismatch with redundancy—but the energy estimate presented here is conservative and made for the ideal

TABLE II: **Energy usage per laterally projected spike-event**, based on energy measures for the DYNAP-SE, from Table III in [29].

SNN model	Hardware operation	Count	Energy
STC	Synaptic pulse extension	1	324 pJ
	Spike generation	1	883 pJ
	Spike encoding	1	883 pJ
	Intercore spike-routing	1	360 pJ
	Intracore spike-routing	1	6.84 nJ
	Sum		9.3 nJ
sSTC	Synaptic pulse extension	2	324 pJ
	Sum		0.65 nJ

case of one synapse per STC connection.

The improved energy efficiency of the sSTC does, however, come at the cost of the relatively broadly tuned receptive fields of the output neurons, see **Fig. 4**. This is a trade-off that could be motivated for example in a deep neural network of stacked STC layers with high fan-in on the B2 neurons. Also, the temporal width of the receptive fields is comparable to that of a coincidence-detection based feature detection circuit found in crickets [32], which originally inspired the disynaptic delays [15] used in the present work. Furthermore, during the experiments, we observed some irregularities in the results, such as widening or narrowing of the receptive fields. This variability is likely due to temperature effects [33] and may, for instance, be addressed with novel nanomaterials in future generations of neuromorphic hardware [34].

To conclude, we have demonstrated how inhomogeneous synaptic dynamics in mixed-signal neuromorphic processors, like the DYNAP-SE, can offer efficient mechanisms for spatiotemporal pattern recognition as a complement to more resource-intensive delay-based coincidence detection networks, and biologically more plausible but resource-intensive models of dendritic integration [27], [28].

REFERENCES

- [1] C. Mead, "How we created Neuromorphic Engineering," *Nature Electronics*, vol. 3, no. 7, pp. 434–435, 2020.
- [2] G. Indiveri and T. Horiuchi, "Frontiers in Neuromorphic Engineering," *Frontiers in Neuroscience*, vol. 5, p. 118, 2011.
- [3] E. Chicca, F. Stefanini, C. Bartolozzi, and G. Indiveri, "Neuromorphic electronic circuits for building autonomous cognitive systems," *Proceedings of the IEEE*, vol. 102, no. 9, pp. 1367–1388, 2014.
- [4] B. Rajendran, A. Sebastian, M. Schmuker, N. Srinivasa, and E. Eleftheriou, "Low-power neuromorphic hardware for signal processing applications: A review of architectural and system-level design approaches," *IEEE Signal Processing Magazine*, vol. 36, no. 6, pp. 97–110, 2019.
- [5] E. Covi, E. Donati, X. Liang, D. Kappel, H. Heidari, M. Payvand, and W. Wang, "Adaptive extreme edge computing for wearable devices," *Frontiers in Neuroscience*, vol. 15, p. 429, 2021.
- [6] G. Indiveri and Y. Sandamirskaya, "The importance of space and time for signal processing in neuromorphic agents: The challenge of developing low-power, autonomous agents that interact with the environment," *IEEE Signal Processing Magazine*, vol. 36, no. 6, pp. 16–28, 2019.
- [7] R. VanRullen, R. Guyonnet, and S. J. Thorpe, "Spike times make sense," *Trends in Neurosciences*, vol. 28, no. 1, pp. 1–4, 2005.
- [8] W. Guo, M. E. Fouda, A. M. Eltawil, and K. N. Salama, "Neural coding in spiking neural networks: A comparative study for robust neuromorphic systems," *Frontiers in Neuroscience*, vol. 15, p. 212, 2021.
- [9] S. Davidson and S. B. Furber, "Comparison of artificial and spiking neural networks on digital hardware," *Frontiers in Neuroscience*, vol. 15, p. 345, 2021.
- [10] C. Stöckl and W. Maass, "Optimized spiking neurons can classify images with high accuracy through temporal coding with two spikes," *Nature Machine Intelligence*, pp. 1–9, 2021.
- [11] G. Haessig, M. B. Milde, P. V. Aceituno, O. Oubari, J. C. Knight, A. van Schaik, R. B. Benosman, and G. Indiveri, "Event-based computation for touch localization based on precise spike timing," *Frontiers in Neuroscience*, vol. 14, p. 420, 2020.
- [12] H. Agmon-Snir and I. Segev, "Signal delay and input synchronization in passive dendritic structures," *Journal of Neurophysiology*, vol. 70, no. 5, pp. 2066–2085, 1993, pMID: 8294970.
- [13] S. Sheik, M. Coath, G. Indiveri, S. Denham, T. Wennekers, and E. Chicca, "Emergent auditory feature tuning in a real-time neuromorphic VLSI system," *Frontiers in Neuroscience*, vol. 6, p. 17, 2012.
- [14] C. Nielsen, N. Qiao, and G. Indiveri, "A compact ultra low-power pulse delay and extension circuit for neuromorphic processors," in *2017 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, 2017, pp. 1–4.
- [15] F. Sandin and M. Nilsson, "Synaptic delays for insect-inspired temporal feature detection in dynamic neuromorphic processors," *Frontiers in Neuroscience*, vol. 14, p. 150, 2020.
- [16] O. Richter, R. F. Reinhart, S. Nease, J. Steil, and E. Chicca, "Device mismatch in a neuromorphic system implements random features for regression," in *2015 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, 2015, pp. 1–4.
- [17] A. Das, P. Pradhapan, W. Groenendaal, P. Adiraju, R. T. Rajan, F. Catthoor, S. Schaafsma, J. L. Krichmar, N. Dutt, and C. V. Hoof, "Unsupervised heart-rate estimation in wearables with liquid states and a probabilistic readout," *Neural Networks*, vol. 99, pp. 134–147, 2018.
- [18] F. C. Bauer, D. R. Muir, and G. Indiveri, "Real-time ultra-low power ECG anomaly detection using an event-driven neuromorphic processor," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 13, no. 6, pp. 1575–1582, 2019.
- [19] E. Donati, M. Payvand, N. Risi, R. Krause, and G. Indiveri, "Discrimination of EMG signals using a neuromorphic implementation of a spiking neural network," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 13, no. 5, pp. 795–803, Oct 2019.
- [20] M. Nilsson, F. Liwicki, and F. Sandin, "Synaptic integration of spatiotemporal features with a dynamic neuromorphic processor," in *2020 International Joint Conference on Neural Networks (IJCNN)*, 2020, pp. 1–7.
- [21] M. Sharifshazileh, K. Burelo, J. Sarnthein, and G. Indiveri, "An electronic neuromorphic system for real-time detection of high frequency oscillations (HFO) in intracranial EEG," *Nature Communications*, vol. 12, no. 1, p. 3095, May 2021.
- [22] M. B. Milde, O. J. N. Bertrand, H. Ramachandran, M. Egelhaaf, and E. Chicca, "Spiking elementary motion detector in neuromorphic systems," *Neural Computation*, vol. 30, no. 9, pp. 2384–2417, 2018, pMID: 30021082.
- [23] T. Dalgaty, J. P. Miller, E. Vianello, and J. Casas, "Bio-inspired architectures substantially reduce the memory requirements of neural network models," *Frontiers in Neuroscience*, vol. 15, p. 156, 2021.
- [24] M. Coath, R. Mill, S. L. Denham, and T. Wennekers, "Emergent feature sensitivity in a model of the auditory thalamocortical system," in *From Brains to Systems*, C. Hernández, R. Sanz, J. Gómez-Ramírez, L. S. Smith, A. Hussain, A. Chella, and I. Aleksander, Eds. New York, NY: Springer New York, 2011, pp. 7–17.
- [25] S. u. A. Sheik, "Autonomous learning in neuromorphic systems for recognition of spatio-temporal spike patterns," Ph.D. dissertation, ETH Zurich, Zürich, 2013, diss., Eidgenössische Technische Hochschule ETH Zürich, Nr. 21425, 2013.
- [26] M. Coath, S. Sheik, E. Chicca, G. Indiveri, S. Denham, and T. Wennekers, "A robust sound perception model suitable for neuromorphic implementation," *Frontiers in Neuroscience*, vol. 7, p. 278, 2014.
- [27] Y. Wang and S.-C. Liu, "Active processing of spatio-temporal input patterns in silicon dendrites," *IEEE transactions on biomedical circuits and systems*, vol. 7, no. 3, pp. 307–318, 2012.
- [28] J. Schemmel, L. Kriener, P. Müller, and K. Meier, "An accelerated analog neuromorphic hardware system emulating NMDA-and calcium-based non-linear dendrites," in *2017 International Joint Conference on Neural Networks (IJCNN)*. IEEE, 2017, pp. 2217–2226.
- [29] S. Moradi, N. Qiao, F. Stefanini, and G. Indiveri, "A scalable multicore architecture with heterogeneous memory structures for Dynamic Neuromorphic Asynchronous Processors (DYNAPs)," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 12, no. 1, pp. 106–122, 2018.
- [30] R. Brette and W. Gerstner, "Adaptive exponential integrate-and-fire model as an effective description of neuronal activity," *Journal of Neurophysiology*, vol. 94, no. 5, pp. 3637–3642, 2005, pMID: 16014787.
- [31] C. Bartolozzi and G. Indiveri, "Synaptic dynamics in analog VLSI," *Neural Computation*, vol. 19, no. 10, pp. 2581–2603, 2007, pMID: 17716003.
- [32] S. Schöneich, K. Kostarakos, and B. Hedwig, "An auditory feature detection circuit for sound pattern recognition," *Science Advances*, vol. 1, no. 8, 2015.
- [33] S. Song, J. Hanamshet, A. Balaji, A. Das, J. L. Krichmar, N. D. Dutt, N. Kandasamy, and F. Catthoor, "Dynamic reliability management in neuromorphic computing," 2021.
- [34] D. V. Christensen, R. Dittmann, B. Linares-Barranco, A. Sebastian, M. L. Gallo, A. Redaelli, S. Slesazek, T. Mikolajick, S. Spiga, S. Menzel *et al.*, "2021 roadmap on Neuromorphic Computing and Engineering," *arXiv preprint arXiv:2105.05956*, 2021.