KTH ROYAL INSTITUTE
OF TECHNOLOGY

Doctoral Thesis in Electronics

Germanium layer transfer and device fabrication for monolithic 3D integration

AHMAD ABEDIN

Stockholm, Sweden 2021

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Academic Dissertation which, with due permission of the KTH Royal Institute of Technology, is submitted for public defence for the Degree of Doctor of Philosophy on Friday the 21st May 2021, at 1:00 p.m. in Sal C, Kistagången 16, Stockholm, Sweden.

Doctoral Thesis in Electronics
KTH Royal Institute of Technology
Stockholm, Sweden 2021

ISBN 978-91-7873-834-2
TRITA-EECS-AVL-2021:23

Printed by: Universitetsservice US-AB, Sweden 2021

Abstract

Monolithic three-dimensional (M3D) integration, it has been proposed, can overcome the limitations of further circuits' performance improvement and functionality expansion. The emergence of the internet of things (IoT) is driving the semiconductor industry toward the fabrication of higher-performance circuits with diverse functionality. On the one hand, the scaling of devices is reaching critical dimensions, which makes their further downscaling technologically difficult and economically challenging, whereas, on the other hand, the field of electronics is no longer limited only to developing circuits that are meant for data processing. Sensors, processors, actuators, memories, and even power storage units need to be efficiently integrated into a single chip to make IoT work. M3D integration through stacking different layers of devices on each other can potentially improve circuits' performance by shortening the wiring length and reducing the interconnect delay. Using multiple tiers for device fabrication makes it possible to integrate different materials with superior physical properties. It offers the advantage of fabricating higher-performance devices with multiple functionalities on a single chip. However, high-quality layer transfer and processing temperature budget are the major challenges in M3D integration. This thesis involves an in-depth exploration of the application of germanium (Ge) in monolithic 3D integration.

Ge has been recognized as one of the most promising materials that can replace silicon (Si) as the channel material for p-type field-effect transistors (pFETs) because of its high hole mobility. Ge pFETs can be fabricated at substantially lower temperatures compared to Si devices which makes the former a good candidate for M3D integration. However, the fabrication of high-quality Ge-on-insulator (GOI) layers with superior thickness homogeneity, low residual doping, and a sufficiently good interface with buried oxide (BOX) has been challenging.

This thesis used low-temperature wafer bonding and etch-back techniques to fabricate the GOI substrate for M3D applications. For this purpose, a unique stack of epitaxial layers was designed and fabricated. The layer stack contains a Ge strain relaxed buffer (SRB) layer, a SiGe layer to be used as an etch stop, and a top Ge layer to be transferred to the handling wafer. The wafers were bonded at room temperature, and the sacrificial wafer was removed through multiple etching steps leaving 20 nm Ge on the insulator with excellent thickness homogeneity over the wafer. Ge pFET devices were fabricated on the GOI substrates and electrically characterized to evaluate the layer quality. Finally, the epitaxial growth of the highly doped SiGe and sub-nm Si cap layers have been investigated as alternatives for improved performance Ge pFETs.

The Ge buffer layer was developed through the two-step deposition technique resulting in defect density of $10^7 cm^{-3}$ and surface roughness of 0.5 nm. The fully strained $Si_{0.5}Ge_{0.5}$ film with high crystal quality was epitaxially grown at temperatures below 450°C. The layer was sandwiched between the Ge buffer and the top 20 nm Ge layer to be used as an etch-stop in the etch-

back process. A highly selective etching method was developed to remove the 3 µm Ge buffer and 10nm SiGe film without damaging the 20 nm transferring Ge layer.

The Ge pFETs were fabricated at temperatures below 600°C so that they could be compatible with the M3D integration. The back interface of the devices depleted at $V_{BG} = 0V$, which confirmed the small density of fixed charges at the Ge/BOX interface along with a low level of residual doping in the Ge channel. The Ge pFETs with 70 % yield over the whole wafer showed 60 % higher carrier mobility than Si reference devices.

Low-temperature epitaxial growth of Si passivation layer on Ge was developed in this thesis. For electrical evaluation of the passivation layer, metal-oxide-semiconductor (MOS) capacitors were fabricated and characterized. The capacitors showed an interface trap density of $3 \times 10^{11} eV^{-1} cm^{-2}$, and hysteresis as low as 3 mV at Eox of 4MV/cm corresponding to oxide trap density of $1.5 \times 10^{10} cm^{-2}$. The results indicate that this Si passivation layer substantially improves the gate dielectric by reducing the subthreshold slope of Ge devices while increasing their reliability. The in-situ doped SiGe layer with a dopant concentration of $2.5 \times 10^{19} cm^{-3}$ and resistivity of 3.5 mΩcm was selectively grown on Ge to improve the junction formation.

The methods developed in this thesis are suitable for large-scale M3D integration of Ge pFET devices on the Si platform. The unique Ge layer transfer and etch-back techniques resulted in the fabrication of GOI substrates with high thickness homogeneity, low residual doping, and sufficiently good Ge/BOX interface. The process temperatures for Ge transfer and pFETs fabrication are kept within the range of the M3D budget. Integration of the Si cap for gate dielectric formation and SiGe layers in the source/drain region may increase device performance and reliability.

Keywords: Monolithic, sequential, 3D, silicon, germanium, wafer bonding, etch back, germanium on insulator, GOI, Ge pFET, low temperature, Si passivation, pn junction

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Sammanfattning

Sakernas internet (eng. Internet of Things, IoT) driver halvledarindustrin mot tillverkning av högprestanda komponenter och kretsar med flertal funktionaliteter. Å ena sidan skalas komponenter ned till storlekar där ytterligare nedskalning blir teknologiskt svårt och ekonomiskt utmanande. Å andra sidan är dagens elektronik inte längre begränsad till kretsar för databehandling. För att sakernas internet ska fungera behöver sensorer, processorer, styrdon, datorminne och även energilagringsenheter integreras på ett effektivt sätt i gemensamma chip. Monolitisk 3-dimensionell integration (M3D) baseras på att stapla olika komponentnivåer på varandra. Detta tillvägagångssätt är en av dem mest lovande metoderna för att förbättra kretsarnas prestanda. Prestandan förbättras genom att förkorta elektriska ledare och minska fördröjningen i ledarna. Att ha flera komponentnivåer möjliggör integration av komponenter, som kan använda sig av olika material med högkvalitetsegenskaper för olika tillämpningar och funktioner, i ett enda chip. De stora utmaningarna för M3D är högkvalitétsöverföring av skikt och begränsad processtemperatursbudget.
Germanium (Ge) anses vara det bästa materialet för att ersätta kisel (Si) som kanalmaterial i p-typs fälteffektstransistorer (pFET) tack vare dess höga hålmobilitet. Vidare anses germanium lovande för M3D-integration tack germaniumtransistorernas jämförelsevisa låga processtemperatur mot motsvarande kiseltransistorer. Dock har tillverkning av germanium-på-isolator (eng. germanium on insulator, GOI) flera utmaningar: tjockleken på germaniumskiktet måste vara jämnt över skivan, dopningen måste vara låg och gränssnittet mot den begravda oxiden (eng. buried oxide, BOX) måste vara tillräckligt god.
I denna avhandling används skivbondning vid låg temperatur och tillbaka-ets för att tillverka GOI-substrat för M3D-tillämpningar. En unik stapling av epitaxiellt växta skikt har designats och tillverkats för detta ändamål. Skiktstaplingen innehåller ett relaxerad bufferskikt av germanium, ett etsstoppsskikt av kiselgermanium (SiGe) och ett toppskikt av germanium som i slutändan överförs till en hanteringsskiva. Skivorna direktbondas vid rumstemperatur, och offerskivan togs bort genom flera etssteg som lämnar 20 nm germanium på isolator med utmärkt tjockleksjämnhet över skivan. Germaniumtransistorer tillverkades på GOI-substrat och mättes elektriskt för att utvärdera skiktkvalitén. Epitaxiellt växt av högdopat SiGe och sub-nanometer kiseltäckeskikt (eng. silicon cap layer) utforskades som alternativ för germaniumtransistorer med förbättrad prestanda.
Bufferskikt av germanium togs fram med två-stegs deponeringsteknik vilket gav resultatet att defekttätheten var $10^7 cm^{-3}$ och ytruffighet var 0,5 nm. Töjt $Si_{0,5}Ge_{0,5}$-skikt med hög kristallkvalité växtes epitaxiellt vid temperaturer lägre än 450°C. Skiktet, som infogades mellan bufferskiktet av germanium och toppskiktet av 20-nm tjockt germanium, användes som etsstopp i tillbaka-etsprocessen. En mycket selektiv etsmetod utvecklades för att ta bort den 3-µm tjocka bufferskiktet av germanium och den 10-nm tjocka $Si_{0,5}Ge_{0,5}$-skiktet utan att skada den 20-nm tjocka germaniumtoppskiktet. För att tillverkningen av germaniumtransistorerna ska var kompatibla med M3D-integration så tillverkades dem vid en temperatur lägre än 600°C. Kom-

ponentens baksidesgränsnitt (Ge/BOX-gränssnittet) var utarmat vid $V_{BG} = 0V$, vilket bekräftar att både den fixa laddningstätheten vid gränssnittet och dopningen var lågt. Germaniumtransistorerna hade 70 % avkastning över hela skivan och uppvisade 60 % högre kanalmobilitet än motsvarande komponenter i kisel. In-situ dopat SiGe-skikt med dopningskoncentration på $2.5 \times 10^{19} cm^{-3}$ och resistivitet på 3.5 mcm växtes selektivt på germanium för att förbättra käll- och dräneringsövergångsbildningen. Den unika staplingen av grinddielektrika $Ge/Si/TmSiO/Tm_2O_3/HfO_2/TiN$ som togs fram i denna avhandling uppvisade en gränssnittsfälltäthet på $3 \times 10^{11} eV^{-1} cm^{-2}$ och en hysteres på låga 3 mV vid ett pålagt elektriskt fält över grinddielektrikastapeln på 4 MV/cm, vilket motsvarar en oxidfälltäthet på $1.5 \times 10^{10} cm^{-2}$. Dessa resultat visar att denna grinddielektrikastapel kan potentiellt minska germaniumtransistorernas undertröskelsving samtidigt som den förbättrar tillförlitligheten. Metoderna som har tagits fram i denna avhandling är lämpliga för storskalig M3D-integration av germaniumtransistorer på en kiselplattform. Den unika skiktöverföringmetoden av germanium och tillbaka-ets tekniken resulterade i tillverkningen av GOI-substrat med god tjockleksjämnhet, låg dopning och tillräckligt god Ge/BOX-gränssnitt. Processtemperaturerna för germanium-överföring och transistortillverkning hålls inom ramarna för M3D-integrationens temperaturbudget. Integration av SiGe-skikt i käll/dräneringsområden och kiseltäcket för grinddielektrikumbildning kan öka komponentprestanda och tillförlitlighet.

Nyckelord: Kisel, germanium, epitaxi, selektiv, pn-övergång, germanium på isolator, GOI, Ge PFET, bonding, monolitisk, sekventiell, tre dimensionell, 3D, lågtemperarad

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To my family

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List of Publications

This thesis is based on the following papers in *peer-reviewed international journals and reviewed conference proceedings*:

I. "Epitaxial Growth of Ge Strain Relaxed Buffer on Si with Low Threading Dislocation Density"
A. Abedin, A. Asadollahi, K. Garidis, P.-E. Hellström, M. Östling
ECS Transactions, vol.75, pp.615. (2016)
DOI: 10.1149/07508.0615ecst

II. "Growth of epitaxial SiGe alloys as etch-stop layers in germanium-on-insulator fabrication"
A. Abedin*, K. Garidis*, A. Asadollahi, P.-E. Hellström, M. Östling
Under review.

III. "Germanium on Insulator Fabrication for Monolithic 3-D Integration"
A. Abedin, L. Zurauskaite, A. Asadollahi, K. Garidis, G. Jayakumar, B. G. Malm, P.-E. Hellström, M. Östling
IEEE Journal of the Electron Devices Society, vol.6, pp.588. (2018)
DOI: 10.1109/JEDS.2018.2801335

IV. "Si-passivated Ge Gate Stacks with Low Interface State and Oxide Trap Densities Using Thulium Silicate"
L. Žurauskaitė, **A. Abedin**, P.-E. Hellström, and M. Östling
ECS Transactions, vol.98, pp.387. (2020)
DOI: 10.1149/09805.0387ecst

V. "Selective epitaxial growth of in situ doped SiGe on bulk Ge substrates for p+/n junction formation"
K. Garidis, **A. Abedin**, A. Asadollahi, P.-E. Hellström, M. Östling
Electronics, vol.9, pp.578. (2020)
DOI: 10.3390/electronics9040578

*: Equal Contributions

The contribution of Ahmad Abedin to each publication, major (•••), partial (••), or minor (•):

	Design	Fabrication	Characterization	Analysis	Writing
I.	••	•••	••	•••	•••
II.	•••	••	•••	••	•••
III.	•••	••	••	••	•••
IV.	•••	••	••	•	•
V.	•	••	••	••	•

The work has also been presented at the following *Publications and international conferences*:

VI. "Semiconductor devices for lasing application and methods of manufacturing such devices
A. Abedin, M. Östling *United States Patent Application*, US2021/0104871A1, (2021)

VII. "Sensitivity of the crystal quality of SiGe layers grown at low temperatures by trisilane and germane"
A. Abedin, M.Moeen, C. Cappetta, M. Östling, H.H. Radamson
Thin Solid Films, vol.38, pp.613. (2016)

VIII. "GOI fabrication for monolithic 3D integration"
A. Abedin, L. Zurauskaite, A. Asadollahi, K. Garidis, G. Jayakumar, B. G. Malm, P.-E. Hellström, M. Östling
IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), pp.81-84, Oral Presentation. (2017)

IX. "IR-Photodetector Fabrication on Suspended Gesn Thin Layers"
A. Abedin, K. Garidis, P.-E. Hellström, M. Ostling
ECS Meeting, MA2018-02 1023, Oral Presentation. (2018)

X. "Integration of highly-strained SiGe materials in 14 nm and beyond nodes FinFET technology"
G Wang, **A. Abedin**, M Moeen, M Kolahdouz, J Luo, Y Guo, T Chen, H Yin, H.H. Radamson
Solid-State Electronics, vol.103, pp.222-228. (2015)

XI. "Optimization of SiGe selective epitaxy for source/drain engineering in 22nm node complementary metal-oxide semiconductor (CMOS)"
GL Wang, M Moeen, **A. Abedin**, M Kolahdouz, J Luo, CL Qin, HL Zhu, H.H. Radamson
Journal of Applied Physics, vol.114, 123511. (2013)

XII. "Impact of pattern dependency of SiGe layers grown selectively in source/drain on the performance of 22 nm node pMOSFETs"
G Wang, M Moeen, **A. Abedin**, Y Xu, J Luo, Y Guo, C Qin, Z Tang, H Yin, H.H. Radamson
Solid-State Electronics, vol.114, pp.43-48. (2015)

XIII. "Formation of nickel germanides from Ni layers with thickness below 10 nm"
L Jablonka, T Kubart, D Primetzhofer, **A. Abedin**, PE Hellström, M Östling
J. Vac. Sci. Technol., vol.35, 020602. (2017)

XIV. "Improved designs of Si-based quantum wells and Schottky diodes for IR detection"
M Moeen, M Kolahdouz, A Salemi, **A. Abedin**, M Östling, HH Radamson
Thin Solid Films, vol.613, pp.19-23. (2016)

XV. "Scalability Study of Nickel Germanides"
L. Jablonka, T. Kubart, F. Gustavsson, D. Primetzhofer, **A. Abedin**, P.E. Hellström, Z. Zhang
Paper presented at Materials for Advanced Metallization (MAM), Brussels, March. (2016)

XVI. "Effect of strain on Ni-(GeSn)x contact formation to GeSn nanowires"
M. Noroozi, M. Moeen, **A. Abedin**, M.S. Toprak H.H. Radamson
MRS Online Proceedings Library, vol.1707, pp.7-12. (2015)

XVII. "CVD Growth of GeSnSiC Alloys Using Disilane, Digermane, Tin Tetrachloride and Methylsilane"
M Noroozi, **A. Abedin**, M Moeen, M Östling, HH Radamson
ECS Transactons, vol.64, pp.703. (2016)

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List of Acronyms

3D	three dimensional
ALD	atomic layer deposition
BOX	buried oxide
CDE	cyclic deposition-etch
CMOS	complementary metal oxide semiconductor
CV	capacitance-voltage
CVD	chemical vapor deposition
CVE	chemical vapor etch
DCS	Dichlorosilane
FET	field effect transistor
FDSOI	fully depleted silicon on insulator
IV	current-voltage
LPCVD	low pressure chemical vapor deposition
M3D	monolithic three dimensional (integration)
MOS	metal oxide semiconductor
MOSFET	metal oxide semiconductor field effect transistor
NW	nanowire
PECVD	plasma enhanced chemical vapor deposition
PVD	physical vapor deposition
RIE	reactive ion etching
RPCVD	reduced pressure chemical vapor deposition
RTA	rapid thermal anneal
SEG	selective epitaxial growth
SEM	scanning electron microscope
SIMS	secondary ion mass spectroscopy
SOI	silicon on insulator
SS	subthreshold slope
STL	sidewall transfer lithography
TEM	transmission electron microscope
TMAH	tetra-methyl-ammonium-hydroxide

Chapter 1

Introduction

1.1 Motivation

Electronic circuits dramatically changed in the 1960s as they moved from being conventional discrete devices to be the integrated components on a single chip [1]. Integrated electronics improved the reliability and performance of these circuits even as they reduced the cost of design and fabrication. Since then, the dimensions of MOS devices have been continuously downscaled allowing for a larger number of devices per area and faster switching speed [2]. Such downscaling has increased the performance of these circuits while reducing fabrication costs. Today, however, the field of electronics is facing new challenges.

On the one hand, the scaling of devices is reaching critical dimensions in the order of several atoms. This makes further downscaling technologically difficult and economically not beneficial [3]. In turn, it makes 3D integration involving stacking different layers of devices on each other, one of the most promising methods for improving circuits' performance while keeping the costs down and avoiding atomic-scale challenges [4]. On the other hand, today, the field of electronics is no longer limited to circuits with only data processing applications [4]. IoT systems are emerging, and they require multiple functionalities on a single chip. Sensors, processors, actuators, memories, and even power storage units need to be efficiently integrated to make IoT work [5]. Stacking different device layers on top of each other is one of the most promising methods to overcome these challenges.

One of the advantages of 3D integration over 2D integration is the possibility of using different materials as the active layer in the circuit. As pFETs (p-type field effect transistors) and nFETs (n-type field effect transistors) are fabricated

on different tiers, they can be processed sequentially using different materials and techniques [4]. However, their sequential processing imposes a temperature limit on the process. The processing of the top-tier devices must be tuned such that it minimizes the damages to the bottom tier and maintains the performance of already fabricated devices in the first layer. Therefore, it is important to choose the right material for the top tier which would have high carrier mobility and low processing temperature and be compatible with Si CMOS technology.

Ge as top tier material

Ge is one of the most promising candidates for 3D integration with Si devices. It has high carrier mobility compared to Si and a natural lower processing temperature. The first transistor invented in 1947 at the Bell Telephone Laboratories was made on a Ge block [6]. However, it was replaced by Si in the 1960s due to the many advantages of Si. High purity Si substrates were easier to produce, and Si could stand much higher temperatures. However, the main reason for replacing Ge with Si was the high stability of silicon dioxide. Ge oxide is water-soluble, which made it quite difficult to process. The formation of multiple sub oxides GexOy degraded the surface passivation capabilities and limited its application as a high K dielectric [7]. SiO2, on the other hand, could be thermally grown in a well-controlled manner and used as an efficient passivation layer for transistor fabrication. The high stability of SiO2 made Si the best material for the mass production of transistors, and that has remained so until today [8].

Recently, however, advanced gate dielectric materials have been developed using the atomic layer deposition technique. Therefore, there has been growing interest in Ge as the material for future electronics [4]. Ge has a much smaller effective mass in the heave hole (mhh) and light hole (mlh) bands compared to Si. This small effective mass leads to its potentially higher carrier mobility compared to Si. A comparison of the bulk mobilities of Si, Ge, and III-V semiconductor materials is presented in table 1. It can be seen from table 1 that Ge has considerably higher hole mobility than the other semiconductors, which enables enhancing the drive currents in Ge pFETs. By just considering the mobility values, III-V for NMOS (n-type metal oxide semiconductor) and Ge for PMOS (p-type metal oxide semiconductor) seems to be the best combination. However, the fabrication of nanoscale III-V transistors on Si platform suffers from cost and process compatibility issues.

Besides the higher carrier mobility advantage of Ge, its low-temperature processing also makes it a good candidate for M3D integration. Since Ge is a group IV material, it is compatible with Si technology and does not add any cross-contamination issues. SiGe has been already used in CMOS fabrication. Therefore, integration of Ge as the active material in the existing CMOS technology will be straightforward.

Material/property	Si	Ge	GaAs	InAs	InSb
Electron Mobility $cm^2/(V.s)$)	1600	3900	9200	40000	77000
Hole Mobility $cm^2/(V.s)$)	430	1900	400	500	850
Bandgap (eV)	1.12	0.66	1.424	0.36	0.17
Dielectric Constant	11.8	16	12.4	14.8	17.7

Table 1.1: Bulk properties of Si, Ge, and III-V semiconductors

Although using Ge has many advantages for CMOS applications, its 4% lattice mismatch with Si makes it difficult to grow high-quality layers directly on Si. The low bandgap of Ge and its higher dielectric constant causes the short channel effect and high leakage current, which can be improved by using GoI substrates instead of bulk Ge. Electronic and photonic devices based on GoI have been shown to be promising solutions for addressing the current difficulties that the electronics industry is facing. However, the fabrication of large-scale thin GoI (top Ge layer <40 nm) wafers with high thickness homogeneity, low defect density, low doping level, and good interface quality is challenging.

1.2 Scope, objectives and achievements

This research aims to develop and investigate new methods to use Ge in the sequential fabrication of 3D integrated electronics. Fabrication of high-quality ultra-thin GoI substrate with high thickness homogeneity has been investigated in this research to expand the applications of Ge in M3D integrated circuits fabrication.

Five main objectives were defined for this thesis to address the difficulties in Ge M3D integration. These objectives constitute the main contribution of the thesis. The research objectives and the achievements are the following:

Development of Ge SRB to be used as a virtual substrate for transferring the top tier device layer on an insulator. Since the Ge layer is required to be single crystalline material with a sufficiently low density of defects, a strain relaxed Ge layer is desired to be epitaxially grown on Si substrate. The layer should have ultra-smooth surface morphology (root mean square (RMS) < 1 nm) to be bondable to the insulator layer. The threading dislocation density should be kept low for better device yield over the wafer. By using the two-step method, Ge layers with threading dislocation density (TDD) of 10^7 cm^{-3} were epitaxially grown on Si substrates. Hydrogen thermal annealing was carried out to reduce the surface roughness to values below 1 nm. These contributions are discussed in section 3.3 and paper I (listed earlier in the "List of Publications").

Development of epitaxial growth of fully strained SiGe thin films to be used as etch-stop layers in GoI fabrication process. To transfer the ultra-thin Ge layer to another wafer coated with an insulating material, an etch-stop layer is required, which does not add any defects or roughness to the surface. For this purpose, SiGe layers were epitaxially grown at different temperatures using silane-germane and disilane-digermane gas chemistries. As a result, a SiGe layer containing 50% Ge atoms was developed at temperatures below 450°C, which was fully strained toward Ge SRB. A highly selective etching process was developed that successfully removed microns of Ge while keeping the 20 nm transferring layer intact. The contributions are discussed in section 3.4 and paper II (listed earlier in the "List of Publications").

Wafer bonding and etch-back process development to be adopted for the fabrication of ultra-thin Ge on the Insulator. A wafer bonding technique and an etch-back process were required for transferring the desired Ge layer to another wafer that would be compatible with 3D integration. This process was developed through room temperature wafer bonding, a combination of wet and dry etching of Si wafer, Ge buffer, and SiGe etch-stop layers. The fabricated GoI wafers exhibited 5% thickness inhomogeneity over the whole wafer. To our knowledge, such a high thickness homogeneity was not reported in any other studies. Since no ion implantation was performed for the GoI fabrication, the residual dopant concentration was in the range of $10^{16} cm^{-3}$ which is much lower than the range referred to in the previous reports on GoI fabrication methods. The contributions are discussed in section 4.4 and paper III (listed earlier in the "List of Publications").

Ge pFETs' fabrication process compatible with M3D. The advantages of using Ge as the top-tier device material has been discussed in section 1.1. However, the pFETs' fabrication process needs to be carried out at temperatures below 600°C for it to be compatible with M3D integration. In the course of this research, Ge pFETs' fabrication process was developed on GoI wafers. The maximum processing temperature and duration were 600°C for 60 s respectively during the dopant-activation step. Therefore, this process is fully compatible with M3D integration. The 70% yield over the wafer indicated that the wafer bonding and the etch-back process are sufficiently reliable for large-scale Ge device fabrication. Ge devices have shown 60% higher carrier mobility compared to the reference Si devices. The back-gate bias characterizations showed that the Ge/Box interface is depleted at 0 V which can be interpreted as a low-charge density at the interface and low level of residual dopants in the Ge channel. The SS of 170 mV/dec was extracted from the $I_D - V_G$ characteristics of the GoI devices. This SS value was in the same range as it was in the other studies. The contributions are discussed in chapter 5 and paper III (listed earlier in the "List of Publications").

Development of Si passivation for improvements in Ge devices. Ge MOS field-effect transistors (MOSFETs) suffer from high oxide trap density (N_{ox}) and interface trap density (D_{it}) at the interface of the Ge layer and the high-K stack, which increases the SS significantly and degrades the reliability. In this thesis, the epitaxial growth of an ultra-thin Si cap layer on Ge is developed to passivate the surface and minimize the high-K dielectric degradation. The sub-nm Si cap layer is deposited at temperatures as low as 400°C and reduced pressure by using disilane precursor. The low-temperature deposition reduces the chance of strain relaxation and minimizes the interdiffusion of Si and Ge atoms at the Si/Ge interface. MOS capacitor devices were fabricated and characterized by the collaborators to electrically evaluate the Si passivation layer. The capacitors fabricated on Si passivated Ge layers shown similar behavior as the capacitors fabricated directly on Si substrate. The characterization results shown interface trap density of $3\times10^{11}eV^{-1}cm^{-2}$, and hysteresis as low as 3 mV at E_{ox} of 4 MV/cm corresponding to oxide trap density of $1.5\times10^{10}cm^{-2}$. The results indicate that this Si passivation layer substantially improves the gate dielectric quality and potentially reduces the SS of Ge devices while increasing their reliability. The contributions are discussed in section 6.1 and paper IV (listed earlier in the "List of Publications").

Improving the junction formation in Ge devices. High contact resistance is one of the major issues that Ge devices face. The low doping concentration levels in ion-implanted Ge and high-temperature annealing requirements make it difficult to drive a high current through Ge transistors. To address this issue, we have investigated the selective epitaxial growth (SEG) of highly doped SiGe layers in source and drain areas. The in-situ doped SiGe layer with a dopant concentration of $2.5 \times 10^{19}cm^{-3}$ and resistivity of 3.5 mΩcm was selectively grown on Ge to improve junction formation. PN diodes are fabricated on the heterojunction and characterized to evaluate the layers. The contributions are discussed in section 6.2 and paper V (listed earlier in the "List of Publications").

The following research milestones were achieved while carrying out the work presented in this thesis:

- Process design for fabrication of ultra-thin GoI substrate with superior thickness homogeneity.
- Epitaxial growth of Ge SRB layer on Si substrate with low TDD and smooth surface.
- Epitaxial growth of fully strained SiGe layers on Ge at low temperatures.
- Room temperature wafer bonding and low-temperature post-bonding baking to fabricate large-scale GoI substrates within the M3D integration temperature budget.
- Highly selective etching method to remove the microns of Ge without affecting the 20 nm transferring Ge layer.

- Fabrication of Ge pFETs at temperatures below 600°C with excellent electrical characteristics.
- Development of highly reliable Si passivation layer on Ge resulting in a gate stack with low D_{it} and oxide trap density.
- SEG of highly doped SiGe on Ge to form junctions in the source and drain regions.

1.3 Organization of the thesis

This thesis comprises seven chapters as follows:

Chapter 1 presents the motivations behind this research. This chapter includes the scope, aims, and achievements of this research.

Chapter 2 briefly introduces 3D integration applications and methods and state-of-the-art circuits and devices.

Chapter 3 summarizes the theoretical principles behind the epitaxial growth of Si-Ge alloys. The initial results of the epitaxial growth of Ge SRB and SiGe layers too have been presented in this chapter.

Chapter 4 details the single-crystal Ge layer transfer and GoI substrate fabrication process during this research.

Chapter 5 provides an analysis of the fabrication process and the electrical characterization results of Ge pFET devices fabricated on our GoI wafers.

Chapter 6 focuses on the optimization of Ge devices through Si surface passivation for better high-K material development, and SEG of highly doped SiGe to improve junction formation in the source/drain region.

Chapter 7 the concluding chapter, provides the highlights of this research and an outlook on the application of developed processes for monolithic 3D integration.

Chapter 2

3D Integration

This chapter briefly introduces 3D integration and state of the art. 3D integration that is now seen as the solution for IoT device fabrication along with a discussion on the different methods for achieving 3D integrated circuits.

2.1 3D Integration

3D integration, as an idea, got introduced in 1964 by Texas Instruments [4]. Fujitsu demonstrated the first 3D CMOS integrated circuit in 1983, which included the stack of one type of transistor above a transistor of the opposite type [4]. However, the fabrication costs per transistor in 3D integration were much higher than in 2D miniaturization, which limited the industrial application of this method. The increase in the required investments for further 2D scaling, the need for shorter interconnects to get benefit from high-performance devices, and the introduction of new materials and technologies made 3D integrated circuits interesting again. Nowadays, applications of 3D integration technology are expanding rapidly. Some of the driving forces for 3D integrations are miniaturization, cost reduction, multi-functionality, and performance enhancement. There are three major categories of 3D stacking technologies today: using interposer, parallel through-Si-vias (TSV) integration, and monolithic sequential integration.

3D stacking with interposer (2.5D integration)

In this method, circuits are fabricated separately and attached to an interposer. The interposer provides interconnections between the circuits and acts as a supporting platform for multi-chip solutions. This technique permits high metal thickness but

not high density. Therefore, it is most useful for biosensing and photonic applications with low-density interconnections [9]. Typical thicknesses of interposers are in the 100 µm range with TSV width and space of 1–10 µm. Bumps used for connecting different chips are usually in the range of 40 µm, while the bumps for joining the interposer are typically in 150+ µm pitch. Figure 2.1 illustrates three chips stacked on each other of which two of the chips include TSVs. These two top chips are stacked face-to-face (F2F), while the bottom chips are joined face-to-back (F2B) [10].

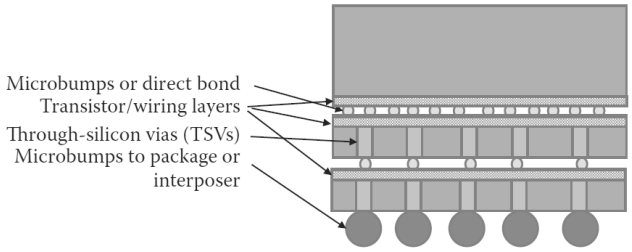

Figure 2.1: Schematic of 3D stacking by using interposer

3D parallel integration TSVs

In this technique, circuits are fabricated on two wafers separately and planarized. Two mirror-polished wafers with metal pads (usually Cu) are aligned and put into contact with each other. Adhesive forces are usually applied at room temperature to form the necessary bonding. The circuits´ electrical contacts are reached through TSVs from the backside of the wafer. This technique becomes more and more attractive because of its advantages such as no temperature limitations for separate circuits' processing and higher interconnection density compared to the flip-chip technology [10]. Nowadays, most image sensors are fabricated using this method [11]. Sony presented the first 3-layer stacked state-of-the-art CMOS image sensor at the IEEE International Electron Devices Meeting (IEDM) 2017. This chip includes pixel, memory, and image signal processor dies mounted on top of each other. They have shown that integrating memory with the logic enhanced the reading speed of the chip from 30 to 120 frame per second [12]. The interconnections pitch in this technique is 1 µm, which is limited by the wafer alignment accuracy. The misalignment between the top and the bottom pads would increase the contact resistivity and reduce the yield. Some other challenges in this technique are choosing the right materials, surface preparation, bonding strength, and metal atoms diffusion.

Sequential M3D

The first 2D integrated circuit introduced by Jack Kilby in 1958 was not monolithic [1]. The components were fabricated on a single piece of semiconductor, but the interconnections were made using hand soldering. In 1961, the first monolithic 2D circuit was presented by Robert Noyce in which both components and interconnections were monolithically integrated on a single piece of semiconductor [13]. The same story has got repeated in the case of 3D integration 50 years hence. The first 3D integrated circuits are separately made circuits, which are connected to each other by wires or TSVs. However, for higher interconnect density, M3D is required.

Sequential M3D is an ideal alternative to parallel stacking to increase the density of interconnections and reach few tens of nanometer pitches. In this method, the tiers are fabricated on top of each other in a sequential manner. Thus, the M3D process has the following five main steps:

- **Step 1:** The first-tier transistors are fabricated on a Si or SoI substrate followed by metallization and contact formation. The first-tier transistors are fabricated on a Si or SoI substrate followed by metallization and contact formation.
- **Step 2:** The surface is passivated with an insulator material and planarized using chemical mechanical polishing (CMP).
- **Step 3:** The wafer is bonded to another wafer for active layer transfer. The second wafer is called a sacrificial wafer. It contains the active layer of the second-tier devices.
- **Step 4:** The active layer is transferred to the insulating material, and the sacrificial wafer is removed.
- **Step 5:** The second-tier devices are fabricated directly on top of the first-tier devices, and the circuits are interconnected through conventional photolithography, etching, and metallization.

This process can be continued with several tiers to add higher devices and functionalities to the 3D integrated chip. Since the same alignment marks can be used for the fabrication of different tiers, lithography alignment precisions of a few nm can be achieved. This high alignment accuracy range enables via densities of more than 100 million/mm2 between different tiers. Since the nFETs and pFETs are fabricated separately, it is possible to use several materials and technologies for the transistors' performance improvements. For instance, channel materials with higher carrier mobility can be used. Substrate orientation and strain level

can be different, and various technologies such as FinFET, fully depleted silicon-on-insulator (FDSoI), and nanowire transistors can be built on top of each other. However, some benefits do not come without attendant troubles.

The major limitation of sequential 3D integration is the thermal budget of top tiers' fabrication. A reasonable max process temperature is determined to be around 500°C for 2 hours, which can be increased to 600°C if the duration would be lesser [14]. Thermal stability of silicide and metal gate function are the bottlenecks for high-temperature processing. Therefore, the top-tier materials and processing must be chosen correctly to prevent degradation of the bottom-tier transistors while achieving excellent top-tier transistor performance. Ge and III-V materials are considered good candidates for top-tier transistors channel material because of their considerably higher carrier mobility and lower processing temperature compared to Si [15]. Stacking InGaAs nFET on top of SiGeOI pFET is one of the best examples of high-performance CMOS circuits made through sequential 3D integration [16], [17]. In the case of using Si as the active layer of the top-tier transistors, new techniques such as laser annealing and solid phase epitaxy are required to keep the bottom tier circuits intact [18], [19].

One of the main challenges in sequential 3D integration is the formation of top-tier channel material. This layer can be achieved by either polycrystalline material deposition followed by recrystallization or direct wafer bonding and layer transfer. Layer transfer is usually more complicated compared to polycrystalline material deposition, and more processing steps are required. However, it has many advantages arising from the single crystallinity of the layer, which compensates for the difficulties.

In this thesis, Ge is investigated as one of the most promising candidates for M3D integration on the Si platform. The reason for choosing Ge is the higher carrier mobility compared to alternative semiconductor materials and the ability to process Ge devices at low temperatures. To monolithically integrate Ge on the already processed Si devices, a unique stack of Si/Ge/SiGe/Ge was epitaxially grown on Si substrates. Low-temperature processes are developed for wafer bonding, etch-back, Ge pFET fabrication, and device performance enhancements. The process steps are discussed in detail in the next chapters.

Chapter 3

Epitaxial growth of Ge and SiGe

Epitaxial growth of Ge, SiGe, and Si layers is discussed in this chapter. The basic concepts behind epitaxial growth are explained with a focus on growth kinetics, and strain relaxation. The layers developed at this step have been used later for the fabrication of Ge on the insulator layer and for Ge pFETs' performance improvements.

3.1 Epitaxy

The term epitaxy has a Greek root meaning "arranged on". It was first used by Royer in 1928. It is defined as oriented growth of a single crystal material arranged upon a single crystal substrate. The mechanism behind epitaxy is that of lowering the internal energy of the system by aligning the atoms of the guest crystal following the same crystal orientations as the host crystal. This enables the growth of exceptionally high-quality crystalline materials without increasing the defect density of the substrate.

Epitaxial growth can be either homoepitaxy if the layer and substrate are the same materials, or hetroepitaxy if the substrate and layer are different materials. Many different techniques have been developed for the epitaxial growth of high-quality materials. Among them, the two most used methods for the epitaxial growth of group IV semiconductors are molecular beam epitaxy (MBE) and chemical vapor deposition (CVD). In MBE, the source materials are evaporated from heated cells and collimated in a single beam before directing them toward the surface of the substrate. MBE is a flexible method as, in it, the growth parameters can be changed independently. However, this flexibility comes with other limitations such as a low deposition rate which limits MBE's application mainly to research purposes. CVD has a much higher throughput compared to MBE, which makes it a popular method for the deposition of a wide range of materials. Currently, it is the most used method

for epitaxial growth of semiconductor materials because it affords high thickness and composition homogeneity, and reproducibility concerning the wafer and over time (wafer-to-wafer).

In CVD, preheated substrates are exposed to precursors in the gas phase, and the desired layers are grown. Since the reactants are chemically stable at room temperature, the deposition is limited only to the heated zones. Chemical reactions determine the composition and the deposition rates of the layers. Therefore, many parameters such as pressure, temperature, and precursor flow control the layer quality, deposition rate, and compositions of CVD. There are many different CVD processes such as low-pressure CVD (LPCVD), reduced pressure CVD (RPCVD), plasma-enhanced CVD (PECVD), and ultra-high vacuum CVD (UHCVD).

There are two types of reactions that happen during epitaxial growth in a CVD process: gas-phase (homogeneous) and solid-surface (heterogeneous) reactions. A homogeneous reaction happens when the source gasses decompose before reaching the surface and produce solid products. The synthesized particles land on the substrate's surface after the reaction causing defects and poor uniformity. Therefore, in our CVD process, gas-phase reactions were not desirable. In a heterogeneous reaction, the reactant molecules are diffused to the surface where the reaction happens, and the desired materials are grown epitaxially. In our process, the layers grown in heterogeneous reactions were more uniform and desired.

The following are two main parameters in a simplified CVD process mechanism:

- Reactant molecules' diffusion to the surface in the gas phase.

$$J_1 = D\frac{dC}{dx} \approx \frac{D_g}{\delta}(C_g - C_s) = h_g(C_g - C_s) \tag{3.1}$$

Where J_1 is the flux of the reactant molecules in gas phase to the substrate surface, D is the diffusion constant of the reactant gasses, C_g is the concentration of reactant molecules in the bulk gas, C_s is the concentration of reactant molecules on the surface, δ is the thickness of the boundary layer, and h_g is the mass transfer coefficient.

- Adsorption of the reactant molecules on the surface.

$$J_2 = K_s C_s \tag{3.2}$$

Where J_2 is the flux of reactant molecules in the reaction site, K_s is the reaction rate constant, C_s is the concentration of reactants on the surface.

The by-products need to be desorbed from the surface after the reaction and diffused from the surface to the gas-phase to be removed from the reactor. When

the deposition rate is limited by the surface reaction, these two steps can be ignored, and a steady-state can be achieved. In the steady-state, the two fluxes are equal to the steady-state flux, which can be calculated as shown below:

$$J_{SS} = k_T C_g \tag{3.3}$$

Where k_T is the overall rate constant defined by the mass transfer coefficient (h_g) and the surface reaction rate constant (k_s):

$$k_T = \frac{h_g k_S}{h_g + k_S} \tag{3.4}$$

At high temperatures $k_s > h_g$ which results in $k_T \approx \mathrm{h}_g$ which means the reaction is in diffusion controlled regime. In the case of low-temperature processing, however, $k_s < h_g$ which corresponds to $k_T \approx K_s$ and the reaction will be in surface reaction controlled regime. This temperature effect is mainly due to exponential variation of surface reaction constant with temperature versus small variation of diffusivity by temperature ($\alpha \mathrm{T}^{3/2}$).

Therefore, the growth rate is highly temperature dependent in the reaction controlled regime. The deposition rate of a film with N number of atoms and the overall deposition rate can be calculated from 3.5 and 3.6.

$$G = \frac{J_{SS}}{N} \tag{3.5}$$

$$G_{tot} = \frac{k_T}{N}(\frac{1}{KT})P_g \tag{3.6}$$

where P_g is the partial pressure of the reactant gasses, and K is the Boltzmann constant.

In this thesis, two different layers are epitaxially grown on Si substrate to be used for fabrication of ultra-thin Ge on insulator layer for 3D integration application. The first layer consists of a strain-relaxed Ge layer grown directly on the Si substrate. The second layer is a SiGe layer that is epitaxially grown on the Ge layer to be used as an etch-stop layer in the GoI fabrication process. There are two important parameters for the transferring layer to achieve a high process yield and sufficiently good quality material for device fabrication. These parameters are low surface roughness (below 1 nm) and low defect density. The epitaxial stack shown in figure 3.1 was designed to achieve high crystal quality with a defect density of $1 \times 10^{17} cm^{-2}$ and surface roughness below 1 nm.

This chapter details reduced pressure chemical vapor deposition (RPCVD) of Ge buffer, SiGe etch-stop, doped SiGe contact, and Si cap layers. The epitax-

ial growth and effects of parameters such as precursors, deposition temperature, thermal annealing, and thickness have also been discussed in detail.

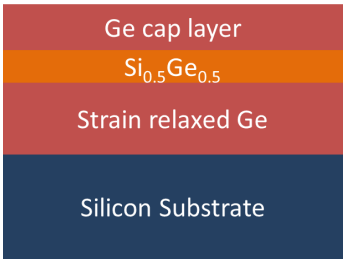

Figure 3.1: Schematic of the epitaxial stack for wafer bonding and Ge layer transfer on insulator

3.2 ASM Epsilon 2000 Reactor

ASM Epsilon 2000 is a single wafer RPCVD tool equipped with a load-lock and wafer handling unit. The wafer handling unit and the load-locks are purged with nitrogen (N) to minimize surface oxidation and oxygen contamination. The wafer handling uses a Bernoulli wand to transfer wafers from the loading cassette to the processing chamber and from the processing chamber to the unloading cassette. In the process chamber, which is made of quartz, the wafers are placed on a silicon carbide coated susceptor which is heated by using lamps from the top and the bottom. The process chamber of Epsilon is shown in figure 3.2.

The gas module handles two Ge sources, four Si sources, two dopant gasses, one tin source, $HCl, H_2, and N_2$. Silane, disilane, trisilane, and dichlorosilane (DCS) are the Si sources. Germane and digermane are the Ge sources. P-type and N-type doping are obtained by diborane and phosphine gasses respectively. $H_2 and N_2$ are used as charrier gasses. HCl can be used in high flow for cleaning the reactor or in low flow for SEG. Each gas line can go to the vent or the reactor separately, which offers the option of depositing different materials on top of each other in a single epitaxial growth step. The processes can be carried out either at reduced pressures (10–100 Torr) or at atmospheric pressure.

The susceptor is heated through radiation from Tungsten-halogen lamps. Therefore, the susceptor's temperature is much higher than the rest of the reactor, and a major part of the reaction happens on the wafer. The temperature is measured through five thermocouples placed in the center, sides, front, and end of the susceptor area. The thermocouples are connected to temperature-controlling units which adjust the power supplied to the lamps separately for each of them so that they

can reach the temperature set-point homogenously over the wafer. The process temperature can be precisely controlled between 200℃ and 1,200℃.

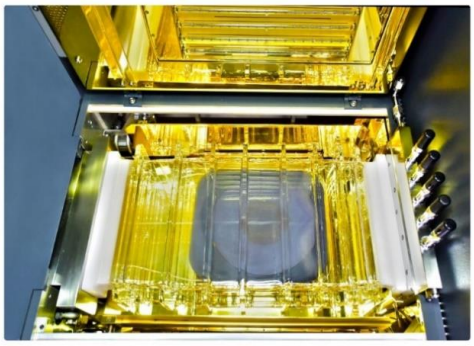

Figure 3.2: Photo of the quartz chamber of ASM Epsilon 2000

3.3 Epitaxial growth of Germanium SRB on Si(001)

Heteroepitaxial growth can be classified into three distinct modes which have been detailed in the following paragraph. Growth mode mainly depends on two parameters, i.e., the lattice mismatch between the growing layer and the substrate and the balance between the free energy of substrate (σ_s), layer (σ_L), and the interface (σ_i).

The Frank-Van der Merwe growth mode is the case where the free energy of the substrate is higher than the free energy of the layer and the interface. In this mode, the single crystalline film is grown layer-by-layer on top of the substrate. It is also called 2D growth. The Volmer-Weber growth mode is the one where the free energy of the substrate surface is lower than the layer and the interface. Therefore, the adatoms bond to themselves to have the minimum free energy and form 3D islands that cause rough surfaces. The third growth mode is the Stranski-Krastanov (SK) mode. It is a combination of both 2D and 3D growth modes. In this case, the growth begins with the 2D layer formation and continues with 3D growth and formation of islands due to gradual strain accumulation. SK is the main mode for epitaxial growth of Ge layers on Si substrate [20].

Ge, with a lattice constant of 5.530 Å, has a 4% lattice mismatch with Si having a lattice constant of 5.530 Å. This lattice mismatch makes it difficult to grow smooth single-crystalline layers having less defect density. The critical thickness of Ge on Si is reported to be less than 9 atomic monolayers and depends on the growth conditions. The first few monolayers of Ge on Si will be compressively strained since the layer's in-plane crystal lattice matches the substrate. However, by growing Ge

layers thicker than the critical thickness, the layer loses the strain gradually through defect formation. By continuing the growth, these defects penetrate through the film and generate threading dislocations that degrade the crystalline quality and electrical properties of the material. Besides the defect formations, the 3D island growth of Ge on Si increases the surface roughness that degrades device performance. Several different techniques have been proposed and developed to improve the surface roughness and lower the defect density. These techniques include graded SiGe buffer layers [21, 22, 23], two-step growth (low temperature and high temperature), and thermal annealing.

Two step Ge epitaxial growth on Si

The two-step method was proposed in 1998 by Colace et al. [24] and further developed by Hartman et al. and Luan et al. [25, 26, 27]. In this method, first, a Ge seed layer is deposited at low temperature (LT) (below 400°C) and then a second Ge layer is grown on the seed layer at higher temperatures (HT) (above 550°C).

In the low temperature step, 50–100 nm Ge layer is grown on Si surface to gradually release the 4% misfit stress through misfit dislocations formation. The surface mobility of Ge atoms is substantially low at temperatures below 400°C. This lower atom mobility leads to 2D growth morphology instead of 3D and lowers surface roughness compared to high temperature growth [28]. The seed layers grown at this step have a high density of threading dislocations in the orders of $10^{12} cm^{-2}$. Therefore, they are not suitable for electronics applications at this stage.

In the second step, Ge layers are grown at temperatures above 600°C to achieve higher crystal quality and faster deposition rates. By growing thicker Ge layers, threading dislocations collide and eliminate each other. As a result, growing thicker layers reduces the level of TDD [29]. However, the thickness cannot be increased more than five microns as the Ge layer has a slight tensile strain and bends the Si wafer. Therefore, post-cycle thermal annealing has been proposed to improve the crystal quality and surface roughness [29]. During cycle thermal annealing, the temperature is increased up to 900°C and reduced to 100°C several times. Yamamoto et al. [29] have shown that by choosing the right temperatures and thickness, it is possible to reduce defect densities to $7 \times 10^5 cm^{-2}$ while keeping the surface roughness below 1 nm (figure 3.3). However, thicknesses as high as 4.5 µm are required.

In this thesis research, a two-step process followed by thermal annealing was used for epitaxial growth of the Ge buffer layer with sufficiently high crystal quality. Two commercially available gas sources, germane and digermane, were used for the epitaxial growth of Ge layers. These layers were thermally annealed at 850°C

directly after growth to reduce the defect density to $10^7 cm^{-2}$. The results of the growth conditions and material characterizations have been presented in this chapter.

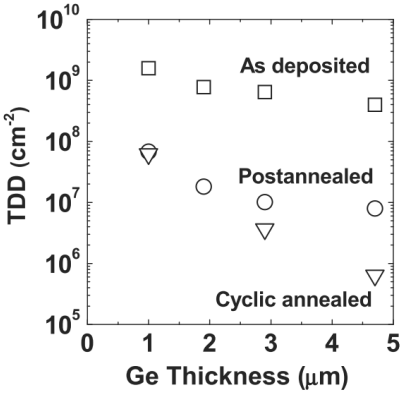

Figure 3.3: TDD vs Ge thickness [30].

Pre-Epitaxy treatment

The surface of the wafers must be perfect and without any contaminations to achieve high-quality epitaxial growth. Basically, an epitaxy-ready surface needs to be free from oxide films, contaminations, and etched-surface damages. The best choice for surface preparation is performing both ex-situ and in-situ cleanings. Different processes for wafer cleaning have been presented in [30]. One of the most common choices for ex-situ cleaning is treatment in a "Piranha" ($H_2SO_4 : H_2O_2$) solution to oxidize the surface and remove organic contaminations. The process is followed by hydrofluoric acid (HF) treatment to remove the native oxide and particles on the surface. The in-situ surface treatment can be performed at different temperatures and gas ambient conditions. Using hydrogen at elevated temperatures is the most common in situ treatment for group IV materials growth. This step can be skipped if cluster tools with in situ wet cleaning stations are being used [31].

For this research, the layers were grown on 100 mm Si wafers that were submerged in a "Piranha" bath for 15 min, rinsed in di-water, and dipped in an HF solution before loading to the nitrogen purged load-lock. Substrates were in-situ hydrogen baked at 1,050℃ for 10 seconds. This prebaking step was enough to remove all oxygen and carbon contaminations that remained on the surface. In the case of Ge wafers and pre-processed wafers, 800℃ and 950℃ for 15 min were enough to prepare a clean surface for epitaxial growth. Ge buffer layers were grown by using

both germane and digermane sources for comparison. In paper 1, we have detailed our investigation of two Ge SRBs which were grown with a two-step method by varying the seed layer growth temperature.

3.3.1 Germanium growth using germane

Germane is the most used gas for Ge and SiGe layer depositions. It is in the gas phase at room temperature and is usually diluted with either H_2 or N_2. For this research, 10% germane in H_2 was used for epitaxial growth of Ge buffers. During the growth and baking steps, the pressure was constantly kept at 20 Torr. Ge layers were grown in two-step processes with the first layer at 400°C and the second layer at 600°C followed by thermal annealing in a hydrogen ambient condition. Ge layers were grown directly on Si at temperatures ranging from 350°C to 600°C for the development of the seed layer. The flow of germane was kept constant at 400 SCCM during the growth step. Figure 3.4 shows the deposition rate versus temperature. The results show that by increasing the temperature from 350°C to 400°C, the growth rate sharply increased from 5 nm/min to 37 nm/min. This growth rate enhancement indicates that the process is controlled by the reaction at these temperatures. However, at a temperature higher than 425°C, the growth rate is not significantly changed by temperature. This shows that the process, at this point, is controlled by the gas flow at these temperatures.

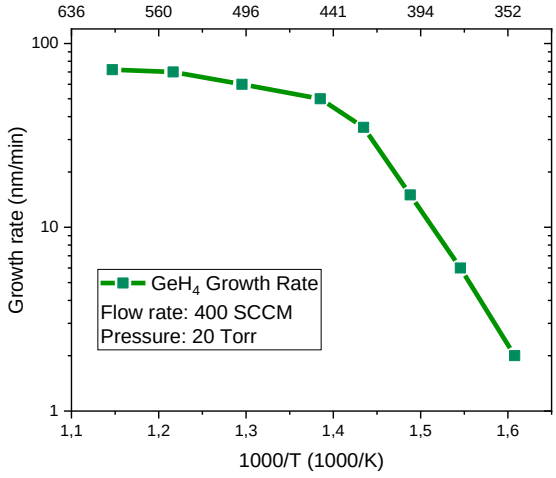

Figure 3.4: Ge growth rate versus temperature with germane flow of 400 SCCM at 20 Torr

From the experimental data, 400°C was chosen for low temperature growth and 600°C was chosen for the high temperature growth. A 100 nm Ge seed layer was grown at 400°C followed by ramping up the temperature to 600°C in hydrogen ambient conditions with the rate of 50°C/min. The second Ge layer with a thickness of 2 µm was deposited at 600°C on top of the seed layer. After the growth, the temperature was increased gradually to 850°C, and the sample was hydrogen baked at this temperature for 10 min. Hydrogen baking smoothens the surface of the Ge layer and reduces its defect density. The layers were characterized by high-resolution X-ray diffraction (HRXRD) rocking curve and reciprocal space mapping to investigate the crystallinity and the residual strain level. Secco solution consisted of 1 part of $K_2Cr_2O_7$ 0.15 M, 2 parts of HF (49%), and 3 parts H_2O [32, 33], and the Iodine solution consisted of $[CH_3COOH(65mL)|HNO_3(20mL)|HF(10mL)|I_2(30mg)]$ [34, 35]. These were used for the delineation of threading dislocations, and the defect density was measured from optical microscope and images from scanning electron microscope (SEM).

The XRD rocking curve of the Ge layer grown on Si can be seen in figure 3.5. It indicates that the layer is under 0.15% tensile strain. This amount of strain is due to the lower thermal expansion coefficient of Si ($2.6 \times 10^{-6}C^{-1}$) compared to Ge ($5.9 \times 10^{-6}C^{-1}$). The Ge layer is grown strain relaxed on Si at high temperature, but during its cooling to room temperature, Ge shrinks faster than Si and becomes tensile strained. The right side of the Ge peak has some broadening. This is because of the interdiffusion of Si and Ge atoms at the interface, which results in a Ge-rich SiGe layer between Si and Ge.

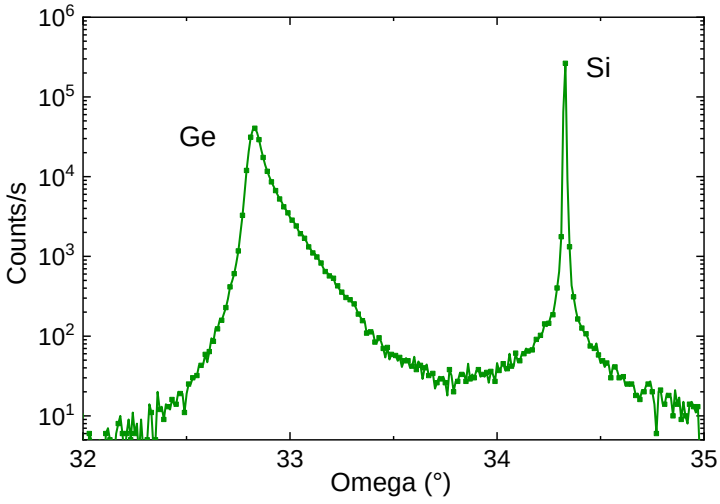

Figure 3.5: XRD Omega/2Tetha scan around (004) direction of Ge buffer layer on Si

Similar TDD of $2 \times 10^7 cm^{-2}$ was delineated after the etching in Secco and Iodine solutions. Scanning electron microscope (SEM) images of the surface topography after defect selective etching are shown in figure 3.6. For further improvement of the crystal quality, the Ge buffer layers were grown on Si substrates by using digermane as the Ge precursor.

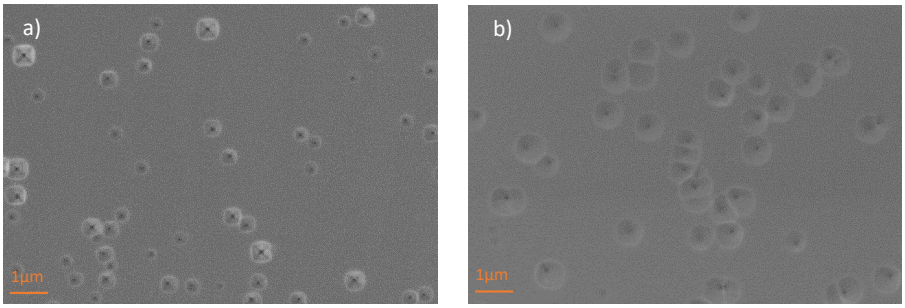

Figure 3.6: Etch pit density of Ge SRB revealed by a) Iodine solution and b) Secco solution

3.3.2 Ge growth using digermane

The lower activation energy of digermane compared to germane makes it possible to deposit the Ge seed layer at temperatures below 300°C. The growth rate of the Ge layer on Si substrate at temperatures ranging from 280°C to 600°C is shown in figure 3.7. The flow of digermane (10% diluted in hydrogen) was 100 SCCM, and the reactor pressure was kept at 20 Torr during the growth. By using digermane, the Ge layers are deposited at much higher rates compared to when germane is used. The lowest growth temperature decreased from 350°C to 280°C by using digermane instead of germane because of the lower activation energy of digermane when compared with that of germane. The activation energy of 1.1 eV was calculated from the slope of the graph, which is in line with previous studies [36]. The reaction is in the kinetic regime at temperatures below 360°C, and the growth rate increases by increasing the temperature. At these temperatures, the deposition is controlled by chemical reactions on the surface, atoms' mobility, and desorption of by-products. At temperatures above 360°C, however, the reaction happens in a diffusion-controlled regime that is limited by the mass flow of the reactants. Therefore, increasing the temperature does not increase the growth rate of the layers. At temperatures above 400°C, the higher gas-phase decomposition of digermane reduces the growth rate.

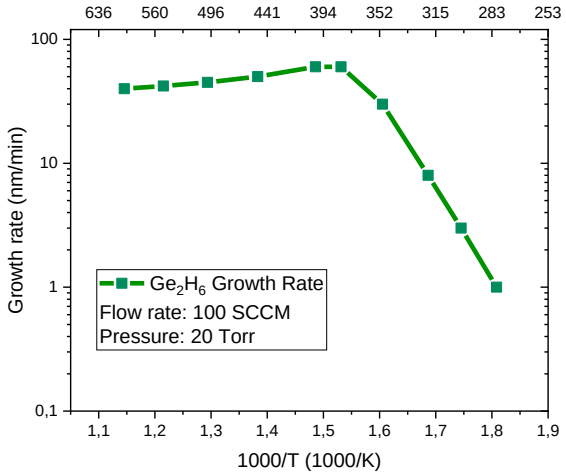

Figure 3.7: Growth rate of Ge layer on Si substrate at temperatures ranging from 280°C to 600°C with digermane flow of 100 SCCM at 20 Torr

Ge SRB was grown directly on Si substrate. The seed layer was grown at 280°C–300°C targeting 40 nm thickness. The atomic force microscopy (AFM) measurement after growth shows the formation of pits and surface roughness below 1 nm. We believe that when the Ge seed layer is deposited at temperatures below brittle-ductile transition, the strain is released through the formation of pits. This type of strain relaxation results in a much smoother surface morphology than the growth at higher temperatures. Growing thicker Ge layers on such seed can result in smooth layers with surface roughness below 1 nm without any need for post thermal annealing.

The growth was continued by increasing the temperature to 680°C and deposition of 460 nm Ge on the top of the seed. No post-thermal annealing was performed, and the layers were characterized by AFM, XRD, transmission electron microscope (TEM), and etch pit density (EPD).

The initial etch-pit density which was revealed by using the Secco etchant showed a very small number of defects $4 \times 10^4 cm^{-2}$, which was in line with the results shown in [37]. However, the TEM images showed a higher number of threading dislocations $5 \times 10^8 cm^{-2}$. Therefore, another selective etching solution known as iodine was used for defects delineation. The result (SEM images in figure 3.8) was in line with the TEM results. Our investigation shows that the use of Secco, which is the most common etching solution in Si and Ge alloys, is not always the best method for revealing threading dislocation density. If the seed layer of Ge is

grown at temperatures below brittle-ductile transition, the type of defects changes from 60° dislocations to 90° Lomer (edge) and screw dislocations that have very few dangling bonds and are less electrically active defects.

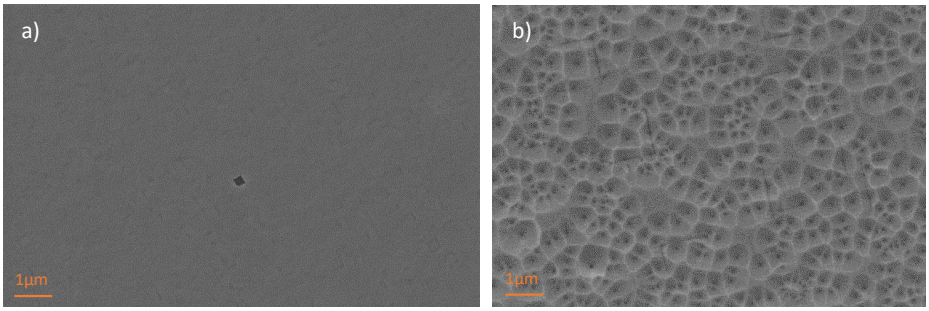

Figure 3.8: EPD revealed by a) Secco solution and b) Iodine solution.

For further analysis, Hall mobility measurements were performed on epitaxially grown Ge layers to investigate the effects of growth conditions on carrier mobility. This measurement showed that when the seed layer is grown at temperatures as low as 300°C, the carrier mobility is twice as much as that of the layers grown at higher temperatures. These results confirm that the defects formed under brittle-ductile transition temperature are less electrically active.

Since digermane is an expensive gas with limited resources and long delivery time, germane was used for Ge buffer growth in the rest of this research work. The two-step method was used for the epitaxial growth of Ge SRBs. The Ge seed layer with a thickness of 100 nm was grown at 400°C. The temperature was increased to 600°C afterward at the rate of 100°C/min, and the second layer was grown at this temperature. The total thickness of Ge SRB was 2.5 µm with a surface roughness of 3 nm. Thermal annealing at 890°C for 10min was done for smoothening the surface and lowering the defect density. TDD of $1 \times 10^7 cm^{-2}$ was delineated by using Iodine and Secco solution. The surface roughness of 0.5 nm was measured by AFM after thermal annealing.

3.4 SiGe epitaxial growth on Si and Ge

Epitaxial growth of SiGe layers with different strain levels has been investigated for many years. The 4% lattice mismatch between Si and Ge creates the possibility to epitaxially grow compressive and tensile strained layers at the same time. Compressive strain in SiGe boosts the hole mobility which results in higher performance pFETs with improved ION current [38]. The tensile strained Si layers grown on strain relaxed SiGe layers showed electron mobility enhancement[39]. Therefore, the strain relaxed SiGe layers can combine these benefits by being used as a virtual substrate to fabricate CMOS with tensile strained Si nFET and compressive strained SiGe pFET. Raised highly doped SiGe source and drain are the mainstream of today's microelectronics[40]. However, most of the research has been focused on the epitaxial growth of SiGe layers with low Ge contents, and the epitaxial growth of fully strained SiGe layers with high Ge content has been not investigated in-depth. In this research, we have investigated the low temperature deposition of SiGe layers with Ge contents above 50% on Ge to be used as an etch-stop layer for GoI fabrication.

As presented in Paper II, the SiGe layers with Ge contents ranging from 20% to 70% were epitaxially grown on Si substrates. Two gas chemistries, silane-germane, and disilane-digermane were used, and the layers were compared in terms of crystal quality, strain relaxation, and growth rate. Since it is difficult to precisely measure the thickness and composition of SiGe layers grown on Ge, the layers were, first, deposited on Si substrates. The final SiGe layer was grown on the Ge buffer layer, and it was evaluated by high-resolution XRD (HRXRD).

3.4.1 SiGe epitaxial growth using silane-germane

Figure 3.9 shows the XRD rocking curve of SiGe layers grown at temperatures ranging from 450°C to 650°C. The partial pressure ratio of germane to silane was kept at 0.24 during the depositions, and the layers were grown at a reduced pressure of 20 Torr. At 450°C, the peak at 33.4° was related to the SiGe layer directly grown on Si substrate. The thickness fringes beside the peak show that the layer is Pseudomorphic under compressive strain with a flat interface between SiGe and Si. The thickness and Ge content values extracted from the XRD curves agree with Ellipsometry measurements. By increasing the temperature, the SiGe peak could be shifted to higher angles, and the thickness fringes disappeared, which indicates partial strain relaxation of the SiGe layer.

The Ge concentration and growth rates of SiGe layers extracted from Ellipsometry and HRXRD measurements are shown in figure 3.10. At fixed partial pressures, the Ge content is slightly reduced with an increase in the growth temperature. The

main reason for this Ge content reduction is the slightly higher activation energy of silane compared to germane. At higher temperatures, more silane atoms decompose and contribute to the growth, which reduces the Ge content. The activation energy of 1.3 eV was calculated from the Arrhenius plot, which is in line with previous studies.

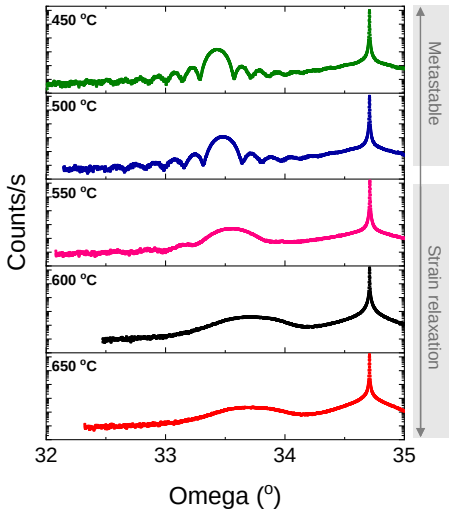

Figure 3.9: XRD Omega/2Tetha scan around (004) direction of SiGe layers grown on Si substrates using silane and germane

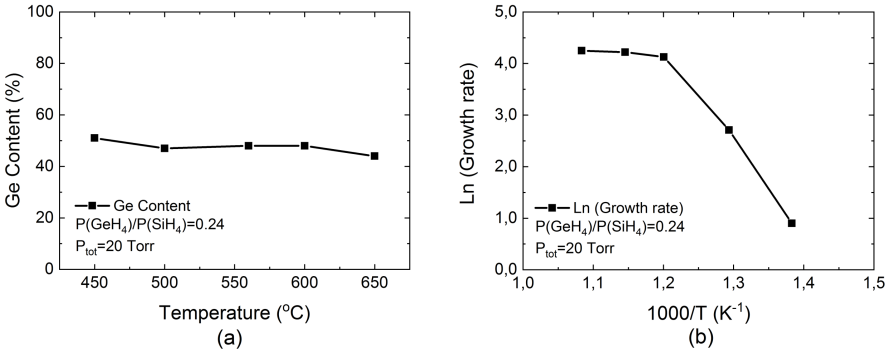

Figure 3.10: Ge content and growth rates of the SiGe layers versus temperature at $P(GeH_4)/P(SiH_4) = 0.24$.

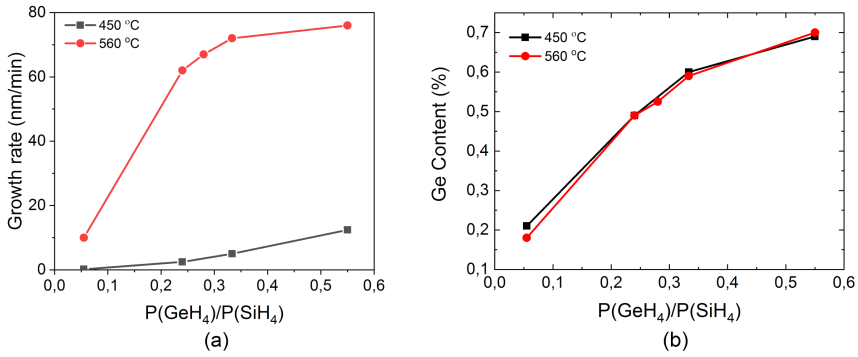

Figure 3.11: Growth rate and Ge contents of SiGe layers versus PPR of germane to silane

The growth rate and Ge contents of SiGe layers versus partial pressure ratio (PPR) of germane to silane are shown in figure 3.11. By increasing the PPR of germane to silane from 0.05 to 0.55, the Ge content in the layer increases from 20% to 70%. AT 450°C, the reactant molecules decompose heterogeneously, and hydrogen desorption controls the reaction. Therefore, increasing the germane to silane PPR increases the growth rate. At 550°C, the growth rate increases sharply from 10 nm/min to 70 nm/min when the PPR of germane to silane is increased from 0.05 to 0.3, and thereafter, it saturates at higher PPRs. The growth rate saturation is mainly due to the homogenous decomposition of germane at high flow rates, which has been studied before.

AFM was utilized to evaluate the surface morphology of SiGe layers as grown, and the images are shown in figure 3.12. The thickness of the SiGe layers was in the range of 25 – 40 nm. The surface roughness at 450°C has not been shown as it is below 1 nm, the same as the sample grown at 500°C. The surface roughness increased at higher temperatures due to the transition in the growth mode from a 2D growth mode (Frank–Van der Merwe) to a 3D growth mode (Stranski–Krastanov) [41] and strain relaxation.

3.4.2 SiGe epitaxial growth using disilane-digermane

To lower the growth temperature even further, SiGe layers were deposited by using disilane (Si_2H_6) and digermane (Ge_2H_6) gasses. The lower dissociation energy of Si-Si and Ge-Ge compared to Si H and Ge H made it possible to grow fully strained SiGe layers with high Ge contents at temperatures below 450°C. At first, SiGe layers were grown at 450°C with different PPRs of digermane to disilane, and the growth rate and Ge content of the layers are shown in figure 3.13. By increasing

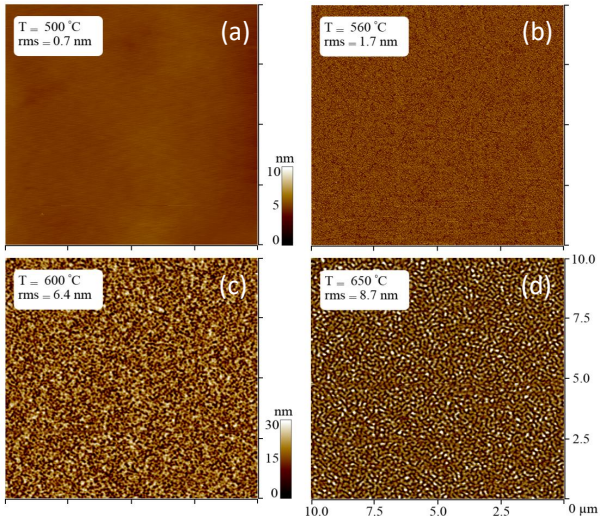

Figure 3.12: 10 µm×10 µm atomic force microscopy (AFM) images of the SiGe surfaces grown at $P(GeH_4)/P(SiH_4) = 0.24$ in a temperature range of (a) 500ºC, (b) 560ºC, (c) 600ºC, and (d) 650ºC

the $P(Ge_2H_6)/P(Si_2H_6)$ ratio from 0.055 to 0.55, the Ge content increased from 45% to 70%

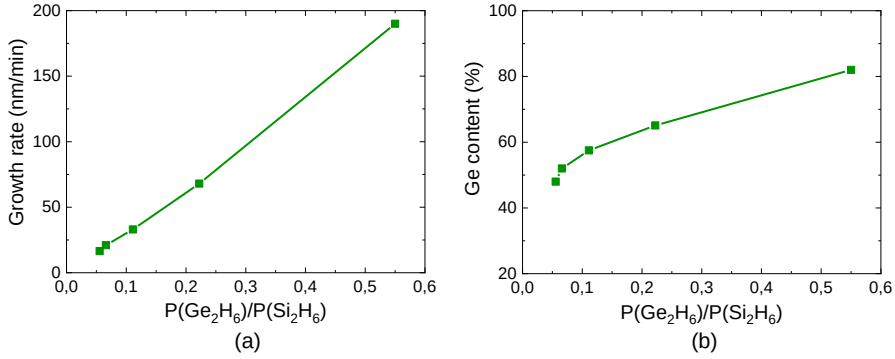

Figure 3.13: Ge content and growth rate of SiGe layers as a function of $P(Ge_2H_6)/P(Si_2H_6)$, at 450°C and P_{tot}=20 Torr

The growth rate and Ge content of SiGe layers are plotted as a function of growth temperature in figure 3.14. The Ge content of the films drops significantly

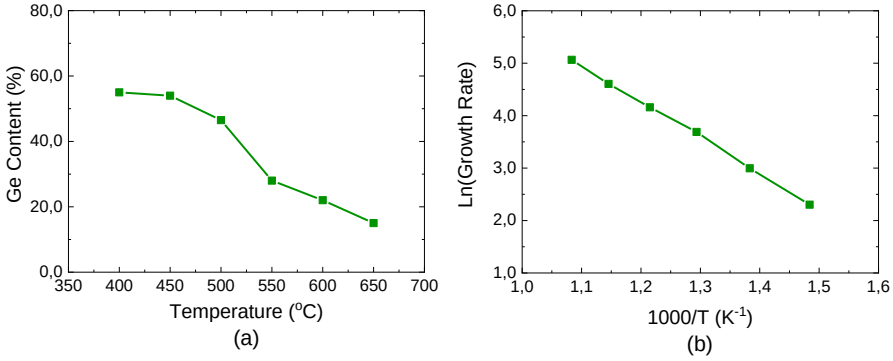

Figure 3.14: The Ge content and growth rate of SiGe layers versus temperature at $P(Ge_2H_6)/P(Si_2H_6)$=0.067 and P_{tot}=20 Torr

by increasing the growth temperature from 55% at 400℃ to 15% at 650℃. This is due to the lower decomposition rate of Si_2H_6 compared to that of Ge_2H_6 at temperatures as low as 400℃. The growth rate of SiGe layers at low temperatures was 8 times higher with $Si_2H_6 - Ge_2H_6$ precursors than with $SiH_4 - GeH_4$. By increasing the temperature, the growth rate difference got reduced as the growth was controlled by the mass flow of the reactants.

Figure 3.15 shows the HRXRD rocking curves of SiGe layers grown with fixed PPR of Si_2H_6/Ge_2H_6 at different temperatures ranging from 450℃ to 650℃. All the SiGe layers are fully strained toward the Si substrate and well-defined thickness fringes are clearly visible beside the SiGe peak. By increasing the temperature, the SiGe peak gets shifted toward higher angles which shows the Ge content, and the amount of strain is reduced. Therefore, the critical thickness increased, and the layers remained fully strained even at growth temperatures as high as 650℃.

3.4.3 $Si_{0.5}Ge_{0.5}$ growth on Ge

To develop the bonding stack for Ge layer transfer, the SiGe layers were grown on the Ge strain relaxed buffers. The SiGe layer was grown at 450°C with silane-germane and 400°C with disilane digermane gasses.

The HRXRD rocking curve of 20 nm $Si_{0.5}Ge_{0.5}$ grown on Ge SRB is shown in figure 3.16. The peak at 34.7 is related to the Si substrate and the peak at 33.2 is related to Ge SRB. The peak associated with the $Si_{0.5}Ge_{0.5}$ layer can be seen at 34.5° with small fringes on the left side. The low intensity of the fringes compared

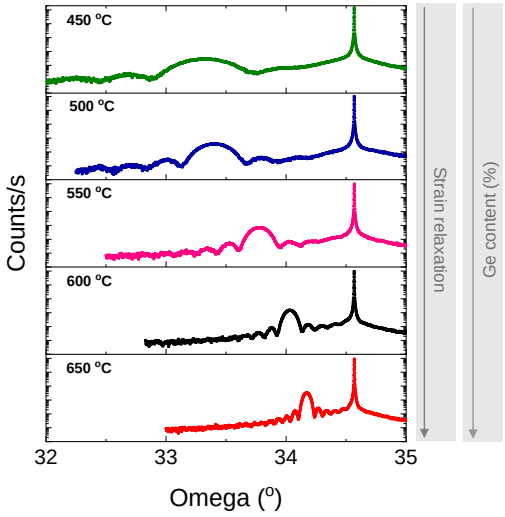

Figure 3.15: XRD rocking curve of SiGe layers grown by digermane and disilane at different temperatures at $P(Ge_2H_6)/P(Si_2H_6)$=0.067 and P_{tot}=20 Torr.

to the layers grown directly on Si is due to the lower thickness of the $Si_{0.5}Ge_{0.5}$ layer and slightly higher surface roughness of Ge SRB (0.5 nm < RMS < 1 nm) compared to Si substrate. The position of the peak also moved from 33.4° on Si to 34.5° on Ge, thus, indicating that the $Si_{0.5}Ge_{0.5}$ layer is 1.6 % tensile strained when grown on relaxed Ge.

The surface morphology of Ge buffer and Ge buffer capped with 10 nm $Si_{0.5}Ge_{0.5}$ is shown in Figure 3.17. The AFM images show that the surface roughness of the layer stack is not increased when the $Si_{0.5}Ge_{0.5}$ layer is deposited on top of Ge SRB at temperatures as low as 450°C. The low surface roughness makes it a suitable material for direct wafer bonding and layer transfer application.

3.5 The full stack growth

The full stack for GoI fabrication consists of a 2 µm Ge SRB, 10 nm fully strained Si0.5Ge0.5, and 20 nm Ge layers. In the first epitaxy step, the Ge buffer layer was deposited on Si substrates with germane and post-thermally annealed to reduce the defect density and surface roughness. The substrates were placed in the nitrogen purged load-lock to avoid any contaminations and minimize surface oxidation. The growth chamber was then cleaned with HCl at 1,100°C to remove the unwanted depositions on the quartz and the susceptor. The wafers were loaded to

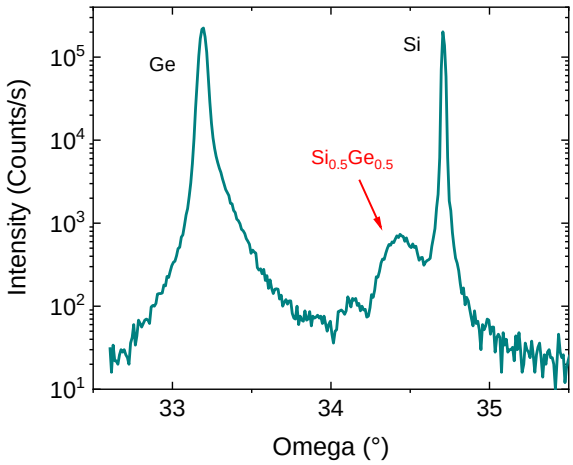

Figure 3.16: XRD rocking curve acquired by -2 scan around (004) direction. The $Si_{0.5}Ge_{0.5}$ peak position at 34.4° and the thickness fringe to the left shows that the layer is under tensile strain with a sufficiently flat interface with Ge SRB

the growth chamber again for the second epitaxy step. They were in-situ baked at 850°C in hydrogen ambient conditions to remove any native oxides before epitaxial growth. Two batches of stacks were grown directly over Si substrates one with silane-germane and the other one with disilane-digermane chemistries.

In the case of silane germane, SiGe and the top Ge were deposited at 450°C. The layers were grown at 400°C when digermane and disilane were used as the precursors. The surface morphology of the whole stack was analyzed using AFM which is seen in figure 3.18. The measurements show surface roughness below 1 nm which indicates the process is not affecting the surface morphology, and the layers can be bonded to the carrier wafer without any need for CMP.

Advantages for M3D

The epitaxial stack designed and developed in this research are suitable for large scale Ge layer transfer and GoI substrate fabrication. The low RMS of as grown layers make it possible to bond wafers without any post CMP.

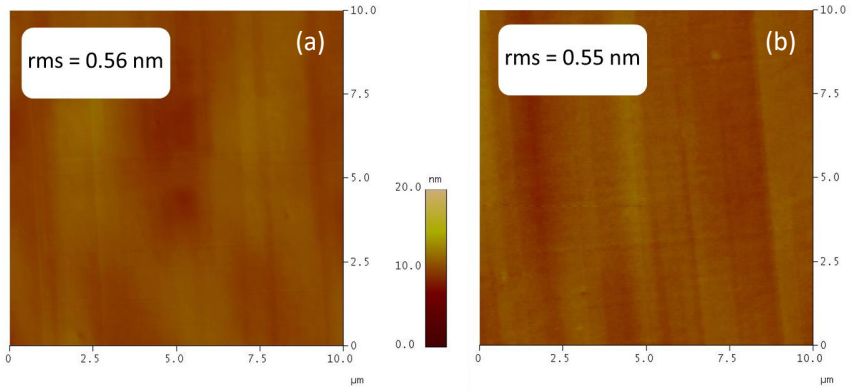

Figure 3.17: AFM image of $Si_{0.5}Ge_{0.5}$ layer grown on Ge strain relaxed buffer. The RMS surface roughness does not change with the deposition of $Si_{0.5}Ge_{0.5}$ on top of the Ge SRB.

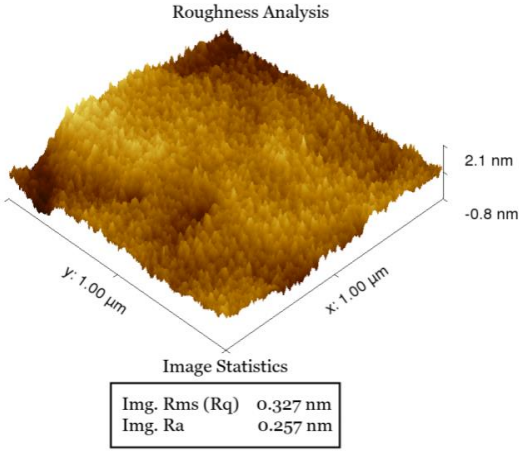

Figure 3.18: AFM surface topology of full-stack containing Si/Ge/SiGe/Ge with RMS of 0.3 nm

Chapter 4

Fabrication of Germanium on insulator

In this chapter, a short introduction about wafer bonding and layer transfer techniques is presented and the GoI fabrication results are discussed.

Thin body GoI structures are particularly needed to realize high-performance Ge MOSFETs and suppress the leakage current and parasitic capacitance. In the past, numerous techniques have been developed for the fabrication of GoI substrates. There are five main techniques that have been used for the formation of Ge on insulator layers:

- *Condensation* method is based on the deposition of a SiGe layer on SoI substrate and thermal oxidation [42, 43, 44].
- *Rapid thermal melting* is another method in which an amorphous Ge layer is deposited and recrystallized through rapid thermal annealing (RTA).
- *Lateral overgrowth* method is based on the growth of the Ge layer on a patterned Si substrate using liquid-phase epitaxy [45, 46].
- *Smart-Cut* process in which ion implantation is used for layer separation after wafer bonding [47, 48, 49].
- *Wafer bonding and etch-back* process in which a sacrificial wafer is used for transferring the Ge layer [50].

Among these methods, the wafer bonding and etch-back processes have many advantages over other methods of M3D integration. Minimal process temperature, high crystal quality, and low level of intrinsic dopants were the main driving forces for using the wafer bonding and etch back method in this thesis work.

4.1 Wafer bonding and layer transfer

The process of wafer bonding and layer transfer is performed in the following two main steps:

- Step 1: Two wafers (handling wafer and sacrificial wafer) are coated with insulating material and placed in contact with and bonded to each other.
- Step 2: The sacrificial wafer is removed leaving the target layer on the handling wafer.

There are many different methods for achieving a high yield bonding with low defects and strong enough surface attachments which will be discussed later in this chapter. The removal of the sacrificial wafer can be done through either the so-called Smart-Cut process or selective etching, which will be discussed briefly in this chapter.

Three general methods that are used for wafer bonding are *intermediate layer bonding*, *anodic bonding*, and *direct bonding*. In intermediate layer bonding, one or both the wafers are first coated with an adhesive layer, which is mostly based on the metals or polymers used, and the wafers are then placed in contact with each other for bonding. Post-baking and high-pressure treatments are needed sometimes for fusion and bond formation. Anodic wafer bonding is based on the direct bonding of two surface-modified wafers in the presence of electric fields. The oxygen ions are driven to the interface of the wafers, and they form an oxide layer that bonds the two mating wafers. In the Direct wafer bonding technique, two wafers are placed in contact with each other, and the bonding forms at the interface through post thermal baking [51]. The direct bonding method was used in this research work. It will be discussed further in detail.

4.1.1 Direct wafer bonding

Direct wafer bonding relies on intermolecular attraction forces that are formed at the interface of two smooth and flat surfaces in proximity. These forces can be electrostatic forces, capillary forces, or Van der Waals forces. The initial bonding energy is weak, and the wafers need to go through a post-thermal annealing process to increase the bonding strength. This method needs extremely clean surfaces with very low surface roughness (< 1 nm) to get a good result. Depending on the surface properties and the form of bonding, direct wafer bonding is divided into two categories: hydrophilic and hydrophobic wafer bonding [51].

In hydrophobic wafer bonding, the Si oxide is first removed from the surface by HF treatment which makes the surface hydrophobic. In this method, the contacting forces between the surfaces are Van der Waals forces or Fluor mediated hydrogen bonding as explained by Bäcklund et al. and Tong et al. [52, 53, 54, 55]. The bonded wafers are then thermally annealed at high temperatures to form chemical bonds. This technique is mostly used for the formation of Si PN junction and bonding III-V materials to Si wafers.

In hydrophilic bonding, the atomic bonds are formed with the reaction of hydroxyl (OH) groups on the surfaces. When two hydrophilic wafers (having a high density of OH groups) are placed in proximity of less than 1 nm, they bond to each other by hydrogen bonds. The hydrogen bonds are formed between hydrogen atoms on one surface and electronegative atoms, such as O, on the other surface. Therefore, a minimum density of polar molecules on the surfaces is required to form hydrogen bonding all over the surfaces.

When hydrogen bonds are formed, water molecules are generated as byproducts (equation 4.1 below) which need to be removed from the interface. These water molecules can be removed through diffusion out of the interface or dissolving in the materials. Removing the water molecules leads to the polymerization of OH groups and the formation of strong covalent Si O Si bonds [56].

$$Si - OH + OH - Si \leftrightarrow Si - O - Si + H_2O \tag{4.1}$$

This reaction is reversible at room temperature, and a thermal annealing step is required to facilitate the reaction. This thermal annealing step can be performed either at low temperatures for a long period or at high temperatures for a shorter duration [57].

There are many methods for making a surface hydrophilic (add OH groups) such as using oxygen plasma and wet chemical treatments. The interaction of water molecules with silica surfaces has been widely studied beyond the wafer bonding application. Water molecules react with silica surface at room temperature to form silanol groups (Si-OH). This makes the surface hydrophilic. The level of hydrophilicity depends on the chemical structure of the silanol groups and their density [58].

The higher the density of OH groups, the higher will be the binding energy. However, the high amount of OH groups will result in the formation of more water molecules during annealing, which increases the density of thermal voids. Thus, there is a trade-off between the bonding strength and the number of thermal voids per area.

4.2 Removing the sacrificial wafer

After bonding two wafers to each other, the sacrificial wafer needs to be removed. This part of the process is critical for achieving a high degree of thickness homogeneity over the wafer. In the case of SoI fabrication, the well-controlled thermal oxidation of Si makes it possible to thin down the top layer precisely and fabricate SoI wafers with a few nm Si on top. However, Ge oxidation is not that straightforward, and with the technology available, today, it is not possible to homogenously remove Ge. In the case of GoI fabrication, a few hundred microns of Si and Ge materials need to be removed while tens of nm of the top layer stay intact. This is one of the reasons why large-scale ultra-thin GoI wafers are not still commercially available.

Different approaches have been developed for removing the sacrificial wafer and keep the transferring layer intact. Two main techniques are Smart-Cut and etch-back.

4.2.1 Smart-Cut and grinding

The Smart-Cut technique was invented and developed by LETI in 1994. In this method, the donor wafer is implanted with hydrogen atoms before bonding it to the carrier wafer that is placed in contact to form the bonding. The bonded wafers are post-thermal annealed at about 400°C to increase the hydrogen pressure in the platelets and force them to grow laterally splitting the sacrificial wafer into two pieces. In the case of Ge layers, the wafer can be split at even lower temperatures about 300°C because of the stress-induced by thermal expansion coefficient mismatch with Si. After splitting, the top surface is ground and polished to remove the damaged and rough surfaces.

This method is the most common method used nowadays for SoI wafer fabrication. One of its benefits is that that the donating wafer can be reserved and reused after chemical mechanical polishing. In SoI wafers, the residual hydrogen atoms coming from ion implantation are removed during post-thermal annealing. In the case of GoI, however, the residual hydrogen atoms act as p-type doping and limit the carrier mobility [59, 49]. In SoI fabrication, the Si layer can be thinned down to several nm by thermal oxidation. However, the thickness of Ge cannot be reduced homogenously by thermal oxidation, and this makes it difficult to fabricate ultra-thin GoI wafers with high thickness homogeneity through the Smart-Cut technique. Therefore, the etch-back technique was used in this research for the fabrication of ultra-thin GoI wafers for an electronic application.

4.2.2 Etch-back

The etch-back technique is based on chemically etching and removing the donor wafer while keeping the target layer intact. Since wafer thicknesses are in the range of hundreds of µm, the etching processes should be highly selective toward the so-called etch-stop layer to minimize damages to the transferring layer(s). This technique does not need any ion-implantation or CMP which is an advantage over the Smart-Cut technique. However, the donating wafer cannot be reserved. As mentioned earlier, it needs a highly selective etching process which limits its application for different materials.

4.3 Methods for evaluating wafer bonding

Several different techniques have been suggested to characterize and inspect the bonding quality, including mechanical, thermal, structural, and electrical properties of the bonding interface. The key quantities which have been investigated in this thesis are the bonding strength and the stability of the layer in a harsh environment, the density of the voids in the interface, and the interface defect density.

4.3.1 Bonding strength measurement

Evaluation of bonding strength is challenging because of the high degree of data uncertainty. Therefore, many different methods have been proposed and developed to evaluate the adhesion strength properly. Some of the most developed methods are the following: Double cantilever beam (DCB), Tensile testing, Chevron testing, Blistering, and Post-bonding process resilience [57].

4.3.2 Post-bonding process resilience

In this method, the resilience of bonded wafers or transferred layers in different processing steps is used for assessing the bonding strength. This method is qualitative and reveals the density of the non-bonded areas. The portion of the transferred layer which remains intact after the processing is done indicates how strong the adhesion is. Some of the common processing steps used for bonding evaluation are wafer dicing, wet chemical treatment, lithography steps, and cleaning steps.

4.3.3 Voids density measurement

The density of bonding discontinuity is another quality factor for wafer bonding assessment. The bonding discontinuities are called voids, and they are mostly caused by contaminations, particles, surface morphology, or trapped gasses. There are two types of voids: primary voids that are revealed when two wafers are placed in contact and thermal voids that appear after heat treatments for strengthening bonding adhesion. There are two main non-destructive measurement methods for the estimation of voids density that work based on the same principles. These are optical inspection, and scanning acoustic microscopy.

Optical inspection is the most common method for the evaluation of bonding integrity. In optical inspection, light passes through the bonded materials, and the areas that are not bonded are revealed through light scattering. The wavelength of the light should be chosen depending on the mating materials. In the case of Si, which is not transparent in visible light, infrared (IR) light can be used. In this case, the bonded wafers are placed between a source of IR light (which can be a hotplate) and an IR camera. Since the voids area has two interfaces with a gap filled with air or water, the heat or IR light transmission will be different, and those spots can be easily seen in the IR image. An IR image of bonded wafers is illustrated in figure 4.1.

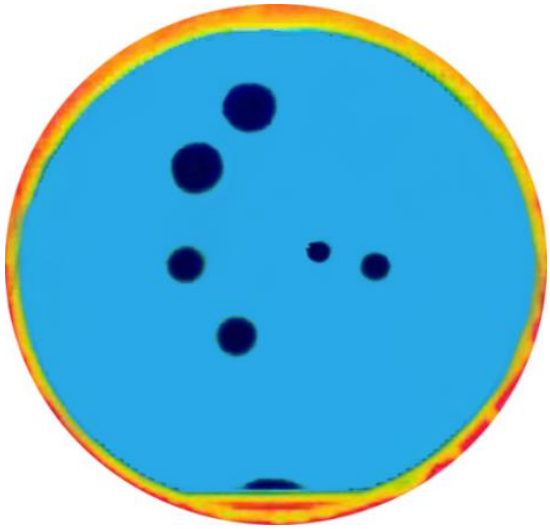

Figure 4.1: IR image of the bonded $SiO_2 - SiO_2$

The IR transmission technique is an inexpensive, fast, and simple method for bonding evaluation. However, the lateral resolution is low, and if the material is not to be transparent to IR light, this technique cannot be applied.

During this research, DBB was used for the evaluation of the initial bonding strength, and IR transmission was used for assessing the bonding integrity. Later, the bonded wafers went through different harsh environments such as wet and dry etching to assess their stability in conventional CMOS processing. In the end, Ge transistors were fabricated on the GoI wafers to investigate the electrical properties of the bonding interface.

4.4 GoI fabrication process in this research

In this research, direct wafer bonding was developed for transferring a single crystalline Ge layer on insulators. Since the epitaxial stack had surface roughness below 1 nm, no CMP was needed for high-yield wafer bonding. However, transferring high-quality Ge layers to insulating materials with sufficiently good yield and thickness uniformity was challenging.

The Ge SRB had an inherent 0.14% tensile strain due to the thermal expansion coefficient mismatch between Si and Ge. This tensile strain led to the formation of micro-cracks when the layer was directly bonded to another wafer and the sacrificial wafer was removed. Despite the low surface roughness of the epitaxial stack, the peak to the valley was in the range of a few nm which means only a portion of the Ge surface was in good contact (distance less than 1 nm) with the insulator to form the needed bonding forces. The unbonded areas are freestanding after removing the sacrificial wafer, and they cannot tolerate the residual strain. As a result. micro-cracks are spread all over the wafer. To overcome this problem, an oxide layer was deposited on the Ge surface by using the atomic layer deposition technique (ALD).

4.4.1 ALD Oxide Deposition

The ALD oxide must fulfill the following requirements to be applicable for wafer bonding and Ge transfer:

- Cover the Ge surface homogeneously,
- Has strong bonding energy with SiO_2,
- Low deposition and baking temperatures,
- Low charge and oxide trap density at the interface with Ge

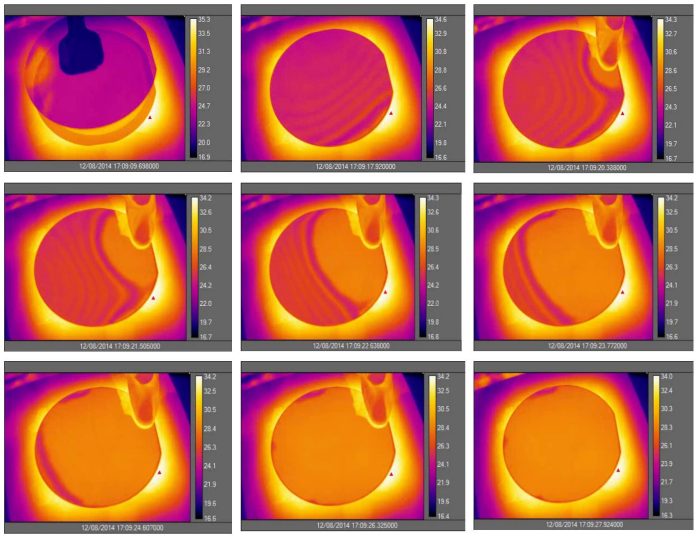

Figure 4.2: IR images of bonding process showing bonding wave propagation through wafer

Among ALD oxides, Al_2O_3 and SiO_2, are well developed and fulfill the requirements. Therefore, they were both deposited on the epitaxially grown stack to be investigated for our wafer bonding process. The Al_2O_3 layer was deposited at 200°C by using trimethylaluminum (TMA) and water as precursors. About 11 nm thick Al_2O_3 was deposited on the Ge layers in 100 cycles of TMA and water. The SiO_2 layer was deposited at 350°C by using AP-LTO-330 and ozone. AP-LTO-330 is the commercial name for the Si precursor manufactured by Airproduct. There were about 100 cycles of exposure to the precursor deposits 11nm of SiO_2.

4.4.2 Wafer Bonding

The wafers were directly bonded to thermally oxidized Si wafers at room temperature. After ALD oxide deposition, the wafers were rinsed in di-water and dried in a rinse-drier tool. The di-water rinsing is mainly for generating OH groups on the surface before wafer bonding. After surface treatment, the wafers were placed in contact with each other, and the bonding process was initiated by applying a small force to the edge of the wafer. The IR images of the bonding process presented in figure 4.2 show how the bonding wave propagated through the wafer. The mated wafers were then post-thermal annealed at different temperatures and durations, investigated by using the IR-camera, and diced in strips for DCB bonding strength measurements.

The initial observations through the IR camera did not indicate any differences between Al_2O_3 and SiO_2, indicating that none of the interfacial layers add roughness to the surface of the layers. There was no statistical relationship between the interfacial layer material and the number of voids before baking. However, the DCB measurements show that the SiO_2 interfacial layer needs baking temperatures higher than 450°C to have a strong bonding with the thermal oxide, whereas baking temperatures as low as 350°C were enough to form a strong bonding between Al_2O_3 and thermal oxide. The higher baking temperature requirement for SiO_2 makes it less attractive for 3D integration applications. Moreover, the interface of Ge/Al_2O_3 has fewer defects when compared to Ge/SiO_2 interface, which makes Al_2O_3 a better candidate for interfacial layer application. For the rest of the experiments during this research, Al_2O_3 was used as the ALD oxide for wafer bonding.

4.4.3 Baking

Baking temperature and duration play an important role in GoI fabrication. In this research, post-bonding baking at different temperatures ranging from 100°C to 600°C was applied to the mated wafers to achieve the highest yield. DCB measurements were performed on the samples, and they show that the bonding strength, in this case, was higher than that in the case of Si bulk in all the samples. However, the DCB method is limited to very low bonding strengths. Therefore, the wafers were post-processed using inductive coupled plasma (ICP) dry etching technique, the TMA hydroxide (TMAH) wet etching technique, and the standard clean 1 (SC1) solution treatment to evaluate the bonding strength through processing. The results show that, if the baking temperature would be lower than 300°C or applied for a too short period, the bonding strength would be low, and the layers get delaminated during the etch-back process. On the other hand, a higher density of thermal voids was observed when the mated wafers were annealed at temperatures higher than 400°C, and the process yield was reduced. Therefore, a baking temperature of 350°C under atmospheric pressure and ambient air conditions, applied for 8 hours, was chosen for the post-thermal annealing of bonded wafers.

4.4.4 Si etching

A combination of dry and wet etching techniques was used for removing the sacrificial Si wafer selectively toward Ge and minimizing the damages that could be caused to the transferring layer. In the first step, the wafer was thinned down to 100 µm by using the ICP etching technique. After etching, about 100 µm of Si was left in the middle of the wafer, while the whole Si layer was etched in the edges. In

the second step, the remaining Si layer was removed in the TMAH bath at 80°C. It should be noted that TMAH etching of Si is strongly selective toward Ge. This selectivity helps in removing the Si layer neatly without causing any damage to the Ge buffer layer.

4.4.5 Ge and SiGe etching

In this research, a novel etching technique was developed for etching 2 µm Ge buffer layer and leave the 20 nm active Ge layer intact. For this purpose, the SiGe layer with 50% Ge content was epitaxially grown on Ge followed by deposition of 20 nm active Ge layer on top. The 50% Ge content was chosen to achieve the highest etch selectivity while minimizing the number of defects in the top layer. Two etching solutions, diluted SC1 and Al etching solution were used for etching the Ge layer and stop on the 10 nm SiGe layer.

For the initial test, a stack of Ge/SiGe/Ge/SiGe (2 µm/30 nm/130 nm/30 nm respectively) was epitaxially grown on a Si substrate. PECVD Si oxide was later deposited on the top and used as a hard mask for patterning and etching mesas. SEM cross-section image of a mesa after selective etching of Ge with the SC1 solution is shown in figure 4.3 from the image, it can be clearly seen that over 400 nm of Ge layer is etched, while 30 nm SiGe layer is intact.

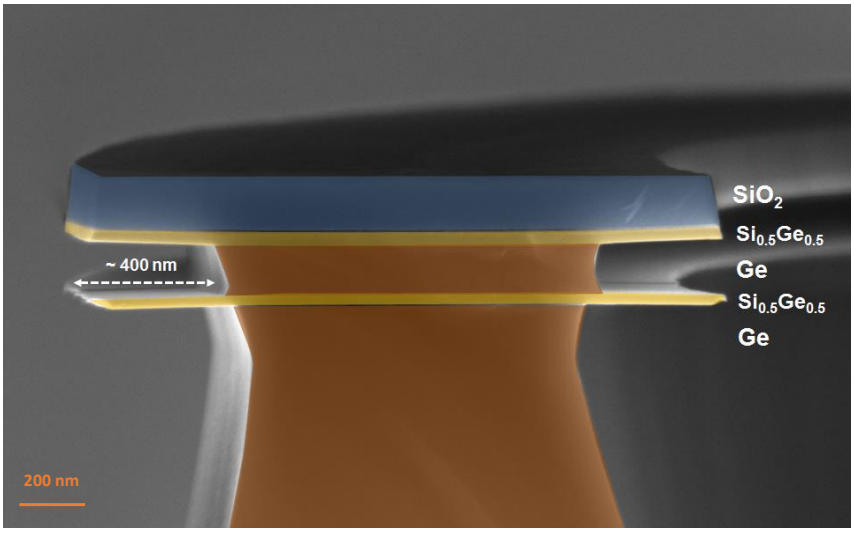

Figure 4.3: SEM cross section image of selectively etched Ge/SiGe/Ge/SiGe stack

The etching mechanism of Ge with the SC1 solution is based on the oxidation of Ge atoms that are soluble in water and deplete from the surface. The etch rate of 200 nm/min was calculated based on the step height measurements before and after etching. In the case of the SiGe layer, Si oxide is not soluble in water and forms a protective layer on the surface and protects the layer from further etching. The thickness of the SiGe layer and formed oxide is shown in figure 4.4. The plot shows that in the initial steps, the SiGe thickness is reduced by 1 nm. This corresponds to fast oxide formation. After 160s of etching with the SC1 solution, the thickness of the SiGe layer is reduced by 1.5 nm, which shows that the further etching rate is negligible. These results prove that a SiGe layer with thickness as low as 3 nm is protective enough to remove a few microns of Ge selectively.

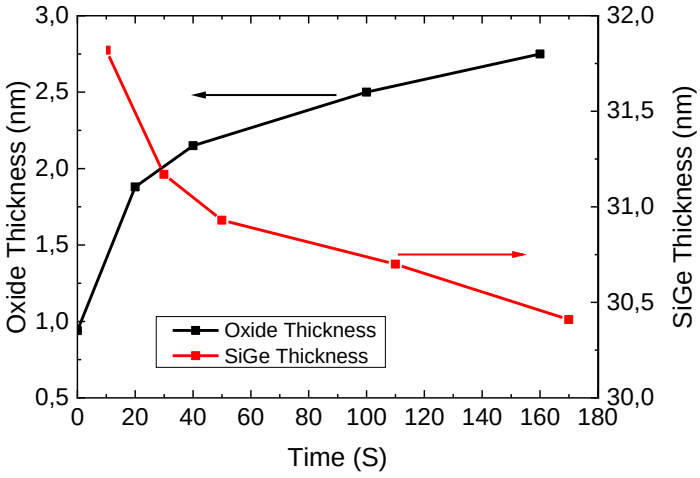

Figure 4.4: Removal of SiGe etch-stop layer and formation of SiO_2 during SC-1 etching

The final step of GoI fabrication is removing the SiGe etch-stop layer. For this purpose, a 5% TMAH solution diluted in Di water at 80°C was used, and the wafers were dipped in the solution for 2 min. The etching selectivity of SiGe to Ge in the TMAH solution was 5, which makes this a good approach for removing the few nm remaining SiGe layer.

An optical image of the final GoI wafer and the thickness wafer map is shown in figure 4.6-a. The few defects on the GoI wafer are due to presence of contaminations which can be improved in the case of industrial-scale fabrications. The thickness of the Ge layer was measured at 25 spots over the wafer with the use of Ellipsometry, and the findings are shown in figure 4.6-b. A thickness homogeneity of over 90% is one of the biggest advantages of this technique compared to conventional GoI fabrication methods. The main cause for thickness non-uniformity is the TMAH

etching of SiGe, which was done by dipping the wafers in the solution bath. This non-uniformity can be resolved by using a single wafer-spraying machine. The unintentional p-type doping of below $10^{16}cm{-}3$ was measured from 4 probe sheet resistance measurements. This residual doping concentration is as per the doping values commonly measured in epitaxially grown Ge layers.

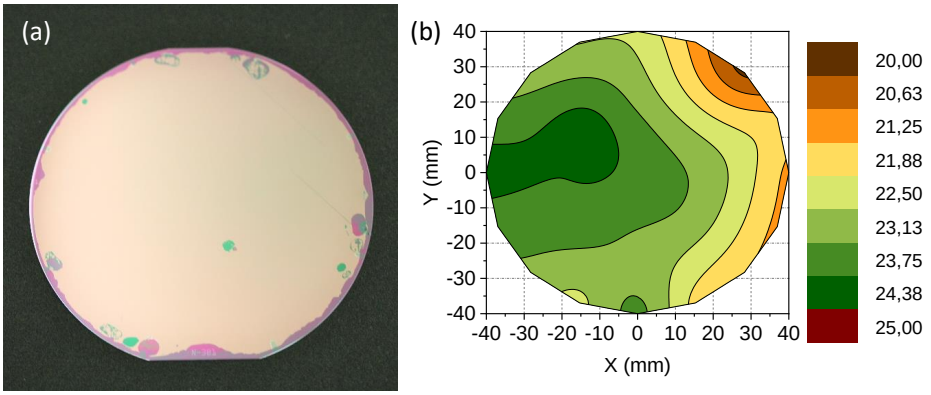

Figure 4.5: a) Optical image of a fabricated GoI substrate, b) Thickness map of a fabricated GoI wafer with 20 nm Ge on top

The surface morphology of the fabricated GoI that was measured using AFM is shown in figure 4.6. The average surface roughness of 0.5 nm was measured over $10 \times 10 \text{ţ} m^2$, which shows that the processes did not add any extra roughness to the surface.

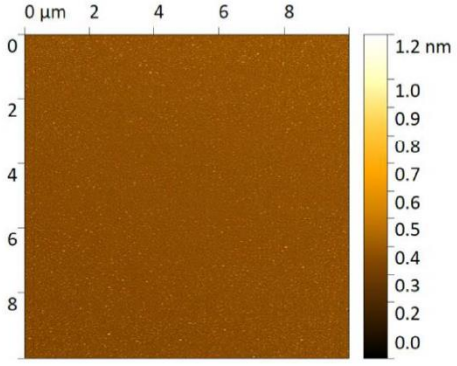

Figure 4.6: AFM image of the surface topography of a fabricated GoI substrate showing RMS below 0.5 nm

Chapter 5

Ge pFET fabrication

In this chapter, the M3D compatible fabrication of Ge pFET devices on GoI substrates are described, and the electrical characterization results are presented.

Ge is one of the best semiconductor choice for high mobility p channel devices to be integrated on Si heterogeneously. Therefore, many papers have reported PMOSFETs fabricated on either bulk Ge [60, 61], or GoI substrates [62]. In [63, 59, 64, 65] GoI PMOSFET devices show promising performances for low power applications. In this part of the thesis, a 3D integration compatible process is developed for the fabrication of Ge pFETs on 25 nm GoI substrates. The pFET devices are characterized to evaluate the quality of the Ge layer and its interface with the insulator box. Device performance homogeneity over the wafer is investigated to evaluate the layer homogeneity and the feasibility of large-scale circuit fabrication.

5.1 Fabrication of Ge pFETs

The fabrication process flow of the Ge pFET devices is described below. The steps involved are the following:

1. The active area of devices and the alignment marks were defined through conventional i-line photolithography and dry etching (HBr, Cl_2) of the Ge layer.
2. Photoresist stripping using oxygen plasma and 1% HF treatment was done before gate dielectric deposition.
3. Gate stack formation:
    - Rapid thermal oxidation at 550°C for GeO_2 formation.
    - 5 nm ALD Al_2O_3 deposition at 200°C.

- 12 nm TiN deposition in a physical vapor deposition (PVD) tool at room temperature.
- 80 nm in-situ P-doped polycrystalline Si deposition in an LPCVD reactor at 560°C.

4. 40 nm PECVD SiO_2 hard mask was deposited on the wafers, and the gate was patterned through photolithography and dry etching.
5. BF_2 ion implantation at 48 keV with dose of $10^{15} cm^{-2}$ for source/drain doping.
6. Gate spacers fabrication:
   - 12 nm ALD SiO_2 deposition at 350°C.
   - 50 nm PECVD SiN deposition at 400°C.
   - SiN anisotropic dry etching.
7. RTA at 600°C for 1 min for dopant activation.
8. Deposition of 400 nm PECVD SiO_2 at 400°C to form interlayer dielectric.
9. Defining and etching the contact holes through lithography and reactive ion etch (RIE) (CHF_2, CF_4) followed by 1% HF treatment.
10. Deposition of 100 nm TiW, 500 nm Al using a PVD tool for metallization.
11. Patterning the contact pads and etching the metal stack using photolithography and RIE.

An optical image of six fabricated chips and a TEM image of a 0.8 µm transistor are presented in figure 5.1. The Ge layer in the active area was not affected or delaminated during the process which is the first indication that the bonding and layer transfer process is sufficiently good for large-scale fabrication. The channel thickness measured from TEM images was 25 nm which is in-line with the ellipsometry values. The gate stack (equivalent oxide thickness [EOT] of 4.3 nm) and the gate spacers are formed with the expected thicknesses showing good process control during device fabrication. The source and drain areas are recrystallized through RTA after ion implantation. However, some crystal damages could still be found.

5.2 Fabrication of SoI pFETs

To have a reference to compare Ge devices with, SoI devices were fabricated through a similar process as the Ge with some minor differences.

- For the gate dielectric, thermal SiO_2 with EOT 4.5 nm was used.
- Ion implantation was done at 9 keV, and dopants were activated with RTA at 1,000°C in N_2 ambient for 10 s.
- Forming gas annealing was performed on the processed wafers at 400°C for 30 min after metallization.

Figure 5.1: Optical image of six chips fabricated on GoI substrate, b) TEM image of 0.8 µm pFET device fabricated on GoI substrate

5.3 Characterizations of Ge pFETs

The $I_D - V_G$ characteristics of a Ge MOSFET with 0.8 µm gate length are presented in figure 5.2-a. The device was turned on and off at both high and low V_D without any need for back biasing which is an improvement over previous GoI pFET studies. The effects of back biasing (V_{BG}) are shown in figure 5.2-b When a positive back bias of more than 20 V was applied, the threshold voltage did not change, and the subthreshold slope (SS) was slightly degraded from the minimum value of 170 mV/dec. When a negative back bias voltage less than -10 V was applied, the back-interface approaches inversion, and the transistor does not turn off anymore. In the absence of back gate bias, the Ge/box interface is depleted. This confirms the low residual dopant density in the Ge layer and the low number of fixed charges at the interface of Ge and the box. The Ge/Box interface state density ($D_{it-back}$), calculated from the linear part of the $V_T - V_{BG}$ curve, was $1 - 2 \times 10^{12} eV^{-1} cm^{-2}$. This interface state density is in line with the D_{it} values extracted from capacitation voltage (CV) curves of Ge/Al_2O_3 MOS capacitors shown in figure 5.3-a.

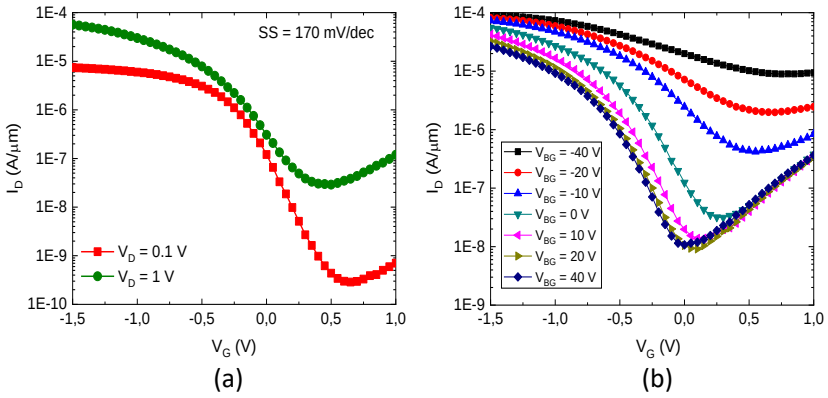

Figure 5.2: a) $I_D - V_G$ characteristics of a Ge MOSFET with 0.8 µm gate length, b) $I_D - V_G$ behavior under back-bias voltage of -40V to 40V

The SS, in this case, is similar to that in the previous studies as is shown in table 2. The $D_{it-front}$ of the front gate calculated from the SS was in the range of $4.5 \times 10^{12} eV^{-1} cm^{-2}$, which can be possibly improved by using better high-K dielectric stacks. The fabricated Ge devices show 60% higher long channel mobility compared to the SoI reference devices as is shown in figure 5.3-b.

LG (μm)	Tb (nm)	EOT (nm)	SS	μh	Reference
0.8	25	4.3	170	170	This research
10	45	-	210	-	[64]
0.07–2.5	60–80	1.8	95–105	110	[65]
9	60	2.1	145	350	[59]
0.1	10	4.5	175	10	[66]
0.17	3	-	116	-	[67]
>100	2.25	-	>190	5–250	[68]
0.1–0.5	25.90	3	165–220	-	[69]

Table 5.1: SS comparison with literature

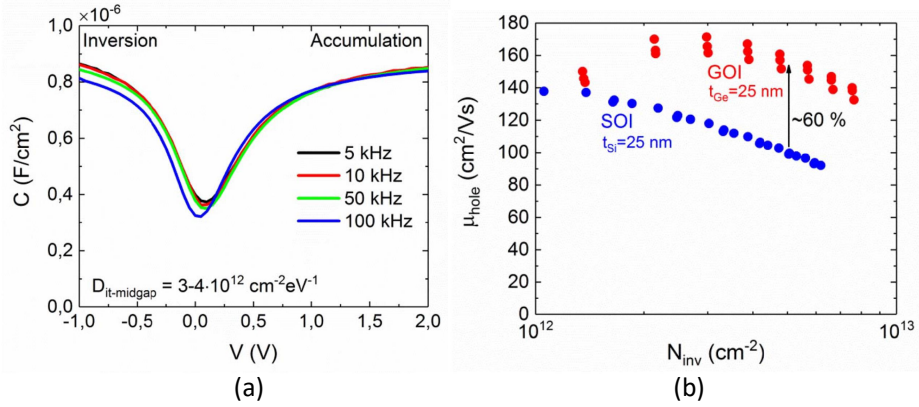

Figure 5.3: a) CV curves of Ge/Al_2O_3 MOS capacitors, b) Carrier mobility in GoI and SoI pFET devices

The threshold voltage of pFETs mapped over the wafer is shown in figure 5.4. The devices with VT out of the presented range and the devices which did not work are shown in black. A yield of 70% was achieved with not working devices mostly where Ge was not attached properly to the box and got removed during the etch-back process. The median V_T of Ge and reference Si pFETS were -0.18 V and -0.65 V respectively. TCAD simulations without considering any fixed charges in neither front nor back interfaces estimated a V_T shift of 0.47 V between GoI and SoI devices which was in line with the data we collected for our experiment.

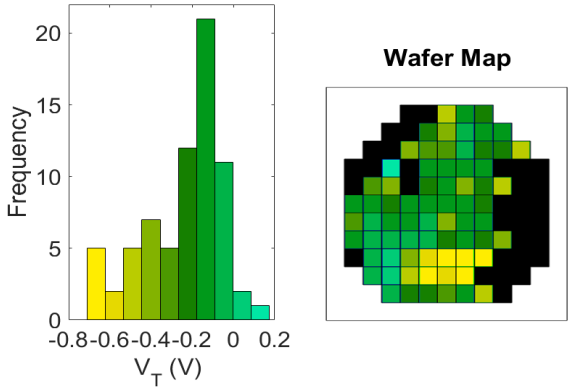

Figure 5.4: Threshold voltage map over wafer

Advantages for Ge M3D integration:

The results of device characterizations show that the Ge/Box interface is not substantially degraded by oxide charges. The yield of 70% proves that our GoI fabrication process can be implemented for large-scale fabrication of SD circuits. The 60% higher carrier mobility compared to Si devices can improve CMOS performance. However, the front gate dielectric and the contact formation need to be improved to decrease the SS and contact resistivity.

The Ge pFETs fabrication process in this work is compatible with M3D integration in terms of temperature budget. The highest processing temperature was kept at 600°C for 1 min, which is in the accepted range for M3D integration. The results presented in this chapter show that the Ge layer transfer process is ready for implementation on Si devices for second-tier and higher-tier device levels in M3D integration.

Chapter 6

Improvement of Ge transistors performance

In this chapter, Si surface passivation, and selective epitaxial growth of SiGe layers in the source and drain area are presented for Ge pFETs performance improvement.

The measurement result from our Ge pFETs' characterizations shows that the following two areas of the fabrication process need to be improved:

- Gate dielectric material
- Contact formation

For improving the SS, a unique Si cap process was developed that was integrated with our thulium oxide dielectric to form a high-quality high-K dielectric on Ge. SEG of highly doped SiGe layers in the source and drain areas was investigated with the objective of reducing contact resistivity.

6.1 Si Cap epitaxial growth on Ge to passivate the surface

The subthreshold slope value achieved in this work is much higher than the theoretical value (60 mV/decade), which can be achieved at room temperature in fully depleted devices. In the main, this discrepancy is due to the parasitic capacitance of interface states and oxide charges at the Ge/Gate dielectric interface. In this part of the thesis, we elaborate about how the Si cap layer was developed for Ge surface passivation and gate dielectric material development.

6.1.1 Si passivation layer deposition

The challenges of creating high-quality GeO_x/Ge interface has inspired interest in the passivation of Ge surface with Si atoms and the development of High-K/Si/Ge gate stack. It has been shown that Si passivation can enhance mobility and reliability of Ge devices while reducing the D_{it} [70, 71]. However, the 4% lattice mismatch between Si and Ge and the Ge atoms' diffusion in the Si layer makes it challenging to grow high-quality Si cap layer. The two main parameters of the Si cap processing that can influence the overall performance of Ge devices are the thickness of the Si passivation layer and the epitaxial growth conditions of the Si layer.

The critical layer thickness of Si on Ge is below 12 monolayers depending on process conditions [72]. At thicknesses above 12 monolayers, the D_{it} value increases as a result of plastic strain relaxation. Therefore, the Si cap layer's thickness should be kept below 10 monolayers to suppress plastic strain relaxation and crystal defect formation. However, it has been found that charge carrier mobility in the channel region decreases by decreasing the thickness of the Si cap layer [73, 74]. As a result, the optimum thickness of the passivation layer is limited to 6–8 monolayers to achieve the highest carrier mobility and the lowest D_{it} value [72].

The second parameter is the epitaxial process conditions, which can be divided into four main parts: the method, the precursor, the temperature, and the pressure. The Si passivation layers have been grown by MBE and CVD techniques by different contributors. The MBE growth results show island formations and Ge diffusion in the Si layer at elevated temperatures and amorphous layer formation at room temperature [75, 76]. The initial CVD epitaxial growth of Si layer on Ge substrates was performed at temperatures as high as 550°C, which resulted in Ge segregation toward the surface [77]. The contributors explained that the first monolayers of Si on Ge are formed based on the lower energy of Ge-H bonds compared to Si-H bonds. However, they used 550°C annealing for hydrogen desorption that resulted in Ge segregation. Later, it was shown that when the Ge surface is covered by hydrogen, a reversible place exchange happened between Si and Ge atoms at temperatures around 350°C. This atomic place exchange drives the Si atoms to the surface to form an H-covered Si surface that has 30meV lower energy compared to H-covered Ge surface. By increasing the temperature to 550°C, all H desorbs from the surface, and Ge atoms return to the surface again [77]. Therefore, the growth process temperature should be limited to temperatures below 550°C to suppress Ge segregation.

Different Si precursors such as SiH_4, Si_2H_6, Si_3H_8, and Si_4H_{10} were investigated by the contributors in the CVD tools to develop Si passivation processes at low temperatures [78, 79]. However, economically beneficial, well-controlled epitaxial growth of Si passivation layer with high thickness homogeneity is still a challenge. The Si cap layers grown by silane were not successful since the growth tempera-

ture needs to be higher than 500°C and the Ge atoms segregate on the Si surface. The higher Si order precursors such as Si_3H_8, and Si_4H_{10} at growth temperatures below 450°C have shown promising results. To achieve high deposition rates and enhance H desorption, the layers are grown at atmospheric pressure and nitrogen ambient conditions. CVD growth of Si passivation layer with Si_2H_6 and Si_3H_8 at reduced pressure and H ambient conditions were not investigated to our knowledge.

In this research, Si_2H_6 and Si_3H_8 at reduced pressure were investigated to develop high-quality ultra-thin Si layers on Ge. The process details and the results in this regard are presented below.

To find a suitable Si precursor a series of Si layers were grown at different temperatures using disilane, and trisilane. These layers were grown at temperatures ranging from 400°C to 650°C, while the pressure was kept at 20 Torr and H_2 was used as the carrier gas. The growth rates versus temperature findings are plotted in figure 6.1. Trisilane and disilane, behaved similarly at temperatures below 500°C. Growth rates as high as 1 nm/min were reported for Si growth at temperatures below 450°C. This result shows that at reduced temperatures, the reaction is more controlled by hydrogen desorption from the surface rather than gas decomposition. Using trisilane needs an evaporation system since it is in the liquid phase at room temperature. Such a system makes it difficult to develop a reproducible homogenous layer over a long period of deposition. Therefore, disilane was used for the epitaxial growth of the Si cap layer at temperatures below 450°C. Deposition temperature of 400°C was chosen, which is the minimum temperature at which Si layers can be epitaxially grown in our process conditions. The deposition rate was $\approx$ 2 nm/hr with thickness inhomogeneity of 2% over 100 mm wafer.

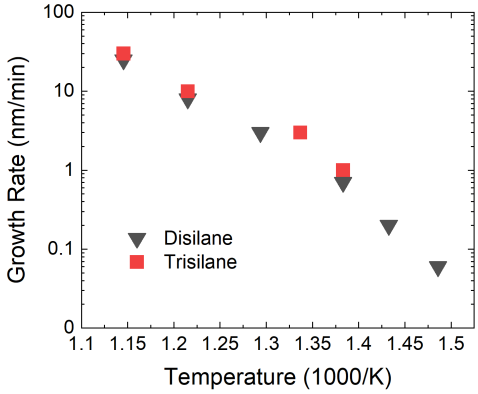

Figure 6.1: Growth rate of Si versus temperature using silane, disilane, and trisilane

The initial presence of Si cap was confirmed by the hydrophobicity test. Later, the thickness was extracted from spectroscopy ellipsometry measurements and TEM

images. The Si cap layers were deposited on in-situ phosphorous dopped Ge buffer layers for MOS capacitor fabrication and electrical characterization. The Si cap deposition duration was changed from 30 min to 60 min to find the right thickness, and the temperature was varied by ± 3°C to evaluate the robustness of the process.

6.1.2 Ge MOS capacitor fabrication using Si passivation

To evaluate the Si passivation layer, the MOS capacitors were fabricated on the Ge/Si layers and electrically characterized by our collaborator at KTH. After Si Cap deposition, the active areas were defined through hard mask deposition, photolithography, and dry etching, and a well-developed, in-house gate dielectric [80, 81] was deposited on top. The remaining hard mask layers was removed from the active areas' surface through 1% HF treatment before gate stack formation. Then 7.4 nm ALD Tm_2O_3 was deposited at 225°C using $TmCp_3$ and H_2O precursors followed by post-RTA at 550°C in nitrogen ambient conditions to form thulium silicate interfacial layer. The ALD HfO_2 layer was deposited at 350°C (targeting 5.6 nm thickness) using $HfDO_4$ and H_2O precursors, and post-deposition it was annealed for 10 min in O_3. The gate stack deposition was completed by deposition of ALD TiN gate metal at 425°C using $TiCl_4$ and NH_3 precursors. Then 500 nm AL was used for metallization. It was patterned and dry etched to define contact pads for electrical probing. The wafers went through forming gas annealing for 30 min at 400°C in H_2/N_2 ambient before characterizations. The process flow of the MOS capacitors' fabrication and the cross-section schematic and TEM images are shown in figure 6.2.

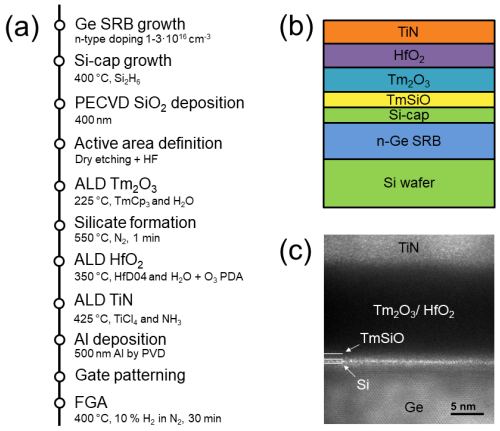

Figure 6.2: a) Process flow for fabrication of MOS capacitors, b) Schematic cross-section of gate stack, and c) TEM cross-section image of fabricated gate stack

CV characteristics of a MOS capacitor are shown in figure 6.3. The Si cap was grown at 400°C for 40 min and no substantial-frequency dispersion was visible in the CV curve. EOT and D_{it} were extracted from CV curves of 10 MOS capacitors over the whole wafer. EOT was found to be 3.75–3.8 nm and D_{it} was 2˘4 × $10^{11}eV^{-1}cm^{-2}$. The reference MOS capacitor showed similar D_{it} values. The D_{it} values were consistent with those of the previously reported $Si/TmSiO/Tm_2O_3$ MOS capacitors ($D_{it} \approx 10^{11}eV^{-1}cm^{-2}$), which indicates that the gate stack is efficiently transferred to Si passivated Ge.

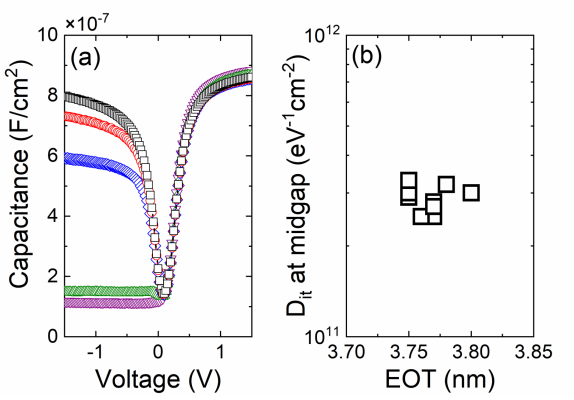

Figure 6.3: (a) CV characteristics of $Ge/Si/TmSiO/Tm_2O_3/HfO_2/TiN$ gate stacks with Si-cap. (b) Interface state density is 2–4 × $10^{11}eV^{-1}cm^{-2}$ at EOT of 3.75-3.8 nm

The D_{it} values of MOS capacitors with different Si cap deposition times (30–60 min) are shown in figure 6.4. The minimum D_{it} of $3 \times 10^{11}eV^{-1}cm^{-2}$ was achieved at 40 min deposition of Si cap at 400°C. Shorter deposition time increased the D_{it} significantly to values above $10^{12}eV^{-1}cm^{-2}$. This higher D_{it} value could be due to the smaller thickness of the Si cap layer, which is partially consumed in the gate stack formation. Longer deposition times also increased the D_{it} values to above $10^{12}eV^{-1}cm^{-2}$, which can be the result of strain relaxation and defect formation in the Si cap layer.

Oxide trap density N_{ox} of both Si passivated and reference MOS capacitors were calculated from hysteresis of a dual CV sweep. The N_{ox} values are presented in figure 6.5 as a function of the oxide electric field Eox which is defined as:

$$E_{ox} = \frac{V_{G,max} - V_{FB}}{CET} \tag{6.1}$$

where $V_{G,max}$ is the maximum voltage applied in the dual sweep, V_{FB} is the flatband voltage, and CET is the capacitance equivalent thickness. The Si passivated gate dielectric shows hysteresis as low as 3 mV at Eox of 4 MV/cm, which

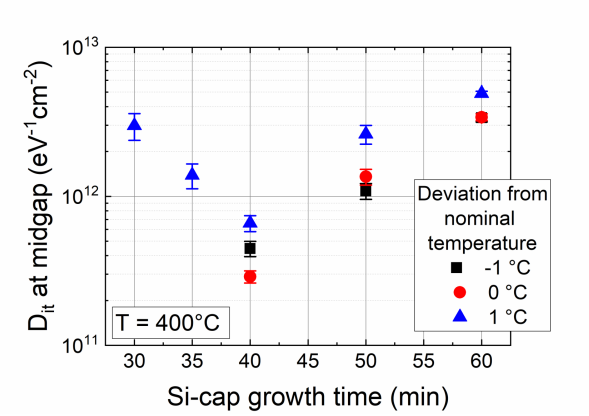

Figure 6.4: Interface state density of $Ge/Si/TmSiO/Tm_2O_3/HfO_2/TiN$ gates as a function of Si-cap growth time. Average over 10 measuring devices is displayed. Standard deviation is indicated with error bars

corresponds to N_{ox} of $1.5 \times 10^{10} cm^{-2}$. This value is significantly lower than the N_{ox} values of the reference devices without Si passivation ($N_{ox} \approx 2 \times 10^{11} cm^{-2}$). The result suggests that the Si passivation method developed in this research can improve the reliability of Ge devices while keeping the D_{it} to low values.

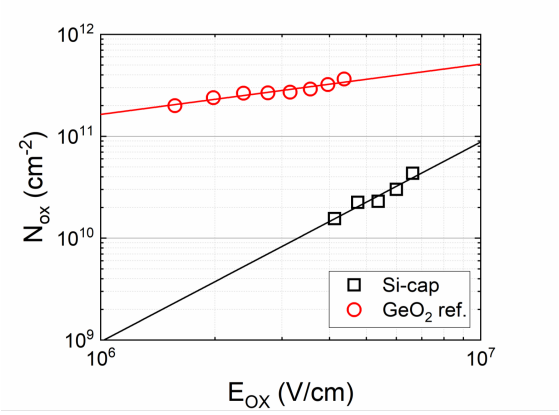

Figure 6.5: Oxide trap density N_{ox} extracted from CV hysteresis as function of oxide field Eox. Si-cap devices exhibit more than 20 times lower oxide trap density than reference GeOx devices

Advantages of M3D integration

In terms of process integration, the epitaxial growth of the Si passivation layer was developed. The MOS cap fabrication and electrical characterization show that this process can be integrated into Ge electronics and has the potential to improve the Ge/gate interface and reliability. In terms of temperature budget for M3D integration, the Si cap layer growth and gate dielectric formation are performed at temperatures below 550°C, which is compatible with 3D integration. However, the Ge surface needs to be in-situ hydrogen baked at 800°C before Si cap deposition. This baking temperature can be reduced by using longer baking times at lower temperatures along with using cluster tools with an in-situ cleaning station.

6.2 Selective epitaxy for source and drain

Junction formation is one of the most critical aspects of Ge transistors' fabrication. Low dopant solubility in Ge makes it challenging to form highly doped source/drain regions and achieve low parasitic resistance. Traditionally, ion implantation and post thermal annealing were used for junction formation in Ge devices [82, 83, 84, 85, 86]. However, Ge crystals are damaged during ion implantation, and high-temperature treatments are required to recrystallize the Ge layer and anneal out the defects [87, 88, 89]. SEG of in-situ doped SiGe has been implemented on Si technology for shallow and abrupt junction formation [90, 91, 92, 93, 94, 95, 96]. The same technique can be integrated on Ge pFET devices for junction formation. SEG of in-situ doped SiGe is an implantation-free process that can be achieved at different temperatures. Therefore, it has the potential to overcome Ge pFET's junction issues.

In this part of the thesis, the findings of an investigation of the SEG of in-situ doped SiGe layers as source/drain material have been provided. Planar p^+/n diodes were fabricated and characterized on both Si and Ge bulk wafers to investigate the junction leakage and benchmark toward other Ge junctions. The reason for performing the experiments on bulk materials was to eliminate the other sources of junction degradation.

6.2.1 In-situ doped SiGe growth

SEG of in-situ boron-doped SiGe layers with 27% Ge content was performed both on n Ge and n Si substrates. The process conditions were as follows:

1. 200 nm PECVD SiO_2 was deposited and patterned through i-line lithography to define the openings.
2. 180 nm of SiO_2 in the openings was removed through dry etching.
3. 20 nm remaining oxide was cleared by 1% HF treatment.
4. The wafers were loaded to the RPCVD tool for SiGe growth right after HF treatment through a load-lock to minimize surface oxidation.
5. Substrates were baked in hydrogen ambient conditions at 800°C for 10 min to remove the native oxide and prepare the surface for epitaxial growth.
6. SiGe layers were deposited at 650°C and pressure of 20 Torr using DCS and germane (10% diluted in hydrogen) as Si and Ge precursors, respectively. For in- situ doping, B_2H_6 (1% in Hydrogen) was used for p-type doping.

7. A metal stack of 100 nm TiW and 500 nm Al was sputtered on the surface and patterned through photolithography and dry etching to form contacts to PN diodes for electrical characterizations of the layers.

Surface morphology was investigated with AFM, and the dopant concentration was measured with secondary ion mass spectroscopy (SIMS) and resistivity measurements (figure 6.6). The AFM images confirm that the surface roughness of the P^+-SiGe layer was below 3 nm after the epitaxial growth. The higher RMS of SiGe layers compared to the Ge buffer was due to partial strain relaxation of the layers. The partial strain relaxation eliminated the thickness fringes besides the SiGe peak in the HRXRD rocking curve shown in figure 6.7. The SIMS spectra show that dopant concentration of $2.5 \times 10^{19} cm^{-3}$ was achieved in the P^+SiGe layer with a resistivity of 3.5 mΩcm. Ge content of 27% was measured with SIMS, which agrees with Ellipsometry values.

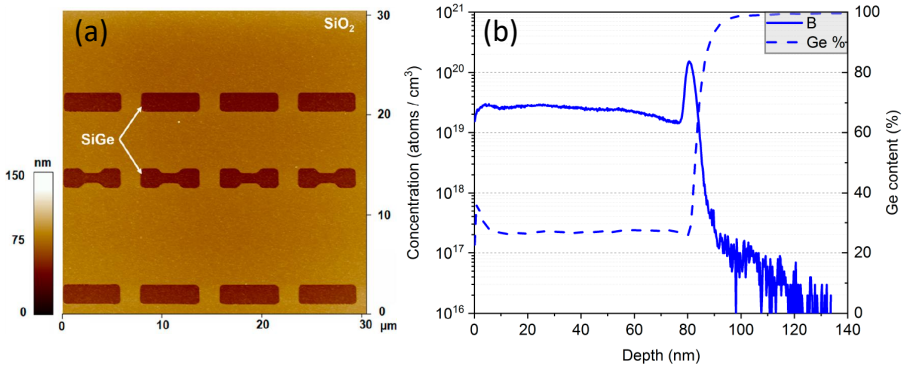

Figure 6.6: a) AFM image (35 µm × 35 µm) of the $p^+Si_{0.73}Ge_{0.27}$ film grown selectively on Ge. b) SIMS analysis on 80 nm $p^+Si_{0.73}Ge_{0.27}$ film grown selectively on Ge

PN diodes were fabricated and characterized by collaborators to evaluate the junction quality by investigating the reverse leakage current (IR) at 1V bias. The forward current was in the same order of magnitude for different diode areas, and it was mainly limited by the resistance of the bulk wafer and the backside contact. The reverse current was, however, scaled with the diode area.

Two types of leakage currents contributed to the total reversed current, i.e., area current (I_A) and perimeter current (I_P). The results show that for small diodes with a perimeter of less than 12 µm, the I_P has the strongest contribution to the leakage current. However, increasing the perimeter to more than 12 µm, the I_A becomes dominant. Leakage current density of $2.2 \times 10^{-2} A(cm)^{-2}$ was measured

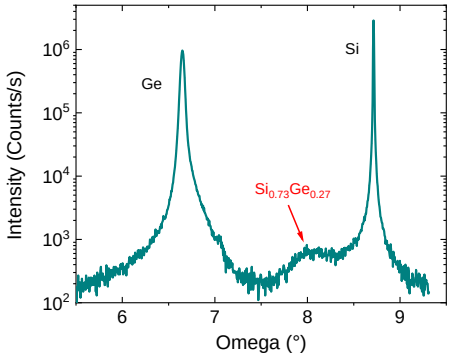

Figure 6.7: XRD rocking curve of selectively grown SiGe layer on Ge buffer layer on Si substrate acquired by scanning omega/2tetha around (224) direction

for the largest diodes with an area of 104 μm^2. This leakage current density is comparable to the values reported in other studies.

M3D integration application

In terms of process integration, selective epitaxial growth of highly doped SiGe material at source/drain is currently integrated into the Si CMOS technology. However, when it comes to integration using M3D Ge MOSFETs, the gate material and the spacers need to be encapsulated in a passivation layer to eliminate non-selective growth. The ex-situ and in-situ surface preparations should be modified to protect the fabricated devices and the interconnections. From the temperature budget point of view, the process temperature should be kept below 600°C, which can be fixed by choosing other precursors with lower cracking temperatures.

Chapter 7

Conclusions and outlook

This chapter concluded the thesis with summary and outlook

7.1 Summary

Our research was focused on the development of a Ge active layer for monolithic 3D integration circuit technology. For this purpose, epitaxial growth, wafer bonding, etch-back technique, device fabrication, and optimization processes were designed and developed to present the proof-of-concept application of Ge in M3D integration.

For the development of the bonding stack, the Ge SRB layer, the fully strained SiGe etch stop, and the Ge active layer were epitaxially grown on Si substrates in an RPCVD reactor. ($PapersI\breve{}II$)

- The process parameters were adjusted to grow 2.5 µm Ge layers with TDD of $10^7 cm^3$ and surface roughness of 0.5 nm without any need for CMP.
- A fully strained $Si_{0.5}Ge_{0.5}$ layer on Ge was developed and implemented as an etch-stop layer to protect the transferring Ge layer.
- The active Ge layer was epitaxially grown on the SiGe layer at low temperatures to prevent strain relaxation of the SiGe layer and minimize Si-Ge atoms' interdiffusion.

Room temperature wafer bonding and a unique etch-back process were developed to remove the sacrificial wafer and leave the 20 nm Ge on the insulator intact. ($PaperIII$)

- Room temperature wafer bonding with a high yield was developed by using ALD Al_2O_3 and SiO_2 intermediate layers.

- Baking temperature of 350°C was used for 8 hrs to form strong bonding at the interface of the wafers while staying in the safe temperature region for M3D integration.
- A series of wet and dry etching techniques were used for removing the sacrificial wafer and 2.5 µm Ge buffer while protecting the 20 nm active Ge layer.
- Further, 20 nm GoI substrates were fabricated with thickness inhomogeneity of 5% over 100 mm substrate and surface roughness of 0.5 nm without using any ion-implantation and CMP.

Ge pMOS devices were fabricated on our GoI substrate for layer and interface characterizations. ($PaperIII$)

- The max processing temperature was kept below 600°C so that it could be M3D integration friendly.
- About 70% device yield over the wafer confirms the high reliability of the GoI fabrication process.
- GoI pFET devices exhibit 60% higher carrier mobility than SoI pFET reference devices.
- Contact resistivity and SS were much higher than expected.

To improve the performance of Ge top-tier devices, alternative junction materials and gate dielectrics were developed. ($PapersIV and V$)

- A Sub nm Si cap layer was developed to passivate the Ge surface for gate dielectric formation.
- Interface state density of $3\times10^{11}eV^{-1}cm^{-2}$ was achieved from the integration of Si passivation layer with an already developed gate stack in MOS capacitor.
- The Si passivated gate dielectric shows hysteresis as low as 3 mV at Eox of 4 MV/cm, which corresponds to N_{ox} of $1.5\times10^{10}cm^{-2}$.
- Selective epitaxial growth of highly doped SiGe was developed for improving the junction quality of Ge devices.
- P^{+}-SiGe/Ge junctions were formed with leakage current in the same magnitude as ion implantation and SoD methods.

In conclusion, the technologies and processes designed and developed in this our research and presented in this thesis can be integrated into monolithic 3D integration of Ge pFETs on top of Si nFETs to fabricate high-performance CMOS circuits. The Ge layer transfer technique shows high process yield and thickness homogeneity over the wafer. The Ge pFET processing temperatures are compatible with M3D integration. The device's performances indicate that integration of Ge as top-tier material is feasible for future 3D circuits. The Si passivation technique can reduce the D_{it} to enhance the charge carrier mobility of Ge while decreasing the oxide trap density to improve reliability. Selective epitaxy of highly doped SiGe on Ge was achieved. This can improve the junction formation in Ge devices.

7.2 Outlook

Fabrication of high-quality GoI substrates and high-performance Ge devices for M3D applications continues to be challenging. Our research that has been presented in this thesis has addressed the many issues that are faced in the utilization of Ge as the top-tier material for pFETs' fabrication. All the steps from Ge epitaxial growth to gate dielectric and further to junction improvement were investigated, and we have provided solutions for dealing with the said challenge. However, we believe that these processes can be further improved in terms of the processing temperature, yield, and integration.

Temperature budget: The processing temperature for pre-epitaxy in-situ cleaning still exceeds the accepted M3D integration temperature budget. This temperature can be reduced further by improving the ex-situ surface treatments and implementing cluster tools with cleaning units. The application of other precursors can be investigated for selective epitaxial growth of highly doped SiGe layer for junction formation to decrease the process temperature even more.

GoI fabrication: The processes described in this thesis were performed in a research facility and were mostly carried out manually. Using cluster tools for wafer bonding would have minimized particle contaminations and voids. The Ge pFETs that did not work were in the areas where Ge got lifted during the etch-back process. By improving the wafer bonding, the overall fabrication yield can be increased significantly. Wet etching was performed by dipping the wafers in solution baths. This method decreased the etching homogeneity and increased the inhomogeneities over the wafer. Using a single wafer wet chemical etching tool would improve the homogeneity.

Ge pFETs fabrication: The highly doped SiGe selective epitaxial growth and the Si passivation layer can potentially enhance Ge pFETs performances and their reliability. These processes need to be integrated with Ge device fabrication while the maximum temperature needs to be kept in the M3D integration budget. The re-crystallization of source and drain area after ion implantation needs to be further investigated. Integration: Finally, Ge pFETs need to be integrated with Si nFETs, and the devices need to be interconnected to form CMOS circuits.

As a conclusion, M3D will be a part of the future circuits' fabrication. The 3D integration is already implemented in memories and sensors showing significant performance enhancements, and the M3D is not far from commercialization.

Acknowledgements

This thesis is a summary of the research achievements during my PhD studies which none of them would be possible without the enormous help I received from all my colleagues, friends, and the people around me. I would like to express my gratitude to the people who shaped me as who I am now.

First, I would like to thank my main supervisor, Prof. Mikael Östling for his continuous supports, mentorship, encouragements, and advices. I have learned a great deal from your positive attitude, valuable insights, and project management approaches. You have been a great source of inspiration for me, and I feel privileged to work under your supervision.

I wish to thank my co-supervisor Per-Erik Hellström. Your invaluable processing advices thought me to always see the bigger picture and think about reproducibility, high yield, and large scale production. I would also like to thank my former supervisor Henry Radamson for introducing crystal growth to me and motivating me to pursue a PhD degree.

I would like to thank Mattias Hammar for the great insights regarding epitaxial growth and the invaluable feedbacks on my thesis. I like to thank my M.SC. thesis supervisor Anand for his supports during all these years. I would like to thank Bellman, Anders, Gunnar, Ana, Saul, Jiantong, Christian, Gabriel, and Yong Bin for the helps and advice they gave me in various areas of my PhD studies. I thank Gunilla, Madeleine, and Susy for enormous helps with the administration tasks.

My great gratitude to our collaborators from Uppsala University. Lukas and Zhen it was nice working with you in the Ge 3D project.

My gratitude and thanks go to the cleanroom friends and colleagues who unconditionally helped me through my work in Electrom. I would like to thank Cecilia Aronsson for being my lab encyclopaedia and giving solution for all my processing issues. Many thanks to Reza for creating a friendly atmosphere in the cleanroom and being such a great friend. Thanks Arman, Anders, Aleks, Sven, Mikke, Krister, Nils, Magnus, and Roger for the nice chats, fixing the tools, and the helps through my work. Nothing would be possible without your helps. Smilja, Susanne, Ulof,

Dan, Helena, Tuan, and Sara thanks you all for sharing the lab, the tools, and your invaluable knowledge with me.

I would like to thank my wonderful office mate and an amazing friend Szymon. I enjoyed every minute I spent with you, and I always admire you. I will never forget the taste of your beers. Konstantinos Garidis, you are the most generous and supportive person I know, and I am grateful for our friendship and the years we worked together. You are excellent at everything you do, especially rolling cigarettes. Thanks for all the helps. Special thanks to Pooria for being such an amazing friend and colleague. I enjoyed all the discussions and collaborations we had all these years. I wish to thank Laura for all the collaborations, fika chats, amazing cakes, and the friendship. I feel so lucky to have such amazing colleagues in our team.

I wish to thank my friends and colleagues at KTH who helped me through this journey and made Electrum my second home. The lunches, fikas, weird discussions, ping pong, and foosball times were one of the best moments of my time at KTH. Sam, Azin, Arash, Hossein, Mohsen, Adrin, Sohrab, Reza, Maz, Carl, , Tobias, Panos, Mattias, Corrado, Victoria, Alex, Gabriel, thank you all! You are all amazing.

And of course, millions of thanks to my wife Mahsa for unconditionally supporting me during all these years.

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Stockholm, 2021

Bibliography

[1] J. S. Kilby, "Miniaturized electronic circuits, US Patent 3138743," *US Patent, US3138743A*, 1959.

[2] G. M. Moore, "Cramming more components onto integrated circuits With unit cost," *Electronics*, vol. 38, no. 8, p. 114, 1965. [Online]. Available: https://newsroom.intel.com/wp-content/uploads/sites/11/2018/05/moores-law-electronics.pdf

[3] D. Frank, R. Dennard, E. Nowak, P. Solomon, Y. Taur, and Hon-Sum Philip Wong, "Device scaling limits of Si MOSFETs and their application dependencies," *Proceedings of the IEEE*, vol. 89, no. 3, pp. 259–288, 3 2001. [Online]. Available: http://ieeexplore.ieee.org/document/915374/

[4] S. Kawamura, N. Sasaki, T. Iwai, M. Nakano, and M. Takagi, "Three-dimensional CMOS IC's Fabricated by using beam recrystallization," *IEEE Electron Device Letters*, vol. 4, no. 10, pp. 366–368, 10 1983. [Online]. Available: http://ieeexplore.ieee.org/document/710867/https://www.jstage.jst.go.jp/article/elex/12/7/12_12.20152001/_articlehttp://ieeexplore.ieee.org/document/1483510/

[5] K. Shafique, B. A. Khawaja, F. Sabir, S. Qazi, and M. Mustaqim, "Internet of Things (IoT) for Next-Generation Smart Systems: A Review of Current Challenges, Future Trends and Prospects for Emerging 5G-IoT Scenarios," *IEEE Access*, vol. 8, pp. 23 022–23 040, 2020. [Online]. Available: https://ieeexplore.ieee.org/document/8972389/

[6] J. Bardeen and W. H. Brattain, "Transistor, a semiconductor triode," *Proceedings of the IEEE*, vol. 86, no. 1, pp. 29–30, 1998.

[7] J. FISHER and H. GATLAND, "The Semiconductor," *Electronics – from Theory Into Practice*, pp. 1–49, 1976.

[8] J. S. Kilby, "Invention of the Integrated Circuit," *IEEE Transactions on Electron Devices*, vol. 23, no. 7, pp. 648–654, 1976.

[9] J. Knechtel, O. Sinanoglu, I. A. M. Elfadel, J. Lienig, and C. C. N. Sze, "Large-Scale 3D Chips: Challenges and Solutions for Design Automation, Testing, and Trustworthy Integration," *IPSJ Transactions on System LSI Design Methodology*, vol. 10, pp. 45–62, 2017. [Online]. Available: https://www.jstage.jst.go.jp/article/ipsjtsldm/10/0/10_45/_article

[10] R. Radojcic, "More-than-Moore Technology Opportunities: 2.5D SiP," in *More-than-Moore 2.5D and 3D SiP Integration*. Cham: Springer International Publishing, 2017, pp. 5–67. [Online]. Available: http://link.springer.com/10.1007/978-3-319-52548-8_2

[11] "Sony IMX260 dual pixel AF sensor.pdf." [Online]. Available: http://image-sensors-world.blogspot.com/2016/03/sony-imx260-in-samsung-galaxy-s7.html

[12] H. Tsugawa, H. Takahashi, R. Nakamura, T. Umebayashi, T. Ogita, H. Okano, K. Iwase, H. Kawashima, T. Yamasaki, D. Yoneyama, J. Hashizume, T. Nakajima, K. Murata, Y. Kanaishi, K. Ikeda, K. Tatani, T. Nagano, H. Nakayama, T. Haruta, and T. Nomoto, "Pixel/DRAM/logic 3-layer stacked CMOS image sensor technology," in *2017 IEEE International Electron Devices Meeting (IEDM)*, vol. 1, no. d. IEEE, 12 2017, pp. 1–3. [Online]. Available: http://ieeexplore.ieee.org/document/8268317/

[13] R. N. Noyce, "Semiconductor device-and-lead structure," 1961.

[14] C. Fenouillet-Beranger, B. Mathieu, B. Previtali, M.-P. Samson, N. Rambal, V. Benevent, S. Kerdiles, J.-P. Barnes, D. Barge, P. Besson, R. Kachtouli, M. Casse, X. Garros, A. Laurent, F. Nemouchi, K. Huet, I. Toque-Tresonne, D. Lafond, H. Dansas, F. Aussenac, G. Druais, P. Perreau, E. Richard, S. Chhun, E. Petitprez, N. Guillot, F. Deprat, L. Pasini, L. Brunet, V. Lu, C. Reita, P. Batude, and M. Vinet, "New insights on bottom layer thermal stability and laser annealing promises for high performance 3D VLSI," in *2014 IEEE International Electron Devices Meeting*, vol. 2015, no. February. IEEE, 12 2014, pp. 1–27. [Online]. Available: http://ieeexplore.ieee.org/document/7047121/

[15] M. Östling, E. Dentoni Litta, and P.-E. Hellström, "Three-Dimensional Integration of Ge and Two-Dimensional Materials for One-Dimensional Devices," in *Future Trends in Microelectronics*. Hoboken, NJ, USA: John Wiley & Sons, Inc., 9 2016, ch. 1.4, pp. 51–67. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/9781119069225.ch1-4http://doi.wiley.com/10.1002/9781119069225.ch1-4

[16] T. Irisawa, K. Ikeda, Y. Moriyama, M. Oda, E. Mieda, T. Maeda, and T. Tezuka, "Demonstration of ultimate CMOS based on 3D stacked InGaAs-OI/SGOI wire channel MOSFETs with independent back gate," *Digest of Technical Papers - Symposium on VLSI Technology*, pp. 3–4, 2014.

[17] V. Deshpande, V. Djara, E. O'Connor, P. Hashemi, K. Balakrishnan, M. Sousa, D. Caimi, A. Olziersky, L. Czornomaz, and J. Fompeyrine, "Advanced 3D Monolithic hybrid CMOS with Sub-50 nm gate inverters featuring replacement metal gate (RMG)-InGaAs nFETs on SiGe-OI Fin pFETs," *Technical Digest - International Electron Devices Meeting, IEDM*, vol. 2016-Febru, no. 1, pp. 1–8, 2015.

[18] P. Batude, M. Vinet, C. Xu, B. Previtali, C. Tabone, C. L. Royer, L. Sanchez, L. Baud, L. Brunet, A. Toffoli, F. Allain, D. Lafond, F. Aussenac, O. Thomas, T. Poiroux, and O. Faynot, "Demonstration of low temperature 3D sequential FDSOI integration down to 50 nm gate length," *2011 Symposium on VLSI Technology - Digest of Technical Papers*, pp. 158–159, 2011.

[19] L. Brunet, P. Batude, C. Fenouillet-Beranger, P. Besombes, L. Hortemel, F. Ponthenier, B. Previtali, C. Tabone, A. Royer, C. Agraffeil, C. Euvrard-Colnat, A. Seignard, C. Morales, F. Fournel, L. Benaissa, T. Signamarcheix, P. Besson, M. Jourdan, R. Kachtouli, V. Benevent, J. M. Hartmann, C. Comboroure, N. Allouti, N. Posseme, C. Vizioz, C. Arvet, S. Barnola, S. Kerdiles, L. Baud, L. Pasini, C. M. Lu, F. Deprat, A. Toffoli, G. Romano, C. Guedj, V. Delaye, F. Boeuf, O. Faynot, and M. Vinet, "First demonstration of a CMOS over CMOS 3D VLSI CoolCube™ integration on 300mm wafers," *Digest of Technical Papers - Symposium on VLSI Technology*, vol. 2016-Septe, pp. 11–12, 2016.

[20] U. W. Pohl, *Epitaxy of Semiconductors*, 1st ed., U. W. Pohl, Ed. Berlin: Springer Berlin Heidelberg, 2013.

[21] M. T. Currie, S. B. Samavedam, T. a. Langdo, C. W. Leitz, and E. a. Fitzgerald, "Controlling threading dislocation densities in Ge on Si using graded SiGe layers and chemical-mechanical polishing," *Applied Physics Letters*, vol. 72, no. 14, pp. 1718–1720, 1998.

[22] E. A. Fitzgerald, Y. Xie, M. L. Green, D. Brasen, A. R. Kortan, J. Michel, Y. Mii, and B. E. Weir, "Totally relaxed Ge x Si 1 x layers with low threading dislocation densities grown on Si substrates," *Applied Physics Letters*, vol. 59, no. 7, pp. 811–813, 8 1991. [Online]. Available: http://aip.scitation.org/doi/10.1063/1.105351

[23] V. A. Shah, A. Dobbie, M. Myronov, and D. R. Leadley, "Reverse graded SiGe/Ge/Si buffers for high-composition virtual substrates," *Journal of Applied Physics*, vol. 107, no. 6, p. 064304, 3 2010. [Online]. Available: http://aip.scitation.org/doi/10.1063/1.3311556

[24] L. Colace, G. Masini, F. Galluzzi, G. Assanto, G. Capellini, L. Di Gaspare, E. Palange, and F. Evangelisti, "Metal–semiconductor–metal near-infrared light detector based on epitaxial Ge/Si," *Applied Physics Letters*, vol. 72,

no. 24, p. 3175, 1998. [Online]. Available: http://link.aip.org/link/APPLAB/v72/i24/p3175/s1&Agg=doi

[25] J. M. Hartmann, A. Abbadie, A. M. Papon, P. Holliger, G. Rolland, T. Billon, J. M. Fédéli, M. Rouvière, L. Vivien, and S. Laval, "Reduced pressure-chemical vapor deposition of Ge thick layers on Si(001) for 1.3-1.55-μm photodetection," *Journal of Applied Physics*, vol. 95, no. 10, pp. 5905–5913, 2004.

[26] ——, "Reduced pressure-chemical vapor deposition of Ge thick layers on Si(001) for 1.3-1.55-μm photodetection," *Journal of Applied Physics*, vol. 95, no. 10, pp. 5905–5913, 2004.

[27] H.-C. Luan, D. R. Lim, K. K. Lee, K. M. Chen, J. G. Sandland, K. Wada, and L. C. Kimerling, "High-quality Ge epilayers on Si with low threading-dislocation densities," *Applied Physics Letters*, vol. 75, no. 19, p. 2909, 1999. [Online]. Available: http://link.aip.org/link/APPLAB/v75/i19/p2909/s1&Agg=doi

[28] S. Akira, T. Toru, and K. Aoyama, "Growth of strain-relaxed Ge films on Si (001) surfaces," *Appl. Phys. Lett.*, vol. 3510, no. October 1997, pp. 1–4, 1997.

[29] Y. Yamamoto, P. Zaumseil, T. Arguirov, M. Kittler, and B. Tillack, "Low threading dislocation density Ge deposited on Si (1 0 0) using RPCVD," *Solid-State Electronics*, vol. 60, no. 1, pp. 2–6, 2011. [Online]. Available: http://dx.doi.org/10.1016/j.sse.2011.01.032

[30] K. A. Reinhardt and W. Kern, "Handbook of Silicon Wafer Cleaning Technology," *Handbook of Silicon Wafer Cleaning Technology*, pp. 1–760, 2018.

[31] "Applied enters wafer cleaning market and finds 'Oasis'," pp. https://www.eetimes.com/applied–enters–wafer–clean.

[32] R. Cariou, R. Ruggeri, X. Tan, G. Mannino, J. Nassar, and P. Roca I Cabarrocas, "Structural properties of relaxed thin film germanium layers grown by low temperature RF-PECVD epitaxy on Si and Ge (100) substrates," *AIP Advances*, vol. 4, no. 7, 2014.

[33] A. Abbadie, S. W. Bedell, J. M. Hartmann, D. K. Sadana, F. Brunier, C. Figuet, and I. Cayrefourcq, "Study of HCl and Secco Defect Etching for Characterization of Thick sSOI," *Journal of The Electrochemical Society*, vol. 154, no. 8, p. H713, 2007.

[34] K. H. Lee, S. Bao, G. Y. Chong, Y. H. Tan, E. A. Fitzgerald, and C. S. Tan, "Defects reduction of Ge epitaxial film in a germanium-on-insulator wafer by annealing in oxygen ambient," *APL Materials*, vol. 3, no. 1, 2015. [Online]. Available: http://dx.doi.org/10.1063/1.4905487

[35] G. Zhou, K. H. Lee, D. H. Anjum, Q. Zhang, X. Zhang, C. S. Tan, and G. Xia, "Impacts of doping on epitaxial germanium thin film quality and Si-Ge interdiffusion," *arXiv*, vol. 8, no. 5, pp. 11 272–11 277, 2017.

[36] F. Gencarelli, B. Vincent, L. Souriau, O. Richard, W. Vandervorst, R. Loo, M. Caymax, and M. Heyns, "Low-temperature Ge and GeSn chemical vapor deposition using Ge 2H 6," *Thin Solid Films*, vol. 520, no. 8, pp. 3211–3215, 2012. [Online]. Available: http://dx.doi.org/10.1016/j.tsf.2011.10.119

[37] B. W. Cheng, H. Y. Xue, D. Hu, G. Q. Han, Y. G. Zeng, A. Q. Bai, C. L. Xue, L. P. Luo, Y. H. Zuo, and Q. M. Wang, "Low threading-dislocation-density Ge film on Si grown on a pitting Ge buffer layer," *2008 5th International Conference on Group IV Photonics, GFP*, pp. 140–142, 2008.

[38] W.-S. Liao, Y.-G. Liaw, M.-C. Tang, K.-M. Chen, S.-Y. Huang, C.-Y. Peng, and C. W. Liu, "PMOS Hole Mobility Enhancement Through SiGe Conductive Channel and Highly Compressive ILD- $\hbox{SiN}_{x}$ Stressing Layer," *IEEE Electron Device Letters*, vol. 29, no. 1, pp. 86–88, 1 2008. [Online]. Available: http://ieeexplore.ieee.org/document/4408741/

[39] M. L. Lee, E. A. Fitzgerald, M. T. Bulsara, M. T. Currie, and A. Lochtefeld, "Strained Si, SiGe, and Ge channels for high-mobility metal-oxide-semiconductor field-effect transistors," *Journal of Applied Physics*, vol. 97, no. 1, p. 011101, 1 2005. [Online]. Available: http://aip.scitation.org/doi/10.1063/1.1819976

[40] T. Uchino, T. Shiba, K. Ohnishi, A. Miyauchi, M. Nakata, Y. Inoue, and T. Suzuki, "A raised source/drain technology using in-situ P-doped SiGe and B-doped Si for 0.1-μm CMOS ULSIs," in *International Electron Devices Meeting. IEDM Technical Digest*, vol. 00, no. c. IEEE, 1997, pp. 479–482. [Online]. Available: http://ieeexplore.ieee.org/document/650428/

[41] M. L. Lee, A. J. Pitera, and E. a. Fitzgerald, "Growth of strained Si and strained Ge heterostructures on relaxed Si[sub 1x]Ge[sub x] by ultrahigh vacuum chemical vapor deposition," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 22, no. 1, p. 158, 2004.

[42] S. Nakaharai, T. Tezuka, N. Sugiyama, Y. Moriyama, and S. I. Takagi, "Characterization of 7-nm-thick strained Ge-on-insulator layer fabricated by Ge-condensation technique," *Applied Physics Letters*, vol. 83, no. 17, pp. 3516–3518, 2003.

[43] S. Huang, W. Lu, C. Li, W. Huang, H. Lai, and S. Chen, "A CMOS-compatible approach to fabricate an ultra-thin germanium-on-insulator with large tensile strain for Si-based light emission." *Optics express*, vol. 21, no. 1, pp. 640–6, 2013. [Online]. Available: http://www.ncbi.nlm.nih.gov/pubmed/23388957

[44] N. Sugiyama, T. Tezuka, T. Mizuno, M. Suzuki, Y. Ishikawa, N. Shibata, and S. Takagi, "Temperature effects on Ge condensation by thermal oxidation of SiGe-on-insulator structures," *Journal of Applied Physics*, vol. 95, no. 8, pp. 4007–4011, 2004.

[45] Y. Liu, M. D. Deal, and J. D. Plummer, "High-quality single-crystal Ge on insulator by liquid-phase epitaxy on Si substrates," *Applied Physics Letters*, vol. 84, no. 14, pp. 2563–2565, 2004.

[46] J. H. Nam, F. Afshinmanesh, D. Nam, W. S. Jung, T. I. Kamins, M. L. Brongersma, and K. C. Saraswat, "Monolithic integration of germanium-on-insulator p-i-n photodetector on silicon," *Optics Express*, vol. 23, no. 12, pp. 15 816–15 823, 2015.

[47] T. Akatsu, C. Deguet, L. Sanchez, F. Allibert, D. Rouchon, T. Signamarcheix, C. Richtarch, A. Boussagol, V. Loup, F. Mazen, J. M. Hartmann, Y. Campidelli, L. Clavelier, F. Letertre, N. Kernevez, and C. Mazure, "Germanium-on-insulator (GeOI) substrates-A novel engineered substrate for future high performance devices," *Materials Science in Semiconductor Processing*, vol. 9, no. 4-5 SPEC. ISS., pp. 444–448, 2006.

[48] Y. L. Chao, R. Scholz, M. Reiche, U. Gösele, and J. C. S. Woo, "Characteristics of germanium-on-insulators fabricated by wafer bonding and hydrogen-induced layer splitting," *Japanese Journal of Applied Physics, Part 1: Regular Papers and Short Notes and Review Papers*, vol. 45, no. 11, pp. 8565–8570, 2006.

[49] C. M. Lim, Z. Zhao, K. Sumita, K. Toprasertpong, M. Takenaka, and S. Takagi, "Effects of hydrogen ion implantation dose on physical and electrical properties of Ge-on-insulator layers fabricated by the smart-cut process," *AIP Advances*, vol. 10, no. 1, 2020. [Online]. Available: https://doi.org/10.1063/1.5132881

[50] K. H. Lee, S. Bao, G. Y. Chong, Y. H. Tan, E. A. Fitzgerald, and C. S. Tan, "Fabrication and characterization of germanium-on-insulator through epitaxy, bonding, and layer transfer," *Journal of Applied Physics*, vol. 116, no. 10, pp. 1–6, 2014. [Online]. Available: http://dx.doi.org/10.1063/1.4895487

[51] S. S. Iyer, "Silicon Wafer Bonding Technology for VLSI and MEMS Applications," *Silicon Wafer Bonding Technology for VLSI and MEMS Applications*, 2002.

[52] M. K. Weldon, "Physics and chemistry of silicon wafer bonding investigated by infrared absorption spectroscopy," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 14, no. 4, p. 3095, 1996.

[53] Q.-Y. Tong, T.-H. Lee, U. Gösele, M. Reiche, J. Ramm, and E. Beck, "The Role of Surface Chemistry in Bonding of Standard Silicon Wafers," *Journal of The Electrochemical Society*, vol. 144, no. 1, p. 384, 1997.

[54] Q. Tong, E. Schmidt, and U. Ggselea, "Hydrophobic," *Encyclopedia of Analytical Science*, vol. 64, no. 2002, pp. 36–42, 2005.

[55] K. Ljungberg, A. Söderbärg, and Y. Bäcklund, "Spontaneous bonding of hydrophobic silicon surfaces," *Applied Physics Letters*, vol. 62, no. 12, pp. 1362–1364, 1993.

[56] V. Masteika, J. Kowal, N. S. J. Braithwaite, and T. Rogers, "A Review of Hydrophilic Silicon Wafer Bonding," *ECS Journal of Solid State Science and Technology*, vol. 3, no. 4, pp. Q42–Q54, 2014.

[57] U. Gösele and Q. Y. Tong, "Semiconductor wafer bonding," *Annual Review of Materials Science*, vol. 28, no. 1, pp. 215–241, 1998.

[58] H. Moriceau, F. Rieutord, C. Morales, A. Charvet, O. Rayssac, B. Bataillou, F. Fournel, J. Eymery, A. Pascale, P. Gentile, A. Bavard, J. Mézière, C. Maleville, and B. Aspar, "Direct Wafer Bonding for Nanostructure Preparations," *Solid State Phenomena*, vol. 121-123, pp. 29–32, 2007.

[59] W. Van Den Daele, E. Augendre, C. Le Royer, J.-F. Damlencourt, B. Grandchamp, and S. Cristoloveanu, "Low-temperature characterization and modeling of advanced GeOI pMOSFETs: Mobility mechanisms and origin of the parasitic conduction," *Solid-State Electronics*, vol. 54, no. 2, pp. 205–212, 2 2010. [Online]. Available: http://dx.doi.org/10.1016/j.sse.2009.12.020https://linkinghub.elsevier.com/retrieve/pii/S0038110109003633

[60] W. Bai, N. Lu, J. Liu, A. Ramirez, D. Kwong, D. Wristers, A. Ritenour, L. Lee, and D. Antoniadis, "Ge MOS characteristics with CVD HfO/sub 2/ gate dielectrics and TaN gate electrode," in *2003 Symposium on VLSI Technology. Digest of Technical Papers (IEEE Cat. No.03CH37407)*. Japan Soc. Applied Phys, 2003, pp. 121–122. [Online]. Available: http://ieeexplore.ieee.org/document/1221115/

[61] N. Wu, Q. Zhang, C. Zhu, D. S. Chan, A. Du, N. Balasubramanian, M. F. Li, A. Chin, J. K. Sin, and D. L. Kwong, "A TaN-HfO2-Ge pMOSFET with novel SiH4 surface passivation," *IEEE Electron Device Letters*, vol. 25, no. 9, pp. 631–633, 2004.

[62] T. Tezuka, S. Nakaharai, Y. Moriyama, N. Sugiyama, and Shin-ichi Takagi, "Selectively-formed high mobility SiGe-on-Insulator pMOSFETs with Ge-rich strained surface channels using local condensation technique," in *Digest of Technical Papers. 2004 Symposium on VLSI Technology, 2004.*, vol. 3920, no. 2001. IEEE, 2004, pp. 198–199. [Online]. Available: http://ieeexplore.ieee.org/document/1345477/

[63] C. Le Royer, L. Clavelier, C. Tabone, C. Deguet, L. Sanchez, J.-M. Hartmann, M.-C. Roure, H. Grampeix, and S. Deleonibus, "105 nm Gate

length pMOSFETs with high-K and metal gate fabricated in a Si process line on 200 mm GeOI wafers," in *ESSDERC 2007 - 37th European Solid State Device Research Conference*, vol. 2007. IEEE, 2007, pp. 458–461. [Online]. Available: http://ieeexplore.ieee.org/document/4430977/

[64] K. Romanjek, E. Augendre, W. Van Den Daele, B. Grandchamp, L. Sanchez, C. Le Royer, J.-M. Hartmann, B. Ghyselen, E. Guiot, K. Bourdelle, S. Cristoloveanu, F. Boulanger, and L. Clavelier, "Improved GeOI substrates for pMOSFET off-state leakage control," *Microelectronic Engineering*, vol. 86, no. 7-9, pp. 1585–1588, 7 2009. [Online]. Available: http://dx.doi.org/10.1016/j.mee.2009.03.069https://linkinghub.elsevier.com/retrieve/pii/S016793170900241X

[65] K. Romanjek, L. Hutin, C. Le Royer, A. Pouydebasque, M.-A. Jaud, C. Tabone, E. Augendre, L. Sanchez, J.-M. Hartmann, H. Grampeix, V. Mazzocchi, S. Soliveres, R. Truche, L. Clavelier, P. Scheiblin, X. Garros, G. Reimbold, M. Vinet, F. Boulanger, and S. Deleonibus, "High performance 70nm gate length germanium-on-insulator pMOSFET with high-k/metal gate," *Solid-State Electronics*, vol. 53, no. 7, pp. 723–729, 7 2009. [Online]. Available: http://dx.doi.org/10.1016/j.sse.2009.01.021https://linkinghub.elsevier.com/retrieve/pii/S0038110109000768

[66] H. Wu and P. D. Ye, "Fully Depleted Ge CMOS Devices and Logic Circuits on Si," *IEEE Transactions on Electron Devices*, vol. 63, no. 8, pp. 3028–3035, 8 2016. [Online]. Available: http://ieeexplore.ieee.org/document/7502114/

[67] S. Yadav, K. H. Tan, A. Kumar, K. H. Goh, G. Liang, S.-F. Yoon, X. Gong, and Y.-C. Yeo, "Monolithic Integration of InAs Quantum-Well n-MOSFETs and Ultrathin Body Ge p-MOSFETs on a Si Substrate," *IEEE Transactions on Electron Devices*, vol. 64, no. 2, pp. 353–360, 2 2017. [Online]. Available: http://ieeexplore.ieee.org/document/7802622/

[68] X. Yu, J. Kang, M. Takenaka, and S. Takagi, "Experimental study on carrier transport properties in extremely-thin body Ge-on-insulator (GOI) p-MOSFETs with GOI thickness down to 2 nm," in *2015 IEEE International Electron Devices Meeting (IEDM)*, vol. 2016-Febru. IEEE, 12 2015, pp. 1–2. [Online]. Available: http://ieeexplore.ieee.org/document/7409611/

[69] H. Wu, Wei Luo, Mengwei Si, Jingyun Zhang, Hong Zhou, and P. D. Ye, "Deep sub-100 nm Ge CMOS devices on Si with the recessed S/D and channel," in *2014 IEEE International Electron Devices Meeting*, vol. 2015-Febru, no. February. IEEE, 12 2014, pp. 1–16. [Online]. Available: http://ieeexplore.ieee.org/document/7047067/

[70] H. Arimura, D. Cott, R. Loo, W. Vanherle, Q. Xie, F. Tang, X. Jiang, J. Franco, S. Sioncke, L.-A. Ragnarsson, E. Chiu, X. Lu, J. Geypen,

H. Bender, J. W. Maes, M. Givens, A. Sibaja-Hernandez, K. Wostyn, G. Boccardi, J. Mitard, N. Collaert, and D. Mocuta, "Si-passivated Ge nMOS gate stack with low Dit and dipole-induced superior PBTI reliability using 3D-compatible ALD caps and high-pressure anneal," in *2016 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 12 2016, pp. 1–33. [Online]. Available: http://ieeexplore.ieee.org/document/7838534/

[71] H. Arimura, L. Witters, D. Cott, H. Dekkers, R. Loo, J. Mitard, L.-A. Ragnarsson, K. Wostyn, G. Boccardi, E. Chiu, A. Subirats, P. Favia, E. Vancoille, V. De Heyn, D. Mocuta, and N. Collaert, "Performance and electrostatic improvement by high-pressure anneal on Si-passivated strained Ge pFinFET and gate all around devices with superior NBTI reliability," in *2017 Symposium on VLSI Technology*, vol. 0. IEEE, 6 2017, pp. T196–T197. [Online]. Available: http://ieeexplore.ieee.org/document/7998169/

[72] N. Wu, Q. Zhang, C. Zhu, D. S. H. Chan, M. F. Li, N. Balasubramanian, A. Chin, and D.-L. Kwong, "Alternative surface passivation on germanium for metal-oxide-semiconductor applications with high-k gate dielectric," *Applied Physics Letters*, vol. 85, no. 18, pp. 4127–4129, 11 2004. [Online]. Available: http://aip.scitation.org/doi/10.1063/1.1812835

[73] D. P. Brunco, B. De Jaeger, G. Eneman, J. Mitard, G. Hellings, A. Satta, V. Terzieva, L. Souriau, F. E. Leys, G. Pourtois, M. Houssa, G. Winderickx, E. Vrancken, S. Sioncke, K. Opsomer, G. Nicholas, M. Caymax, A. Stesmans, J. Van Steenbergen, P. W. Mertens, M. Meuris, and M. M. Heyns, "Germanium MOSFET Devices: Advances in Materials Understanding, Process Development, and Electrical Performance," *Journal of The Electrochemical Society*, vol. 155, no. 7, p. H552, 2008. [Online]. Available: https://iopscience.iop.org/article/10.1149/1.2919115

[74] N. Taoka, M. Harada, Y. Yamashita, T. Yamamoto, N. Sugiyama, and S.-i. Takagi, "Effects of Si passivation on Ge metal-insulator-semiconductor interface properties and inversion-layer hole mobility," *Applied Physics Letters*, vol. 92, no. 11, p. 113511, 3 2008. [Online]. Available: http://aip.scitation.org/doi/10.1063/1.2899631

[75] H. Kawabata, H. Ueba, and C. Tatsuyama, "Heteroepitaxy of Si films on a Ge(100)-2×1 surface," *Journal of Applied Physics*, vol. 66, no. 2, pp. 634–639, 7 1989. [Online]. Available: http://aip.scitation.org/doi/10.1063/1.343530

[76] D.-S. Lin, T. Miller, and T.-C. Chiang, "Si indiffusion on Ge(100)-(2×1) studied by core-level photoemission," *Physical Review B*, vol. 45, no. 19, pp. 11 415–11 418, 5 1992. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevB.45.11415

[77] R. Tsu, H. Z. Xiao, Y. Kim, M. Hasan, H. K. Birnbaum, J. E. Greene, D. Lin, and T. Chiang, "Surface segregation and growth-mode transitions during the

initial stages of Si growth on Ge(001)2×1 by cyclic gas-source molecular beam epitaxy from Si 2 H 6," *Journal of Applied Physics*, vol. 75, no. 1, pp. 240–247, 1 1994. [Online]. Available: http://aip.scitation.org/doi/10.1063/1.355890

[78] B. Vincent, R. Loo, W. Vandervorst, J. Delmotte, B. Douhard, V. Valev, M. Vanbel, T. Verbiest, J. Rip, B. Brijs, T. Conard, C. Claypool, S. Takeuchi, S. Zaima, J. Mitard, B. De Jaeger, J. Dekoster, and M. Caymax, "Si passivation for Ge pMOSFETs: Impact of Si cap growth conditions," *Solid-State Electronics*, vol. 60, no. 1, pp. 116–121, 6 2011. [Online]. Available: https://linkinghub.elsevier.com/retrieve/pii/S0038110111000785

[79] R. Loo, H. Arimura, D. Cott, L. Witters, G. Pourtois, A. Schulze, B. Douhard, W. Vanherle, G. Eneman, O. Richard, P. Favia, J. Mitard, D. Mocuta, R. Langer, and N. Collaert, "Editors' Choice—Epitaxial CVD Growth of Ultra-Thin Si Passivation Layers on Strained Ge Fin Structures," *ECS Journal of Solid State Science and Technology*, vol. 7, no. 2, pp. P66–P72, 1 2018. [Online]. Available: https://iopscience.iop.org/article/10.1149/2.0191802jss

[80] L. Žurauskaitė, L. Jones, V. R. Dhanak, I. Z. Mitrovic, P.-E. Hellström, and M. Östling, "Investigation of Tm 2 O 3 As a Gate Dielectric for Ge MOS Devices," *ECS Transactions*, vol. 86, no. 7, pp. 67–73, 7 2018. [Online]. Available: https://iopscience.iop.org/article/10.1149/08607.0067ecst

[81] E. Dentoni Litta, P.-E. Hellstrom, C. Henkel, and M. Ostling, "Thulium Silicate Interfacial Layer for Scalable High-k/Metal Gate Stacks," *IEEE Transactions on Electron Devices*, vol. 60, no. 10, pp. 3271–3276, 10 2013. [Online]. Available: https://ieeexplore.ieee.org/document/6583336/

[82] M. L. Lee, C. W. Leitz, Z. Cheng, A. J. Pitera, T. Langdo, M. T. Currie, G. Taraschi, E. A. Fitzgerald, and D. A. Antoniadis, "Strained Ge channel p -type metal–oxide–semiconductor field-effect transistors grown on Si1xGex/Si virtual substrates," *Applied Physics Letters*, vol. 79, no. 20, pp. 3344–3346, 11 2001. [Online]. Available: http://aip.scitation.org/doi/10.1063/1.1417515

[83] Chi On Chui, Hyoungsub Kim, D. Chi, B. Triplett, P. McIntyre, and K. Saraswat, "A sub-400°C germanium MOSFET technology with high-κ dielectric and metal gate," in *Digest. International Electron Devices Meeting,*, no. 650. IEEE, 2002, pp. 437–440. [Online]. Available: http://ieeexplore.ieee.org/document/1175872/

[84] Huiling Shang, H. Okorn-Schmidt, K. Chan, M. Copel, J. Ott, P. Kozlowski, S. Steen, S. Cordes, H.-S. Wong, E. Jones, and W. Haensch, "High mobility p-channel germanium MOSFETs with a thin Ge oxynitride gate dielectric," in *Digest. International Electron Devices Meeting,*. IEEE, pp. 441–444. [Online]. Available: http://ieeexplore.ieee.org/document/1175873/

[85] G. Nicholas, B. De Jaeger, D. Brunco, P. Zimmerman, G. Eneman, K. Martens, M. Meuris, and M. Heyns, "High-Performance Deep Submicron Ge pMOSFETs With Halo Implants," *IEEE Transactions on Electron Devices*, vol. 54, no. 9, pp. 2503–2511, 9 2007. [Online]. Available: http://ieeexplore.ieee.org/document/4294227/

[86] J. Mitard, B. De Jaeger, F. Leys, G. Hellings, K. Martens, G. Eneman, D. Brunco, R. Loo, J. Lin, D. Shamiryan, T. Vandeweyer, G. Winderickx, E. Vrancken, C. Yu, K. De Meyer, M. Caymax, L. Pantisano, M. Meuris, and M. Heyns, "Record ION/IOFF performance for 65nm Ge pMOSFET and novel Si passivation scheme for improved EOT scalability," in *2008 IEEE International Electron Devices Meeting*. IEEE, 12 2008, pp. 1–4. [Online]. Available: http://ieeexplore.ieee.org/document/4796837/

[87] S. Decoster and A. Vantomme, "Implantation-induced damage in Ge: strain and disorder profiles during defect accumulation and recovery," *Journal of Physics D: Applied Physics*, vol. 42, no. 16, p. 165404, 8 2009. [Online]. Available: https://iopscience.iop.org/article/10.1088/0022-3727/42/16/165404

[88] J. Slotte, M. Rummukainen, F. Tuomisto, V. P. Markevich, A. R. Peaker, C. Jeynes, and R. M. Gwilliam, "Evolution of vacancy-related defects upon annealing of ion-implanted germanium," *Physical Review B*, vol. 78, no. 8, p. 085202, 8 2008. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevB.78.085202

[89] R. A. Kelly, B. Liedke, S. Baldauf, A. Gangnaik, S. Biswas, Y. Georgiev, J. D. Holmes, M. Posselt, and N. Petkov, "Epitaxial Post-Implant Recrystallization in Germanium Nanowires," *Crystal Growth & Design*, vol. 15, no. 9, pp. 4581–4590, 9 2015. [Online]. Available: https://pubs.acs.org/doi/10.1021/acs.cgd.5b00836

[90] G. Wang, M. Moeen, A. Abedin, M. Kolahdouz, J. Luo, C. Qin, H. Zhu, J. Yan, H. Yin, J. Li, C. Zhao, and H. Radamson, "Optimization of SiGe selective epitaxy for source/drain engineering in 22 nm node complementary metal-oxide semiconductor (CMOS)," *Journal of Applied Physics*, vol. 114, no. 12, 2013.

[91] G. Wang, A. Abedin, M. Moeen, M. Kolahdouz, J. Luo, Y. Guo, T. Chen, H. Yin, H. Zhu, J. Li, C. Zhao, and H. Radamson, "Integration of highly-strained SiGe materials in 14 nm and beyond nodes FinFET technology," *Solid-State Electronics*, vol. 103, 2015.

[92] J. Hartmann, V. Benevent, J. Barnes, M. Veillerot, D. Lafond, J. Damlencourt, S. Morvan, B. Prévitali, F. Andrieu, N. Loubet, and D. Dutartre, "Mushroom-free selective epitaxial growth of Si, SiGe and

SiGe:B raised sources and drains," *Solid-State Electronics*, vol. 83, pp. 10–17, 5 2013. [Online]. Available: http://dx.doi.org/10.1016/j.sse.2013.01.033https://linkinghub.elsevier.com/retrieve/pii/S0038110113000464

[93] J. Hartmann, M. Py, J. Barnes, B. Prévitali, P. Batude, and T. Billon, "Low temperature boron and phosphorous doped SiGe for recessed and raised sources and drains," *Journal of Crystal Growth*, vol. 327, no. 1, pp. 68–77, 7 2011. [Online]. Available: https://linkinghub.elsevier.com/retrieve/pii/S002202481100457X

[94] Y. Qi, J. Peng, H.-C. Lo, J. R. Holt, M. Willemann, C. Gaire, S. Evans, P. Flanagan, H. Yu, O. Hu, and M. Kennett, "In-Situ Boron Doped SiGe Epitaxy Optimization for FinFET Source/Drain," *ECS Transactions*, vol. 75, no. 8, pp. 265–272, 9 2016. [Online]. Available: https://iopscience.iop.org/article/10.1149/07508.0265ecst

[95] H. Radamson, M. Kolahdouz, R. Ghandi, and J. Hållstedt, "Selective epitaxial growth of B-doped SiGe and HCl etch of Si for the formation of SiGe:B recessed source and drain (pMOS transistors)," *Thin Solid Films*, vol. 517, no. 1, pp. 84–86, 11 2008. [Online]. Available: http://dx.doi.org/10.1016/j.tsf.2008.08.106https://linkinghub.elsevier.com/retrieve/pii/S0040609008009590

[96] J. M. Hartmann, V. Benevent, J. F. Damlencourt, and T. Billon, "A benchmarking of silane, disilane and dichlorosilane for the low temperature growth of group IV layers," *Thin Solid Films*, vol. 520, no. 8, pp. 3185–3189, 2012. [Online]. Available: http://dx.doi.org/10.1016/j.tsf.2011.10.164

Appended papers