

Growth of epitaxial SiGe alloys as etch-stop layers in germanium-on-insulator fabrication

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Abstract

In this study, the application of epitaxially grown $\text{Si}_x\text{Ge}_{1-x}$ films as etch stop layers in a germanium-on-insulator substrate fabrication flow is investigated. Layers with Ge contents from 15% to 70% were epitaxially grown on Si (1 0 0) using silane and germane. It was found that the Ge content in the films is independent of the growth temperature for fixed partial pressure ratios. At low growth temperatures the activation energy is found to be 1.8 eV which points to a hydrogen desorption limited growth rate mechanism. At growth temperatures of less than 500 °C, the surface roughness is <1 nm. This surface roughness does not change when the films are grown on Ge substrates. Finally, a fully strained $\text{Si}_{0.5}\text{Ge}_{0.5}$ film was grown on Ge strain relaxed buffer at 450 °C. This layer demonstrates etch selectivity of >400:1 towards Ge in diluted SC-1. This result enables the integration of the $\text{Si}_{0.5}\text{Ge}_{0.5}$ film as an etch stop layer for single crystalline germanium-on-insulator substrate fabrication.

Introduction

New materials and technologies are required to fabricate faster electronic devices and circuits with lower power consumption. 3D integration is a promising technology to reduce interconnect lengths and increase the packing density of devices by stacking transistors on top of each other in tiers, connected with inter tier vias [1,2]. 3D integration give the possibility to integrate different devices such as memories, optical communication components, sensors and energy sources on a single chip to achieve multi functionality. The sequential 3D integration technology enables a high density of inter tier vias between device tiers. However, there are challenges to implement sequential 3D integration, with one of the most important one being the limited thermal budget available during device fabrication [3]. The processing temperature of the top tier devices must be compatible with the fabricated devices in the bottom tier devices and interconnects, typically limiting the process temperature to less than 550 °C [3,4]. Ge with its inherently lower processing temperature is a candidate device material in sequential 3D integration. Ge based sequential 3D integration requires formation of single crystalline Ge on an amorphous inter-layer dielectric (GOI) at a low temperature which excludes fabrication schemes requiring high temperature processing such as condensation [5–7] or lateral overgrowth [8]. However, low temperature direct wafer bonding and etch-back is a promising method for fabrication of the top tier devices in monolithic 3D integration [9]. In such processes, a good etch-stop layer is required in order to remove the sacrificial wafer while keeping the thin active layer intact. Etch stop $\text{Si}_x\text{Ge}_{1-x}$ layers have been routinely used for silicon-on-insulator fabrication [REF]. Its application can be extended to GOI fabrication as well. This layer should have a good etch selectivity toward Ge. $\text{Si}_x\text{Ge}_{1-x}$ is a good candidate for this purpose since it can have high etch selectivity toward Ge, does not add any residual dopants to the layer, can be grown fully strained on Ge and does not induce any crystal defects. . From a sequential 3D integration point of view, this can have the added benefit of a one step process: epitaxial growth of the complete layer stack can be done in a single epitaxial step without breaking vacuum. It is of particular importance for the next generation Ge technology, to enable a reproducible and robust technique for GOI fabrication.

In this work, we have investigated the epitaxial growth of $\text{Si}_x\text{Ge}_{1-x}$ layers using reduced pressure chemical vapor deposition (RPCVD), as an etch-stop layer in the fabrication of single crystalline GOI substrate and layer transfer. A $\text{Si}_{50}\text{Ge}_{50}$ layer has been successfully implemented as an etch stop layer in a GOI fabrication process as shown in [10].

Experimental details

In this work, 100 mm Si (001) substrates have been used. All samples were subjected to standard clean ($\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ [1:1:5] + $\text{HCl}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ [1:1:5]) and 5% HF dip before loading into the load-lock of the epitaxy tool. Epsilon 2000 RPCVD tool from ASM has been used for the epitaxial growth of the layers. The films were grown at temperatures ranging from 450 °C to 650 °C by using silane (SiH_4) and germane (10% GeH_4 in H_2) as sources for Si and Ge. The flow rate of SiH_4 was kept constant at 90 sccm for all the samples, and the flow rate of 10 % GeH_4 in H_2 was varied from 50 to 500 sccm. The reactor pressure was kept at 2666 Pa and 20 slm of H_2 was used as the

carrier gas. The layers were first grown on Si wafers to evaluate the growth conditions and achieve fully-strained $\text{Si}_{1-x}\text{Ge}_x$ with high crystal quality and smooth surface. Then the $\text{Si}_{1-x}\text{Ge}_x$ layers were grown on Ge strain-relaxed buffers (SRB) for GOI fabrication. In the GOI fabrication the $\text{Si}_{1-x}\text{Ge}_x$ layer serves as an etch stop layer towards Ge. The targeted Ge concentration $x=0.5$ was selected since $\text{Si}_{0.5}\text{Ge}_{0.5}$ layers have been shown to be possible to grow up to 20 nm thickness on Si without plastic deformation at a low temperature of 500 °C [11]. Fully strained $\text{Si}_{0.5}\text{Ge}_{0.5}$ layers with low defect concentration on top of Ge SRB can function as effective etch-stop layers in the GOI fabrication process.

The thickness and the Ge content of the films were measured by Spectroscopic Ellipsometry (SE), high resolution X-Ray diffraction (HRXRD), and weighting. SE measurements were performed in the photon energy range of 1.5-4.5 eV, the light spot size of 100 μm x 300 μm , immediately after the sample growth using Horiba UVISSEL ER tool. The SE wafer mapping (25 points of measurements with 10 mm edge of exclusion) was performed on the $\text{Si}_{1-x}\text{Ge}_x$ thin films grown at various temperatures to evaluate the thickness homogeneity over the wafer. A Philips X'Pert Panalytical tool with a copper x-ray source, a 4 bounce symmetric Ge (220) monochromator was used for XRD measurements. Differential weighting characterizations were also used to confirm the thickness and Ge concentration measurements.

SiGe growth using SiH_4 and GeH_4

The concentration of Ge (x) in $\text{Si}_{1-x}\text{Ge}_x$ layers as a function of the partial pressure ratio of GeH_4 (P_{GeH_4}) to SiH_4 (P_{SiH_4}) is shown in Figure 1(a). The partial pressure of SiH_4 was held constant to 12 Pa and the incorporated Ge concentration in the $\text{Si}_{1-x}\text{Ge}_x$ layers is found to increase with increasing GeH_4 partial pressure in accordance with literature [12–15]. Assuming that the concentration of Ge in the growing $\text{Si}_{1-x}\text{Ge}_x$ film is govern by the impingement rate of SiH_4 and GeH_4 times their respective sticking coefficients σ_{SiH_4} and σ_{GeH_4} , the inverse of the Ge concentration can be expressed as:

$$\frac{1}{x} = 1 + \sqrt{\frac{m_{\text{GeH}_4}}{m_{\text{SiH}_4}} \frac{\sigma_{\text{SiH}_4}}{\sigma_{\text{GeH}_4}} \frac{P_{\text{SiH}_4}}{P_{\text{GeH}_4}}} \quad (1)$$

where m_{GeH_4} and m_{SiH_4} is the mass of GeH_4 and SiH_4 , respectively. In Figure 1(b) the inverse of

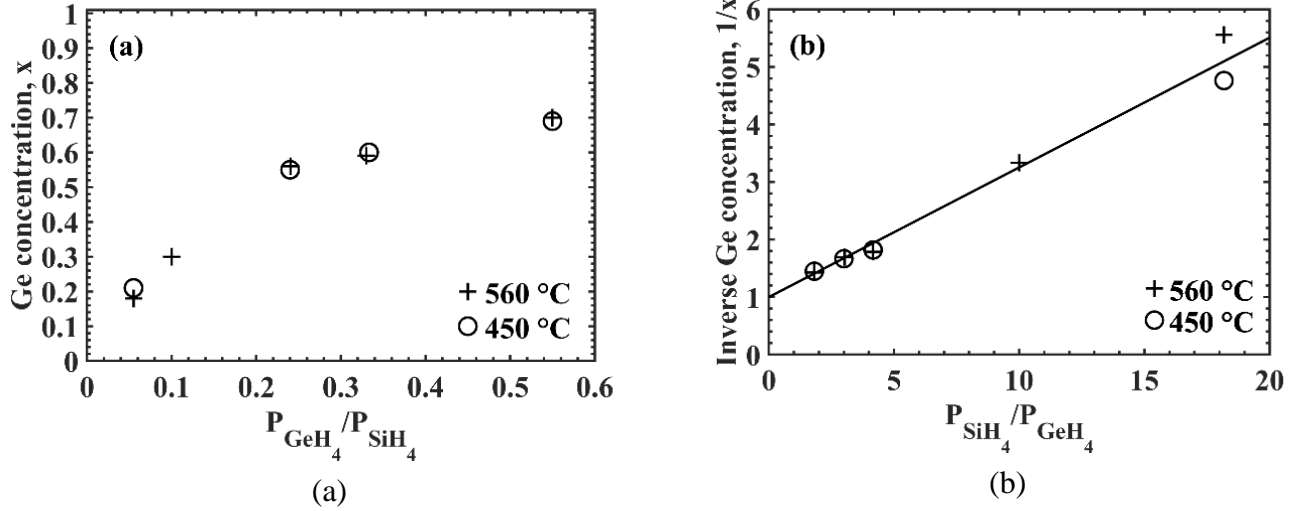


Figure 1. (a) Ge content in the $\text{Si}_{1-x}\text{Ge}_x$ layer plotted over increased partial pressure ratios of GeH_4 to SiH_4 for growth at 450 °C and 560 °C. SiH_4 partial pressure was held constant to 12 Pa. The data are plotted in (b) with the ratio of SiH_4 to GeH_4 sticking coefficients as the fitting parameter according to Eq. 1.

versus the ratio of P_{SiH_4} to P_{GeH_4} is plotted. The solid line displays Eq. (1) fitted to the data with the ratio of the sticking coefficients as fitting parameter. From the slope of the line we extract that the sticking coefficient of SiH_4 is 0.15 times the sticking coefficient of GeH_4 . Figure 2 shows the Ge concentration x at a fixed partial pressure of GeH_4 to SiH_4 versus growth temperature. The Ge concentration in the growing $\text{Si}_{1-x}\text{Ge}_x$ film is independent of the growth temperature, indicating that the ratio of the sticking coefficients is temperature independent within the investigated temperature range of 450 °C to 560 °C.

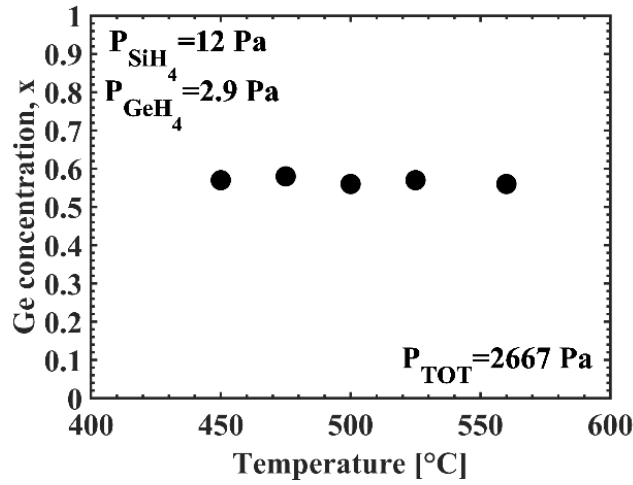


Figure 2. The Ge content in the $\text{Si}_{1-x}\text{Ge}_x$ film is independent of the growth temperature for fixed partial pressures of GeH_4 and SiH_4 .

An Arrhenius plot of the $\text{Si}_{0.45}\text{Ge}_{0.55}$ growth rate is shown in Figure 3. At growth temperatures below 560°C the growth rate displays an Arrhenius dependence with an activation energy of 1.8 eV. At low temperature the growth rate of Si from SiH_4 is known to be limited by hydrogen desorption with an activation energy of 2.1 eV [16]. Germanium is known to increase the growth rate compared to Si and to have a catalytic effect on the hydrogen desorption. The activation energy for hydrogen desorption on Ge from GeH_4 has been experimentally determined to be ~ 1.65 eV [17]. The activation energy of 1.8 eV is between those found for Si and Ge. This activation energy is consistent with the observation that the growth rate of $\text{Si}_{0.45}\text{Ge}_{0.55}$ from SiH_4 and GeH_4 is limited by hydrogen desorption at low temperature. Although the growth rate decreases with decreasing temperature, and is only 2.5 nm/min at 450°C , it is still practical to grow fully strained $\text{Si}_{0.45}\text{Ge}_{0.55}$ layers with thicknesses below 40 nm. At temperatures above 560°C , the growth rate deviates from an Arrhenius behavior and saturates at ~ 70 nm/min due to limited supply of SiH_4 and GeH_4 .

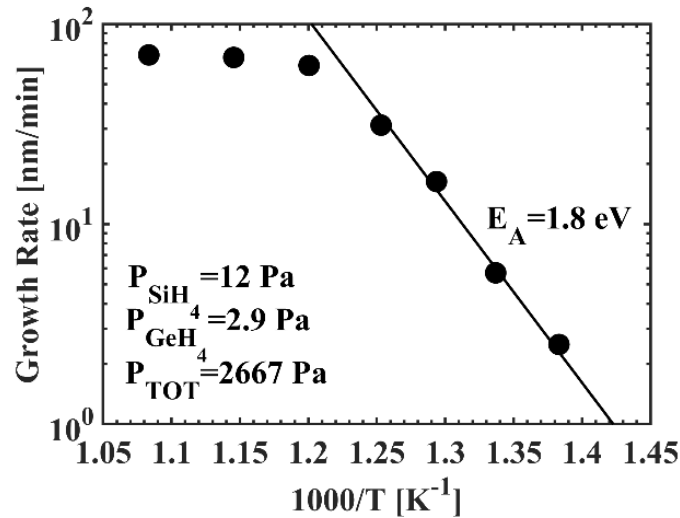


Figure 3: Arrhenius plot of the growth rate of $\text{Si}_{0.45}\text{Ge}_{0.55}$ grown with SiH_4 and GeH_4 pressures fixed at 12 Pa and 2.9 Pa respectively.

Conventional ω -2 θ HRXRD scan around the (004) Bragg peak was performed on 40 nm $\text{Si}_{0.45}\text{Ge}_{0.55}$ layers grown at different temperatures ranging from 450°C to 650°C . The peak at 34.7° is related to the Si substrate and the peak at 33.4° is related to $\text{Si}_{0.45}\text{Ge}_{0.55}$ layer. The well-defined thickness fringes beside the $\text{Si}_{0.45}\text{Ge}_{0.55}$ peak of the layer grown at 450 and 500°C shows that the layer is fully strained with flat interfaces. This indicates that defects are not formed at the interface of $\text{Si}_{0.45}\text{Ge}_{0.55}/\text{Si}$. The location of the peak at 33.4° and the concentration $x=0.55$ determined from spectroscopic ellipsometry infers that the $\text{Si}_{0.45}\text{Ge}_{0.55}$ is 1.3% compressively strained. As the temperature increases from 450°C to 650°C , the angular separation of the $\text{Si}_{0.45}\text{Ge}_{0.55}$ peak from the Si substrate peak decreases. Increasing the growth temperature induces strain relaxation and the $\text{Si}_{0.45}\text{Ge}_{0.55}$ films grown at temperatures higher than 500°C were partially strain relaxed.

Because of strain relaxation, defects are formed at the interface of $\text{Si}_{0.45}\text{Ge}_{0.55}/\text{Si}$ which results in peak broadening and lack of thickness fringes in the ω - 2θ HRXRD scans.

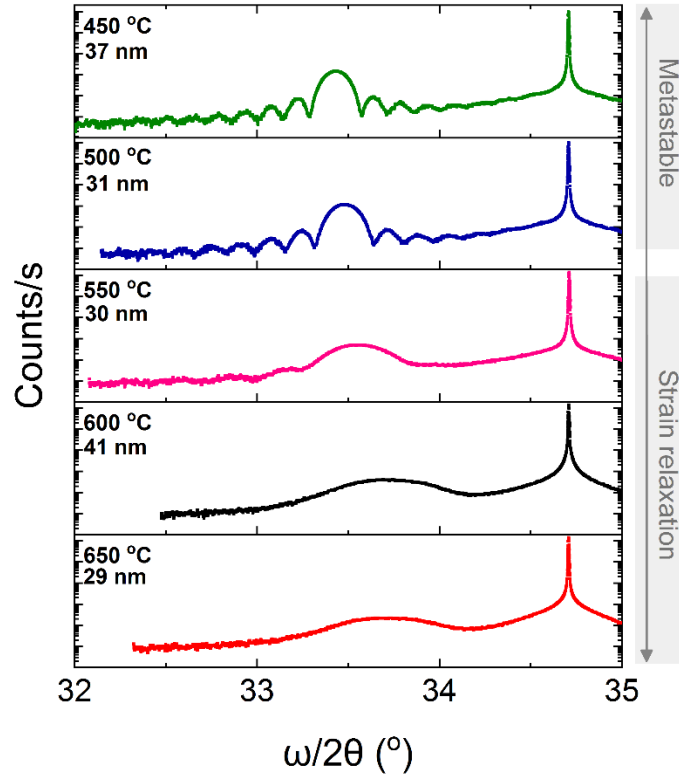


Figure 4. ω - 2θ scan around the (004) x-ray diffraction Bragg peak of the $\text{Si}_{0.45}\text{Ge}_{0.55}$ layers grown at $T=450 - 650$ °C.

The surface morphology of $\text{Si}_{0.45}\text{Ge}_{0.55}$ layers grown on Si at different temperature from 500 °C to 650 °C measured with atomic force microscope (AFM) are shown in figure 5. The AFM images show that when growth temperature is lower than 500 °C the surface roughness is kept below 1 nm. Layers grown at temperatures higher than 500 °C exhibited an increased surface roughness which correlates with the growth temperatures where strain relaxation occurs, which has also been reported by Hartman *et. al.* in [11].

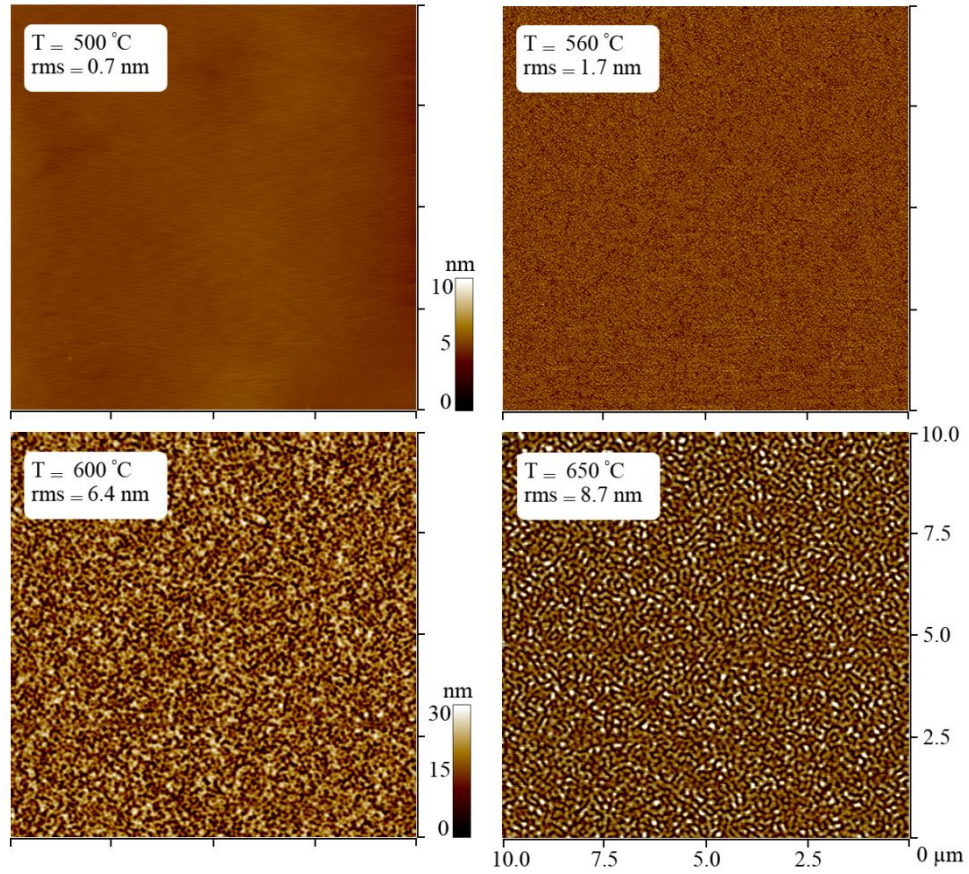


Figure 5. $10\ \mu\text{m} \times 10\ \mu\text{m}$ atomic force microscopy (AFM) images of the $\text{Si}_{0.45}\text{Ge}_{0.55}$ surfaces grown at $\text{P}(\text{GeH}_4)/\text{P}(\text{SiH}_4) = 0.24$ in a temperature range of (a) $500\ ^\circ\text{C}$, (b) $560\ ^\circ\text{C}$, (c) $600\ ^\circ\text{C}$, and (d) $650\ ^\circ\text{C}$. Surface root-mean-square (rms) roughness and the growth temperatures are provided in each image.

$\text{Si}_{0.5}\text{Ge}_{0.5}$ on Ge as an etch stop layer for GOI fabrication

The GOI fabrication process is explained in detail our previous work in [10]. In short, this process employs a single epitaxial growth step, room temperature wafer bonding and a etch-back process. For a $\text{Si}_{1-x}\text{Ge}_x$ layer to be integrated in such a process flow the Ge concentration needs to be controlled to about 50 % and thicknesses less than 30 nm has to be grown with good uniformity. Furthermore, the surface roughness $<1\text{nm}$ is required for successful bonding. An additional property the $\text{Si}_{1-x}\text{Ge}_x$ layer is to have a high etch selectivity towards Ge. Following the layer development reported in the previous section, a $\text{Si}_{0.5}\text{Ge}_{0.5}$ layer was grown on Ge strain relaxed buffer (SRB) and etched in diluted SC-1 ($\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$, 1:1:500) in order to evaluate the etch selectivity to Ge.

The HRXRD rocking curve of 20 nm $\text{Si}_{0.5}\text{Ge}_{0.5}$ grown on Ge SRB is shown in Fig. 6. The peak at 34.7° is related to the Si substrate and the peak at 33.2° is related to Ge SRB. The peak associated to $\text{Si}_{0.5}\text{Ge}_{0.5}$ layer can be seen at 34.5° with small fringes in the left side. The low intensity of the fringes compared to the layers grown directly on Si is due to lower thickness of the $\text{Si}_{0.5}\text{Ge}_{0.5}$ layer

and slightly higher surface roughness of Ge SRB (RMS<1nm) compared to Si substrate. The position of the peak has also moved from 33.4° on Si to 34.5° on Ge, indicating that the $\text{Si}_{0.5}\text{Ge}_{0.5}$ layer is 1.6 % tensile strained when grown on relaxed Ge. .

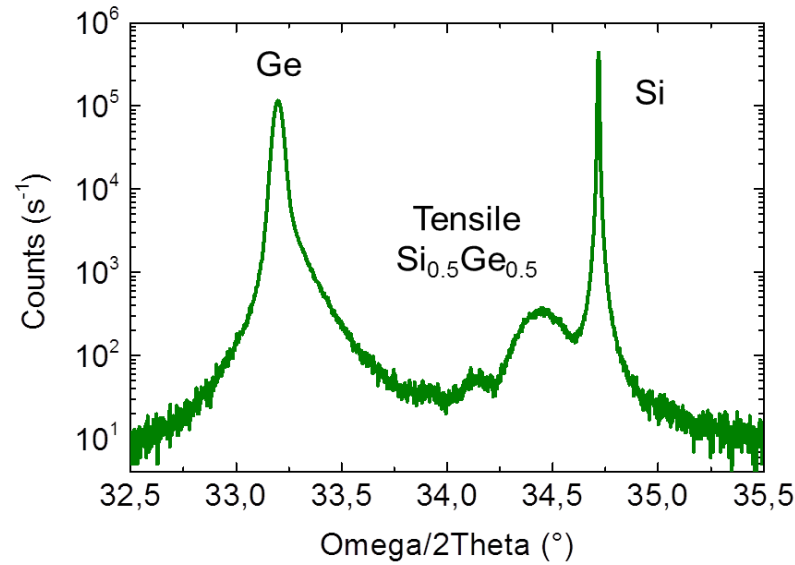


Figure 6. Conventional ω -2 θ scan around the (004) x-ray diffraction Bragg peak of the $\text{Si}_{0.5}\text{Ge}_{0.5}$ layer grown on Ge strain relaxed buffer.

The surface morphology of Ge buffer and Ge buffer capped with 10 nm $\text{Si}_{0.5}\text{Ge}_{0.5}$ is shown in Figure 7. The AFM images show that the surface roughness of the layer stack is not increased when $\text{Si}_{0.5}\text{Ge}_{0.5}$ layer is deposited on top of Ge SRB at temperatures as low as 450°C. Low surface roughness makes it a suitable material for wafer-bonding and layer transfer application.

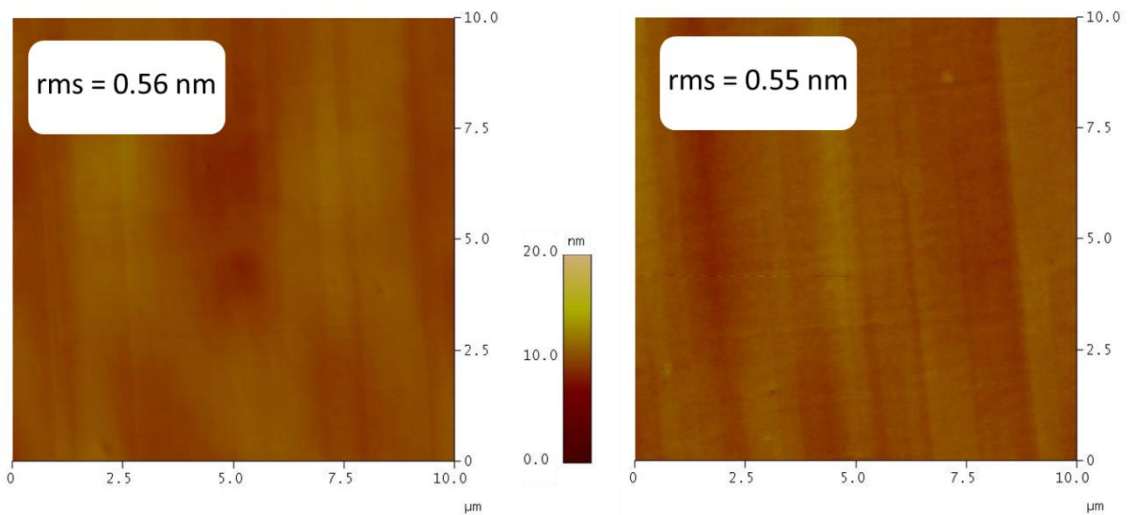


Figure 7. AFM image of $\text{Si}_{0.5}\text{Ge}_{0.5}$ layer grown on Ge strain relaxed buffer. The RMS surface roughness does not change with the deposition of $\text{Si}_{0.5}\text{Ge}_{0.5}$ on top of the Ge SRB.

In order to test the efficiency of the $\text{Si}_{0.5}\text{Ge}_{0.5}$ etch stop layer, the stack in Figure 8 was grown on a 2 μm Ge strain relaxed buffer. Structures of various sizes were patterned with i-line lithography on the layer stack. The photoresist was subsequently removed in O_2 plasma. Reactive ion etching (HBr, Cl_2 and He- O_2) with PECVD SiO_2 as a hard mask was applied to etch the Ge/SiGe/Ge/SiGe layer stack.

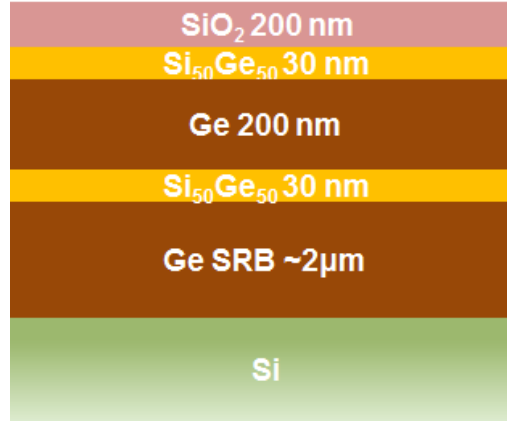


Figure 8. Schematic of the stack grown to test the efficiency of the $\text{Si}_{0.5}\text{Ge}_{0.5}$ etch stop layer in diluted SC-1.

Diluted SC-1 was dispensed for 80 s on the wafer using an automatic etch spray tool. Figure 9 shows a cross section SEM image of the wafer after the wet etch process. It is clear that the $\text{Si}_{0.5}\text{Ge}_{0.5}$ remains intact after 80 s of etch while the Ge is recessed by approximately 400 nm. The etching shows a selectivity of $>400:1$ towards $\text{Si}_{0.5}\text{Ge}_{0.5}$. The etch stop behavior is based on the formation of a thin SiO_2 film around the $\text{Si}_{0.5}\text{Ge}_{0.5}$ which essentially stops further etching. This mechanism is described in detail in reference [10] where a 10 nm thin $\text{Si}_{0.5}\text{Ge}_{0.5}$ is grown with SiH_4 and GeH_4 on 25 nm of high quality crystalline Ge. This film is then successfully applied as an etch stop layer during Ge etch in diluted SC-1 for the fabrication of a germanium-on-insulator substrate. This application expands the established use of silicon germanium alloys as etch stop layers from the SOI to GOI fabrication areas. It further demonstrates its success as a key fabrication step in sequential 3D integration.

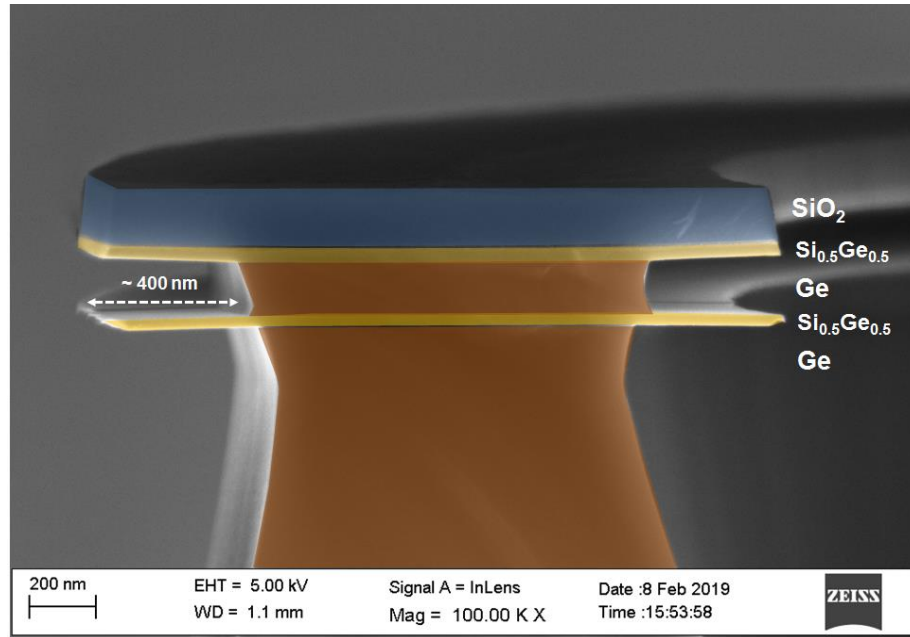


Figure 9. Cross section of the stack shown in Fig. 9 after 80 s of diluted SC-1. The Ge layers are recessed by approximately 400 nm while the $\text{Si}_{0.5}\text{Ge}_{0.5}$ layers remain intact.

Conclusions

In this paper, silane and germane were used to grow epitaxial SiGe layers with Ge contents ranging from 15% to 70% was investigated. The growth rate, crystal quality, strain level, and surface morphology of the layers were investigated in order to develop a fully strained SiGe layer with 50% Ge content. This layer was successfully integrated in a stack of Ge/SiGe/Ge/Si, showing minimized surface roughness and thickness inhomogeneity. An etch selectivity of $>400:1$ towards $\text{Si}_{0.5}\text{Ge}_{0.5}$ was achieved when etching Ge in diluted SC-1. This result facilitates the use of the $\text{Si}_{0.5}\text{Ge}_{0.5}$ film as an etch stop layer for GOI fabrication, in a similar way to SOI fabrication by using direct wafer bonding and etch back.

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