employing simpler and cheaper communication protocols and hardware. The submodule capacitor voltage transmission to the central controller is avoided in [14], [15] to lower the communication bandwidth. However, the features of the resulting network are not clearly provided in [14] and communication between the neighboring submodules is required as well as with the central controller in [15]. In [16], a three-layer control hierarchy is proposed by inserting arm controllers between the central controller and the submodules. An inter-integrated circuit (I^2C) bus with 350 kHz clock frequency is used for communication between the central controller and the arm controllers.

In this paper, a distributed control method is proposed and implemented on a lab-scale MMC. The control workload is divided between the central controller and local controllers located in the submodules. One-to-one asynchronous unidirectional serial-communication is used for data transmission with a 2 Mbit/s bit rate. This approach has only two layers of control, and the number of submodules can be increased with no latency penalty in the overall cycle time, increase in the bit rate or number of bits to be transmitted. The pulse width modulation carriers generated in the submodules are synchronized over the same communication channel. Indeed, the suitable synchronization accuracy of the local carriers is found to be much less than offered by the field-bus communication protocols, which are down to a couple of nanoseconds [6], [10]. By this way, the synchronization frequency is kept in the range of tens or hundreds of milliseconds which relaxes the communication requirements further.

The outline of this paper is as follows. The next section explains the proposed distributed control architecture including the central and local controllers design and implementation, also the communication between these controllers. Then simulation and experimental results of the proposed distributed control is presented with the related discussion of results and the conclusions of the paper.

Distributed Control Architecture

The distributed control architecture is founded on a two-level control hierarchy: a central controller and local controllers for each submodule located in them. This is the distributed control architecture mostly proposed in the literature. In the centralized control, all the control algorithms and modulation of the ac-side voltage are run in the central controller, and then the resulting switching signals are sent to the submodules. In the distributed control, on the other hand, the central controller executes the control algorithms which are based on the operator defined set-points and converter-level measured signals. Here, the ac-side voltage modulation references for each arm of the converter are periodically generated and transmitted to the local controllers. The measured arm currents, the dc-bus voltage, and the synchronization data for the modulation carriers in the local controllers are transmitted along with the modulation references. The local controllers run individual pulse width modulation and capacitor voltage balancing control by using the data received from the central controller and own capacitor voltages. No capacitor voltage is transmitted from the local controllers to the central controller or any other submodule by using proper control algorithms which relieves the requirements on the communication bandwidth and cycle time. All the auxiliary signals that may be sent from the local controllers to the central controller (such as semiconductor states, temperature, or current through the submodule) are eliminated. Thus, the communication between the central controller and the local controllers is kept unidirectional. Serial asynchronous communication with half duplex RS-485 (TIA/EIA-485) physical layer is used for the communication between the central controller and the local controllers. The communication network is digitally isolated from the high-power circuit in the submodules. The block diagram of the control architecture is shown in Fig. 1.

The proposed control architecture is generic and can be applied as is to MMCs with any number of submodules per arm. The data transmission cycle time and number of bits to be transmitted stay the same (details of the transmitted data are given in the next section). The unidirectional data transmission contributes to lower the communication bandwidth and allows the central controller to update the modulation references more frequently. On the other hand, the submodules should be able to handle their internal faults themselves, which results in increased autonomy and processing in the submodules. However, these related research subjects are not in the contents of this paper.

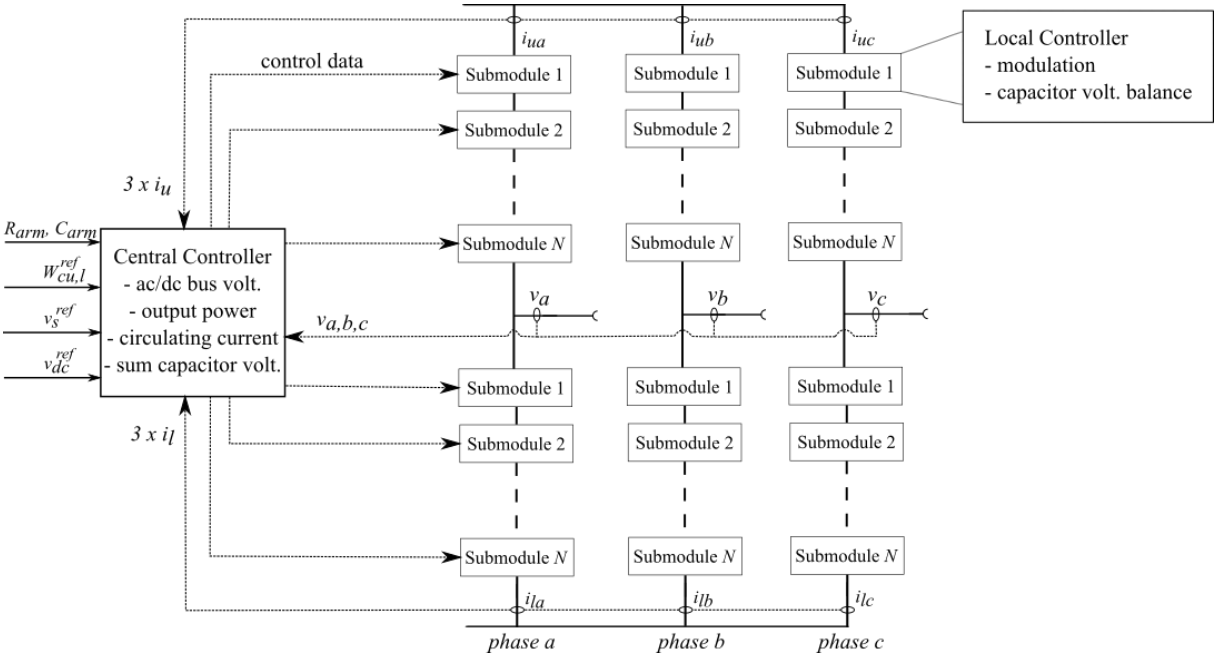

Fig. 1: Block diagram of the distributed control architecture.

Central Controller Design

The central controller is responsible for the high-level control tasks of the converter, specifically, controlling the ac-bus and dc-bus voltage, the output power, circulating currents, and sum capacitor voltages. The output current controller can be implemented as proportional-resonant (PR) controllers in each phase or as a vector output-current control in the *dq* frame [17]. Circulating current control and sum capacitor voltages control comprises the arm-balancing (internal) control of the converter. Circulating current controller can be implemented similar to the output current controller: either with a PR controller per-phase or as a vector circulating-current control in the *dq* frame. The open-loop voltage control method is proposed as the sum capacitor voltages control [18]. This method does not use capacitor voltages and provides inherent asymptotic stability making it suitable for a simple distributed control application. The central controller block diagram is shown in Fig. 2(a). In the figure, i_s* and i_s are the reference and instantaneous ac-side output currents; i_c* and i_c are the reference and instantaneous circulating currents; v_{dc} is the input dc-bus voltage; v_s* and v_c* are the reference modulation indices for the output and circulating current controllers; v_{cu}^{Σ}* and v_{cl}^{Σ}* are the sum capacitor voltage references for the upper and lower arm; n_u and n_l are the modulation references for the upper arm and lower arm, respectively.

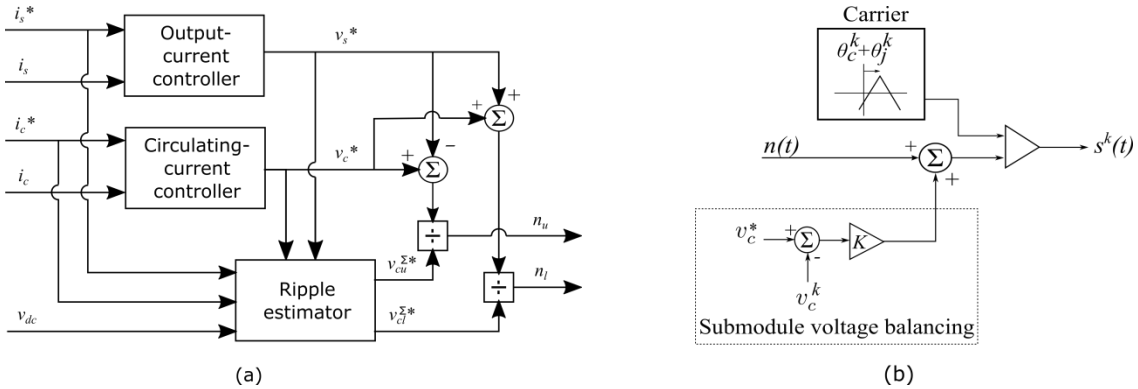

Fig. 2: (a) Open-loop voltage control in the central controller [18]. (b) Local controller in the submodules [17].

The central controller is implemented on a Xilinx Zynq XC7Z020 system-on-chip (SoC). This SoC comprises a programmable logic (PL) and a dual-core processing system (PS). Arm currents and ac-

side voltages are acquired by the PL from analog-to-digital conversion integrated circuits and are shared to the PS, where the control algorithms run. The generated modulation references for each arm are sent back to the PL to be transmitted to the local controllers. Optionally, the proportional gain of the individual submodule capacitor voltage balancing controllers which run in the local controllers can be sent from the central controller. Thus, six data packages are formed corresponding to the six arms of the converter. A sample data package is shown in Fig. 3. The data is sent asynchronous serially with 480 ns bit length (2.08 Mbit/s), and the total packet length is 54 bits. The modulation reference update frequency (and correspondingly the data transmission frequency to the local controllers and the analog-to-digital conversion sampling frequency for arm currents and ac-side voltage) is set to 10 kHz.

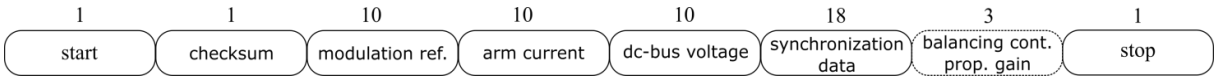

Fig. 3: Data to be transmitted from the central controller to the all submodules of an arm with the corresponding number of bits on top.

There are possibilities in the proposal to decrease the amount of data and the bandwidth of the communication. Firstly, the arm current can be sensed locally in the submodules. Together with the gain of individual submodule capacitor voltage balancing controller, 13 bits can be saved resulting in 41 bits of data to be transmitted which takes less than 20 µs to transmit with the current 2.08 Mbit/s bandwidth. Then, depending on the processing time of the transmitted data in the local controllers, the bandwidth of the communication can be decreased or the modulation reference update frequency can be increased.

Local Controller Design

Local controllers are responsible for the modulation of the submodules and their capacitor voltage balancing. Phase-shifted carrier-based modulation with non-integer pulse number is employed in the local controllers together with individual submodule-capacitor-voltage control [17]. In this way, modulation and capacitor voltage balancing of a single submodule is rendered independent from the capacitor voltages of the other submodules. Using open-loop voltage control in the central controller and phase-shifted carrier-based modulation in the local controllers, the communication bandwidth between the central and local controllers is relieved. Although phase-shifted carrier-based modulation with non-integer pulse number provides energy balance between submodules, individual submodule-capacitor-voltage control helps to keep the balancing against component variations, measurement, and communication errors. The block diagram of the local controllers is shown in Fig. 2(b) where $n(t)$ is the modulation reference sent from the central controller, θ_c^k and θ_j^k are the phase-shift and phase synchronization offset, v_c^* and v_c^k are the reference and instantaneous capacitor voltages, respectively, and s^k is the switching pulse.

One critical challenge of the distributed control is the need for modulation carrier synchronization of the submodules. If the phase-shifted carriers are adequately synchronized, the first group of ac-side voltage harmonics appears around the number of submodules per arm times the carrier frequency, which is one of the MMCs substantial advantages. In case of loss of synchronization, carrier and sideband harmonics are generated at every odd integer multiple and around every integer multiple of the pulse number, respectively. The suitable frequency of the synchronization depends on the synchronization accuracy, individual clock stability of the local controllers, and the ac-side harmonic content limitations. In the proposed design, the carrier synchronization is conducted every 100 ms by the phase offset sent from the central controller [19]. The proposed synchronization procedure is as follows: Together with the carriers generated in the local controllers, a carrier with the same frequency is generated in the central controller. The instantaneous phase of the carrier in the central controller is broadcasted to all the local controllers periodically and is used as the reference phase offset. The local carrier with zero phase-shift synchronizes, as soon as it receives, to this offset while the others add their phase-shift on top. In this procedure, there is some time delay between when the phase is sampled in the central controller and when this offset is received in the local controllers. However, this delay does not constitute a distortion in the ac-side harmonic content as long as the differences between reception times of the phase offset in the local controllers are in a proper range [19]. Then the local

carriers are built on top of the very same phase offset. This requirement is applicable for one-to-one communication channels for all the submodules with the same hardware, software, and similar communication medium length. It is important to note that after the first synchronization, in the next synchronizations, the broadcasted phase offset is not arbitrary for the local carriers. The difference between the broadcasted phase and the local phase depends on the difference between individual clock stabilities of the central and local controllers.

In Fig. 4, switching pulses (V_{GS} of half-bridge MOSFETs) generated in two local controllers with the same phase-shift and the same modulation references are shown. The controllers receive the modulation and synchronization data over similar length cables. The sum of synchronization accuracy and the gate turn-on time difference is approximately 48 ns. The synchronization accuracy itself, which is not shown here, is found as approximately 10 ns.

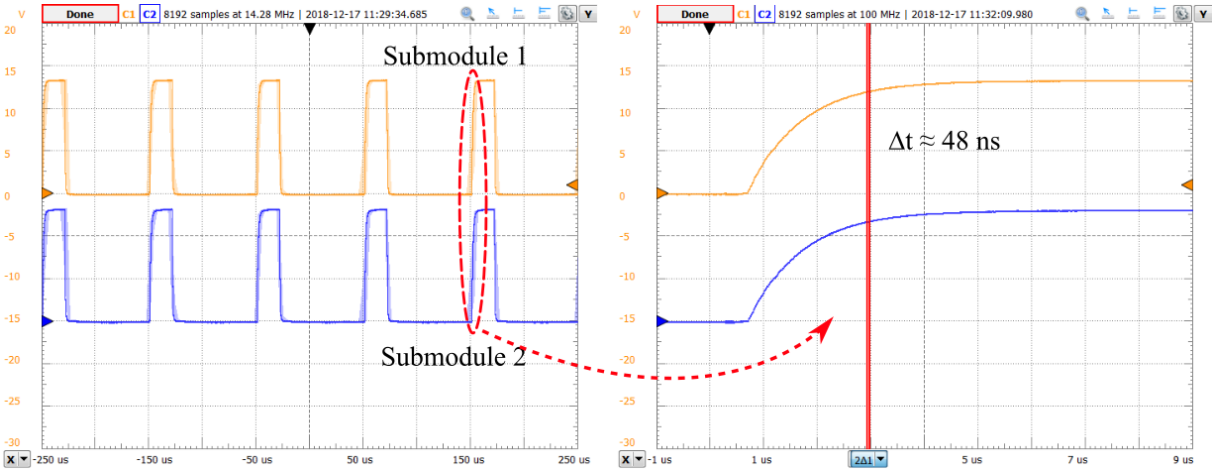

Fig. 4: Measurement results of the carrier synchronization accuracy in the submodules.

Local controllers are always in receiving mode of operation to receive data from the central controller. The reception of the data package starts with the start bit shown in Fig. 3, and each bit is sampled at the middle of the bit length. The central controller and the local controllers have the same clock frequency in PL, where the communication is conducted. In case of asynchronous serial communication, the small differences between the frequencies of the transmitter's and the receiver's clocks integrate over time, and the receiver may sample the data before or after the point it should, as shown in Fig. 5. Thus, for proper data reception, the difference between the clock frequencies of the transmitter and the receiver, Δf_{cl}, should comply with the criterion

$$\Delta f_{cl} < \frac{T_{bit}/2}{N_{bit} \cdot T_{bit}} = \frac{1}{2 \cdot N_{bit}}, \tag{1}$$

where T_{bit} is the bit length and N_{bit} is the number of bits in the data package. Having 54 bits in the data package, Δf_{cl} is 1/108 for the proposed design. The contemporary FPGA clock source frequency stability is less than ±100 ppm (in our case ±50 ppm for the transmitter and the receivers) making Δf_{cl} equal to ±200 ppm and much less than Δf_{cl} of the proposed design. Consequently, the data transmission remains synchronous from the beginning till the end of the data package. Nonetheless, in the local controllers, the receivers are designed such that at every received data transition from 0 to 1 or 1 to 0, receiver sampling counter is reset and, by this way, synchronization is repeated.

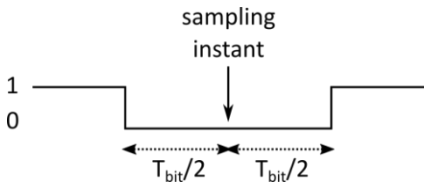

Fig. 5: Data sampling in serial communication.

Local controllers are implemented on DIPFORTy1 "Soft Propeller" which is equipped with Xilinx Zynq-7 XC7Z010 SoC comprising PL and a dual-core PS. The local controller measures capacitor voltage with an analog-to-digital conversion integrated circuit (with twice the carrier frequency, to use in the individual capacitor voltage balancing control), receives the transmitted data from the central controller and runs the modulation and individual capacitor voltage balancing control. All these functions are implemented on the PL.

Simulation Results of the Distributed Control

The proposed distributed control method is simulated with MATLAB Simulink with the parameters of a lab-scale MMC [20]. The simulation parameters are listed in Table I, and simulation results are shown in Fig. 6.

Table I: Simulation and experiment parameters

	Symbol	Value
Fundamental frequency	f_1	50 Hz
Dc-bus voltage	V_{dc}	200 V
Submodules per arm	N	5
Submodule capacitance	C	2.7 mF
Arm inductance	L_{arm}	8 mH
Arm parasitic resistance	R_{arm}	0.5 Ω
Load resistance (Y connected)	R_o	9.5 Ω
Modulation index	m_a	0.95
Pulse number (frequency ratio)	m_f	15.26
Phase-shift offset between upper and lower arm modulation carriers	$\delta\theta_c$	0 rad
Synchronization period of carriers in submodules	-	100 ms
Frequency stability of the clocks generating the modulation carriers	$\Delta f/f_{osc}$	50 ppm

In the simulation results, the ac-side phase voltages, ac-side currents, and circulating currents are stable in the steady state. All the ac-side phase voltage harmonics are well below 1 % of the fundamental harmonic, the largest being sideband harmonics around the equivalent switching frequency with 0.25 % of the fundamental. The individual capacitor voltages are balanced around 40 V, but have negligible differences sourcing from the integration of carrier asynchronism in the local controllers between consecutive synchronizations.

Experimental Results of the Distributed Control

The proposed distributed control method is implemented on the lab-scale MMC (Fig. 7) in the inverter mode of operation. Parameters of the experimental setup are shown in Table I. In the central controller, the output current and the circulating current controllers are implemented as vector output-current control in *dq* frame and PR controller in each phase, respectively. Measured results are shown in Fig. 8. The ac-side voltage waveform in Fig. 8 shows the first three cycles of fifteen consecutive ten cycle measurement windows which are defined as “very short time harmonic measurements” in [21]. Individual harmonics larger than 0.1 % of the fundamental harmonic and up to the 100^{th} harmonic are shown in the figures and included in the total harmonic distortion (THD) calculation where applicable. Interharmonic components are included in the THD calculation. The ac-side current waveform and its harmonic spectrum are necessarily the same as the ac-side voltage waveform and its harmonic spectrum due to the resistive load. Therefore, the current figures are not shown.

The experimental results show consistency in the simulation results. Ac-side phase voltage and currents are stable in the steady-state. All the ac-side phase voltage harmonic components are well below 1 % of the fundamental. There are some low-frequency odd harmonic components. The largest of those is the 13^{th} harmonic with 0.35 % of the fundamental. In the high-frequency range, $\pm5^{th}$ sideband harmonics of the equivalent switching frequency are the largest with 0.62 % of the fundamental. Total harmonic distortion of the ac-side phase voltages is 1.13 %. Individual submodule

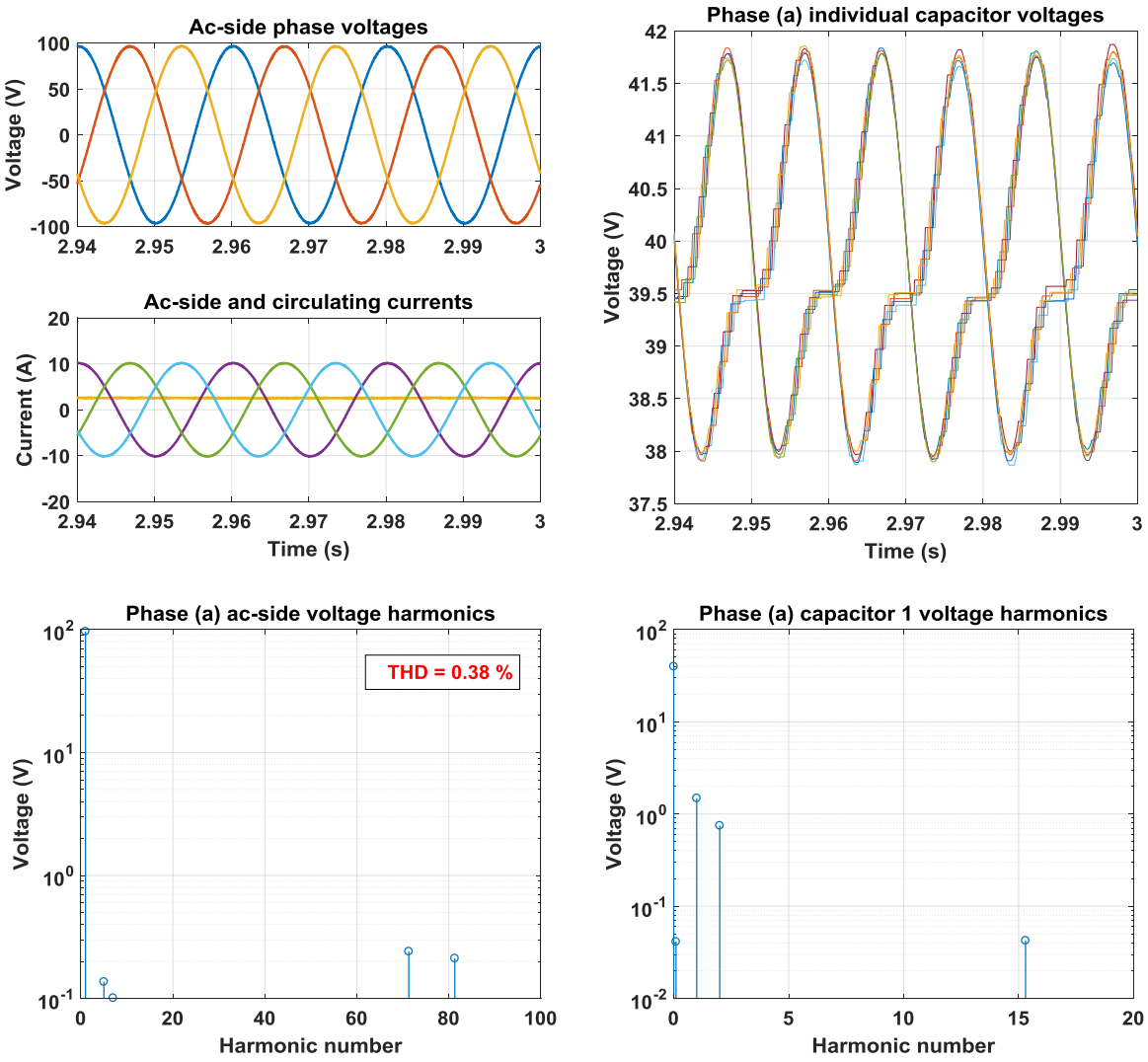

Fig. 6: MMC ac-side phase voltages, ac-side currents, and circulating currents (top left), phase (a) individual capacitor voltages (top right), phase (a) ac-side phase voltage harmonic spectrum (bottom left) and voltage harmonic spectrum of a submodule capacitor in phase (a) (bottom right).

capacitors are balanced around 40 V and have small fundamental (4.37 % of the dc) and second (1.95 % of the dc) harmonic components resulting from the imbalance-energy ripple between the phase arms and the total-energy ripple of the two arms, respectively. In light of these figures, the proposed simple distributed control method is able to provide satisfactory steady-state performance.

Conclusion

For the MMC, it is topologically convenient to scale up the voltage and power ratings of the converter by increasing the number of submodules. However, centralized MMC control gets demanding in terms of processing power and communication bandwidth between the controller and the submodules. Distributed control of MMC can overcome these limitations by splitting the workload between different controllers at hierarchical levels. However, distributed control has challenges as well. The complexity and the cost of the distributed control and communication should be minimized. In this paper, a distributed control method is proposed, simulated on MATLAB Simulink and implemented on a lab-scale MMC. Asynchronous serial-communication with 2 Mbit/s bit rate is used for unidirectional data transmission from the central controller to the local controllers. The carrier synchronization is repeated with 10 Hz frequency. It is shown that distributed control can be realized with simple hardware and low communication bandwidth without specialized field-buses and sophisticated synchronization mechanisms. The unidirectional data transmission and the fixed control

Fig. 7: MMC prototype.

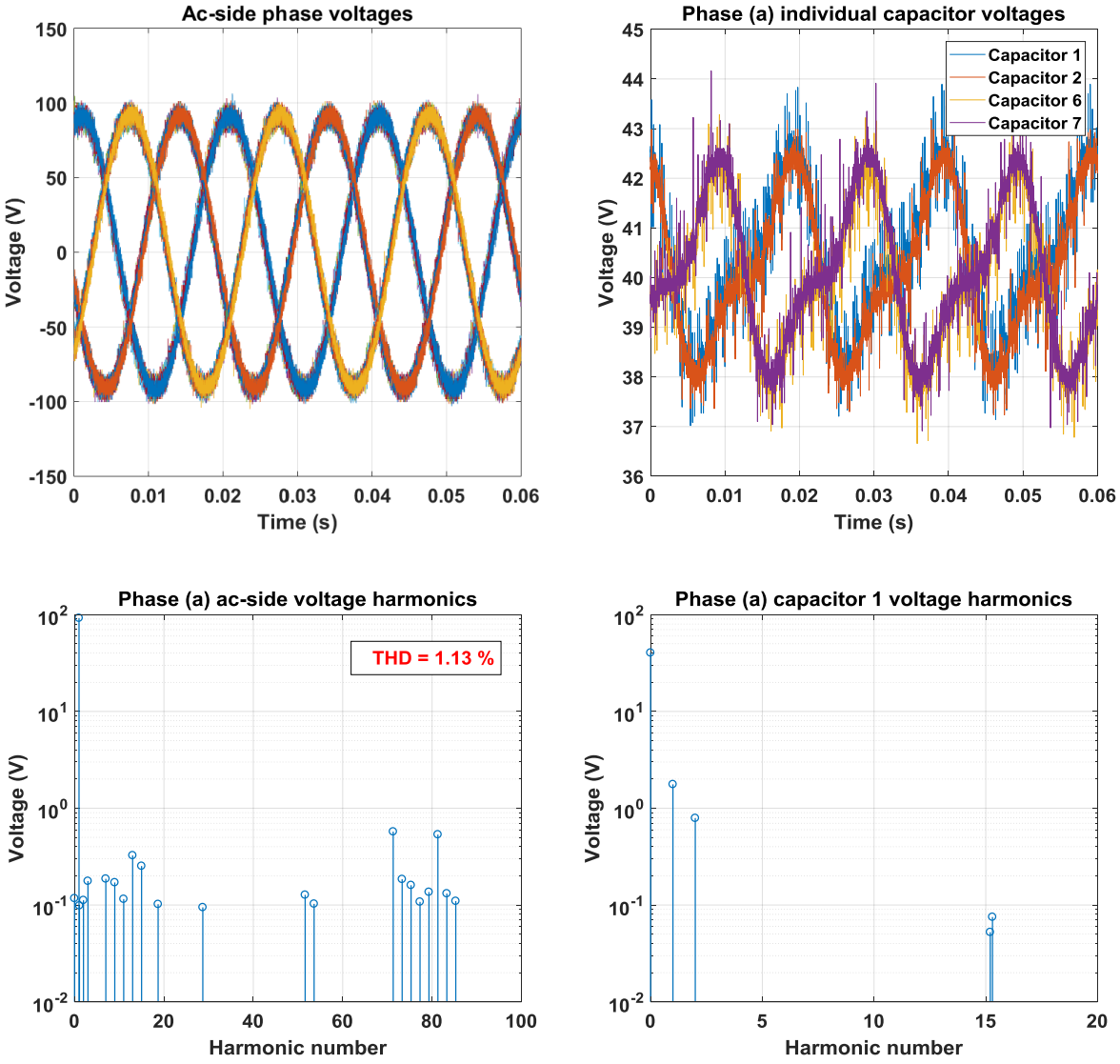

Fig. 8: MMC ac-side phase voltages (top left), phase (a) individual capacitor voltages (top right), phase (a) ac-side voltage harmonic spectrum (bottom left) and voltage harmonic spectrum of a submodule capacitor in phase (a) (bottom right).

data structure and length provide good scalability for the MMC especially for wireless communication between the central controller and the local controllers where they can share the same communication channel for broadcast type of messages.

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