# Implementation of a Highly Efficient Solid State RF Power Source for Superconducting Cavities

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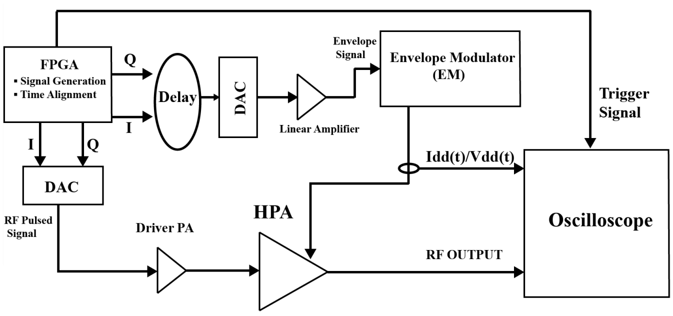
## I. INTRODUCTION

RF super conductive cavities (SC) used to accelerate charged particles, need to be charged to a nominal voltage after which the beam can be injected. The nominal voltage is provided by using high power RF sources such as: Klystrons, Tetrodes, Inductive Output Tubes, and Solid State Power Amplifiers (SSPAs). A step charging profile is used as a conventional procedure in order to fill such cavities to the nominal voltage. During the initial filling time, the cavities behave as a mismatched load and a large amount of RF power is then reflected. In a previous work [1], a novel strategy was proposed for SC filling, by shaping in time the profile of the RF power applied in order to minimize the total reflected power. A time filling profile for the SC spoke cavities of the European Spallation Source (ESS) is proposed, theoretically demonstrating a better performance, as compared to step charging. The optimal charging scheme shows the best performance when using SSPAs, demonstrating an overall power efficiency improvement of 10%. One disadvantage of using this filling scheme is the dynamic efficiency of the SSPAs, essentially in the low power range.

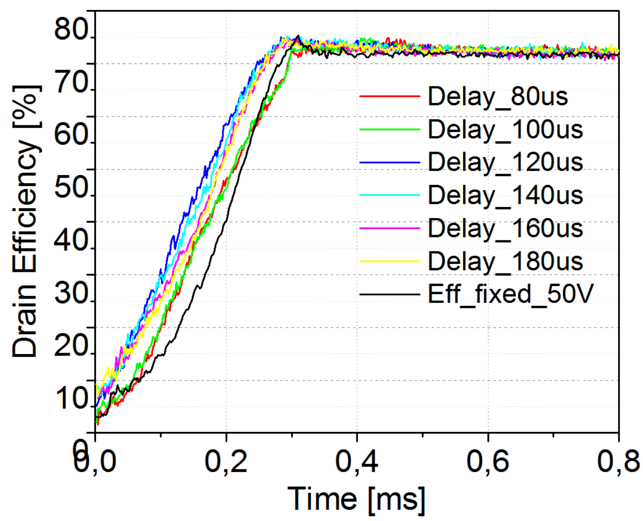
In this paper, we present the proof of concept of the theoretical development [1] using a highly efficient SSPA by drain supply-modulation. This implementation is relatively more accessible for SSPA, as the supply modulation is at 50V level. therefore, we implement the optimal charging power profile, without compromising the energy efficiency improvement by using drain voltage modulation. The proof-of-concept implementation is realised using a 352 MHz single-ended SSPA module [3] demonstrating an improvement of 25% of the overall power efficiency, **cite your paper 1**, by improving the drain efficiency of the SSPA in the low power range, thus enhancing the overall efficiency of the solid-sate based RF power sources.

## II. RESULTS

The high power RF SSA with supply-modulation consists of a fast envelope modulator (SM52) from Delta, the SSPA module [3], the FPGA-based control board, and a 4-channel DAC reference board (DAC34SH84EVM). The FPGA control




board is a Xilinx Kintex-7 (XC7K325T-2FFG900C). We use the FPGA to generate the envelope signal to control the supply modulator and we digitally generate the RF signals to feed the power amplifiers chain. In order to test the delay mismatch between the envelope and the RF signals, the envelope signal is programmable aligned with positive and negative delays, while the RF signal is fixed. The shaped baseband signal, as introduced in [1], is represented in IQ signals. The IQ signals from FPGA processor then are upconverted to 352 MHz before inputing to 16-bit D/A converter of channel A. The RF pulsed signal is linearly driven by a 100W amplifier from Minicircuits (ZHL-100W-52+) before feeding to the 1 kW SSPA module. The ET system is characterized using the measurement setup, as described in [4].




The temporal drain efficiency is presented at Fig.1. During the filling time, the drain efficiency at low power levels is improved by 100% as compared to the case when using a constant drain voltage. In the presented implementation, the overall wall plug efficiency is improved by 24%, **see cite your paper 1**.

## III. CONCLUSIONS

The paper demonstrates the implementation of a high power supply modulated SSPA using an optimal strategy for SC filling, saving about 24% energy from wall plug.

## REFERENCES

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