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Abstract—This paper presents a monolithic fully-differential amplifier implemented in a low-voltage 4H-SiC BJT technology. The circuit has been designed considering the variation of device parameters over a large temperature range. A base-current compensation technique has been applied to overcome the low input-resistance of the amplifier. The bare chip of the amplifier has been measured from 27 ºC to 500 ºC using a hot-chuck probe station. Its open-loop gain is 58 dB at 27 ºC, and monotonically decreases to 37 dB at 500 ºC. Its closed-loop gain reduction is around 5 dB over the investigated temperature range. The gain-bandwidth product drops from 2.8 MHz at 27 ºC to 1.3 MHz at 500 ºC with 470 pF off-chip compensation capacitors. A low total-harmonic-distortion of -58.4 dB at 27 ºC and -46.9 dB at 500 ºC is achieved due to the fully-differential implementation. A low input offset voltage of 0.5 mV at 27 ºC and 6.9 mV at 500 ºC is achieved without calibration. The relative high linearity and low offset demonstrate the potential of this technology to be further investigated for front-end sensor circuits in high-temperature applications.

Index Terms—Silicon carbide (SiC), bipolar junction transistor (BJT), integrated circuits (ICs), fully-differential amplifier, common-mode feedback (CMFB), high temperature, wide band-gap (WBG), Spice Gummel-Poon (SGP).

I. INTRODUCTION

Analog front-end electronics, able to operate reliably up to 500 ºC without external cooling, are widely needed to support active sensor applications in harsh environment, such as down-hole instrumentation, space exploration and turbine engine monitoring [1], [2]. To reduce noise and interference, the front-end electronics as shown in Fig. 1 is preferable to be located in close proximity to the sensor. The amplifier is a crucial block in the mentioned system, which can significantly enhance the weak output signal of the sensor and relax the design requirements of the succeeding analog-to-digital converter.

Several Silicon-based amplifiers have been demonstrated to operate up to 300 ºC [3]-[5]. At this temperature, Silicon-based electronics has already reached its limit, because the intrinsic carrier concentration of Silicon begins to approach device doping levels. Above 300 ºC, instead, Silicon Carbide (SiC) is a promising candidate for high-temperature electronics due to its wide bandgap. Its bandgap is almost three times that of Si, which results in low intrinsic carrier concentration, orders of magnitude lower than that of Si [1]. High-temperature MOSFET SiC amplifiers have been demonstrated in [7]-[10], in which the maximum operation temperature is 500 ºC [10]. On the other hand, JFET SiC amplifiers can operate stably at ambient temperature up to 576 ºC [11], [12] by eliminating gate oxide. Compared to JFETs, BJTs are potentially better for high-precision (lower offset/noise) and high-speed analog integrated circuits (ICs) (larger $g_m/I_c$), as discussed in [13].

Unlike digital ICs, analog ICs are more sensitive to device performance variation (e.g. current gain of BJT, resistor values), especially over a large temperature range. Moreover, technology immaturity such as only one metal layer and lack of PNP transistors (currently available in [6]) limits the circuitry performance and topology. Considering the mentioned challenges, the first 4H-SiC BJT fully-differential amplifier has been designed and characterized up to 500 ºC in this work. Section II gives the measured characteristics of the selected SiC devices and the corresponding extracted models used for circuit simulation. Section III describes the detailed circuit design including the amplification stages, the common-mode feedback circuit and the base current compensation circuit. Subsequently, the measurement setup and results of the amplifier are presented and discussed in Section IV. Finally, the conclusion is given in Section V.

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II. DEVICE PERFORMANCE

The SiC NPN BJT is fabricated using an in-house process on 4-inch 4H-SiC wafers with six epitaxial layers, which is illustrated in [14]. A BJT on the same die, near the amplifier has been characterized from 27 °C to 500 °C on a hot-chuck probe station. Accordingly, the forward DC parameters of the Spice Gummel-Poon (SGP) models have been extracted at six temperature values over the considered temperature range. The DC performance of the amplifier mainly relies on the BJT forward current gain $\beta_F$, Fig. 2(a) shows the measured $\beta_F$ versus collector current over the considered temperature range, in which two simulation results are plotted. The targeted operating region (500 $\mu$A ~ 2.4 mA) is determined by simulating the circuit using the SGP DC parameters, which were extracted from the previous batch fabricated in the same process [15]. Fig. 2(b) shows that in the operating region, the temperature dependency of the maximum $\beta_F$ is not monotonic. This behavior can be attributed to two competing mechanisms that affect $\beta_F$ when the temperature increases: reduction of the emitter injection efficiency due to increased ionization degree of base dopants and increase of carrier lifetime [16]. In addition, Fig. 2(b) also shows that when $I_C$ is 2.4mA, $V_{BE}$ of the BJT presents a negative temperature dependency.

III. CIRCUIT DESIGN

Fully-differential design has been employed due to its advantages such as noise immunity, even-order harmonics cancellation and wider output swing. Compared to single-ended output amplifier, an additional terminal $V_{REF}$ in Fig. 4 is used to control the output common-mode voltage, which offers more controllability to accommodate temperature variations.

A. Two-stage amplification

To achieve an open-loop gain of 60 dB, a generic two-stage amplifier is adopted from [17] with alteration to the fully-differential architecture and the additional input emitter-follower stage, as shown in Fig. 4. Due to the absence of PNP transistors in this technology, all the loads are resistors. Since the SiC BJT has small input resistance (≤ 1 kΩ), the input emitter-follower stage ($Q_{1,3}$) is used to increase the input resistance as given by:

$$R_{in} = 2(r_{s1} + (\beta + 1)(R_{E1} \parallel r_{s1}))$$  \hspace{1cm} (1)$$

where $r_{s1,3}$ represent the equivalent input resistance of $Q_{1,3}$.
respectively. Compared to the design without the input emitter-follower, a diode-drop voltage (2.8V at 27°C and 2V at 500°C) below ground is introduced which decreases the input voltage of Q3 and Q4. Thus to maintain the operating point of Q9-Q10, the values of RC3-RC6 are carefully chosen by simulation using the models discussed in Section II. However, the additional emitter-follower will increase the input offset voltage and reduce the gain. The open-loop DC-gain \( A_{dc} \) is given by:

\[
A_{dc} \approx \frac{g_{m1} \left[ R_{C3} \left| (r_{x3} + r_{x6}) \right| g_{m3} \left[ R_{C5} \left| (r_{x11} + \beta R_{x11}) \right| \right] \right]}{1 + g_{m1} R_{x1}} \tag{2}
\]

where \( g_{m1,2,3} \) are the transconductance of Q1,3,5 respectively. The 2nd-stage (Q5, Q6) is biased by high current to provide high gain and high slew-rate. The off-chip Miller capacitor \( C_C \) is used to improve stability, which is determined by \( g_{m1} \) and the gain-bandwidth \( g_{m1}/\text{GBW} \). The output node \( (V_{OP}/V_{ON}) \) of the 2nd-stage determines the bandwidth.

B. Common-mode feedback

The fully-differential amplifier requires a common-mode feedback (CMFB) circuit [18] as shown in Fig. 4, since mismatch or process/temperature variation can change the output common-mode voltage. The Darlington configuration of Q1 and Q6 has been employed to improve the matching of the current source. The common-mode voltage \( (V_{O,CM}) \) at output nodes \( V_{OP} \) and \( V_{ON} \) is sensed by two large matched resistors \( R_{CM} = 500 \text{ kΩ} \) without lowering the open-loop gain. The emitter-follower stage \( (Q1_1, Q1_2) \) is interposed to further eliminate the resistive loading. However this technique produces a new common-mode voltage \( (V'_{O,CM}) \) lower than \( V_{O,CM} \) by \( V_{BE} \), which varies with temperature (-2 mV/°C). Subsequently, an amplifier \( (Q3_1, Q3_2) \) is employed to detect the difference between \( V_{O,CM} \) and the reference voltage \( V_{REF} \). The comparison result \( V_{CNTRL} \) is negatively fed back to control the two current sources \( (Q_9, Q_{10}) \). If \( V_{O,CM} \) rises, so does \( V_{CNTRL} \) thereby the collector current of \( Q_9 \) and \( Q_{10} \) increase but the output \( V_{O,CM} \) decreases.

\( V_{REF} \) is temperature-dependent due to the temperature-drift of \( V_{BE} \) of Q11 and Q12, thus its value needs to be determined by simulation. ±7.5 V has been chosen for power supply by considering the trade-off between enough output swing and power dissipation. Fig. 5(a) indicates that when \( V_{REF} \) is between -4.8 V and -3.8 V, \( A_{dc} \) is constantly over 50 dB up to 500 ºC. The reduction of operational range for \( V_{REF} \) beyond 300 ºC is attributed to the gain degradation of the CMFB circuit. Thus the midpoint of -4.2 V in the operational range has been chosen for \( V_{REF} \) to accommodate the entire temperature range. Fig. 5(b) indicates that when \( V_{REF} \) is chosen -4.2 V, the corresponding \( V_{O,CM} \) is between -2.7 V at 27 ºC and -1.1 V at 500 ºC.

C. Input base current compensation

The SiC BJT base current is quite high due to its low \( \beta_F \). Moreover, \( \beta_F \) is decreasing with temperature, thus the base current needs to be compensated, especially when the amplifier is used in the closed-loop mode. As shown in the right side of

\[ V_{CNTRL} \text{ vs. } V_{REF} \]

Fig. 5. Simulations results of amplifier (a) \( A_{dc} \text{ vs. } V_{REF} \) and (b) \( V_{O,CM} \text{ vs. } V_{REF} \) for 27 ºC to 500 ºC.

\[ V_{CNTRL} \text{ vs. } V_{REF} \]

Fig. 6. Input base current compensation circuit for the amplifier in closed-loop mode.

\[ V_{CNTRL} \text{ vs. } V_{REF} \]

Fig. 6, an improved current mirror is proposed to compensate the temperature effect. Darlington configuration of Q9 and Q10 has been employed to improve the matching of the current source. The emitter degeneration resistors \( R_9 \) and \( R_{10} \) are used to compensate the temperature effect. Diode-connected Q12,2 and R1 are used to compensate the amplifier input transistor's \( V_{BE} \) with respect to the temperature drift (-2 mV/°C).

IV. MEASUREMENT RESULTS

Fig. 7 shows the optical image of the fabricated amplifier including 24 NPN BJTs, 19 resistors and 12 metals-interconnect crossing-connectors (in collector layer) due to one metal layer used in this work. Fig. 8 illustrates the high-temperature measurement setup for the amplifier with configurable closed-loop and open-loop test-modes. By connecting the amplifier outputs to feedback resistors \( (R_{11,3}) \) and capacitors \( (C_{IP,N}) \), a signal-conditioning preamplifier is obtained. In addition, by choosing different input resistors \( (R_{O1,2}=500 \text{ Ω}, 5 \text{ kΩ}, 50 \text{ kΩ}) \), the corresponding closed-loop gains (100×, 10×, 1×) are obtained. All the components are implemented on-chip except the Miller capacitors \( (C_{L}=470 \text{ pF}) \).
external discrete component), because they consume large area in this technology (~30 pF/mm²). The power supply is ±7.5 V.

A. Closed-loop measurement

The Agilent MSOX-3024A oscilloscope is used to both generate input and acquire output. Except the Miller capacitors and the loads, the amplifier chip with resistors and capacitors (in orange color) is placed on a hot-chuck probe station as shown in Fig. 8. Fig. 9 shows the closed-loop gain frequency response (RF1,2/RG1,2=10), which is measured from 27ºC to 500ºC with two identical off-chip Miller capacitors. The closed-loop DC-gain (Adc,CL) decreases monotonically with increasing temperature. A ~5dB gain reduction of the amplifier has been observed from 27 ºC to 500 ºC. The gain-bandwidth determined by $g_m$ also presents a negative temperature dependency of ~ -0.21 kHz/ºC, which in turn indicates that the temperature drifts of $g_m$ is ~ -0.62 µS/ºC ($g_m = 57$ mS at 27ºC).

A square-wave input has been used to measure the response time of the amplifier in the closed-loop mode at 27 ºC and 500 ºC, as shown in Fig. 10(a). The positive slew-rate (SR+) of the amplifier is given by the slope ($\Delta V/\Delta t$) of the output signal rising-edge. As shown in Fig. 10(b), the temperature dependency of SR+ follows the curve of total current consumption. Since the SR+ is determined by the ratio of biasing current in the first amplification stage (~14% of total current consumption) and the Miller capacitor. Moreover, the positive output-level reduces more than the negative part (+6.2/-6.5 V at 27 °C to +2.8/-6.3 V at 500 °C), due to the positive temperature dependency of collector-layer load resistors.

B. Open-loop measurement

In the open-loop measurement (for open-loop gain and input offset voltage), the amplifier’s high gain makes it very hard to avoid errors from very small voltages at the amplifier input. Thus the proposed circuit as shown in Fig. 11 is made to minimize the measurement errors. It employs an auxiliary OpAmp (100 dB gain, low-offset) as an integrator to establish a negative-feedback loop for DC voltage, which forces the amplifier output to ground potential.

To measure the open-loop AC gain at node TestAC, a sinusoidal signal is applied to the amplifier input via a 100:1 attenuator. Fig. 12 shows the open-loop gain frequency response measured from 27 °C to 500 °C. At 27 °C, the
Adc,OL open-loop DC gain is 58 dB, and it monotonically drops to 37 dB at 500 ºC. According to (2), the gain is affected by operating region. Elevated temperature can drive the BJTs out of the targeted reality the input offset and drift of common-mode voltage at 27ºC to 500ºC (without Miller capacitors). Although the simulated open-loop gain-bandwidth have been achieved in this work.

TestDC by 1000 amplification (RFdc/RIdc). Relatively low Vos of 0.5 mV at 27 ºC and 6.9 mV at 500 ºC have been observed. Fig. 13(a) shows the transient output signals measured at 500ºC in the open-loop mode with a sinusoidal input. In addition, frequency-domain performance of the amplifier has also been characterized. Fig. 13(b) shows the power-spectrum-densities (PSDs) of the amplifier’s differential output measured at 27 ºC and 500 ºC respectively. Benefitting from the fully-differential design, even-order harmonics are canceled in the differential output response at 27ºC. At 500ºC, some even-order harmonics (6th, 8th and 10th) arise since the device mismatch becomes more significant, and the odd-order harmonics (5th, 7th) are attributed to the reduction of the output voltage swing. Considering the first 5 harmonics and fundamental frequency of 490 Hz in the PSDs, the total-harmonic-distortion (THD) is -58.4 dB at 27 ºC and -46.9 dB at 500 ºC.

Finally, a comparison of high-temperature monolithic voltage amplifiers is provided in Table I. Up to 300 ºC, Si-based CMOS amplifiers [3], [4] have demonstrated higher gain and gain-bandwidth than those in SiC NMOSFET [7]-[10]. Above 300 ºC, SiC dominates, and compared to the SiC JFET amplifier [11], lower offset and higher gain-bandwidth have been achieved in this work.

V. CONCLUSION

A fully-differential amplifier with common-mode feedback has been designed and implemented in a low-voltage 4H-SiC BJT technology. It has been measured on a hot-chuck probe station with/without off-chip Miller capacitors. From 27ºC to 500ºC, a closed-loop gain degradation of around 5 dB has been observed due to the open-loop gain reduction with increasing temperature. The bandwidth of the amplifier without Miller capacitors is constant around 1 MHz over the investigated temperature range without using Miller capacitors. The input offset voltage (Vos) is measured at node TestDC by 1000 amplification (RFdc/RIdc). Relatively low Vos of 0.5 mV at 27 ºC and 6.9 mV at 500 ºC have been observed.

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REFERENCES


