Automatic Design-Space Exploration of Integrated Multi-Standard Wireless Radio Receivers

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Tryck: Universitetsservice US AB
A mi abuelo,
que es un Ángel.
Abstract

One of the main challenges posed by 4G wireless communication systems is achieving flexible, programmable multi-standard radio transceivers with maximum hardware share amongst different standards at a minimum power consumption. Evaluating the feasibility and performance of different multi-standard/multi-band radio solutions at an early stage, i.e. system level, is key for succeeding in surmounting this challenge. This entails formulation of the transceiver budget for several RF architectures and frequency plans with different degrees of hardware sharing. This task is complicated by the fact that transceiver blocks can have different implementations that lead to different performances. The tools that are available for use at present have only analysis capabilities or address only one standard and/or receiver architecture at a time.

In the belief that a new approach to this problem is necessary, the work that has led to this thesis proposes a novel methodology that automates the design-space exploration of integrated multi-standard wireless radio receivers. This methodology has been implemented in a multi-standard RF Transceiver Architecture Comparison Tool, TACT. TACT helps surmounting many of the challenges faced by RF system designers targeting multi-standard/multi-band radio receivers.

The goal of the algorithms TACT is built upon is to find a multi-standard receiver frequency plan and budget that meets or exceeds the specifications of the addressed wireless standards while keeping the requirements of each of the receiver blocks as relaxed as possible. TACT offers RF engineers a deep insight into the receiver behavior at a very early stage of the design flow. It models the impact of critical circuit non-idealities using a high level of abstraction. This reduces the number of design iterations and, thus, the time-to-market of the solution. The reuse of already available intellectual property (IP) blocks is also considered in TACT, what can result in a significant cost reduction of the receiver implementation.

A case study of a WCDMA/WLAN multi-standard receiver designed using TACT is presented in order to illustrate the capabilities of the proposed techniques.
List of Publications


Publications not Included in this Thesis


Swedish System-on-Chip Conference (SSoCC), April 2004 (Non-reviewed publication).
Main Contributions of this Thesis

Professor Mohammed Ismail and Dr. Ana Rusu have acted as my advisors along the realization of the work that has led to my licenciate thesis. They have been available for discussion and evaluation of my proposed ideas and their practical implementation. The authors of RaMSiS research proposal should be acknowledged for identifying the need of performing architectural analysis of multi-standard systems that allows to break down the requirements of the system in an effective manner.

My contributions, related with the work that lead to this thesis and the publications mentioned above, can be summarized as:

- Identifying the need of automating the multi-standard receiver design and implement it in an EDA tool. This tool is called TACT, a multi-standard Transceiver Architecture Comparison Tool.

- Designing TACT's architecture [1] and implementing:
  - TACT's Frequency Planning Tool [2]. This tool provides the performance of different frequency plans. The main research contribution of this tool is the evaluation method of the effect out-of-band blockers.
  - TACT's Budget Tool [3]. This tool distributes the receiver specs keeping the specs of the individual blocks as relaxed as possible. The impact oriented parameter redistribution algorithm is the main contribution in this case.

- Showing the usefulness of the tool by means of a case study [5] and a comparative study [6] showing the decision making process that accompanies a receiver design and the way TACT helps RF designers making those decisions and getting closer to a Software Radio (SR).

- Publication [4] gives an overview of the challenges of designing an RF receiver and the way TACT can help. The contribution of this publication is to give perspective and show the place of TACT in the big picture of multi-standard receiver design.
• My contribution in paper [?] is providing the requirements for the ADC whose design is addressed in the rest of the paper.
Acknowledgments

Let me start by expressing my deepest gratitude to my advisor, Professor Mohamed Ismail. He is an endless source of inspiration and an example to follow. I would like to thank him for believing in me and giving me the chance to go through the exciting (and sometimes a bit scary) process of pursuing a PhD. I will never be able to thank him enough for his unconditional support and encouragement, and for allowing me to fly with my own wings.

Dr. Ana Rusu definitely deserves a special place in this section. She is a model of academic and personal excellence for me. I would like to thank her for having her door always open for me. Her guidance and support, both professional and personal, have been key in my development as a researcher and as a person.

Thanks to Professor Hannu Tenhunen for his valuable comments. It is with pleasure that I thank the rest of the RaMSiS group and my colleagues at the ECS lab for their valuable comments and continuous encouragement throughout this work. Many thanks to the administration staff and the system group for keeping things up and running around me. Special thanks to Adam Strak, Jad Atallah, Saúl Rodríguez Dueñas, Martin Gustafsson, Jintang Huang, Professor Li-Rong Zhen, Dr. Steffen Albrecht, Dr. Wim Michielsen, Dr. Xinzhong Duo, Fredrik Jonsson, Petri Färn, Dr. Elena Dubrova, Maxim Teslenko, Dr. Andrés Martinelli, Johan Wennlund, Fredrik Lundevall, Thomas Sjöland, Lena Beronius, Agneta Herling, Rose-Marie Lövenstig, Gunnar Johansson, Hans Larsson, May-Britt Eldlund-Larsson, Hans Berggren, Peter Magnusson, Julio Mercado, and Yajie Quin. It is a pleasure to have you around :).

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My warmest thanks to Werner Riegler, Stefan Parkvall, Ángel Álvarez Rodríguez, Javier Macías Guarasa, Elías Muñoz Merino, and Giovanni Anelli, for mentoring me along the past few years. I would like to express my appreciation to my former colleagues at CERN, Chalmers University of Technology, and the Technical University of Madrid.

I thank the authors of the publications that have inspired my research. I sincerely apologize for any reference omissions.

My love and gratitude to my family and friends, especially to my mum, María Jesús González Valbuena, and my brother, Luis Rodríguez de Llera González for
being always there for me. As for my friends, you guys know who you are (normally I leave no room for misunderstanding ;). Thanks for bringing a ray of light into my life :).

In sum, I would like to thank all the people that during the course of my life have helped me becoming who I am.
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<th>Abbreviation</th>
<th>Description</th>
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<tbody>
<tr>
<td>ADC</td>
<td>Analog-to-Digital Converter</td>
</tr>
<tr>
<td>AGC</td>
<td>Automatic Gain Control</td>
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<tr>
<td>Att</td>
<td>Attenuation</td>
</tr>
<tr>
<td>BB</td>
<td>Baseband</td>
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<tr>
<td>BER</td>
<td>Bit Error Rate</td>
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<tr>
<td>BPF</td>
<td>Band Pass Filter</td>
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<tr>
<td>BW, B</td>
<td>Bandwidth</td>
</tr>
<tr>
<td>CAD</td>
<td>Computer Aided Design</td>
</tr>
<tr>
<td>CDMA</td>
<td>Code-Division Multiple Access</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal-Oxide-Semiconductor</td>
</tr>
<tr>
<td>COTS</td>
<td>Commercial-off-the-Shelf</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital-to-Analog Converter</td>
</tr>
<tr>
<td>dB</td>
<td>Decibel</td>
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<tr>
<td>DC</td>
<td>Direct (continuous) Current</td>
</tr>
<tr>
<td>DR</td>
<td>Dynamic Range</td>
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<tr>
<td>DSSS</td>
<td>Direct-Sequence Spread Spectrum</td>
</tr>
<tr>
<td>DVB-H</td>
<td>Digital Video Broadcasting for battery powered handheld devices.</td>
</tr>
<tr>
<td>EDA</td>
<td>Electronic Design Automation</td>
</tr>
<tr>
<td>ENOB</td>
<td>Effective Number of Bits</td>
</tr>
<tr>
<td>ETSI</td>
<td>European Telecommunications Standard Institute</td>
</tr>
<tr>
<td>f</td>
<td>Frequency</td>
</tr>
<tr>
<td>FDMA</td>
<td>Frequency-Division Multiple Access</td>
</tr>
<tr>
<td>FHSS</td>
<td>Frequency-Hopping Spread Spectrum</td>
</tr>
<tr>
<td>GSM</td>
<td>Global System for Mobile communications (Groupe Spécial Mobile originally)</td>
</tr>
<tr>
<td>IEEE</td>
<td>Institute of Electrical and Electronics Engineers, Inc.</td>
</tr>
<tr>
<td>IF</td>
<td>Intermediate Frequency</td>
</tr>
<tr>
<td>IPk</td>
<td>k-th order Input Referred Intercept Point</td>
</tr>
<tr>
<td>IM</td>
<td>Intermodulation</td>
</tr>
<tr>
<td>IP</td>
<td>Intellectual Property</td>
</tr>
<tr>
<td>IR</td>
<td>Image Rejection</td>
</tr>
<tr>
<td>LNA</td>
<td>Low Noise Amplifier</td>
</tr>
<tr>
<td>LO</td>
<td>Local Oscillator</td>
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<tr>
<td>LPF</td>
<td>Low Pass Filter</td>
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### LIST OF ABBREVIATIONS

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<th>Abbreviation</th>
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<tbody>
<tr>
<td>NF</td>
<td>Noise Figure</td>
</tr>
<tr>
<td>nf</td>
<td>Noise Factor (normally represented as f in literature)</td>
</tr>
<tr>
<td>NRE (cost)</td>
<td>Non-Recurring Engineering (cost)</td>
</tr>
<tr>
<td>OIPk</td>
<td>k-th order Output Referred Intercept Point</td>
</tr>
<tr>
<td>PDA</td>
<td>Personal Digital Assistant</td>
</tr>
<tr>
<td>PG</td>
<td>Processing Gain</td>
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<tr>
<td>PLL</td>
<td>Phase-Locked Loop</td>
</tr>
<tr>
<td>PN</td>
<td>Phase Noise</td>
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<tr>
<td>QoS</td>
<td>Quality-of-Service</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>RFIC</td>
<td>Radio Frequency Integrated Circuit</td>
</tr>
<tr>
<td>RoC</td>
<td>Radio-on-a-Chip</td>
</tr>
<tr>
<td>Rx</td>
<td>Receiver</td>
</tr>
<tr>
<td>SDR</td>
<td>Software Defined Radio</td>
</tr>
<tr>
<td>SIR</td>
<td>Signal-to-Interferer Ratio</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal-to-Noise Ratio</td>
</tr>
<tr>
<td>SoC</td>
<td>System-on-Chip</td>
</tr>
<tr>
<td>SR</td>
<td>Software Radio</td>
</tr>
<tr>
<td>TACT</td>
<td>Transceiver Architecture Comparison Tool</td>
</tr>
<tr>
<td>TDMA</td>
<td>Time-Division Multiple Access</td>
</tr>
<tr>
<td>THSS</td>
<td>Time-Hoped Spread Spectrum</td>
</tr>
<tr>
<td>TV</td>
<td>Television</td>
</tr>
<tr>
<td>Tx</td>
<td>Transmitter</td>
</tr>
<tr>
<td>UR</td>
<td>Usable Region</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage Controlled Oscillator</td>
</tr>
<tr>
<td>VGA</td>
<td>Variable Gain Amplifier</td>
</tr>
<tr>
<td>WCDMA</td>
<td>Wireless Code-Division Multiple Access</td>
</tr>
<tr>
<td>WLAN</td>
<td>Wireless Local Area Network</td>
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Chapter 1

Introduction

As we move beyond third generation (3G), the wireless scenario is rapidly becoming rather complex as shown in Figure 1.1. A mobile device, be it a phone, a PDA or a notebook, is expected to be feature-rich, and able to work with several wireless standards while achieving the highest performance/price ratio. The existing wireless standards are very different from one another. Moreover, each of them is fragmented in different operating frequency bands both due to the limited spectrum availability and the particular regulations in different geographical areas. Hence, 4G systems need to provide multi-band multi-standard capabilities in order to be competitive. In the effort of providing the user with an always best connected experience, handhelds are to roam among these coexisting standards in a seamless manner. Thus, the system will adapt to the environment offering the best available quality of service (QoS) and/or price for the different applications (data, voice, multimedia) the mobile terminal is running at a given time. Future mobile terminals would be able to seamlessly deal with the different services/standards at hand providing them with an always best connected experience for a given price level. This situation is highlighted in Figure 1.2, which shows examples of the various services available in different scenarios. Advances in both integrated circuits design and process technology permit the higher level of integration these systems require at a sufficiently low power consumption.

One of the main challenges for 4G wireless communications systems comes from trying to integrate the hardware of a number of wireless systems that have been conceived independently without being meant to be integrated [1, 2]. The requirements these various standards impose on the different blocks of the transceiver chain may vary immensely. This variation complicates their integration since the receiver architectures and block implementations that suit them best might be very different.

Building a receiver able to handle all these different standards is not an easy task. So why the effort? The answer comes in the form of product increased portability and reduced price, which are closely related to a reduction in silicon area and power
consumption. One way of obtaining this is by finding a programmable architecture where most of the blocks can be reused for different standards [3].

1.1 Receivers for Handheld Applications

The receiver in a mobile terminal is one of the most challenging cases to solve. The receiver's selectivity measures its ability to select a (possibly) weak desired signal channel in the (possible) presence of much stronger interferers (blockers, adjacent channels, etc.). As opposed to the transmitter, the receiver's input signals lie in an uncontrolled environment full of interferers. The desired channel may be a weak signal in a hostile environment. This makes detecting the desired signal in a receiver a David vs. Goliath type of situation. In mobile terminals low power consumption is a must in order to ensure as long a battery life time as possible. Asking a mobile terminal receiver to perform its task is like asking David to fight Goliath on an empty stomach: High performance level with a smart management of the available resources is required in all operation modes.

1.2 Design-Space Exploration

Some of the major decisions to be made when designing a receiver are the architecture, the frequency translation scheme, the way to distribute the radio specs among the individual receiver blocks, and the partitioning of the system [4, 5]. These de-
1.2. DESIGN-SPACE EXPLORATION

![Diagram showing different wireless scenarios and the connectivity options they provide.](image)

Figure 1.2: Different wireless scenarios and the connectivity options they provide.

cisions have to be made at a very early stage of the design cycle and will strongly determine the overall performance of the receiver as well as its cost and time-to-market. The higher the level a bad decision is made, the more time consuming and costly fixing the problem will be [6]. Hence, a thorough study of the different possibilities is crucial at the system level in order to ensure that the market window for a product is not missed.

When aiming at a multi-standard receiver the problem is further complicated in comparison with the single standard case. Obviously, a high level of performance is desired while keeping area and power consumption small. However, it is no longer adequate or possible to tweak the design of the receiver blocks until they satisfy an optimal performance for a particular application. Flexibility has to be provided both at the architectural and block levels so as to increase the level of hardware sharing. Being able to digitally tune and program the receiver at different levels is
CHAPTER 1. INTRODUCTION

key in order to succeed in achieving the selectivity and sensitivity levels required by the ever changing target applications.

Even though we are getting closer to the Software Radio (SD) paradigm, there are still a number of major practical problems associated with placing the ADC right after the antenna [7]. It will take some time before we can carry a true Software Radio in our pocket. Software Defined Radios (SDR), where digital techniques are applied to the analog world by means of digitally programmable analog circuits, can provide multi-standard capabilities with reasonable block requirements using today's technologies.

1.3 RF Systems Evolution

Advances in both integrated circuits design and process technology permit the increasing level of integration communication systems require at a sufficiently low power consumption [8]. Much of this evolution is due to the appearance of CMOS circuits suitable for RF [9, 10]. RF CMOS changed completely the landscape of radio transceivers. It produced a shift from systems assembled from discrete blocks built in different technologies and mostly based on the superheterodyne architecture to levels of integration that could only be dreamed of only few years ago [9-11]. Different technologies suit best the needs of the different parts of the system (RF front-end, digital baseband, etc.) leading to a high chip count and, therefore, larger area and cost. Even if CMOS did not look like a winner in the RF battlefield due to its inferior RF performance levels with respect to other technologies, it is becoming the technology of choice in the interest of integrability and cost.

Technology scaling has benefited enormously the digital world this far. Scaling related effects entail also some drawbacks, especially in the case of analog and RF circuits. Performing the analog-to-digital conversion as close to the antenna as possible sounds desirable considering that RF and analog circuits do not scale as well as their digital counterparts. Then the radio, which would then be a Software Radio (SR) [12, 13], would also take full advantage of the flexibility and programmability digital circuits provide. The system could even evolve into a cognitive radio [14] where user needs are better satisfied with a more efficient use of the available radio spectrum.

1.4 Reliability and Yield in Fully Integrated Radios

Providing a "true single chip" solution is in the interest of area and power save. Full System-on-Chip (SoC) where digital, mixed signal and RF blocks are put together presents serious reliability and yield issues, though. The low yield of the RF and mixed signal blocks would affect immensely the yield of the overall system. In contrast with their digital counterparts, analog and RF blocks have an extremely large design cycle. Moreover, the level of uncertainty between simulated and fabricated circuits and the limitations of available automated design tools for analog circuits
1.5 Challenges in Multi-standard Systems

Even in the single standard case, the level of complexity of a wireless communications receiver is enormous. When the multi-standard case comes into the picture, this problem is aggravated. The design of a multi-standard system is substantially more complex than the combination of the system level design of separate single-standard systems. One of the main challenges multi-standard systems have to overcome is interference. The increasing complexity of multi-mode systems entails the presence of many on-chip signals\(^1\) that may act as potential interferers to the neighbouring systems. Therefore the need of designing a careful frequency planning that takes into account the signals coming from all the standards. Careful layout and on-chip isolation mechanisms should not be forgotten later in the design cycle.

The advantage of programmable blocks and architectures comes in terms of reusability, flexibility, and area and power consumption. Moreover, using digitally tunable blocks allows to compensate for process variations and other effects that greatly affect analog circuits increasing, thus, the reliability of the overall system [15]. However, adding programmability entails an extra design effort that may not pay off in terms of performance. As opposed to a fully stacked solution, hardware reuse favours in principle the area reduction sought in multi-standard systems. But... shall we use programmable blocks that can handle several operation modes in all cases or is there any block that should be duplicated? Is a stacked solution that bad? In some cases, it may actually pay off having a completely independent signal path for some of the target standards. How do we decide that?

The realization of an efficient receiver budget and frequency planning is one of the most compelling problems RF engineers face nowadays. Even in the single standard case, the level of complexity of a wireless communications receiver is enormous. Keeping the performance levels high and the power consumption low in such a system is not an easy task. When the multi-standard case comes into the picture, coexistence issues and hardware sharing aggravate matters enormously.

1.6 The Need for EDA Tools

The system level design is still nowadays done in many instances using the help of spreadsheets. Besides being error prone, this method is very limited in the number of different design possibilities that can be explored within a given time [16, 17].

\(^1\) These signals might be generated on-chip or come from external sources.
EDA tools are clearly needed at different levels [4, 8, 11, 13, 18–20]. Different tools or methodologies focus on different aspects of RF receiver design. Tools connecting all the design stages from system level design to measurement of fabricated circuits are key for system verification purposes and fast time-to-market [21, 22]. There is a number of EDA tools [6, 21, 23–36] that automate parts of the RF system design process. Most of these tools help engineers in the design process, but the tools themselves focus on analysis [19, 23, 24, 27–29, 34–36]. They may provide accurate models for the blocks, the frequency behavior of certain parts of the circuit, or focus on the effect of parasitics in the performance of RF systems. In general, most of these tools provide little or no help at all to the RF engineer in defining the system level design specifications. Other reported tools [6, 26] and methodologies [37] help in the design process, but they only address the single-standard case [25] or are ad hoc tools [31, 32]. There is an enormous number of tools and methodologies that address the design of specific blocks of the receiver chain down to the layout level. They are not mentioned here since they are out of the scope of this thesis, where the focus is the design of the system, not of its individual blocks.

1.7 Aim of this Thesis

The work described in this thesis is aimed at easing the RF engineer’s job as it fills a gap left by the already available CAD tools that address the receiver design problem: the automation of the design-space exploration of multi-standard receivers at RF system level.

A multi-standard RF Transceiver Architecture Comparison Tool, TACT\(^2\), introduced in [38], has been devised to this end. TACT is an attempt to automate the know-how of an experienced RF system designer. Automating this design process reduces the design time since it replaces expensive manpower with cheap computational horsepower and evolutionary techniques.

This thesis describes TACT and its underlying methodology. TACT is a hierarchical, user friendly, MATLAB based tool. It automates the design-space exploration procedure for 4G wireless receivers at a high abstraction level [39]. This allows to explore a large design-space at the beginning of the design cycle. Thus, RF system engineers can get “the big picture” of what performance levels can be expected when making different choices along the design process [40]. Already available tools addressing other design levels, such as the ones mentioned in Section 1.6, can use the results produced by TACT in order to complete the design cycle as in [41].

TACT proposes an interference oriented approach when evaluating the performance of each possible frequency in order to find the most suitable frequency plan. This evaluation takes into account both signals belonging to the standards as well as out-of-band interferers. As far as the budget design is concerned, TACT finds a multi-standard receiver budget that meets or exceeds the specs of the addressed

\(^2\)For the time being, only the receiver side is implemented in TACT.
wireless standards while keeping the requirements of each of the receiver blocks as relaxed as possible.

The main differentiators of TACT in comparison with previously published work are that it performs an automatic search of the design-space comprising the system level specifications of RF receivers (as opposed to tools addressing lower abstraction levels) and the fact that it addresses the multi-standard case (as opposed to tools addressing single standard). To the best of the author's knowledge, no similar work has been published so far.

1.8 Organization of this Thesis

This thesis is organized as follows: Chapter 2 goes through some communication systems basics, Chapter 3 describes more thoroughly the communications receiver design considerations focusing on the blocks located between the antenna and the analog-to-digital converter, Chapter 4 introduces TACT, its components and simulation flow, Chapter 5 discusses frequency planning issues and the approach implemented in TACT's Frequency Planning Tool, Chapter 6 describes the budget design methodology proposed for and implemented in TACT, Chapter 7 shows a case study for a WCDMA/WLAN receiver design carried out using TACT in order to show the usefulness of the tool and, finally, Chapter 8 draws some conclusions based on the previous chapters, and describes briefly the future work.
Chapter 2

Communication Systems Basics

“Speech is civilization itself. The word, even the most contradictory word, preserves contact - it is silence which isolates”

Thomas Mann

As many philosophers have pointed out, “Man is by nature a social animal”\(^1\) [42-44]. Communication seems to be a basic need, not only for human beings, but also for most living organisms [45]. Communication can happen in the form of exchange of words, both written and spoken, body language, signs, smoke, sounds, smells, etc. [45]. Information can be coded (ex., Morse code) or encrypted (ex., using different languages).

In order for communication to actually take place both the transmitter and the receiver have to be able to interpret the signals (“speak the same language”), the signal level has to be adequate and the communications scenario has to be such that disturbances coming from the channel do not prevent the message detection at the receiving side.

The objective of a communications system is to transmit information between a transmitter and a receiver. Information loss might be an issue as Figure 2.1 highlights. The physical channel that lies between the transmitter (Tx) and the receiver (Rx) and that is used as a physical support for the information transmission is unfortunately not ideal. Depending on the nature of the physical channel, the waveform carrying the information can be affected by a number of different non-idealities: attenuation, fading, non constant group delay, non-linear distortion, multi-path fading, etc. [46-48]. In the case of the wireless environment this is aggravated since the spectrum is shared among different communication systems. This causes interferences. The non-idealities of the transmission channel are not the only problem. The Tx and Rx themselves are not ideal either. Each of their components add noise, distortion, etc.

A lot of innovations have allowed humankind to go from sending short distance messages using a tam-tam to making a video call over a mobile phone to another

\(^1\) Woman too.
continent. This keeps us connected and... that is why we are in this business, isn’t it?

2.1 Analog vs. Digital Communication Systems

In the race for providing high performance services to the subscribers digital systems have been ahead of analog systems for several years [47]. Digital systems perform better than analog systems for wireless communications purposes.

Wireless communications require larger and larger system capacity due to their increasing number of subscribers and the evolution towards applications that require larger data transfers. Digital communications allow for Time Division Multiple Access (TDMA) and Code Division Multiple Access (CDMA) besides Frequency Division Multiple Access (FDMA), which is the only multiple access technique supported by analog systems. This, together with their superior spectrum utilization efficiency, gives them a competitive advantage when it comes to increasing the system capacity. Another advantage of digital systems is that error detection/correction techniques can be applied to digital communications. Their high flexibility when it comes to implement new services that generate additional revenues for the operators without requiring big investments and the ease of implementation of security mechanisms on digital platforms contribute to making them the leading technology.

We live in an analog world, though. Therefore, analog-to-digital (A/D) and digital-to-analog (D/A) conversion processes are necessary if digital communication is chosen. Where and how this conversion is carried out determines the specs of the different components of the system.
2.2 Baseband vs. Modulated Communications

Normally, the information source generates the information at baseband, that is, in the band that goes from DC to the maximum frequency occupied by the signal. Although baseband communication is used in some systems, such as fixed telephone lines, it is not practical in most communication systems. Particularly, that is the case of wireless communications where the physical channel is shared by a multitude of actors. Applying a modulation technique to the signal band allows to send several signals over the same channel.

2.3 Multiple Access Techniques

The basic strategies, shown in Figure 2.2 that allow several users to share a fixed spectrum resource are [48, 50]:

- Frequency-Division Multiple Access (FDMA)
  In FDMA users are assigned different frequency bands in the available spectrum leaving guard bands between adjacent channels in order to minimize crosstalk. Once all the frequencies have been assigned, it is not possible to add more users to the system until one or more of the frequencies are liberated. This is the only possibility for analog systems.

- Time-Division Multiple Access (TDMA)
  In TDMA users are assigned different time slots for the same transmission frequency. Once all the time slots have been assigned to different subscribers it is not possible to add more users to the system until one or more time slots are liberated. It requires digital transmission. In practice, it is nearly always combined with FDMA.
• Code-Division Multiple Access (CDMA)
CDMA is a Spread Spectrum (SS) system where users are separated by codes. The number of CDMA users that can be active at the same time sharing the same spectrum depends on the interference level the system can tolerate. Since the system can admit some interference level users can be added as long as the maximum tolerated interference is reached. It requires digital transmission. It may be combined with FDMA with few carriers.

2.4 Spread Spectrum Systems

In spread spectrum systems, the signal is transmitted on a bandwidth considerably larger than the information bandwidth [48, 50]. The different types of spread spectrum (SS) systems that can be used are:

• Frequency-Hopping Spread Spectrum (FHSS)
In FHSS a code sequence determines the discrete increments by which the carrier frequency is shifted and when this shift happens. The time in which the carrier frequency is kept constant is called time chip $T_c$.
In fast-hop systems the frequency hopping rate is larger than the message bit rate. In slow-hop systems the carrier hopping rate is smaller than the message bit rate.
The spreading codes can be chosen so as to avoid interference to or from other systems.
FHSS system are subject to occasional bursty errors due to fading or single-frequency interference (which is time and frequency dependent).

• Time-Hopped Spread Spectrum (THSS)
In THSS the transmission time is divided into time frames and each frame is divided into time slots. During each frame the message modulates one and only one time slot. The modulated time slot can be different for different frames.

• Direct Sequence Spread Spectrum (DSSS)
In DSSS systems the whole wideband transmission channel is made available to all users at the same time. Users are separated by a code that is used to spread and de-spread the data. The DSSS technique spreads the information in both the time and the frequency domains minimizing, thus, the effects of fading and interference.
The errors present in a DSSS system are continuous and low level random errors. Single errors are randomly distributed over time whereas in FHSS systems the errors are distributed in clusters.
2.4. *Spread Spectrum Systems*

All spread spectrum systems have in common their relatively high interference rejection. The degree of interference rejection is measured through the system processing gain $PG$

$$PG = \frac{B_w}{R}$$  \hspace{1cm} (2.1)

where $B_w$ is the RF bandwidth and $R$ is the information rate.
Chapter 3

Communications Receiver Design in a Nutshell

In a wireless communications system, information is coded, compressed, sometimes encrypted, modulated and sent over the air interface between the transmitter and the receiver. The goal of a communications receiver is to retrieve the information contained in a given channel. This is a very challenging task. The wireless environment is very hostile. At the input of the receiver the desired channel might be a very weak signal surrounded by high power interferers.

The key figures of merit that fix the specifications of a receiver are the sensitivity and the selectivity. The sensitivity refers to the minimum detectable signal in the presence of noise (thermal noise generated at the RF front-end constitutes its main component). It can be quantified as the noise figure of the receiver needed to achieve a certain bit error rate (BER). The selectivity measures the ability to select a weak desired signal channel in the presence of much stronger adjacent interferers (blockers). It depends not only on the filtering characteristics, but also on the linearity and dynamic range of the receiver blocks and the phase noise of the local oscillator(s). When this selection is done at baseband the dynamic range and linearity of the ADC will have a strong effect on the receiver selectivity.

Many factors affect the sensitivity and selectivity of a receiver (such as receiver architecture, analog-digital partitioning, noise figure, phase noise, linearity, etc.). The following sections will discuss these issues and will walk us through the procedure to follow in order to find the specs the receiver has to meet in order to be compliant with a certain standard. They comprise receiver noise figure, local oscillator phase noise, non-linearities and selectivity requirements. The parameters needed to compute them can be obtained in most cases from the radio specs of the standard. Some of them may not be specified for certain standards. Commonly used values for them are usually easy to find from commercial products.
CHAPTER 3. COMMUNICATIONS RECEIVER DESIGN IN A NUTSHELL

3.1 Multi-standard Receiver Design Considerations

The general considerations to follow when designing a multi-standard receiver could be summarized as follows:

1. Choose the target standards.

2. Obtain the standard specifications from the corresponding standardization body (IEEE, ETSI, etc.).

3. Develop a detailed list of requirements the receiver should meet based on the specs. Some of them have to be worked out based on the information given in the standard, others are given directly. These specifications include parameters such as LO’s phase noise limits, required noise figure, second and third order intermodulation, filtering characteristics, etc. The following section give detailed information on how to map the standard specs into receiver specs.

4. Compare the obtained receiver specs with common practice and update the specs if needed (you may not want to lag behind your competitors).

5. Choose the receiver architecture. For the multi-standard case, the receiver architecture should be as similar as possible for all the targeted standards in order to maximize the hardware sharing.

6. Develop a careful frequency plan that minimizes the effect of interferences along the receiver chain.

7. Design the receiver budget itself. This means distributing the gain, noise figure and intermodulation product levels among the receiver blocks. It may require considerable time to work out all the numbers so that the specs for each of the blocks can be achieved in a given process technology and the overall receiver meets the specs and is compliant with the test procedures specified in the standard. When targeting multi-standard receivers this gets more complicated.

8. Follow the signal levels through the blocks up to the ADC. All the signals related to the standard should be considered: the maximum and minimum input signals, the blockers and the input thermal noise. This allows the calculation of the required dynamic range of the A/D converter, and therefore the necessary number of bits.

Usually several iterations between the last three steps are necessary in order to reach a fair distribution of the requirements. Both the multi-standard and the single standard cases should studied at the architectural and the block level. Basically, what has to be done once the specs are set is:
3.2. RECEIVER ARCHITECTURES

for all combinations of multi-standard and single-standard
for all possible receiver architectures
  * find the frequency plan with less interferers
  * find a Rx budget that meets specs
    with block requirements as relaxed as possible
end;
end;

Overwhelming, isn't it? Each individual task is certainly easy to perform on its own, as we will see in the next sections. It is the number of times these operations have to be carried out, the endless possibilities of parameter distributions and the correlation between these parameters that makes this problem not only difficult but also complex.

Some degree of automation would certainly be appreciated by the RF systems engineer. The rest of this chapter will focus on general considerations related to receiver design. The remaining chapters will address these issues from the standpoint of our proposed automated solution implemented in TACT.

3.2 Receiver Architectures

This section gives a brief overview of the most widely used receiver architecture and compares them in terms of their suitability for multi-standard applications [46,50].

Superheterodyne Receiver The traditionally most widely used architecture in RF applications is the superheterodyne receiver shown in Figure 3.1. This receiver is able to select with high reliability high frequency narrow band signals from an environment full of interferers. Since the channel selection is carried out at IF the dynamic range requirements are relaxed at baseband. This simplifies the design of the ADC. However, this receiver is not particularly suited for multi-standard integration. When high Q filtering is required by a standard, the image rejection (IR) filter and/or the channel selection IF filter have to be implemented off-chip. Different image rejection and channel selection filters have to be used for different standards, making it impossible to achieve a highly integrated low cost solution.

Zero IF Receiver A superheterodyne receiver with its IF set to zero is called zero IF, direct conversion or homodyne receiver. This type of receiver architecture is shown in Figure 3.2. The advantage of down-converting the signal to baseband without passing through an intermediate frequency is the avoidance of image problems. This architecture is more suitable for integration than the standard superheterodyne receiver because no image rejection filter is needed\(^1\) and low pass filters are more suitable for integration with lower power consumption than IF filters.

\(^1\)Remember that this filter had to be implemented off-chip in most cases.
Zero IF receivers have another major advantage over superheterodyne receivers: they can be used for multiple standards only by making programmable the LO frequency and the baseband chain (low-pass filter, variable gain amplifier and A/D converter).

One of the main problems these receivers present is the appearance of DC offset, both static and dynamic, at the mixer output. Due to leakage, the same signal, with different power levels, might appear at the two inputs of the mixer. Self-mixing of the local oscillator (LO) signal and/or out-of-band blockers with large power levels are the most detrimental scenarios. The leaked signal can appear at different points of the chain (mixer input, LNA input, etc.) and even be re-radiated and re-received leading to different power levels. These effects are discussed in Section 5.1 and illustrated in Figure 5.1.

Even-order distortion can cause additional DC offset problems, which together with the flicker noise degrade the dynamic range of the whole receiver chain.

**Low IF Receiver** A low IF receiver has a block diagram similar to the Zero-IF one shown in Figure 3.2. Low IF receivers perform frequency downconversion of the signal to frequencies close to, but larger than zero, solving most of the DC offset and flicker noise problems of the zero IF receivers. This does not come for free. The image problem is back and this time with the additional difficulty of filtering it out at a rather low frequency. This makes mandatory dealing with the image rejection problem on the mixer and even so the rejection ratio is lower than what is required by most standards. This tightens the requirements for the band-pass ADC\(^2\) whose order and bandwidth should be increased with the higher power consumption this involves.

**Wideband IF Double-Conversion Receiver** A wideband IF double-conversion architecture is basically a dual down-conversion heterodyne receiver. It performs a down conversion using two IFs as it is shown in Figure 3.3. All the channels

\(^2\) or the band-pass filter plus low-pass ADC.
are down-converted to the first IF using LO1, which is fixed. The programmable conversion to baseband is performed using LO2.

This architecture has a high degree of integrability and programmability. Since the first downconversion is done at IF the re-radiation and self-mixing problems the zero IF receiver presents are overcome. Hence, the DC offset problems are reduced, which relaxes the requirements of the ADC. The second LO is programmable, which makes this architecture suitable for multi-standard applications.

Table 3.1 shows a comparison of the receiver architectures described above in terms of integration and multi-standard capabilities.
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Table 3.1: Comparison of the integration and multi-standard capabilities of the discussed receiver architectures

<table>
<thead>
<tr>
<th>Receiver Architecture</th>
<th>Integration Capabilities</th>
<th>Multi-Standard Capabilities</th>
<th>ADC Design</th>
</tr>
</thead>
<tbody>
<tr>
<td>Superhet</td>
<td>Low</td>
<td>Medium</td>
<td>Simple</td>
</tr>
<tr>
<td>Homodyne</td>
<td>High</td>
<td>High</td>
<td>Challenging</td>
</tr>
<tr>
<td>Low IF</td>
<td>High</td>
<td>Medium</td>
<td>Challenging</td>
</tr>
<tr>
<td>Wideband IF</td>
<td>High</td>
<td>High</td>
<td>Simple</td>
</tr>
</tbody>
</table>

3.3 Noise Figure

The noise figure of a system measures how much the signal to noise ratio (SNR) degrades when a signal passes through it [46, 50]. The noise factor \( n_f \) of a system is given by

\[
n_f = \frac{SNR_{in}}{SNR_{out}}
\]  

(3.1)

And the noise figure \( NF \) is the expression of the noise factor in dBs, that is:

\[
NF = 10 \log n_f
\]  

(3.2)

The noise factor can also be expressed as:

\[
n_f = \frac{P_{in}/P_{RS}}{SNR_{out}}
\]  

(3.3)

Where \( P_{in} \) is the input signal power and \( P_{RS} \) the source resistance noise power. Therefore,

\[
P_{in} = P_{RS} \cdot n_f \cdot SNR_{out}
\]  

(3.4)

which integrated over the signal bandwidth gives the total mean square power of:

\[
P_{in,tot} = P_{RS} \cdot n_f \cdot SNR_{out} \cdot B
\]  

(3.5)

for a flat channel where \( B \) is the channel bandwidth. Expressing this equation in decibel units we obtain:

\[
P_{in,tot|dBm} = P_{RS|dBm/Hz} + NF|dB + SNR_{out|dB} + 10 \log B
\]  

(3.6)

The source resistance noise power \( P_{RS} \) for a matched input at room temperature is given by:

\( ^{3} \) In this chapter the noise factor of a system is abbreviated as \( n_f \) instead of \( f \) (the most extended notation) in order to avoid confusion with frequency, which is referred to as \( f \).
\[ P_{RS} = \frac{4kT R_s}{1} \frac{1}{R_{in}} |_{R_s = R_{in}} = kT |_{T = 290K} = -174 dBm/Hz \] \hspace{1cm} (3.7)

where \( k = 1.3810^{-23} \) is the Boltzmann’s constant.

Hence, Equation 3.6 can predict the system sensitivity \( P_{in, min} \), that is, the minimum signal level that the system can detect with acceptable SNR, as:

\[ P_{in, min}|_{dBm} = -174dBm/Hz + NF|_{dB} + 10 \log B + SNR_{min}|_{dB} \] \hspace{1cm} (3.8)

where the sum of the first three terms is the total integrated noise or noise floor of the system. It immediately follows from this equation that:

\[ NF|_{dB} = P_{in, min}|_{dBm} - SNR_{min}|_{dB} + 174 dBm/Hz - 10 \log B \] \hspace{1cm} (3.9)

Hence, the maximum noise figure a receiver chain is allowed to have can be calculated using the receiver sensitivity, the signal bandwidth and the minimum required signal to noise ratio at the output.

### 3.4 Noise Figure of Cascaded Stages

The overall noise factor for the cascaded receiver blocks can be calculated using Friis equation:

\[ nf = 1 + (nf_1 - 1) + \frac{nf_2 - 1}{A_1} + \cdots + \frac{nf_m - 1}{A_1 \cdots A_{(m-1)}} \] \hspace{1cm} (3.10)

where \( nf_i \) is the noise factor and \( A_i \) is the power gain of the i-th block. The noise figure is the equivalent in dB of the noise factor, \( NF = 10 \log(nf) \).

This equation is only valid for cascaded components where no frequency translation is performed [46]. When frequency translation is carried out, as is the case in most receivers, the contribution of the image noise band should be considered too. The characteristics of most receiver blocks in this image noise band is very difficult to predict at this early stage of the design, tough.

As Equation 3.10 clearly shows, the overall noise figure will be determined by the first stages of the cascaded receiver. Hence, front end blocks with small NF and high gain are crucial for a receiver meeting the NF specs.

It should be noted as well that lossy blocks will amplify the noise contribution of the stages following them.

### 3.5 Non-linearities

Non-linearities of the analog/RF components may produce intermodulation products and/or harmonics of their input signals. These unwanted signals appear at
Figure 3.4: Third order intermodulation in a non-linear system 3.4(a). Two adjacent channels whose third order intermodulation product falls in the desired signal band 3.4(b). Two blockers whose third order intermodulation product falls within the desired signal band 3.4(c).

the output of the receiver blocks along with the input signals. The intermodulation (IM) products fall at frequencies $f_{n,m}$ defined as:

$$f_{n,m} = \pm n \cdot f_1 \pm m \cdot f_2$$  \hspace{1cm} (3.11)

where $n$ and $m$ are integer numbers and $f_1$ and $f_2$ are the input frequencies. The order of the intermodulation product is $n + m$. In case of harmonic distortion Equation 3.11 is used with $m = 0$.

In a communications receiver, most of these IM products have very low power and/or are filtered out along the receiver chain. Nevertheless, some intermodulation products may fall close or within the desired signal frequency band and may have a power level large enough to significantly distort it.

Take for instance the third order intermodulation products depicted in Figure 3.4(a). Signals at frequencies $f_1$ and $f_2$ will produce third order intermodulation products at $2f_1 - f_2$ and $2f_2 - f_1$ when going through a non-linear system. Imagine now the situation shown in Figure 3.4(b). The desired channel and two adjacent channels are present at the input of an RF component of the receiver chain. This is quite common since the channel selection is usually done at some intermediate frequency or at baseband. One of the third order intermodulation products originated by these adjacent channels will fall right on top of the desired channel producing a disturbance in the system. A similar effect will occur for any combination of blocker frequencies $f_{b1}$ and $f_{b2}$ such that

$$|f_{b1} - f_{b2}| = |f_{b1,b2} - f_{inband}|$$  \hspace{1cm} (3.12)

Any such pair of blockers will produce a third order intermodulation product that will fall within the desired channel bandwidth at a frequency $f_{inband}$. This effect is illustrated in Figure 3.4(c).
Both the linearity of each block and the gain and filtering characteristics of the receiver chain will have an impact on the overall linearity of a receiver.

A means of comparing the linearity of different circuits is provided by the $k^{th}$ order intercept point (IPk). This point is located where the output level of the fundamental and the $k^{th}$ order IM product meet. The input power level corresponding to this point is the $k^{th}$ order input intercept point (IIPk). The output power level corresponding to this point is the $k^{th}$ order output intercept point (OIPk).

The power of the intermodulation products grows at a higher pace than the power of the signals that originate them as shown in Figure 3.5 when the devices work in weakly non-linear regions [9]. This plot highlights also the fact that after a certain power level, the system starts saturating. This means that a linear increase in the input power level does not produce a linear increase in the output power level after a certain point. The 1-dB compression point, located where the actual curve is 1 dB away from the ideal one, is a measure of the saturation behaviour of a component or system. The IPk is, therefore, a mathematical construction more than a physical point that can be measured. It is calculated as the intersection point of the linear extrapolation of the fundamental and the $k^{th}$ intermodulation product lines. It is, nevertheless, a very useful construction. Since it is independent of the power of the input signals, it can be used to compare the linearity of different circuits as was mentioned before.

The power of an intermodulation product is inversely proportional to its order for the region where the system is weakly non-linear [9]. Since the receiver will normally work in this region we will limit our discussion to second and third order.
Second Order Non-Linearity

where $P_{in}^m$ is the receiver sensitivity and $M$ is taken into consideration.

\[ IM_{2dBm} = P_{in}^{m} - SNR_{min} - M dB \]

\[ \Delta P_{in} = P_{in}^{m} + \Delta P \]

The second order IM products $\Delta f$ or $f + f$ can become an issue in LNA-IF and especially in zero-IF receivers since they fall in the low frequency band. In these types of receivers, the second order IM products can be more limiting than the third order ones.

The input second order intercept point (IIP2) can be calculated as \([46, 50]\):

\[ IIP2_{dBm} = P_{in}^{m} + \Delta P_{2dB} \]

Third Order Non-Linearity

where $P_{in}^{m}$ is the receiver sensitivity and $M$ is taken into consideration. These formulas can be used to calculate the minimum requirement of communications receiver should meet in terms of third order non-linearity.

The input third order intercept point (IIP3) can be calculated as \([46, 50]\):

\[ IIP3_{dBm} = P_{in}^{m} + \Delta P_{3dB} \]

\[ \Delta P_{in} = P_{in}^{m} + \Delta P \]

3. COMMUNICATIONS RECEIVER DESIGN IN A NUTSHELL

Higher order non-linearities could have a significant impact on the system in certain situations though they will be taken into account. It should be noted that the relative significance of odd and even intermodulation products depends on the chosen architecture. For instance, even order non-linearities are very detrimental in heterodyne-like receivers whereas they do not have such a strong impact in heterodyne-like receivers.
3.6 Non-linearity of Cascaded Stages

As far as linearity is concerned, the third order intercept point at a given frequency is equal to:

\[
\frac{1}{IP_{3}^{2}} = \frac{1}{IP_{3,1}^{2}} + \frac{A_1}{IP_{3,2}^{2}} + \cdots + \frac{A_1 \cdots A_{n-1}}{IP_{3,n}^{2}}
\]  

(3.19)

where \( IP_{3,i} \) is the third order intercept point and \( A_i \) is the gain of the \( i \)-th block at that frequency. The second order intercept point has an equivalent equation.

3.7 Local Oscillator Phase Noise

The phase noise of an oscillator at an offset frequency \( \Delta f \) of the carrier \( \mathcal{L}(\Delta f) \) is given according to Leeson's model by:

\[
\mathcal{L}(\Delta f)(dBc/Hz) = P_s(dBm) - P_b(\Delta f)(dBm) - 10 \log B - SIR(dB) \tag{3.20}
\]

where \( P_s \) denotes the input signal power, \( P_b(\Delta f) \) the blocker power at an offset frequency \( \Delta f \), and \( SIR \) the signal to interferer ratio. Depending on the standard, the blocker power at a certain offset frequency from the carrier \( P_b(\Delta f) \) may be given by the blocking characteristics or by the adjacent channel characteristics. The one setting more stringent characteristics on the LO’s phase noise performance should be taken.

The mechanisms originating phase noise are very complex and not fully understood [51]. Using Leeson’s model for setting the local oscillator phase noise is an oversimplification, but it is a good starting point when setting the specs.

Phase noise affects both the sensitivity and the selectivity of the receiver. The sensitivity is affected since the in-band phase noise modifies the desired signal’s SNR. The selectivity is affected because of the additive broadband noise coming from the mixing of the LO with interferes that falls in-band.

3.8 ADC’s Dynamic Range and Effective Number of Bits

The effective number of bits of the ADC is related with the dynamic range (DR) of its input, where the \( DR_{ADC} \) is [52, 53]:

\[
DR_{ADC} = P_{max} - P_{noise} + M \tag{3.21}
\]

where \( P_{max} \) is the maximum signal power present at the ADC input, \( P_{noise} \) is the input noise floor, and \( M \) a margin set by the user. It should be stressed that in this equation \( P_{max} \) does not correspond to the maximum power input signal coming from the standard, but to the signal with maximum power present at the ADC input. Noise, distortion components and/or blockers will be added to the desired signal affecting the power level present at each point of the receiver chain.
It should be, therefore, highlighted that both the gain distribution and the filtering characteristics of the receiver chain play an important role in determining the dynamic range of the ADC.

The effective number of bits of the ADC $ENOB_{ADC}$ can be calculated as [52, 53]:

$$ENOB_{ADC} = \frac{DR_{ADC} - 1.76}{6.02} \quad (3.22)$$

### 3.9 Sensitivity and Gain Levels

The gain budget is done both for the sensitivity value (maximum gain option) and the maximum input power signal (minimum gain option). The automatic gain control (AGC) tuning range is determined by the difference between the minimum and the maximum gain levels.

AGC is introduced in receivers in order to be able to adjust the total gain of the chain. The maximum gain option will be used when receiving signals close to the sensitivity level. The minimum gain option will be used when receiving signals of large power. The control mechanism introduced by the AGC allows to address the far-near problem leading to an overall power save and avoidance of undesired effects such as desensitization [50].

The gain distribution should be done bearing in mind:

- The signal levels of the standards (maximum, minimum, noise floor, blockers, etc.).
- Reasonable gain/loss levels for all the blocks (with some margin for circuit non-idealities).
- The gain range for the programmable gain stages (LNA, VGA) so that the dynamic range requirements for the ADC are as relaxed as possible for the chosen analog-digital partitioning.
- The impact of the gain in the aggregate NF, II^3P and II^2P.

The aggregate gain for the maximum and minimum gain options is given by the addition of the individual gains in dB.

### 3.10 Selectivity Requirements

The selectivity requirements are determined by the analog-digital partitioning and the blocking and the adjacent channel selection characteristics given by the standard. Depending on the filter type (Butterworth, Elliptic, etc.) they may translate into different filter orders. The filter type choice should be done according to its pass-band ripple, stop-band attenuation and transition band so that not only the desired attenuation levels are reached but also the group delay, ripple, etc are acceptable in all bands. The channel selection may be performed entirely in the analog
3.11 TRADE-OFFS

Figure 3.6: Different orderings of the amplification, filtering and A/D conversion operations.

domain thus relaxing the requirements of the ADC. When part or all of the filtering is moved to the digital domain the ADC specs become tougher. The amount of operations performed in the digital domain defines the analog-digital partitioning of the system. This partitioning has a strong impact on the system performance and requirements of the individual blocks.

The order in which amplification, filtering and A/D conversion are performed determines how the distribution of the burden is carried out [30]. The possible configurations are shown in Figure 3.6. In the configuration shown on top, the linearity requirements of the amplifier are relaxed thanks to the placement of the filter before it. This makes the noise performance of the filter critical, though. Since both filtering and amplification are performed before the analog-to-digital conversion the requirements of the ADC are moderate. Swapping the position of the amplifier and the filter as shown in the configuration located in the middle, relaxes the noise performance requirements of the filter, while asking high linearity to the amplifier and keeping the requirements of the ADC moderate. In the configuration located at the bottom, the filtering is carried out in the digital domain, which is very demanding on the amplifier’s linearity and the ADC.

3.11 Trade-offs

It can be seen by inspection of Equations 3.10 and 3.19 that qualitatively, linearity and noise performance impose opposed conditions to the gain distribution. In terms of noise figure a high front-end gain is desirable whereas in terms of linearity a low
front-end gain is desirable. A fairly small front-end gain makes intuitive sense when thinking of all the blockers entering the receiver front-end together with the desired signal. Having a high front-end gain before any filtering of these undesired signals might be very detrimental for the performance of the system if the RF front-end components are not extremely linear and have a high dynamic range.

The order in which amplification, filtering and A/D conversion are performed has an enormous impact on both the specs of the individual blocks and the overall receiver performance. This is intimately related with the way in which the analog-digital partitioning is performed. The amount of operations carried out in the analog and the digital domain will have a strong impact in the block specs and the overall power consumption.

The pass and stop bands of the filters as well as their type and order have a strong impact in both the receiver performance, its area, and power consumption. From the performance standpoint very selective filters are desirable, but they require large areas and normally consume more power. The choice of intermediate frequencies also has a strong impact in the filter requirements as well as in the behaviour of the receiver in the presence of interferers.

These are just few considerations to bear in mind when exploring the design-space of wireless communications receivers. The following chapter will describe how to approach them not only qualitatively, but also quantitatively.
Chapter 4

TACT and its underlying methodology

TACT, a multi-standard RF Transceiver Architecture Comparison Tool [38], is an open, user friendly MATLAB based tool. It combines the top-down and bottom-up approaches to the problem filling the gap of a middle ground where system level transceiver specifications and actual electronic circuit implementation issues meet.

The inputs to the tool are the wireless communication standards to design for, the transceiver architectures, and the block implementations to consider. The performance metrics of the tool are based on a set of cost functions, namely area, power consumption, noise figure, local oscillator’s phase noise, linearity, dynamic range and availability of already designed RFIC and mixed signal IP’s, which may have a strong impact on the overall cost (NRE) of the solution. TACT evaluates these cost functions and provides the user with the performance of each solution. This permits to identify the advantages and disadvantages of different solutions at a very early stage allowing optimization of the design at the system level. The user steers the search through the allowable values of the cost functions and the ranges of the block parameters.

For the moment only the receiving side of the transceiver is dealt with in the tool since it poses a harder challenge than the transmitting side as was mentioned in Chapter 1. Nevertheless, the generic methodology underlying TACT applies to both Tx and Rx.

Conceptually, TACT consists of four interacting components: (1) a standard radio specifications to transceiver specifications mapping tool, (2) a pool of transceiver architecture models, (3) a pool of transceiver block models, and (4) a comparison tool. Figure 4.1 shows how they relate to each other. The following sections describe these components and the way the user can interact with them.
4.1 The standard to transceiver specifications mapping tool

The standard to transceiver specifications mapping tool takes the RF specifications of different standards (intermodulation characteristics, transmission mask, adjacent channel selection, blocking characteristics, etc.) and converts them into transceiver specifications (required noise figure, IIIP3, etc.). It does so by using MATLAB basically as a calculator. It is a “static” component of TACT. As Figure 4.1 shows, the resulting transceiver specifications are fed into the comparison tool.

A library of standards is provided with the tool. The user can specify new standards and make them part of TACT. The user can interact with the mapping tool by choosing the standard(s) to address. Moreover, he can also vary the margins that are provided by default in order to extract the RF specifications.

For instance, the default set of receiver specifications given for WCDMA (TDD) is $\text{NF} = 9 \text{ dB}$, $\text{PN}(\@ 5 \text{ MHz}) = -120 \text{ dBc/Hz}$, $\text{PN}(\@ 10 \text{ MHz}) = -127 \text{ dBc/Hz}$, $\text{PN}(\@ 15 \text{ MHz}) = -139 \text{ dBc/Hz}$, $\text{Att}(\@ 5\text{MHz}) = 33 \text{ dB}$, $\text{Att}(\@ 10\text{MHz}) = 61 \text{ dB}$, $\text{Att}(\@ 15\text{MHz}) = 73 \text{ dB}$, $\text{Att}(\@ 20\text{MHz}) = 71 \text{ dB}$, IIIP3 = -17 dBm and IIIP2 = 14 dBm.
4.2 Pool of transceiver architecture models

The pool of transceiver architectures contains different possible architectures where the blocks are generic. As Figure 4.2 illustrates, any transceiver architecture can be conceptually expressed as a series of the following sections:

- Sections providing either amplification, filtering or both. They are referred to as AF sections in TACT. These sections may work at radio frequencies (RF sections), intermediate frequencies (IF sections) or at baseband (BB sections). These generic blocks represent the combination of real amplifiers and filters.

- Mixer sections that allow for frequency translation. They represent real mixers.

- Frequency generators that provide the mixer with the signals needed to perform the frequency conversion. They represent the local oscillator, that might comprise voltage controlled oscillators (VCOs), phase locked loops (PLLs) and/or frequency dividers.

- Analog-to-digital and digital-to-analog converters (ADCs/DACs).

The way in which these sections are combined determines the transceiver architecture. For instance, the model of a zero-IF receiver consists of an RF section followed by a mixer with its corresponding frequency generator, a BB section and an ADC. TACT currently provides models for zero-IF, low-IF and heterodyne receivers. The position of the data converter determines the analog-digital partitioning. Different options for the analog-digital partitioning in these architecture will be explored by the comparison tool. The ordering of amplification and filtering, as well as the number of amplifiers and filters per section, can be set by the user.

Besides being able to select the architectures to consider in the simulation, the user can combine the transceiver sections in a custom way.

4.3 Pool of transceiver block models

The transceiver blocks are modeled at different abstraction levels. This allows the comparison tool to choose whatever level of the model to use depending on
Figure 4.3: TACT simulation flow.

The high-level models abstract the behaviour of the blocks through a set of parameters, namely their gain (G), noise figure (NF), non-linear behaviour (IIP3, IIP2), dynamic range (DR), center frequency ($f_c$), bandwidth (BW), input and...
output impedance ($Z_{in}, Z_{out}$), group delay ($\tau_g$), area (A), power consumption (P), implementation cost (C), multi-standard capability (M) and integrability (I).\(^1\)

These parameters may represent:

- an absolute or a relative value. For instance, the gain is an absolute value whereas we treat the implementation cost as a relative parameter: the cost of an already available IP block is many times lower than the cost of a block that has to be designed from scratch.

- an allowable range of values or an assigned value. The allowable range of values of a parameter is used in the design flow in order to determine whether the desired value for this parameter can be assigned.

Medium-level models use MATLAB/Simulink blocks to model both the ideal behaviour and the non-idealities that come from the actual circuit design and the particular implementation of the block. For instance, the same filter can be implemented using different architectures (Gm-C, active RC, etc.) that lead to disparity in power consumptions, dynamic range, linearity, etc. At this level these differences are modeled.

Low-level models can only be used in already available IP blocks. They characterize the blocks using data coming either from the transistor level simulations or from measurements. Therefore, they model the behaviour of the block much more accurately than higher level models, still without having to run expensive transistor level simulations within TACT. They are used in the last stages of the simulation flow since they belong more to the analysis and verification part of the tool rather than to the architectural level design.

A TACT user can specify nearly everything regarding the block models: the allowable range of values, the non-idealities to be considered, the different block implementations to be taken into account, etc.

4.4 The comparison tool

The comparison tool is the heart of the simulator. It takes the transceiver specifications of the different standards coming from the mapping tool. Then, it runs through the different architectures and block implementations available evaluating the cost functions mentioned above. Finally, it provides the user with the performance of each solution. Thus, the advantages and disadvantages of each approach are determined and compared so that the user can find the best solution that meets the design specification and requirements at hand. This is a “dynamic” tool that uses a simulated annealing-based optimization algorithm.

The comparison tool considers the multi-standard as well as the single standard cases at both the architectural and the block level. Although current trends call

\(^1\)For the time being the parameters that are already included in the high level models are G, NF, IP3, IP2, $Z_{in}$, and $Z_{out}$.
for implementation of different standards into one common radio architecture [54]
using programmable blocks, this may not be feasible and may come at the expense
of a degraded overall performance of the transceiver chain. As a consequence, it
might be better to duplicate a block, rather than using a programmable common
block, or even two separate signal paths.

There are three different components within the comparison tool: the transceiver
design and partitioning tool, the integration assessment tool and the component
tool. Figure 4.3 shows TACT’s simulation flow where the interactions between
these three tools are illustrated. They are described in the following sections.

The transceiver design and partitioning tool

The two main operations carried out by this tool are the frequency planning and
the budget design of the receiver, including the analog-digital partitioning. These
operations are performed not only taking into account the characteristics of the
standard(s), but also the user preferences as illustrated in Figure 4.4.

The transceiver design and partitioning tool takes as input:

- the standard(s) specifications provided by the mapping tool
- the set of transceiver architectures to be considered
- the high-level models of the transceiver blocks

It evaluates the performance of different frequency plans using an interference
oriented approach as explained in Chapter 5. Afterwards, it provides as output a set
of candidate transceiver budgets meeting the specifications with their performance
for a given frequency plan chosen by the user. At this stage of the flow, the cost
functions that are evaluated are the overall noise figure, IP2, IP3, and number of
bits of the ADC. The budget is iterated in order to optimize these cost functions
as discussed in Chapter 6.

The performance parameters are distributed along the blocks according to a
criteria based on the allowable range of each parameter, their impact in the overall
performance and the aimed value for the cost functions. The allowable parameter
range is dictated by the block models and can be modified by the user.

As was mentioned in Section 3.10, the order in which the amplifying and filtering
operations occur has a big impact in the performance that is required from these
blocks [50]. In each of the different AF sections\(^2\) the cases where amplification
occurs prior to filtering, filtering prior to amplification and all the combinations
thereof where these two operations are distributed in several cascaded stages are
evaluated according to the user preferences.

In the last AF section, the analog-digital system partitioning is introduced. The
position of the ADC determines the boundary between the analog and the digital
processing of the signals. The filtering might be done fully in the analog domain,

\(^2\)Transceiver sections providing amplification and filtering (see Section 4.2)
fully in the digital domain or distributed between the analog and the digital sections. This has an enormous impact in the requirements of the A/D converter and in the power consumption of the overall system [6]. The analog-digital partitioning is done at different points in the system depending on the weight assigned by the user to the cost functions.

**The Integration Assessment tool**

This tool assesses the multi-standard and radio-on-chip (RoC) integration capabilities of the different solutions. It justifies the need of such capabilities in comparison with and in contrast to stacked radio solutions and solutions that often require off-chip components or may be packaged in a multi-chip module.

The multi-standard capabilities of a solution are evaluated using as measure the impact in the cost functions of hardware reuse versus separate implementations of a block, section or the full transceiver chain. Big differences in the value of a parameter required by different standards may need tuning ranges from the blocks...
that make the integrated multi-standard solution at the block or architectural level impractical or highly inefficient. Small differences in a parameter value lead to small tuning ranges that clearly make the multi-standard solution the best choice. It is in the middle ground where a trade-off between the different cost functions has to be made. In this case this tool explores both options and allows the user to choose what cost functions to optimize.

A highly integrated solution is desirable. Going off-chip is expensive, especially in terms of power consumption, 50Ω have to be driven in every interface, and area. Therefore, every solution requiring an off-chip transition is penalized not only in terms of area and power consumption, but also on its degree of possible integration level.

The integration assessment tool is to be implemented.

The component tool

The component tool runs input signals through the transceiver chain using medium and low level models of the blocks. In the design phase medium levels of the blocks are used. This allows to refine the specs for the blocks since the non-idealities introduced by the models bring to about issues that were not considered when using higher level models. Low level models verify the validity of the tool when available. It is possible to combine in the same run low and medium level blocks. This is very useful when determining the re-usability in the current system of an already available IP.

An interface with a commercially available tool, ADS [27], is being built. Thus, the block models can be implemented in Matlab/Simulink, C (supported by Matlab) and ADS.

4.5 General considerations

TACT contains tools and models that make possible its use in a hierarchical way. It is conceived as a set of separate tools that can be used independently or following TACT’s design flow, which is shown in Figure 4.3.

In order to take advantage of this hierarchical approach when using the full TACT flow, the search space will be larger in the first steps of the design and it will narrow down as we advance in the flow. At an early stage, high level models of the components are used. Hence, doing a thorough search is fast and allows to discard possibilities that even meeting the specs, do not meet the performance criteria set by the user through the cost functions. Thus, the cost in simulation time of exploring all these possibilities at this stage is relatively small. Only solutions with a certain probability of survival will step into the next level of the flow.
Chapter 5

Frequency planning

Even though we are getting closer to the Software Defined Radio (SDR) paradigm, there are still a number of major practical problems associated with placing the ADC right after the antenna. Therefore, frequency translation in the analog domain is still a must in most receivers used in handheld devices at present. This, together with filtering and amplification stages enhances the job of the analog-to-digital converter and keeps the power consumption sufficiently low to make the system practical for mobile terminals [55].

An interference oriented on-chip frequency planning is key in order to prevent the desensitization of the receiver as well as the interference of unwanted signals. These unwanted signals may appear in the different frequency bands where the desired channel falls during the different frequency transformations carried out in a receiver chain [46, 50, 56].

The objective of frequency planning is to find a frequency translation scheme with low distortion components, small limitations coming from the out-of-band blockers and lower filter order for maximum selectivity. The performance of the different possible intermediate frequencies (IF) can be measured through the levels of spurs falling in band as well as the bandwidths of the required filters. TACT takes into account not only the center frequencies of the signals, but also their bandwidths when performing all the computations [56].

The set of parameters that have to be determined at this stage when carrying out the on-chip frequency planning are:

- The number of intermediate frequencies needed.
- The center frequency of the intermediate frequency band(s).
- The bandwidth of the filter(s) at RF, IF and BB.

The rest of the parameters that define the frequency behaviour of the receiver such as filter types and orders, etc. will be determined at a later step in conjunction with the budget design as explained in Chapter 6.
5.1 Generic Receiver Architecture

Figure 4.2 shows an abstracted model that represents most of the architectures used in wireless communications receivers as explained in Section 4.2. In these receivers the RF input signal goes through a series of amplification, filtering and frequency translation stages until it is converted into a digital signal for digital post-processing.

Several factors have to be considered when choosing the set of frequencies and bandwidths for the successive frequency translation stages the signal goes through [46, 50]. The compromise made between the filtering characteristics, the linearity of the components of the receiver chain, and the ADC dynamic range will depend on the particular application and the availability of already designed IPs.

Unwanted signals may have different origins, namely: channels using the same frequency at the same time in neighbouring cells (FDMA systems) or in the same cell with a different code (CDMA systems), channels located in adjacent frequencies, out-of-band blockers present in the wireless environment, other interfering signals present on-chip coming from other parts of the circuit (signals coming from the transmitting side that appear in the receiving side through on-chip coupling mechanisms, for instance), etc.

Non-linearities of the analog/RF components may produce intermodulation products and/or harmonics of their input frequencies as was explained in Section 3.5.

5.2 Mixing and Frequency Translation

The mixing process itself takes advantage of this non-linear behaviour, so undesired in other blocks of the receiver chain, in order to perform the frequency translation along the receiver chain. Mixers are not ideal components either. Due to their finite input-output isolation, an attenuated version of the input signals appear at the output. This phenomenon is known as signal feed-through and is illustrated in Figure 5.1. It could have detrimental consequences in the system if these feed-through signals experience further non-linear processes that place them within the signal band. Another problem, acute in the case of zero-IF receivers, is self-mixing.
of the local oscillator and/or interfering signals. These signals, which might have a high power level, will leak under certain conditions to the other input terminal of the mixer as shown in Figure 5.1, and mix with themselves falling within the desired channel band. Different receiver topologies suffer from different problems related to their particular characteristics. These effects, described thoroughly in [9, 46, 50], are modeled in TACT [38, 56].

5.3 Number of Frequency Translation Steps

The first step is to determine the number of recommended translations. The aim of performing more than one frequency translation is to obtain a good selectivity while keeping the requirements of the filters as relaxed as possible. The method described in [46] is used in TACT. For receivers with a narrow relative bandwidth with respect to the carrier signal $B/f_s$, a double downconversion is recommended. This is the case of a GSM receiver, for instance. In a receiver with wide tuning range $f_{s_{max}}/f_{s_{min}}$ an upconversion stage employed to ease the filtering of the image band is followed by a downconversion. This is commonly used in mobile TV terminals (DVB-H systems), for instance.

The aim of performing more than one frequency translation is to obtain a good selectivity while keeping the requirements of the filters as relaxed as possible. It must be highlighted that the result of this evaluation is shown to the user as a recommendation. Multiple frequency translations are not carried out in the tool by default. There are other factors that may push for a single frequency translation. Integability, reduction of the overall complexity and power consumption as well as the possibility of doing some of the processing in the digital domain have to be weighted as well. For instance, many commercial GSM systems are implemented nowadays using zero-IF receivers [9], which entail a single frequency translation.

5.4 Intermediate Frequency Search

The next step is to determine the range of possible intermediate frequencies. There is a number of conditions the intermediate frequency band has to meet [46], namely: the intermediate frequency band should not overlap with the signal band or the local oscillator, the relative bandwidth of the filters should make them feasible, and the image band should be rejected when the receiver architecture is sensitive to it.

These conditions are translated into different expressions depending on the relative location of the signal RF band, the local oscillator and the IF band. This leads to different intermediate frequency ranges. An extended version of the expressions proposed in [46] is used in TACT as follows:
1. The $IF/IF_{i+1}$ band should not overlap with the $RF/IF_i$ signal band:

   if downconversion then
      $f_i < f_{RF,min}$
   else
      $f_i > f_{RF,max}$
   end;

2. The $IF/IF_{i+1}$ band should not overlap with the LO:

   if $f_o < f_{RF}$ then
      if $f_i < f_o$ then
         $f_i < f_{RF,min}/2$
      else
         $f_i > f_{RF,max}/2$
      end;
   else
      condition 2 $\subseteq$ condition 1
   end;

3. The relative bandwidth at IF should be reasonable:

   $2 < \frac{B}{f_i} < 100$

4. The RF filter should filter out interferers (especially the image band) while its design should be relatively easy (its relative bandwidth not too narrow):

   if tunable filter then
      $f_{RF,max}/f_i < 50$
   else (fix filter or filter bank)
      $f_{RF,max}/f_i < 100$
   end;
5.5. FILTERS BANDWIDTH RANGE

Example The IF frequency range for WCDMA TDD in the 2010-2025 MHz band. Assuming downconversion, high side LO and a fix filter would be:

1. Downconversion ⇒ \( f_i < f_{RF,min} \)
   \( f_i < 2010 MHz \)
2. High side LO ⇒ condition 2 ⊆ condition 1
3. \( 2 < \frac{f_i}{f_{RF,\max}} < 100 \)
   \( 10 MHz < f_i < 500 MHz \)
4. \( f_{RF,\max}/f_i < 100 \)
   \( f_i > 20.25 MHz \)

The resulting IF range will be: \textbf{20.25 MHz < f_i < 500 MHz}.

The tool also displays commonly used frequency values within the intermediate frequency range [46]. This can be a valuable piece of information when using commercial-off-the-shelf (COTS) components. The use of standard components, which are produced in large volumes by several vendors, can have a positive impact on the cost.

Once the intermediate frequency ranges are determined for all the signal bands the evaluation of the different possibilities starts. These signal bands can belong either to different or the same standard and may or may not overlap.

The user can set the number of intermediate frequency values \( N \) to be evaluated. Thus, the granularity of the frequency search space is determined. These points are distributed along the different IF ranges in such a way that in the frequency intervals common to two or more of them the evaluation is performed exactly for the same intermediate frequency values. This eases the evaluation of the multi-standard case.

The evaluation of the performance of each IF with respect to the interferers is a two step process. First the interferences coming from signals related to the given standard are considered as explained in Section 5.6. Then, the effect of out-of-band blockers is analyzed as discussed in Section 5.7.

5.5 Filters Bandwidth Range

The bandwidth ranges for the RF and IF filters are initially set so that [46]:

1. They are larger than the channel bandwidth \( B_{RF}, B_{IF} > B_{ch} \).
2. Their relative bandwidths \((B_{RF}/f_{RF}, B_{1F}/f_{1F})\) make them feasible.

3. They are smaller than the channel separation for the last IF filter \(B_{1F} < B_{sep}\).
   In the case of the RF filter bandwidth, the filtering of the image band has to be ensured. Therefore \(B_{RF} < 2f_{1Fmin}\).

---

**Example**  Following with the WCDMA example, the ranges for the filter bandwidths for \(f_i = 100\,MHz\) would be:

1. \(B_{RF} > B_{ch}\)
   \[B_{RF} > 3.84\,MHz\]

2. \(f_{RF}/B_{RF} < 100\)
   \[B_{RF} > 20.25\,MHz\]

3. \(B_{RF} < 2f_{1Fmin}\)
   \[B_{RF} < 98\,MHz\]

The resulting RF bandwidth range will be: \(20.25\,MHz < B_{RF} < 98\,MHz\)

1. \(B_i > B_{ch}\)
   \[B_i > 3.84\,MHz\]

2. \(2 < f_i/B_i < 100\)
   \[1\,MHz < B_i < 200\,MHz\]

3. \(B_i < B_{sep}\)
   \[B_i < 5\,MHz\]

The resulting IF bandwidth range will be: \(3.84\,MHz < B_i < 5\,MHz\)

---

### 5.6 Intermodulation and Harmonics

As mentioned before, the signals related to the standard under analysis are considered first. These are signals whose characteristics are known a priori. They comprise the different input channels, their corresponding local oscillator frequencies and a number of other signals present on-chip that may cause disturbances due to on-chip coupling. These signals may be the output of the power amplifier
of a transmitter sitting on the same die, the voltage controlled oscillator (VCO)
frequency, any digital clock present on chip, etc.

All the frequency bands of the undesired intermodulation products, harmonics,
self-mixing products and mixer feed-through signals coming from the combination
of these "known" signals are computed. Should any of these signals fall within the
signal band, either at the RF or the IF frequency bands, the overlapping range,
m and n in Equation 3.11, and the frequencies of the signals that originate that
distortion component are stored in TACT for further display to the user both in
numerical and graphical form. At this stage the actual power levels of the signals
at every point of the receiver chain are not known, but the origin of the distortion
component and the order give clues to an RF designer about the power level and
final impact of these signals in the receiver performance.

The minimum (most detrimental) order of the distortion components falling
within each of the intermediate frequency bands for the standards under consider-
ation is displayed to the user. Chapter 7 shows an example of such plot. When
looking at a single intermediate frequency, all the distortion components with their
order, overlapping range with the signal band and origin are identified.

5.7 Out-of-band Blockers

When evaluating the effect of out-of-band blockers that fall within the RF filter
pass-band a different method from the one discussed in the previous section is
implemented. The characteristics of the out-of-band signals are not known. The
national or international regulatory bodies of the radio spectrum may enforce a
maximum power level for signals close in frequency to a licensed band. However,
information on the bandwidth or dynamics of potential interferers might be un-
known.
It is well known that any combination of blocker frequencies \( f_{b1} \) and \( f_{b2} \) satisfying Equation 3.12 will produce third order intermodulation products that will fall in band at a frequency \( f_{\text{inband}} \). This effect, illustrated in Figure 5.2 cannot be avoided. Its impact will depend on the linearity of the receiver blocks. Increasing the linearity of these components and/or reducing the RF filter bandwidth mitigates the impact of these effects, but changing these parameters is not always possible.

When an out-of-band blocker and one of the “known” signals mentioned above are involved in the non-linear process, equation 3.11 cannot be used directly. Nevertheless, the same principle can be applied from a different standpoint. This process, illustrated in Figure 5.3, unveils the out-of-band frequency regions that may produce disturbances in the system. This information provides a deeper insight into the performance of each of the evaluated intermediate frequencies. It may change either the frequency plan choice or the requirements of the filters for some of the intermediate frequencies. These undesired blocker bands are computed as follows:

- The combinations \( |f_i \pm n \cdot f_{\text{o/ch}}| \) are calculated.
- The combinations \( m \cdot f_{\text{blockerband}} \) are calculated. The blocker bands are the RF filter pass-band without the signal bands.
- The overlap between the resulting bands is computed.
- The blocker bands corresponding to the overlapping range are computed.

This process is illustrated graphically in Figure 5.3 and through the following numerical example:
**Example**  Let us continue with the WCDMA example and follow the calculation of a potentially dangerous frequency band falling within the passband of the RF filter:

<table>
<thead>
<tr>
<th>Band</th>
<th>Frequency range (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_{bl1} )</td>
<td>1919.9 - 2010</td>
</tr>
<tr>
<td>( 2 \times f_{bl1} )</td>
<td>3839.9 - 4020</td>
</tr>
<tr>
<td>(</td>
<td>f_1 + 2 \times f_{ch1}</td>
</tr>
<tr>
<td>( f_{overlap} )</td>
<td>3922.4 - 3927.4</td>
</tr>
<tr>
<td>( f_{bl, out} )</td>
<td>1961.2 - 1963.7</td>
</tr>
<tr>
<td>( B_{RF, stopmin ; revised} )</td>
<td>1963.7</td>
</tr>
</tbody>
</table>

As this example illustrates, the described evaluation technique provides the RF engineer with the information that allows him to choose another frequency plan, harden the filtering requirements, or to take a calculated risk. In the particular case shown in this example, a fourth order intermodulation product between the first signal channel and a blocker within the \( f_{bl, out} \) range would fall within the intermediate frequency range centered at 100.12 MHz.
Chapter 6

Receiver Budget

Many tradeoffs have to be made when fixing the characteristics of each of the blocks. The interdependency between the overall noise and non-linearity characteristics on the gain and selectivity of all the blocks makes this task difficult.

The receiver budget is realized taking the radio specifications of the standards under consideration, the receiver architectures a user wants to explore and the high level models of the receiver blocks [57]. At the output comes a set of candidate receiver budgets with their performances shown to the user. The cost functions that are evaluated at this stage are the overall noise figure (NF), the second and third order intercept points (IIP2, IIP3), and the number of bits of the analog-to-digital converter (ADC).

This parameter distribution should be done in such a way that:

- The specs for each block are practically feasible.

- The aggregate parameters computed determined using the procedure described in Chapter 3 meet the specs and test procedures set by the standards.

We will see how to check this last condition in the coming sections. As for setting reasonable specs for each of the blocks, there is no common procedure or methodology that can be used. It is based on rules of thumb, experience, contact with experts and a lot of digging in published work. This is a key issue without an easy answer.

Besides the block characteristics, the architecture selection, the frequency plan and the order in which the amplifying and filtering operations are performed [50] will lead to different block combinations and therefore, different results as was mentioned in the previous chapters.

Both the multi-standard and the single standard cases are studied at the architectural and the block level for the reasons mentioned in Chapter 4.
Power and noise figure budget for a WCDMA receiver. 3.84 Mcps TDD Option

### Gain Budget (Voltage)

<table>
<thead>
<tr>
<th></th>
<th>Switch</th>
<th>RF Filter</th>
<th>LNA</th>
<th>Mixer</th>
<th>LPF</th>
<th>VGA</th>
<th>ADC</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Minimum/Nominal Voltage Gain (dB)</strong></td>
<td>-0.5</td>
<td>-3</td>
<td>10</td>
<td>8</td>
<td>-3</td>
<td>6</td>
<td>0</td>
</tr>
<tr>
<td><strong>Maximum Voltage Gain (dB)</strong></td>
<td>-0.5</td>
<td>-3</td>
<td>25</td>
<td>8</td>
<td>-3</td>
<td>45</td>
<td>0</td>
</tr>
<tr>
<td><strong>Cumulative Minimum/Nominal Voltage Gain</strong></td>
<td>-0.5</td>
<td>-3.5</td>
<td>6.5</td>
<td>14.5</td>
<td>11.5</td>
<td>17.5</td>
<td>17.5</td>
</tr>
<tr>
<td><strong>Cumulative Maximum Voltage Gain (dB)</strong></td>
<td>-0.5</td>
<td>-3.5</td>
<td>21.5</td>
<td>29.5</td>
<td>26.5</td>
<td>71.5</td>
<td>71.5</td>
</tr>
<tr>
<td><strong>Minimum/Nominal Linear Voltage Gain</strong></td>
<td>0.9440609</td>
<td>0.70795</td>
<td>3.16228</td>
<td>2.51189</td>
<td>0.70795</td>
<td>1.99526</td>
<td>1</td>
</tr>
<tr>
<td><strong>Maximum Linear Voltage Gain</strong></td>
<td>0.9440609</td>
<td>0.70795</td>
<td>17.7828</td>
<td>2.51189</td>
<td>0.70795</td>
<td>177.828</td>
<td>1</td>
</tr>
<tr>
<td><strong>Cumulative Minimum/Nominal Linear Voltage Gain</strong></td>
<td>0.9440609</td>
<td>0.66834</td>
<td>2.11349</td>
<td>5.20884</td>
<td>3.75837</td>
<td>7.49894</td>
<td>7.49894</td>
</tr>
<tr>
<td><strong>Cumulative Maximum Linear Voltage Gain</strong></td>
<td>0.9440609</td>
<td>0.66834</td>
<td>11.885</td>
<td>29.8538</td>
<td>21.1349</td>
<td>375.837</td>
<td>375.837</td>
</tr>
<tr>
<td><strong>Minimum/Nominal Linear Power Gain</strong></td>
<td>0.8912509</td>
<td>0.50119</td>
<td>10</td>
<td>6.30957</td>
<td>0.50119</td>
<td>3.98107</td>
<td>1</td>
</tr>
<tr>
<td><strong>Maximum Linear Power Gain</strong></td>
<td>0.8912509</td>
<td>0.50119</td>
<td>316.228</td>
<td>6.30957</td>
<td>0.50119</td>
<td>3162.28</td>
<td>1</td>
</tr>
</tbody>
</table>

### Noise Budget (Power)

<table>
<thead>
<tr>
<th></th>
<th>Switch</th>
<th>RF Filter</th>
<th>LNA</th>
<th>Mixer</th>
<th>LPF</th>
<th>VGA</th>
<th>ADC</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Noise Figure (dB) for Min Gain</strong></td>
<td>0.5</td>
<td>0.5</td>
<td>3</td>
<td>18</td>
<td>25</td>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td><strong>Noise Figure (dB) for Max Gain</strong></td>
<td>0.5</td>
<td>0.5</td>
<td>1.5</td>
<td>18</td>
<td>25</td>
<td>15</td>
<td>30</td>
</tr>
<tr>
<td><strong>Input Referred NF (dB) Min/Nom Gain</strong></td>
<td>20.68416</td>
<td>20.1842</td>
<td>17.2204</td>
<td>27.0614</td>
<td>34.4873</td>
<td>30.9724</td>
<td>30</td>
</tr>
<tr>
<td><strong>Input Referred NF (dB) Max Gain</strong></td>
<td>4.835023</td>
<td>4.335023</td>
<td>2.5468</td>
<td>20.8902</td>
<td>25.7679</td>
<td>15.0043</td>
<td>30</td>
</tr>
<tr>
<td><strong>Noise Factor f for Min Gain</strong></td>
<td>1.1220185</td>
<td>1.1220185</td>
<td>1.99526</td>
<td>63.0957</td>
<td>316.228</td>
<td>1000</td>
<td>1000</td>
</tr>
<tr>
<td><strong>Noise Factor f for Max Gain</strong></td>
<td>1.1220185</td>
<td>1.1220185</td>
<td>1.41254</td>
<td>63.0957</td>
<td>316.228</td>
<td>31.6228</td>
<td>1000</td>
</tr>
<tr>
<td><strong>Input Referred Noise Factor for Min/Nom Gain</strong></td>
<td>117.06204</td>
<td>104.332</td>
<td>52.7274</td>
<td>508.321</td>
<td>2810.18</td>
<td>1250.94</td>
<td>1000</td>
</tr>
<tr>
<td><strong>Input Referred Noise Factor for Max Gain</strong></td>
<td>3.044404</td>
<td>2.71333</td>
<td>1.79754</td>
<td>122.75</td>
<td>377.391</td>
<td>31.6544</td>
<td>1000</td>
</tr>
</tbody>
</table>

The parameters that will be affected by a gain change on the LNA are shadowed in light grey.
### Power and noise figure budget for a WCDMA receiver. 3.84 Mcps TDD Option

#### Gain Budget (Voltage)

<table>
<thead>
<tr>
<th></th>
<th>Switch</th>
<th>RF Filter</th>
<th>LNA</th>
<th>Mixer</th>
<th>LPF</th>
<th>VGA</th>
<th>ADC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum/Nominal Voltage Gain (dB)</td>
<td>-0.5</td>
<td>-3</td>
<td>10</td>
<td>8</td>
<td>-3</td>
<td>6</td>
<td>0</td>
</tr>
<tr>
<td>Maximum Voltage Gain (dB)</td>
<td>-0.5</td>
<td>-3</td>
<td>8</td>
<td>-3</td>
<td>45</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Cumulative Minimum/Nominal Voltage Gain</td>
<td>-0.5</td>
<td>-3,5</td>
<td>6.5</td>
<td>14.5</td>
<td>11.5</td>
<td>17</td>
<td>17.5</td>
</tr>
<tr>
<td>Cumulative Maximum Voltage Gain (dB)</td>
<td>-0.5</td>
<td>-3,5</td>
<td>16.5</td>
<td>24.5</td>
<td>21.5</td>
<td>66.5</td>
<td>66.5</td>
</tr>
<tr>
<td>Minimum/Nominal Linear Voltage Gain</td>
<td>0.9440609</td>
<td>0.70795</td>
<td>3.16228</td>
<td>2.51189</td>
<td>0.70795</td>
<td>1.99526</td>
<td>1</td>
</tr>
<tr>
<td>Maximum Linear Voltage Gain</td>
<td>0.9440609</td>
<td>0.70795</td>
<td>10</td>
<td>2.51189</td>
<td>0.70795</td>
<td>177.828</td>
<td>1</td>
</tr>
<tr>
<td>Cumulative Minimum/Nominal Linear Voltage Gain</td>
<td>0.9440609</td>
<td>0.66834</td>
<td>2.11349</td>
<td>5.30884</td>
<td>3.75837</td>
<td>7.49894</td>
<td>7.49894</td>
</tr>
<tr>
<td>Cumulative Maximum Linear Voltage Gain</td>
<td>0.9440609</td>
<td>0.66834</td>
<td>6.68344</td>
<td>16.788</td>
<td>11.885</td>
<td>2113.49</td>
<td>2113.49</td>
</tr>
<tr>
<td>Minimum/Nominal Linear Power Gain</td>
<td>0.8912509</td>
<td>0.50119</td>
<td>10</td>
<td>6.30957</td>
<td>0.50119</td>
<td>3.98107</td>
<td>1</td>
</tr>
<tr>
<td>Maximum Linear Power Gain</td>
<td>0.8912509</td>
<td>0.50119</td>
<td>100</td>
<td>6.30957</td>
<td>0.50119</td>
<td>31622.8</td>
<td>1</td>
</tr>
</tbody>
</table>

#### Noise Budget (Power)

<table>
<thead>
<tr>
<th></th>
<th>Switch</th>
<th>RF Filter</th>
<th>LNA</th>
<th>Mixer</th>
<th>LPF</th>
<th>VGA</th>
<th>ADC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Noise Figure (dB) for Min Gain</td>
<td>0.5</td>
<td>0.5</td>
<td>3</td>
<td>18</td>
<td>25</td>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td>Noise Figure (dB) for Max Gain</td>
<td>0.5</td>
<td>0.5</td>
<td>1.5</td>
<td>18</td>
<td>25</td>
<td>15</td>
<td>30</td>
</tr>
<tr>
<td>Input Referred NF (dB) Min/Nom Gain</td>
<td>20.68416</td>
<td>18.842</td>
<td>17.2204</td>
<td>27.0614</td>
<td>34.4873</td>
<td>30.9724</td>
<td>30</td>
</tr>
<tr>
<td>Input Referred NF (dB) Max Gain</td>
<td>6.909151</td>
<td>6.40915</td>
<td>4.19962</td>
<td>20.8902</td>
<td>25.7679</td>
<td>15.0043</td>
<td>30</td>
</tr>
<tr>
<td>Noise Factor f for Min Gain</td>
<td>1.1220185</td>
<td>1.12202</td>
<td>1.99526</td>
<td>63.0957</td>
<td>316.228</td>
<td>1000</td>
<td>1000</td>
</tr>
<tr>
<td>Noise Factor f for Max Gain</td>
<td>1.1220185</td>
<td>1.12202</td>
<td>1.41254</td>
<td>63.0957</td>
<td>316.228</td>
<td>31.6228</td>
<td>1000</td>
</tr>
<tr>
<td>Input Referred Noise Factor for Min/Nom Gain</td>
<td>117.06204</td>
<td>104.332</td>
<td>52.7274</td>
<td>508.321</td>
<td>2810.18</td>
<td>1250.94</td>
<td>1000</td>
</tr>
<tr>
<td>Input Referred Noise Factor for Max Gain</td>
<td>4.9081189</td>
<td>4.37437</td>
<td>2.63003</td>
<td>122.75</td>
<td>377.391</td>
<td>31.6544</td>
<td>1000</td>
</tr>
</tbody>
</table>

The parameters affected by the the gain change in the LNA are shadowed in light grey.
6.1 Definitions

We define the Usable Region $UR$ of a receiver block as the subset of $\mathbb{R}^N \times \mathbb{R}^N$ where the specs of the block are both feasible and useful in the context of radio receivers. $N$ is the number of parameters that define the characteristics of each block. The usable region $UR$ is a very small subset of $\mathbb{R}^N \times \mathbb{R}^N$, which helps reducing the convergence time. The usable regions are the mechanism that allows to include the experience of an analog/RF designer into the tool. For instance, a filter with $10dB$ in-band attenuation is not an useful block to have in a receiver. Hence, there is no need to consider a filter with such characteristics during the design process.

Let $B$ be the number of blocks of the receiver chain, $x_i \in UR_i \forall i \in \{1, B\}$ the parameter vector that contains the specs of the $i^{th}$ block, $S \subset UR$ the set of parameter distributions $x = (x_1, \ldots, x_B)$ that meet the receiver specs, $x_{r,i} \in UR_i$ contains the most relaxed (and therefore easier to meet) block specs, that is, $A_{\min}$, $NF_{\max}$, $IIP3_{\min}$, etc. $x_i \in UR_i$ contains the toughest block specs, that is, $A_{\max}$, $NF_{\min}$, $IIP3_{\max}$, etc.

6.2 The Receiver Budget Problem

The main goal of this tool is to find a parameter distribution $x = (x_1, \ldots, x_B)$ such that $x \in S$ and $d(x_i, x_{r,i})$ is minimized, where $d(x_i, x_{r,i})$ is the Euclidean distance between $x_i$ and $x_{r,i}$.

In other words, find a multi-standard receiver budget that meets or exceeds the specs of the addressed wireless standards while keeping the requirements of each of the receiver blocks as relaxed as possible.

6.3 The Traditional Approach: Spreadsheets

The traditional approach to solve this problem, used still nowadays, is to find this parameter distribution that meets specs using spreadsheets. Tweaking the budget using this method is an extremely cumbersome and error prone method. It is not very flexible and extremely time consuming, which limits the number of solutions that can be explored in a short time. It relies completely in the RF system designer when it comes to handle the parameter interdependencies. An experienced designer knows, of course, “the tricks of the trade”, that is, he or she knows very well how to distribute the specs among the receiver blocks qualitatively and, to a certain extent, quantitatively. Let us illustrate the limitations of this approach with a small example. Imagine we are tweaking the budget of a receiver whose linearity does not meet specs and the linearity requirements of the receiver blocks are already at the limit. Decreasing the gain of the LNA is one of the actions that we could take in order to improve the linearity performance of the overall system. Figure 2 shows how this gain change does not affect only the gain and linearity distribution. Improving linearity this way worsens the noise performance of the receiver. This
is just a simple example showing only how noise and linearity requirements set
different constraints to the gain distribution, but there are many other parameter
interdependencies [9, 46, 50].

It is very difficult for a designer to keep track of the evolution of the receiver
performance using this method, not to mention the difficulty in ensuring a fair
distribution of the specs among the blocks. Having EDA tools coming to the rescue
in this task is certainly dreamed by many RF system engineers.

6.4 Receiver Budget Optimization in TACT

Finding a parameter distribution that meets specs is the first goal the algorithm
implemented in TACT focuses on. Then, both the solution and the room for
improvement for each of the parameters is presented to the user. Further optimization
is performed using basically the same algorithm as when finding the initial distrib-
ution that meets specs. This algorithm works as follows:

The loop of finding a solution that meets the specs is entered. The first step
is to check for convergence, that is, whether or not the specs are achievable at all.
In this test, the best possible value for each parameter within the usable region is
employed when calculating the cost functions. If any of the cost functions is not
achievable, execution is halted and the usable regions revised.

The first step is to generate a seed solution. Each parameter of each block is
set to the value that makes its specs most relaxed. Then, the operations sketched
in Figure 6.3 are performed.

The reassignment of the block parameters is done according to their impact on
the overall system. The margin for change of each parameter is also taken into
account. This parameter reassignment only takes place when the overall value does
not meet specs.

The budget optimization problem could be classified as a multi-variable opti-
mization problem. A conflict arises from trying to meet all the goal functions (noise
figure, linearity, etc.) as was highlighted in Section 3.11. The parameter distrib-
utions that optimize each goal function are very different from one another. There
is no parameter distribution that optimizes all of them at the same time. Instead
of setting weights to the different goal functions to generate a single cost function,
TACT's budget tool has meeting all the specs as optimization objective. Thus,
there is no need to adjust the weight functions. Even when the solution offered by
the tool might not be the one providing less conflict, it is ensured that it is feasible (i.e.,
that it belongs to the usable regions) and that it meets specs [25].

The implemented algorithm is based on simulated annealing [58–61]. The algo-
rithm takes advantage of an impact oriented parameter distribution as explained in
the following sections. Thus, convergence time is reduced while ensuring that the
requirements of the individual blocks are as relaxed as possible.
while specs_set == false  
    if gain_redistrib_needed == true  
        redistribute_gain;  
    else  
        if rand < p  
            change it anyway sometimes  
        redistribute_gain;  
    else  
        redistribute_params_not_meeting_specs;  
    end;  
end;  

cost = check_specs;  
if cost < specs  
    specs_set = true;  
end;  
if cost < best_cost  
    best_budget = this_budget;  
end;  
end;

Figure 6.3: Algorithm to find a budget meeting specs.

6.5 Impact Oriented Parameter Distribution

We propose a reassignment scheme for the values of the block parameters based on their impact on the overall system. It also takes into account how much margin for changing the parameter has, that is, its distance to the toughest block specs \(d(x_i, x_{t,i})\).

6.6 Noise Figure Optimization

Let us describe first the way this algorithm works in the case of the noise figure. Table 6.1 shows a numerical example of the noise figure reassignment. Equation 3.10 shows the aggregated noise factor, which is a function of the noise factors and gains of each of the blocks. The difference \(\Delta\) between the current noise factor value and a new noise factor value is, therefore:

\[
\Delta = \Delta_1 + \Delta_2 + \ldots + \frac{\Delta_m}{A_1 \cdots A_{(m-1)}},
\]

(6.1)

Hence, a change in the front-end noise factor has a bigger impact in the overall noise factor. Let \(A_i\) be the power gain of the \(i\)-th block and \(\delta_i\) the margin for
Table 6.1: Noise figure reassignment

<table>
<thead>
<tr>
<th>Parameter</th>
<th>RF filter</th>
<th>LNA</th>
<th>Mixer</th>
<th>IF filter</th>
<th>VGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>nf max</td>
<td>10</td>
<td>10</td>
<td>100</td>
<td>10</td>
<td>1000</td>
</tr>
<tr>
<td>nf min</td>
<td>1.26</td>
<td>1.26</td>
<td>3.16</td>
<td>1.99</td>
<td>3.16</td>
</tr>
<tr>
<td>$A_i$</td>
<td>0.36</td>
<td>65.8</td>
<td>5.5</td>
<td>0.3</td>
<td>5e+5</td>
</tr>
<tr>
<td>current nf</td>
<td>1.55</td>
<td>1.5</td>
<td>6.38</td>
<td>2.26</td>
<td>36.3</td>
</tr>
<tr>
<td>overall nf</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>4.17</td>
</tr>
</tbody>
</table>

\[
\Delta = 0.23
\]

\[\delta_i = \begin{cases} 
\delta_1 & \text{if } i = 1 \\
\frac{\delta_i}{A_i - A_{i-1}} & \text{if } i \neq 1
\end{cases}
\]

\[\chi_i = \begin{cases} 
\chi_i & \text{if } i = 1 \\
\frac{\Delta_i \cdot \chi_i}{\sum_i \chi_i} & \text{if } i \neq 1
\end{cases}
\]

which, in relative value, turns into:

\[\chi_i' = \frac{\chi_i}{\sum_i \chi_i}
\]

If an improvement of value $\Delta$ is desired in the noise factor, the individual $\Delta_i$ values will be:

\[\Delta_i = \begin{cases} 
\Delta \cdot \chi_i' & \text{if } i = 1 \\
\Delta \cdot \chi_i' \cdot A_i \cdots A_{i-1} & \text{if } i \neq 1
\end{cases}
\]

When the current noise factor is within an $\epsilon$ of the desired one, $\Delta = n_f \text{current} - n_f \text{specs}$. Otherwise, $\Delta$ is a fraction of that difference. Since the gain distribution often changes along the process of optimizing all the parameters this measure leads to designs that meet specs while keeping the requirements of the individual blocks as relaxed as possible. A very small value of $\epsilon$ or of the factor that scales $\Delta$ may increase significantly the time for converging to a parameter distribution meeting specs. These values should be chosen carefully.
6.7 Linearity Optimization

A similar procedure is followed when reassigning the linearity parameters. Since the equations are slightly different, using a multiplicative factor between the current and the new linearity values is more convenient. Taking:

\[ IP_{new} = \mu IP_3 \]  

(6.5)

where \( IP_3 \) is the current IP3 value, makes the difference:

\[
\frac{1}{\eta_3} - \frac{1}{\eta_{new}^3} = \frac{1}{\eta_3} - \frac{1}{\mu \eta_3^2} = \frac{\mu^2 - 1}{\mu^2 IP_3^2} = \\
\frac{\mu^2 - 1}{\mu^2 IP_3^2} + A_1 \frac{\mu^2 - 1}{\mu^2 IP_3^2} + \cdots + A_1 \cdots A_{n-1} \frac{\mu^2 - 1}{\mu^2 IP_{n-1}^2} 
\]

(6.6)

This equation can be rewritten as:

\[
\frac{1}{\eta} = \frac{1}{\eta_1} + \frac{1}{\eta_2} + \cdots + \frac{A_1 \cdots A_{n-1}}{\eta_n} 
\]

(6.7)

where \( \frac{1}{\eta_i} = \frac{\mu^2 - 1}{\mu^2 IP_{i-1}^2} \).

Equation 6.7 is very similar to Equation 6.1. Therefore, an equivalent procedure to the one described by equations 6.1 to 6.4 is followed when computing the \( \frac{1}{\eta_i} \) values. The obtained \( \frac{1}{\eta_i} \) are ultimately converted to the \( \mu_i \) scaling factors providing, thus, the new values for the \( IP_3 \) components.

6.8 ADC’s Dynamic Range Steering the Search

The \( DR_{ADC} \) is calculated according to Equation 3.21. The noise and signal levels along the receiver blocks are calculated in order to be able to determine the signal of maximum power \( P_{max} \) and the noise power \( P_{noise} \) at the input of the ADC. The proper gain and filtering settings have to be applied for the different types of input signals. For instance, the maximum input signal will use the minimum gain option of the AGC loop and the in-band gain of the filters; the minimum input signal will use the maximum gain option of the AGC loop and the in-band gain of the filters; blockers and adjacent channels will use the maximum gain option and the attenuation provided by the filters at their offset frequencies from the desired channel (worst case scenario). If the ENOB specs are not met, the gain of the AGC is adjusted, the filtering specs are hardened or both. The probability of choosing each of these options depends on the origin of the signals that determine the ADC dynamic range.
6.9 Gain Distribution

The routine that changes the gain distribution has to determine both the direction of the change (increase or decrease the gain), the location of the change (front-end, back-end, everywhere) and the amount of gain change to be introduced. When changing the gain, it is ensured that the new gain value is within the range limits. The absolute value of the gain variation is random within these limits.

When only the noise figure specs are not met, the routine will increase the front-end gain. The opposite will happen when only the linearity specs are not met. In this situation, the front-end gain will be decreased. In the event of both the noise figure and linearity specs not being met, changes of random direction are made in the gain distribution. As was mentioned in Section 6.8 not meeting \( DR_{ADC} \) specs may change the gain distribution. In this case gain changes are introduced in all the blocks.

In a receiver chain, there are blocks with variable gain and blocks with fixed gain. When the multi-standard case is being evaluated, the gain changes for the blocks programmable in gain are introduced with probability one. If the block is not programmable in gain, the gain reassignment is taken into consideration with probability \( p \), where \( p \) is decided by the user. Depending on the gain values the various standards try to assign to a block and the direction they are trying to push the new value to, a different gain value will be resolved.

6.10 Evolution of the Budget Design

The RF standard specs are mapped into receiver specs. In order to find a parameter distribution meeting these receiver specs the budget design tool is executed.

Figure 6.4 illustrates one aspect the evolution of the optimization process of the WCDMA/WLAN multi-standard budget taken as an example. The resulting signal levels along the receiver blocks are shown at three simulation steps. The level of the desired input signals (maximum and minimum option), adjacent channels, blockers and noise floor is plotted against the different blocks. These signal levels are shown at the input of the RF filter (1), the LNA (2), the mixer (3), the baseband filter (4), the baseband VGA (5), and the ADC (6).

The redistribution of the block characteristics performed during the optimization of the budget makes these signals evolve with the simulation step as illustrated in this figure. The distribution of the gain, noise figure, linearity performance, and filtering characteristics changes along with the simulation step. These parameters are readjusted in order to meet the requirements of the standards. Note how in time this adjustments attenuate adjacent channels and out-of-band blockers that may interfere with the desired signal. This figure shows how the power level of the signals along the blocks is adapted in time to meet the performance levels set by the wireless communication standards.
Figure 6.4: Evolution of the signal levels along the blocks for WCDMA and WLAN for different simulation steps. The WCDMA signals shown in 6.4(a), 6.4(c) and 6.4(e) correspond to: + $P_{\text{max}}$, o $P_{\text{min}}$, * Adjacent Channel at 5 MHz offset, x Adjacent Channel at 10 MHz offset, □ Adjacent Channel at 15 MHz offset, © Out-of-band Blocker at 15 MHz offset, ▽ Out-of-band Blocker at 60 MHz offset, △ Out-of-band Blocker at 85 MHz offset, ★ Noise Floor. The WLAN signals shown in 6.4(b), 6.4(d) and 6.4(f) correspond to: + $P_{\text{max}}$, o $P_{\text{min}}$, * Adjacent Channel at 25 MHz offset, ★ Noise Floor.
Figure 6.5: Evolution of the cascaded IIP3 for (a) WCDMA and (b) WLAN for a typical run

As an example, Figure 6.5 shows how the IIP3 evolves in a typical run for WCDMA and WLAN as a function of the gain and iteration number. IIP2, NF,
and $DR_{ADC}$ convergence to the goal values in a similar manner. Their plots are not shown here for the sake of brevity.

### 6.11 Power Considerations

The proposed multi-standard budget design tool is implementation independent. Hence, it is not possible to perform a fairly accurate power consumption estimation. Power is, nevertheless, one of the major concerns in circuit design. Therefore, the optimization algorithm takes some high-level general measures that help keeping the power consumption low:

- Initialization in the most relaxed conditions: $x_{initial} = x_{r} = x_{r,1} \ldots x_{r,B}$. Smaller gain, higher NF, smaller IP's mean less current. The algorithm then moves slowly towards a solution meeting specs but staying as close to $x_{r}$ as possible as was explained in Section 6.2.

- The order of the filters is increased only when it is absolutely needed. Smaller order means less filtering stages and, therefore, less area and power consumption coming from the filters.

- ADC with as small DR as possible.

### 6.12 Block Reuse and Reliability Issues

Having the whole design flow of an RF receiver from system to silicon into focus, the use of a high level tool such as the one described in this paper can save a significant amount of time and manpower. In comparison with their digital counterparts, the analog and RF blocks have an extremely large design cycle. The level of uncertainty between simulated and fabricated circuits and the limitations of the available automated design tools for analog circuits worsen this situation. Intellectual Property (IP) block reuse is, therefore, very important not only due to the time saved it entails but also due to reliability issues. Including already tested blocks in a new design increases the chances of first pass success.

The proposed tool and methodology help RF designers in taking the right choices at system level increasing, thus, the chances of first pass success. Reducing the probability of silicon re-spins, common in analog and RF designs, months can be saved in a project [15].

### 6.13 Timing analysis

The budget optimization is based on simulated annealing. Its execution time is non-deterministic and very dependent on the cooling temperature and the goal functions. Table 6.2 shows the maximum, minimum, mean and standard deviation.
of the execution time. The statistics are calculated over 200 runs of the tool where a multi-standard WCDMA/WLAN zero-IF receiver is the target for the optimization.

### 6.14 Comparison with other Tools

The low execution time shown in Section 6.13 is due to the fact that this is an implementation independent high level tool. A similar design carried out using the already available tools mentioned in Chapter 1 would take much longer time. Our approach is, hence, very good as a first step when designing an RF receiver, especially if the multi-standard case has to be considered.

TACT’s budget tool cannot be used alone, though. Once the receiver specs have been set using our approach, tools providing more accurate models should be used so that further non-idealities can be accounted for as was described in Section 1.7. Final adjustments in the block specs may have to be done at this point. It is recommended to provide some margin in the cost functions when doing the budget design using our tool in order to minimize the number of design iterations.

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>$t_{\text{min}}$ (s)</th>
<th>$t_{\text{max}}$ (s)</th>
<th>$t_{\text{mean}}$ (s)</th>
<th>$\sigma$</th>
</tr>
</thead>
<tbody>
<tr>
<td>WCDMA/WLAN</td>
<td>3.07</td>
<td>25.47</td>
<td>9.69</td>
<td>3.73</td>
</tr>
</tbody>
</table>
Chapter 7

Case Study

This section illustrates the capabilities of TACT by means of a case study that considers a WCDMA/WLAN multi-standard receiver [39, 40]. The radio characteristics of these two standards are summarized in Table 7.1.

Let us see what involves moving from a zero-IF receiver up in frequency to a low-IF configuration or even to a high-IF solution. Single downconversion receivers are quite popular architectures for multi-standard applications. Their characteristics make them relatively easy to program, turning them into an attractive architectural choice. Hence, this discussion will be limited to them. One of the challenges RF system designers face is finding a frequency plan that suits both standards and that fosters hardware sharing. Of course, in the case of the zero-IF receiver the frequency plan is determined by the architecture: there is direct conversion to baseband having a center frequency of 0 Hz.

Table 7.1: Summary of the WCDMA (TDD) and WLAN(802.11b) RF specifications.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>WCDMA</th>
<th>WLAN</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>RF Frequency Band</strong></td>
<td>2010-2025 MHz</td>
<td>2400-2485 MHz</td>
</tr>
<tr>
<td></td>
<td>1900-1910 MHz</td>
<td></td>
</tr>
<tr>
<td><strong>RF Channel Bandwidth</strong></td>
<td>3.84 MHz</td>
<td>20 MHz</td>
</tr>
<tr>
<td><strong>Channel Separation</strong></td>
<td>5 MHz</td>
<td>5/25 MHz</td>
</tr>
<tr>
<td><strong>Sensitivity</strong></td>
<td>-117 dBm</td>
<td>-76 dBm</td>
</tr>
<tr>
<td><strong>Max Power Level</strong></td>
<td>-25 dBm</td>
<td>-10 dBm</td>
</tr>
<tr>
<td><strong>Adjacent Ch. Selectivity</strong></td>
<td>33 dB</td>
<td>35 dB</td>
</tr>
</tbody>
</table>
7.1 Frequency Plan Choice

In order to evaluate the immunity from interferers of the different possible frequency plans for a single downconversion receiver as the one shown in Figure 7.1, TACT’s frequency planning tool is executed. Figure 7.2 shows one of the outputs provided by the frequency planning tool. This plot gives a snapshot of the intermodulation and harmonic content due to in-band interferers for different intermediate frequencies. This figure depicts the worst case intermodulation or harmonic order due to in-band interferers up to distortion of order 10 for 1000 frequencies within the possible intermediate frequency range. The y-axes shows the lower order of the distortion components falling within each of the intermediate frequency bands, whose center frequency is represented in the x-axis. This plot considers only signals directly related to the standards (channels, local oscillators, etc.). It could also include any other signal that the user would like to include so that, for instance, on-chip signals known a priori (signals coming from the transmitter, a digital clock, etc.) can be considered. The execution time of TACT’s frequency planning tool for this run was 36 seconds.

For a given pair of input signals, distortion components have larger power the smaller their order is in the weakly non-linear region [9]. Hence, low order distortion components are, in general, more detrimental to the system. However, the order is not the only important factor as was mentioned in Section 3.5. The impact of odd and even distortion components depends on the receiver architecture [46, 50]. Moreover, different cancellation techniques may apply when addressing odd or even distortion components.

The origin of the signals producing distortion components and the frequency overlap with the desired signal’s bandwidth are also key in determining the performance of each intermediate frequency. For instance, the intermodulation between the local oscillator and an adjacent channel will have different characteristics than
7.1. **FREQUENCY PLAN CHOICE**

![Intermodulation and Harmonics Chart vs. Intermediate Frequency](image-url)

Figure 7.2: Minimum order of distortion components vs. the intermediate frequency band within which they fall.

...the intermodulation between two adjacent channels and, therefore, affect the system in a different way. TACT stores information about the origin of the signals causing undesired distortion components that fall in the band of interest as well as the frequency overlap range. This information is available to the user when only one intermediate frequency is selected.

Direct inspection of Figure 7.2 shows that WCDMA is somewhat better behaved than WLAN when it comes to intermodulation performance. For the granularity of frequency space exploration of this run (1000 evaluated IFs), the spot where WLAN starts showing really good performance is around 350MHz. This is a fairly high frequency that may be quite stringent in the specifications of some of the IF blocks, mainly the ADC whose design would be very challenging. If this made a user decide on lower IF frequencies, two fairly good spots for both standards shown in this run of TACT are $f_{IF} = 54.16\,MHz$ and $f_{IF} = 103.1\,MHz$, much more suitable for a practical implementation.

Out-of-band blockers are a fact of life. In most cases, the only thing we can do to prevent their impact is to increase the linearity of the receiver’s blocks.

Out-of-band blockers that fall within the RF filter pass band may cause a lot of problems in a receiver. Section 3.5 described how odd order intermodulation...
products of out-of-band interferers and adjacent channels that are not filtered out may fall in the signal band. Figure 3.4 illustrates this fact. Sometimes, the only things that can be done to prevent their impact is to increase the linearity and/or the filtering characteristics of the receiver’s blocks. However, taking these measures may be too costly or even unfeasible.

It is possible, though, to identify the frequency locations that could potentially cause more damage in the system should an undesired signal fall in that frequency band and go through a non-linear process in combination with signals belonging to the standard. The sensitivity to out-of-band blockers falling within the RF filter’s band is evaluated using the method described in in Section 5.7. As an example of TACT’s capabilities with respect to this matter, Figure 7.3 shows the out-of-band blocker locations identified as potentially dangerous by TACT. The bands depicted in this figure correspond to the side of the RF filter band situated under the signal band for WCDMA for both \( f_{IF} = 54.16 \, MHz \) 7.3(a) and \( f_{IF} = 103.1 \, MHz \) 7.3(b). These plots show the frequency bands that would produce beats falling within the IF band when mixed with local oscillators, channels, etc. From the standpoint of sensitivity to out-of-band blockers, \( f_{IF} = 103.1 \, MHz \) is a better choice than \( f_{IF} = 54.16 \, MHz \). Since part of the potentially dangerous blocker bands are more far apart from the signal band, the same filter characteristics would provide better immunity to out-of-band blockers. Even if the design of the ADC is more challenging for the \( f_{IF} = 103.1 \, MHz \), let us see how the receiver budget would look like for this frequency plan since the Software Radio (SR) trend is pushing towards higher and higher IFs.

### 7.2 Budget Design

Once a frequency plan has been chosen, it is time to move on to designing the receiver budget. In order to find a parameter distribution meeting the receiver specs, TACT’s budget tool is executed. The distribution of the gain, noise figure, linearity performance, and filtering characteristics evolve with the simulation step. These parameters are re-adjusted in order to meet the noise figure and linearity specs set by the standard, the ADC dynamic range specified by the user and the analog-digital partitioning that results from them.

Figure 7.4 shows the resulting signal levels along the receiver blocks for both WCDMA 7.4(a) and WLAN 7.4(b) for an example receiver with \( f_{IF} = 103.1 \, MHz \). The levels of the desired input signals (maximum and minimum option), adjacent channels, blockers and noise floor are plotted against the different blocks. These signal levels are shown at the input of the RF filter (1), the LNA (2), the mixer (3), the baseband filter (4), the baseband VGA (5), and the ADC (6). Table 7.2 summarizes the performance of this receiver and Table 7.3 shows the parameter distribution obtained running TACT’s budget tool. The obtained performance is shown to meet or exceed the requirements of the WCDMA/WLAN standards. As such, the case study validates the benefits of the proposed tool.
7.2. BUDGET DESIGN

![Graphs showing dangerous blocker bands WCDMA with \( f_{1F} = 54.16 \text{MHz} \) and \( f_{1F} = 103.1 \text{MHz} \)](a)

![Graphs showing dangerous blocker bands WCDMA with \( f_{1F} = 54.16 \text{MHz} \) and \( f_{1F} = 103.1 \text{MHz} \)](b)

Figure 7.3: Out-of-band blocker bands identified as potentially dangerous for WCDMA with \( f_{1F} = 54.16 \text{MHz} \) 7.3(a) and \( f_{1F} = 103.1 \text{MHz} \) 7.3(b)

These results are obtained from scratch in only few seconds [56, 57] and provide very valuable information to RF systems engineers. They provide a starting point
Figure 7.4: Signal levels along the blocks (1 RF filter, 2 LNA, 3 Mixer, 4 IF filter, 5 VGA, 6 ADC). The WCDMA signals shown in 7.4(a) correspond to: + $P_{\text{max}}$, ◦ $P_{\text{min}}$, * Adjacent Channel at 5 MHz offset, x Adjacent Channel at 10 MHz offset, □ Adjacent Channel at 15 MHz offset, ◊ Out-of-band Blocker at 15 MHz offset, ▽ Out-of-band Blocker at 60 MHz offset, △ Out-of-band Blocker at 85 MHz offset, ★ Noise Floor. The WLAN signals shown in 7.4(b) correspond to: + $P_{\text{max}}$, ◦ $P_{\text{min}}$, * Adjacent Channel at 25 MHz offset, ★ Noise Floor.
7.2. **Budget Design**

Table 7.2: Specifications and performance of a typical run for a WCDMA/WLAN multi-standard receiver.

<table>
<thead>
<tr>
<th>Standard Parameter</th>
<th>WCDMA</th>
<th></th>
<th></th>
<th>WLAN</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$DR_{ADC}(dBm)$</td>
<td>60</td>
<td>50.65</td>
<td>49</td>
<td>44.33</td>
<td></td>
</tr>
<tr>
<td>$ENOB_{ADC}$</td>
<td>10</td>
<td>8.12</td>
<td>8</td>
<td>7.07</td>
<td></td>
</tr>
<tr>
<td>Gain($dB$)</td>
<td>-</td>
<td>69.05</td>
<td>-</td>
<td>66.36</td>
<td></td>
</tr>
<tr>
<td>$NF(dB)$</td>
<td>9</td>
<td>6.06</td>
<td>11</td>
<td>7.85</td>
<td></td>
</tr>
<tr>
<td>$IIP_3(dBm)$</td>
<td>-17</td>
<td>-15.68</td>
<td>-5</td>
<td>-4.88</td>
<td></td>
</tr>
<tr>
<td>$IIP_2(dBm)$</td>
<td>14</td>
<td>27.02</td>
<td>23</td>
<td>27.92</td>
<td></td>
</tr>
</tbody>
</table>

Table 7.3: Parameter distribution for the proposed WCDMA/WLAN multi-standard receiver.

<table>
<thead>
<tr>
<th><strong>WCDMA</strong></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter</td>
<td>RF filter</td>
<td>LNA</td>
<td>Mixer</td>
<td>BB filter</td>
<td>VGA</td>
</tr>
<tr>
<td>Gain ($dB$)</td>
<td>-2.9</td>
<td>16</td>
<td>3.4</td>
<td>-2.6</td>
<td>55.2</td>
</tr>
<tr>
<td>NF ($dB$)</td>
<td>2</td>
<td>2.4</td>
<td>6.2</td>
<td>11.1</td>
<td>11.5</td>
</tr>
<tr>
<td>$IIP_3(dBm)$</td>
<td>4</td>
<td>0.8</td>
<td>2.6</td>
<td>-4.1</td>
<td>5.1</td>
</tr>
<tr>
<td>$IIP_2(dBm)$</td>
<td>40</td>
<td>35</td>
<td>55</td>
<td>45</td>
<td>50</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>WLAN</strong></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter</td>
<td>RF filter</td>
<td>LNA</td>
<td>Mixer</td>
<td>BB filter</td>
<td>VGA</td>
</tr>
<tr>
<td>Gain ($dB$)</td>
<td>-2.9</td>
<td>14.9</td>
<td>3.4</td>
<td>-2.6</td>
<td>53.54</td>
</tr>
<tr>
<td>NF ($dB$)</td>
<td>2</td>
<td>2.9</td>
<td>7.6</td>
<td>14.5</td>
<td>14.7</td>
</tr>
<tr>
<td>$IIP_3(dBm)$</td>
<td>13.8</td>
<td>11.4</td>
<td>12.8</td>
<td>13.8</td>
<td>14.1</td>
</tr>
<tr>
<td>$IIP_2(dBm)$</td>
<td>40</td>
<td>35</td>
<td>55</td>
<td>45</td>
<td>50</td>
</tr>
</tbody>
</table>

from where the receiver specs can be readjusted using more accurate models for the receiver blocks as they are available. In order to ease the step to lower level models an interface between ADIS and TACT is under development so that the use of these tools can be integrated in a single design flow. This combination of tools at different levels is a powerful way of achieving a good architectural design at an early stage in the design cycle allowing for a very fast time-to-market.
Chapter 8

Conclusions

The integration trends imposed by the market push towards the Software Radio (SR) paradigm, 4G radio receivers where different wireless standards converge make RF engineers face harder and harder challenges. EDA tools come to the rescue facilitating the design of multi-band, multi-mode receivers at different levels. EDA tools will definitely play an increasing role in design and verification of wireless systems.

Advances in technology allow for ever increasing integration levels leading to System-on-Chip (SoC) solutions. This, combined with low power circuit techniques, leads to very compact systems with low power consumption. This bargain does not come for free, though. Increased complexity levels and reliability issues are some of the “side-effects” the race for a true single chip radio brings along. Design for manufacturability is a must in present systems. Using EDA tools at different abstraction levels allow to apply the “divide and conquer” strategy to the problem of designing receivers suitable for 4G wireless.

The overview of the design considerations given in Chapters 1 and 3 shows that designing a multi-standard wireless communications receiver is not an easy task. The drawbacks of the traditional approach, illustrated in Chapter 3, justifies the need for an automated methodology that addresses the problem.

A design and optimization methodology that can be used for system level specification of wireless communication receivers for both the multi-standard and the single-standard case has been proposed in this thesis. This methodology has been implemented in a tool called TACT, a multi-standard RF Transceiver Architecture Comparison Tool.

TACT is an attempt to map the know-how of an experienced RF system designer into a CAD tool that facilitates the design-space exploration at the system level. The use of this tool/methodology helps RF engineers in the design-space exploration of frequency plans and receiver budgets for different receiver architectures.

The focus of the proposed methodology is to meet or exceed specs without overdesigning the receiver blocks while fostering hardware shareability. This tool
can be employed for educational, research and industrial purposes.

TACT is a modular tool. Each sub-tool can be used independently or as part of the TACT simulation flow as shown in Chapter 4. The two operations that lay the foundation of the design methodology are the frequency plan evaluation and the budget design and optimization.

The frequency planning algorithm used in TACT evaluates the possible on-chip frequency plans providing designers a valuable insight on the implications of choosing a particular intermediate frequency. The performance of each frequency conversion setting is measured in terms of its degree of freedom from interfering signals. One of the main contributions of this thesis is the introduction of the out-of-band blockers in the performance evaluation. This allows to choose a frequency plan which is less stringent with the filter specs while keeping an as high as possible immunity to interferers.

The results of this frequency planning algorithm are combined with the budget tool in order to provide full radio receiver specs for the different wireless communications standards specifications.

The budget design algorithm is simulated annealing based. The developed impact oriented parameter distribution allows for a faster convergence of the algorithm while serving the purpose of not setting too tough requirements in blocks where it is not needed.

TACT is also a hierarchical tool. Using high level models at the beginning of the design process narrows down the search space with a very small time penalty. The next step is to focus on this handful of solutions and explore them more thoroughly using more elaborated models. The interface with ADS which is under construction will help increasing the access to lower level models of the blocks. This may help reducing the number of design iterations and silicon spins and, consequently, the time-to-market.

The usefulness of the proposed methodology is illustrated in a case study of a programmable multi-standard WCDMA/WLAN receiver for fourth generation (4G) wireless in Chapter 7.

8.1 Status of the Project and Future Work

The full methodology for the automatic design-space exploration of integrated multi-standard wireless radio receivers has been devised. The foundation of TACT has already been laid. Both the frequency planning and budget design and optimization tool are up and running. It is now time to deepen in the different aspects that affect TACT’s performance and to incrementally build its remaining components. A thorough study of the impact of the different parameters that steer the design-space exploration is yet to be done. This study will hopefully lead to better performance of the tool. New optimization techniques such as genetic algorithms will be included in TACT.
Both the Graphical User Interface (GUI) and an interface with ADS are under construction. The later will allow to include a larger number of block models and help verifying the validity of TACT. The construction of a physical demonstrator that will ultimately verify the tool is planned.
Bibliography


