Evaluation of Chemical Mechanical Planarization Capability of Titan™ Wafer Carrier on Silicon Oxide

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Abstract

Chemical mechanical polishing (CMP) has emerged as a critical technique for the manufacture of complex integrated circuits to achieve low surface roughness and high degree of planarization. In particular, the continuous progression of the wafer carrier has been driven by the interest of diminishing the waste on a wafer by reducing the edge of exclusion area, and hence, increasing the amount of chips per wafer. In this thesis, a standard wafer carrier and the state of the art Titan™ wafer carrier are compared and evaluated by planarizing a set of blank wafers with a PECVD oxide film on an IPEC 472 CMP tool. The surface roughness was analyzed before and after the planarization step using an atomic force microscope (AFM) and the nonuniformity across the wafer was characterized by ellipsometry. The material removal rate and the reproducibility of the nonuniformity from wafer to wafer was also observed and compared. A second set of experiments with patterned wafers planarized with the Titan™ carrier was also performed. The impact of the pattern density in the step height reduction ratio and surface roughness was analyzed with AFM. The results obtained from the blank wafers planarized with the standard wafer carrier showed a nonuniformity average of ± 6.96% with a 3 mm edge of exclusion, a wafer to wafer nonuniformity of ± 4% and a surface roughness of 0.34 nm. However, the Titan™ carrier delivered a nonuniformity average of ± 2.17%, a wafer to wafer nonuniformity of ± 0.3% and a surface roughness of 0.22 nm. The Titan™ carrier outmatched the standard wafer carrier forcing it to shift the edge of exclusion area to 7mm to be able to achieve a nonuniformity of ± 2.90%. The results for the set of patterned wafers showed a step height reduction ratio (SHRR) average of 98.35%. The surface roughness for the oxide above the patterned polysilicon structures decreased from 9.46 nm to 0.33nm and the surface roughness on the recessed areas decreased from 3.70nm to 0.7nm.
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List of Acronyms

AFM  Atomic Force Microscopy
BCD  bulk chemical distribution
CMOS complementary metal-oxide semiconductor
CMP  Chemical Mechanical Planarization
CoO  cost of ownership
CTR  Compact Thermal Reactor
DI   deionized
DWI  dry-wafer-in
DWO  dry-wafer-out
EFF  Planarization Efficiency
ICs  Integrated Circuits
ILD  Interlayer Dielectric
IMD  Inter Metal Dielectric
IT   Inner Tube
LPCVD Low Pressure Chemical Vapour Deposition
MRR  Material Removal Rate
NU   Nonuniformity
PAC  Photoactive Compound
PECVD Plasma Enhanced Chemical Vapour Deposition
PLC  Programmable Logic Controller
PMD  Premetal Dielectrics
**List of Tables**

**PVA** polyvinyl alcohol
**RIE** Reactive Ion Etching
**RR** Retaining Ring
**SEM** Scanning Electron Microscope
**SH** Step Height
**SHRR** Step Height Reduction Ratio
**STD** standard deviation
**STI** Shallow Trench Isolation
**TTV** Total Thickness Variation
**UV** Ultra Violet
**WG** wafer guide
**WIWNU** Within-wafer Nonuniformity
**WTWNU** Wafer-to-wafer Nonuniformity
Chapter 1

Introduction

Today’s manufacture of advanced Integrated Circuits (ICs) require global planarization of interconnects and flat wafer surfaces; hence Chemical Mechanical Planarization (CMP) has evolved into an extensively used technique to achieve the aforementioned planarity [1, 2, 3, 4]. In the CMP process, the material removal takes place by pressing a wafer against a pad at two different rotational speeds in order to reduce the surface roughness [5]. Nonetheless, the main drawbacks of CMP are the Within-wafer Nonuniformity (WIWNU) or the roughness variation across a single wafer and Wafer-to-wafer Nonuniformity (WTWNU), this is, the reproducibility of the same results between wafers and from batch to batch. This mainly derives from the relative velocities at different points on the wafer and due to the Von Mises effect which is an axial stress [6].

Moore’s law states that the number of transistors per area doubles every two years [7], [8], [9]. The reduction of structure dimensions in the ICs has led to increase the number of transistors hence achieving a higher performance in IC chips. Consequently, the multilevel interconnection requires a higher degree of planarization [10]. This thesis focuses on the evolution of the CMP instrument over time, the planarization process and the performance of the state of the art CMP wafer carrier Titan™ where the edge effect, WIWNU, WTWNU and planarization degree are analyzed and compared to a third generation carrier.

1.1. Background

Planarization processes are governed by the wafer carrier, this is, the most critical component of a CMP tool designed to hold and press the wafer against the polishing pad. Ideally, after planarizing a wafer, the conformal coverage step caused by any deposition technique is removed and the uniformity across a wafer kept to ±0% across the whole wafer. However, the influence that the design of formers wafer carriers has on the Nonuniformity (NU) generates an extensive deviation at the edge from the rest of the wafer. This region where the NU varies consistently from the rest is know as the edge of exclusion area. The wafer yield is related to
the edge of exclusion area, where a larger area deliver less amount of structures and vice versa.

![Diagram](image.png)

Figure 1.1: Cross-section of a planarized wafer from its center or origin towards the edge. For the first and second generation carriers, the amount of material removed on the center is considerably larger than at the edge. However, the ideal wafer carrier keeps the NU at ±0% across the entire wafer.

Reducing the cost of ownership (CoO) by increasing the yield on a wafer starts by reducing the edge of exclusion area and hence redesigning the mechanism of the wafer carrier in order to achieve an ideal NU value.

### 1.2. CMP Equipment

The CMP process began aiming to enhance local and global planarization to improve lithographic and metal interconnect accuracy. The yield enhancement delivered by the CMP led to its use in applications such as Interlayer Dielectric (ILD), tungsten plugs and damascene processes. By the end of the 90’s, CMP was used in regular production in more than 40 companies [11]. However, the main problem for the semiconductor industry relied on the CoO [12], the lack of CMP integration and process knowledge. CMP tools have evolve with the scope of reducing the CoO by integrating in-situ steps such as film thickness metrology, post-cleaning steps and especially by optimizing the throughput [13].

There were several approaches to obtain a high wafer throughput: i) depositing less material in former steps, ii) increasing the mechanical wafer handling efficiency, iii) increasing the polishing removal rate, iv) increasing the number of wafers being polished at once, or v) optimizing the process parameters (down force and relative
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velocity).

The evolution of the CMP tool has overcome some of the former drawbacks by
for instance polishing several wafers on one platen at once, or by improving the
Material Removal Rate (MRR), the wafer handling or by adding in-situ metrology
to save process time [11].

1.2.1. First Generation CMP Tools

First generation tools usually have two rotating platens of 22 inches each in size
[11], [14]. For different step processes, one of the platens is mounted with a hard pad
for bulk removal (improve planarization) and the other platen with a soft pad for
buffing (improve NU). The wafer handling through the tool is operated by a single
multitask robot which also holds the wafer on the head carrier with the device side
towards the platen. During the process, the slurry is dispensed near the center of
the platen and distributed across the polishing pad with help of the centrifugal force
and the grooves patterned on the surface of the pad. The head carrier presses the
wafer against the rotational pad on the platen and by the interactions between the
slurry (chemistry and abrasives) and the pad (i.e., roughness, hardness) the surface
roughness of the wafer is reduced and the step height planarized.

First generation tools have several limitations. The lack of a slurry reprocessing
unit implies that when the slurry is delivered and expelled out of the platen due to
the centrifugal forces, it is discharged and wasted. Consumables in the CMP process
such as slurry, pads, DI water or test wafers increase the CoO. A small fraction
of the slurry distributed across the platen is in direct contact with the wafer and
used for the purpose of planarizing, the remaining non-used slurry is discharged.
Reprocessing systems where the slurry is recovered, chemically rejuvenated and
filtered for its reuse would imply a cut in the CoO and the next step towards
CMP integration. Another limitation was the platen wobbling under high rotational
speeds. In order to achieve higher MRRs, the platen speed is maxed out while
avoiding its run-out and impact in the final NU [15].

First generation tools require to keep the batch of wafers soaked on water until
the whole batch is polished to decrease the wafer defectivity. The main idea, is to
avoid the slurry, wafer and pad residues to dry on the wafer surface.

1.2.2. Second Generation CMP Tools

Second generation tools introduced some variations within rotatory carriers and
platens. Efforts to reduce the CoO by increasing the throughput led the industry
into two types of designs; i) the multiwafer per platen in which several wafers
are polished on a large pad (22 inches) at the same time; and ii) the sequential
multiplaten system. The polishing rate in this type of tools is enhanced by polishing
the wafers at the edge or corner of the platen taken advantage the larger relative
velocities found at a displacement from the center (origin) of the platen. Some of
these systems have already the possibility of being linked to a post-CMP cleaning step.

Multiwafer per platen

The multiwafer per platen tool comes with several head carriers to planarize various wafers at once thus increasing the throughput [16]. The drawback of this tool is that while polishing several wafers (i.e. 4 wafers at a time) if one breaks, all the shattered pieces will scatter across the polishing pad scratching the remaining wafers. The load balance while working with several wafers at a time can be another drawback. For instance, while working with a lot of twenty-five wafers and polishing 4 at a time, this leave one wafer left at the end of the lot. The pad wear behaves differently when planarizing one wafer than when planarizing four at once, hence the processing results may differ regarding the NU from wafer to wafer.

Multistep rotational systems

The multistep platen has the ability of assigning different tasks to each platen and at the same time avoiding the risk for damaging several wafers at a time [17]. In a three step tool, one of the platens can be used for removing bulk material without any care of scratching the surface. The next platen can be used to optimize the planarity and the last platen as a buff step to polish the surface removing final scratches. Nonetheless, this type of tool has also several drawbacks including; i)
the throughput is limited by the slowest step. If one step is slower than others, it
creates the bottleneck effect, ii) if one of the pads is damaged, all the pads have
to be changed as it is not possible to identify the pad causing the problem and
iii) if one of the platens is down, the whole process will be stopped decreasing the
throughput.

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1.2.3. Third Generation CMP Tools

The focus of improvement for the third generation tool is to enhance the relative
velocity by improving the pad-wafer motion and the slurry delivery to the pad-wafer
interface. The dry-in-dry-out feature is also present in this generation reducing
wafer defects caused by the corrosion of the metal from the CMP metal process.
Two different tools appeared in this generation and were classified depending on the
movement of the polishing pad, either linear or orbital [11].

Linear polishers

Linear CMP toolshave a polishing pad attached to a continuous belt that works
as a caterpillar track. The belt reaches higher relative speeds than in previous
generations enhancing the removal rate [18]. The process is similar to the second
generation multiplaten tools in which two stations are used, one for bulk removal
and the other one for buffing.

Orbital polishers

Orbital polisherscomes in different concepts: in some tools, the wafer carrier
orbits while the platen rotates; in others, the platen orbits while the carrier rotates;
or the platen is completed fixed while the carrier orbits.

Orbital polishers have the ability of achieving uniform relative speeds with small
circle movements at any point in the wafer maintaining a low NU profile [18]. Besides
the NU, these tools can achieve high level of planarization used with a polyurethane
pad and at low down force. The orbital motion of the pad favors the slurry distri-
bution directly into the wafer as long as the pad has Cartesian grooves.

An introduced advantage in the third generation tools is the use of a double
air bladder. One bladder located at the back of the wafer in the head carrier [19]
and the other one in the back of the platen [20]. During the polishing process, the
wafer, held by a Retaining Ring (RR), is flattened by increasing or decreasing the
air bladder on the carrier before being in contact with the pad. Alternatively, the
bladder on the platen allows to lift specific locations on the pad to counteract the
effect of polishing faster at the edges of the wafer. The uniformity at the exclusion
edge can be improved by controlling the pressure difference between the pad and
the RR [19].
CHAPTER 1. INTRODUCTION

Pad feed polishers

The pad polisher feed has the same mechanism as a camera film rolls forward after every picture. After polishing a wafer, the pad roll moves forward so the next wafer can be polished with a fresh pad. The drawback of this mechanism is that the pad characteristics have to be consistent from the beginning to the end. The advantage of this tool is that if the roll is long enough, there is no need of changing pad as often as in other systems reducing the amount of tool qualification performed after every pad change [11].

Rotatory inverted

Nikon Corporation inverted the CMP system by placing the device side of the wafer up and this time, the polishing pad approaches the wafer [21]. Head carrier speeds on these tools are up to 8 times faster than in conventional systems allowing to keep higher polishing rates meanwhile keeping a low pressure (higher platen and pad speeds with the addition of low pressure/down force leads to an increase in the NU profile). The advantages found in this system are several; the polishing pads are smaller in size (i.e., for a 200 mm wafer, the pad is 150 mm), this fact helps to keep the footprint of the tool considering that for a conventional tool, in a 300 mm wafer, a 600 mm pad is required; the slurry is directly supplied from the pad into the wafer so the waste is considerably reduced [22].

1.2.4. Wafer Carrier

The wafer carrier or head carrier (Figure 1.3) is the most critical component of the CMP tool. The main function of the carrier is to hold the wafer with the use of vacuum during planarization to keep it on place and with either a RR or a wafer guide (WG), depending on the generation tool, to avoid its dislodgement. Carriers have two requirements to fulfill: i) the planarized wafer must be flat within a certain specification excluding the edge exclusion region; and ii) they have to be able to planarize a vast range of films with different ranges of film stress [5].

![Figure 1.3: First and second generation carrier types: A) Gimbaled; B) Multizone membrane; C) Direct air-pressure [19].](image)

The edge of exclusion region is the area of the wafer where the MRR deviates from the rest of the wafer. The edge of exclusion arises from the interactions be-
1.2. CMP EQUIPMENT

tween the carrier and the pad (i.e. relative velocity, Von Misses effect, design and mechanics of the head carrier).

Film stress makes CMP process challenging as it causes the wafer to deform and change the pressure distribution at the wafer-pad interface. Those changes in pressure will cause a variation in the planarization rates across the wafer increasing the NU. The film stress tends to vary depending on the deposition technique and the type of film being deposited. Depending upon the lattice mismatch between films, the stress can be either tensile or compressive. The effect of having a tensile stress is that the wafer edges will bow up and the center of the wafer will be planarized slower than the edges. On the other hand, if the stress is compressive, the center of the wafer will bow up and it will be planarized faster than the edges. One main feature of the head carriers is the possibility of applying a zonal back pressure to try to flatten the wafer without cracking it [23].

Former Carriers

Former carriers such as the one in Figure 1.4 uses a wafer guide to hold the wafer. The distance between the wafer guide and the wafer should be as narrow as possible to avoid nonuniform pressure distribution on the wafer, however the gap is in the range of 0.5 to 1.0 mm [19]. The backing film located right behind the wafer has holes on it varying from a dozen to several hundred. High pressure fluid is delivered directly on the back of the wafer through this holes to increase the polishing rate and improve the uniformity therefore, the more holes, the higher the pressure hence, the higher the planarization rates.

Two zone carriers as the one shown in Figure 1.5 have two main features; i) a membrane divided in multiple zones to apply individual pressure (pneumatic or hydraulic) to different radial positions at the back of the wafer and ii) a RR which
besides using it to avoid the dislodgement of the wafer, it can apply pressure onto the polishing pad completely independent from the back of the wafer.

\[8 \text{ Shaft} \]
\[7 \text{ Holes} \]
\[6 \text{ Carrier head-2} \]
\[5 \text{ Carrier head-1} \]
\[4 \text{ Retainer ring} \]
\[3 \text{ Membrane} \]
\[2 \text{ Wafer} \]
\[1 \text{ Pad} \]

Figure 1.5: Two zone control carrier (Adapted from [25]).

The gap between the wafer and the RR is also in the range from 0.5 to 1 mm [19]. However, the RR helps to distribute the pressure across the wafer improving the removal rate uniformity at the edge area. The membrane located at the back of the wafer is made of an elastic rubber divided into multiple zones. Through the shaft and the holes (Figure 1.5), an independent back load can be supplied to a specific area giving the possibility of controlling the planarization rate. Measuring the deposition distribution and adjusting the back pressure to specific areas can make a big improvement in handling the WIWNU.

Three Zone Control Carriers

The design of this type of carrier has the ability to deliver independent pressure to different areas; the flexible back membrane located at the back of the wafer which in its turn it has several areas where pressure can be applied independent of each other; the inner ring or Inner Tube (IT) membrane that is surrounding the wafer edge and at the same time its lower side is in contact to the polishing pad exerting pressure; and the outer ring or RR which can apply a down pressure against the pad.

Figure 1.6 shows a schematic of a three zone carrier. The gimbal mechanism located between the loading chamber and the back membrane allows the carrier (base assembly) to follow the wafer topography when in contact to the polishing pad while rotating with help of a shaft. The loading chamber has several purposes; it applies a downward pressure to the base assembly and sets the vertical distance between the base assembly and the polishing pad. The wafer, fixed by a vacuum clamping system at the base assembly is also held at its edge by the IT on its inner side. The upper side of the IT is connected to a flexible membrane that if pressure is applied, it can be displaced vertically up and down providing extra control at the edge of the wafer. The RR, located surrounding the IT with its interior part and it is in contact to the polishing pad with its lower side, can also apply a downward pressure on the pad. The upper part of the RR is made of a metallic material and
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Figure 1.6: Schematic of a three zone control carrier with a back membrane, inner tube and retaining ring. (Adapted from [26]).

the lower part which applies the pressure onto the pad is made of a plastic material. The fact that the IT is very narrow, it allows the RR to be close to the wafer edge allowing to control the pressure distribution across the wafer.

The design of the Titan™ wafer carrier shown in Figure 1.7 introduced by Applied Materials and Axus Technology with a zone control pressure; a RR pressure, a IT pressure and the membrane (MM) pressure falls under this category.

Figure 1.7: Titan™ wafer carrier (Courtesy of Axus Technology).

Head carrier designs and their impact in the edge of exclusion area

During the planarization process, the head carrier presses the wafer against the pad compressing it. The pressure exerted on the wafer by the pad while recovering its original shape varies due to the design of the head carrier. Figure 1.8 shows the
head carrier design for a 1st- (Figure 1.8a) and 3rd generation tool (Figure 1.8b). For the first generation carrier, the back load of the wafer dents the pad forcing it to recover its original shape creating an intense load at the edge of the wafer thus increasing the MRR at that location. The design of the 3rd generation carrier comes with the inclusion of a RR to reduce the intense load at the edge of the wafer. Now, the pressure exerted by the pad is distributed between the wafer and the RR reducing the MRR at the edge of the wafer.

The RR becomes an improvement to reduce the edge of exclusion area however, the design for the 3rd generation carrier leaves an empty space or gap between the wafer and the RR of 0.5 to 1 mm. The lack of pressure at the gap originates a pad rebound effect increasing the pressure some millimeters away from the edge of the wafer (Figure 1.9) inducing a higher MRR. However, when the pad bounces off of the edge causes a lower pressure effect at the adjacent region decreasing the MRR [11].

Figure 1.8: Schematic of 1st and 3rd generation head carriers

Figure 1.9: Pad rebound effect (rabbit-ear shape) on a wafer planarized in a 3rd generation carrier. 49 points scan across a 100 mm diameter wafer.
1.2. CMP EQUIPMENT

1.2.5. Platen

The mere purpose of the first and second generation platens were to be used on hard pads to achieve a surface as flat as possible to press the wafer against. However, the platen has also evolved through time, and its functions have increased from a simple rotatory table to features such as temperature control, pressure control and slurry delivery routing.

Temperature control

Platen features such as temperature control gives extra room for process improvement as the chemical component of the slurry can be manipulated by heating it up or cooling it down. An increase in temperature leads to an increase in the chemical reaction rate and therefore higher MRR. The drawback of increasing the temperature is that the pad wear will also increase shortening its lasting life. However, softening and deforming the pad leads to an improvement in the uniformity though with the trade-off of worsening the surface planarity. Alternatively, decreasing the platen temperature makes the pad stiffer, there is less deformation, hence improving the planarity but risking to remove more material than necessary from some locations [27]. There are different ways to achieve the temperature control, i) controlling the temperature of the slurry before being dispose into the pad, ii) inserting a channel in the platen where controlled heat fluid flows through and iii) building a heating device in the wafer carrier and control the temperature on the back of the wafer [28].

Direct slurry delivery

The slurry delivery through the platen occurs on orbital polishers allowing the direct delivery on the surface of the wafer. The slurry is delivered through holes in the platen and between the grooves of the polishing pad enhancing the slurry distribution across the wafer [29].

1.2.6. Pad Conditioner

In order to maintain a consistent process, the pad conditioner is used to re-vitalize the polishing pad either in between wafers or in situ. While planarizing, the interaction at the wafer-pad interface generates residues coming from different sources; i) from the material removed form the topmost layer of the wafer, ii) cluster formation due to the agglomeration of the abrasive particles contained in the slurry and iii) from the polymer material of the pad that becomes abraded [30]. These materials combined will fill the pores of the pad making its surface smooth and reducing its capability of planarizing. Besides reducing the MRR, the ability to distribute the slurry through the pad grooves will also decay.

The pad conditioner is made of a diamond-coated disk which is pressed against the polishing pad. It rotates around its own axis and it moves radially across the
pad. The purpose of the diamond is to scratch the outermost layer of the pad to remove the accumulated material inside the pores and retrieve higher and constant MRR. The impact in the process of the absence of the pad conditioner leads to a constant decrease in the planarizing rate. However, it allows the user to modify the pad profile by conditioning certain regions for longer or lesser period of times hence, improving the NU.

1.2.7. CMP Equipment Integration

From the moment a batch of wafers is loaded in a CMP tool, this is soaked in deionized (DI) water and it remains wet until the whole batch is processed and ready for post-CMP cleaning. Prior planarizing a whole set of wafers with a specific recipe, a single monitor wafer has to be planarized, cleaned and measured to see if the recipe used fulfills the required specifications before planarizing the remaining batch. Besides the addition of the cleaning step, the assurance of the final quality of the process requires a reliable and continuous slurry distribution by adding slurry distribution systems.

First generation tools came with a narrow set of functions which were entirely reduced to the single task of planarizing. So in order to reduce the cost of the CMP process, the tool evolution has been oriented to increase the quality and reliability of the wafers by integrating bulk chemical distribution (BCD) and reprocessing systems, speed up the process time and efficiency by adding metrology equipment into the CMP tools and introducing the dry-wafer-in (DWI) - dry-wafer-out (DWO) concept by integrating cleaners. The DWI-DWO merely consists of having an incoming wafer dry, and after being process, it leaves the CMP processed dry after a cleaning step [31].

Slurry reprocessing system

Slurries are classified into three categories, silicon, oxide and metal. For silicon and oxides, the type of abrasive particles are reduced to silica or alumina. However, for metal polishing it is required to apply a specific slurry for each specific material.

Slurry variables such as pH, or flow rate have a direct impact in the effectiveness of the CMP tool. The use of slurry as a consumable is highly costly and it is required to achieve a fine process (low NU). The slurry is continuously distributed into the center of the platen and by the rotation of the polishing pad, the centrifugal forces spreads the slurry across the wafer, flings off at the edge of the platen and is carried away by the drain system. The flow rate, depending on the process, tends to vary from 20 ml/min to 500 ml/min making some processes to increase the CoO. CMP tools where the slurry has been tossed have systems to recover the slurry, treat it chemically, filter it and send it back to the dispenser. This process of rejuvenating the slurry reduces the waste by consuming one-fifth of what it would have been if compared with CMP tools without reprocessing units [15]. Temperature, pH and conductivity of the rejuvenated slurry is monitored to be able to be adjusted to
1.2. CMP EQUIPMENT

the standard slurry solution. In order to prevent contamination, a small percentage of the rejuvenated solution is sent through pH and conductivity sensors controlled by a Programmable Logic Controller (PLC) to avoid contacting with the platen [15]. Tools such as the Speedfarm IPEC 372 or the IPEC 472 used during the experimental part have the aforementioned slurry reprocessing system.

Post-CMP cleaning integration

The Post-CMP cleaning step has evolved with different generation tools starting from being treated as an independent step in the first generation tools as being a part of the overall process.

Cleaning integration arises from the need of not letting the slurry dry on the wafer. So in order to prevent it, it is favorable to include pre-cleaning, rinse and buffing steps after bulk CMP removal. Besides keeping the wafers wet, it is important to anticipate to other factors that will favor or minimize the labor of the cleaning step, such as the selection of the particle size. Smaller particles have higher electrostatic forces leading to higher efforts to remove them. Or if a high level of roughness is added to the size of the particles, the sites at which the particles can adhere will increase [32].

Figure 1.10 shows an schematic of the cleaning mechanism of an OnTrak DSS cleaner which basically consists on a couple of polyvinyl alcohol (PVA) brush rollers rotating and scrubbing both surface and back side of the wafer to remove particles.

Figure 1.10: Post-CMP double side roller brushes [11].

Metrology

Quality control while maintaining a high throughput requires in situ metrology methods that allows the user to reduce the planarization and characterization time of a monitor wafer. There are two methods for metrology: wet and dry. Wet measurements are performed right after planarizing a wafer by bathing it in DI water and measuring the remaining material using software pattern recognition. The dry
measurements follow the same method as the wet technique except that the wafers have gone through a cleaning step and are measured on air. Both methods have pros and cons, for instance, wet measurements avoid inclusion of contamination as for dry measurements, the difference of refraction index between the air and the oxide layer is greater than the one between the oxide and the water.

Top manufacturer Nova® Measuring Instrument Ltd. provides optical techniques such as scatterometry capable of analyzing changes of the diffracted light out of a sample to measure its dimensions.

1.3. Slurry

Since the arrival of the CMP technique to the IC manufacturing, more and more applications have been suitable for its use. CMP can be used for Shallow Trench Isolation (STI), ILD, Premetal Dielectrics (PMD) and all type of damascene processes. As different applications require different specifications, trying to understand if one application can be suited for another requires knowledge about slurry behavior and the impact in the applied material as this will be chemically affected. The slurry is made of two components, the abrasive particles and a solution; and depending on the type of particles, solution and the synergy between them, the slurry will behave differently [33].

1.3.1. Abrasive Particles

There are different kind of abrasive particles in the market such as cerium oxide, zirconium, diamond or multiparticle blend but the two most common base materials are silica ($\text{SiO}_2$) and alumina ($\text{Al}_2\text{O}_3$). Before the abrasives are blended in the solution, they are ultrapure (> 99.99%) [33], white powders with a uniform size and shape. The particle size distribution has to be tight to ensure a constant planarization rate and to avoid larger particles that can become a source of scratches.

Oxide slurry

For oxide CMP, only silica is used which the particle size is between 10 – 100 nm [34]. There are two types of silica, fumed and colloidal. Fumed silica is manufactured by oxidizing chlorosilane ($\text{SiCl}_4$) in a blaze at 1800°C [33]. Its shape tends to be irregular due to its crystallization in the gas phase making its use a risk for inducing scratches. Having said that, colloidal silica, synthesized in the liquid phase, is made by blending water with either sodium silicate ($\text{Na}_2\text{SiO}_3$) [35] or sodium metasilicate ($\text{Na}_2\text{H}_2\text{SiO}_3$) [36]. The reaction will form and suspend the crystals at the same time. The spherical shape and its tight particle distribution makes colloidal silica the most common abrasive base material to be found in the market.
1.3. SLURRY

Metal slurry

Metal slurry is made by blending different types of abrasives in the same mixture. By doing so, the particle size will vary between abrasives but for metals, the oxidizer has a more important role. Once the oxidizer is determined for a specific application, the abrasives can be chosen to fit with the solution. For tungsten and nickel applications, aluminum oxide is the most common abrasive in the market. In the case of aluminum sulfate \( \text{Al}_2(\text{SO}_4)_3 \), this is precipitated together with ammonium sulfate \( (\text{NH}_4)_2\text{SO}_4 \) and then filtered and calcined [33].

Agglomeration

Since the slurry is contained in barrels without any kind of re-dispersion systems, after a period of time (up to a year for most of the slurries [37]) the particles may precipitate and form aggregates and agglomerate. As the abrasive particles are not synthesized as single particles, aggregates may also appear due to chemical and physical forces that attract each other becoming big clumps with catastrophic effects as they may cause scratches. Adding either a milling or a filtering step can solve this problem. If the problem is spotted at the particle synthesis step, milling is the right process to prefer but if the problem appears at CMP processing, the use of filters can save the expenses from discarding a whole barrel of slurry.

1.3.2. Slurry Solution

The slurry solution has two different roles depending upon the application: for oxides it behaves as a hydrolizer and for metals as an oxidizer. For ILD processes, oxide slurries are quite simple as the material to be removed is just oxide but for metal applications such as damascene processes the material will differ (i.e. titanium nitride, tungsten oxide) and the selectivity towards each material has to be optimized.

Oxide slurry

The solution of the slurry has two main purposes; i) the water component of the slurry will weaken the \( Si - O \) bonds and make the surface soft by hydration, and ii) to enhance the hydration rate by having a high pH value (oxide slurries in the market provide a pH value of 10 to 11) which in its turn will enhance the polishing reaction. The other benefit of a high pH value is to guarantee a dispersed and well suspended solution by increasing the repulsion between particles due to an increase in the zeta potential.

There are different types of chemistry oxide slurries available in the market, \( \text{NaOH} \)-based, \( \text{NH}_4\text{OH} \)-based and the \( \text{KOH} \)-based. \( \text{NaOH} \)-based slurry is cheap and stable but contains \( \text{Na}^+ \) ions which tend to migrate to the gate oxide and ruin the IC transistors. \( \text{NH}_4\text{OH} \)-based slurry is ion free but it is expensive and it has
an unstable suspension. The most popular slurry is the KOH-based because it is stable and the $K^+$ ion can be gettered [33].

Metal slurry

The challenges for the metal slurry solution (oxidizer) are to optimize the selectivity between different materials. Regarding different metals, the selectivity should be very equal but between metals and oxides, the selectivity should be as large as possible. Another challenge is to minimize the dishing or plug recession in patterned wafers.

The purpose of the solution is to oxidize the metal to soften it up so the surface can be easily removed mechanically. For instance, the idea in the case of tungsten slurries is to convert tungsten into tungsten oxide ($WO_3$). There are different ways to go for tungsten slurries, $Fe(NO_3)_3$-based, $KIO_3$-based, $H_5IO_6$-based and $H_2O_2$-based, and each of them has a different mechanism. The first three, the oxidizer will dissociate into ions and cations and the anions will oxidize the tungsten. For the remaining one, $H_2O_2$-based, the slurry will decomposes into $H_2O$ and dissolved $O_2$ to react with the tungsten [33].

1.4. Polishing Pad

Grinding a wafer in a accurate manner to obtain a uniform and planarized surface requires a degree of control and reproducibility given by the material and properties of the polishing pad.

1.4.1. Types of Pads

There are four types of pads depending on their structural characteristics: i) felts and polymer impregnated felts, ii) microporous synthetic leathers, iii) filled polymer films and iv) unfilled textured polymer films [38]. The properties that define the polishing pad are its thickness, compressibility and hardness. The compressibility measures how much of the volume of the pad is reduced by applying a uniform force across the body meanwhile the hardness of the material is characterized by a durometer test where the scale varies depending upon the force of the spring used to perform the measurement.

For oxide processes, such as $SiO_2$ removal, the Dow®IC1000™ belonging to the type III is the most common used in the industry. The IC denomination stands for a polyurethane cast filled with microporous which allows the pad to carry bigger volumes of slurry [39] and . One of its manufacturing processes is done by mixing a polyether-based liquid (urethane) with a curing agent and a pore forming agent at 66°C. The mixture is cast into a mold for 15 minutes till it becomes a gel. Afterwards, the mold is inserted in a curing oven for 5 hours at 93°C and then cool down for 4-6 hours until it reaches a temperature of 21°C. Then is the mold cut to
1.4. POLISHING PAD

form several polishing pads [40]. The resulting product has a compressibility below 2.5% and a hardness defined as shore D 57°.

1.4.2. Pad Influence in the CMP Process.

Pad-Wafer contact area

The applied load is transferred to the wafer through the asperities present in the polishing pad and the abrasive particles contained in the slurry (fluid layer). At low platen rotation speeds, the hydrodynamic pressure of the slurry is slow and the load is mainly coming from the pad asperities [41]. Vice versa, at high platen rotational speeds, the hydrodynamic pressure and the fluid layer will increase and become dominant. Briefly, wafer-pad interface is a balance between lubrication, solid-liquid or solid-solid interactions [42].

Experiments performed on the polishing pad Dow®IC1000TM at average contact velocities between 50 to 100 RPM have shown that the thickness of the lubrication layer is equal to the peak to valley roughness of the pad which is around 26µm [41], [43]. Experiments with minimum applied pressure to show the polishing capability of the lubricant layer have been performed [44] where the lack of material removal by the lubricant itself indicated that the asperity contact is the principal wear factor in CMP.

Pattern density influence

The contact area between the pad and a structure or topography may vary depending on the pattern density and structure dimensions (width and height). In an ideal CMP process, removing the unwanted topography is more favored than removing the material from a recessed area.

Figure 1.11: Effective contact width of a narrow and wider trench [41]

From the previous model [41], the spatial selectivity is determined by the radius \( \beta \) of the pad asperity. If the width of a trench is smaller than the critical dimension width (\( w_{cr} \)) shown in Equation 1.1, then the asperity will not be able to enter the
trench and only the material outside the trench will be removed.

\[ w_{cr} = 2 (2 \beta h - h^2)^{0.5} \]  \hspace{1cm} (1.1)

But for a trench with a \( w > w_{cr} \), then the asperity will be in contact with the bottom of the trench and remove its material. The effective width (\( w^* \)) at which the asperity is in contact to the bottom of the trench is determined by Equation 1.2.

\[ w^* = w - w_{cr} \]  \hspace{1cm} (1.2)

Summarizing, the selectivity towards protrusions is higher when \( w^* \ll w \) and lower or almost none when \( w^* \approx w \) [41].

1.5. Mechanics of the CMP Process

CMP process modeling and optimization requires an understanding of the mechanical and chemical interactions at the wafer-pad interface. However, there is no explicit literature available that describes the wafer-pad interfacial effects with process parameters. Some analysts assumed that the wafer hydroplanes while being polished and determine the Reynolds equation [42], [45]; others have stated that the wafer is in contact or partially in contact with the pad and ascribed the pad elastic modulus to the displacement of the pad and resolve the stress field [46]. However, due to the elastic deformation of the back film of the head carrier and of the pad, direct measurement of the film thickness is inaccurate [47].

1.5.1. Kinematics of a Rotatory CMP tool

Figure 1.12 shows a schematic with the interaction between the wafer and the pad for a rotational polisher.

The center of the wafer and the pad are denoted as \( O_w \) and \( O_p \) respectively and the angular velocities \( \omega_w \) and \( \omega_p \). The axes are normal to both surfaces and the distance between the two axes is denoted as \( r_{cc} \). If the rotational velocities of the platen and wafer are equal, this is, \( \omega_p = \omega_w \), then \( v_{x,R} = 0 \) and \( v_{y,R} = \omega_p r_{cc} \), indicating that the velocity of the wafer relative to the pad happens only in the \( y \)-direction but because the wafer rotates at a frequency of \( \omega_w / 2\pi \), the polishing is isotropic [47].

1.5.2. Contact Mode Analysis

The interfacial conditions between the wafer, slurry and pad can be analyzed as hydroplaning, contact or mixed mode.

Contact mode

The contact mode appears when the down force exerted by the carrier is high or the relative velocity is low. In this case, the influence of the slurry is discontinuous
1.5. MECHANICS OF THE CMP PROCESS

Figure 1.12: Schematics of the coordinate system for rotational CMP systems [48].

therefore the asperities of the polishing pad interact mechanically with the wafer surface deforming both surfaces at the contact site. Generally, at a microscale, all the surfaces have some roughness, therefore the real contact between the two bodies is a small fraction of the nominal area.

Figure 1.13: Forces exerted on a contact point during wafer-pad contact mode interactions. (* Notice that the gravity vector is pointing in the other direction thus, $F_N$ increases.)

A site or point in a circular motion as shown in Figure 1.13 has a changing velocity ($\dot{V}$) at a constant speed connoting that the acceleration of that point is centripetal ($\dot{a}_c = V^2/r$) therefore the centripetal force ($F_c = (V^2 \cdot m)/r$) exerted on the bodies towards their respective origins. The tangential (or linear) force ($F_T = a_T \cdot r$) which causes a deceleration at the contact point ($\dot{a}_T = \text{angular acceleration} \cdot r$) is responsible for the shearing of the surface asperities. The friction coefficient tends to be on the order of 0.1 [48].
CHAPTER 1. INTRODUCTION

Being the slurry discontinuous, meaning that it has no presence at the contact point, the normal force is sustained by the asperity of the polishing pad, therefore the only interaction during the process is mechanical.

Hydroplaning

The hydroplaning occurs when the wafer slides on the slurry without contacting the pad asperity (see Figure 1.14). This results either when the velocity is high or if the down force (carrier pressure) is low. During hydroplaning, the pressure gradient ($F_N$) is formed in the slurry to counteract the down force ($F_{carrier}$) of the carrier resulting in the shear of the contact part of surface wafer due to the frictional force of the abrasive particles.

Mixed Mode

The mixed mode occurs during the transition from the contact to the hydroplane mode, this is, either when the velocity is increased or the pressure decreased. In this case, neither the velocity is high enough nor the pressure is low enough to form a thicker slurry layer to counteract $F_{carrier}$ hence, some contact between the pad asperities and the wafer occurs.

1.5.3. Mechanics of Material Removal

Surface Melting

The heat generated at a contact point caused by the work done by the relative slide of the wafer and pad diffuses through that exact contact point. When the temperature at that specific point rises from the one in the bulk, it may be enough to soften or melt the contact surface and detach it from the interface. The wear happens when the melted point is spread over the surface and eventually leaves the interface.
1.6. POST-CMP CLEAN STEP

The slurry circulation on the polishing pad helps to remove the heat from the wafer interface keeping the bulk temperature below the melting point. However, as soon as the melted point moves to an adjacent location with a lower temperature, the point re-solidifies. This conclusion makes the surface melting mechanism not viable [48].

**Microcutting**

The microcutting mechanism occurs when the abrasive particles behave as single-point cutting “knives” to generate shallow grooves that penetrates under the surface. The hardness of these particles will determine the depth hence, the MRR and surface finish.

**Brittle Fracture**

When the radius of the edge of an abrasive particle is smaller than a critical value, the small-scale contact leads to fractures by plastic indentation in brittle materials.

**Burnishing**

Burnish occurs when the material is removed on a molecular scale from the higher locations on the surface by adhesive forces between the wafer and the abrasive particles [48].

1.6. Post-CMP Clean Step

The CMP process is a dirty step which leaves a considerable amount of residues coming from the removed materials, the slurry and the parasitic metallic contamination which can end up damaging the layer at the top surface. During the CMP step, the residual particles come mostly from the slurries (i.e. silica, alumina) and from the polished material. The particles either get adsorbed at the surface or in worst case scenario, embedded in the top layer due to the pressure applied by the pad.

The metallic contamination arises from the excess of metals in the slurries applied, being critical for back-end processes as they can generate shorts between metallic lines and they can facilitate the diffusion of copper to reach the active area during the upcoming thermal processes.

The damage of the top layer due to the distortion of the crystal structure caused by the abrasive particles and the pressure applied by the pad ranges between $1 - 10 \text{ nm}$ [19, 49] depending on the material being polished and the CMP process. Therefore, it is convenient to remove the scratched layer as its physical properties such as stress, insulation and contamination would fail. Accordingly, an effective cleaning process that removes the particles, the metallic contamination and the damaged layer must be added for each CMP step.
1.6.1. Slurry Removal

The particle adhesion to the substrate is originated either by the van der Waals or by the electrostatic forces depending upon the distance between the particle and the substrate [50].

In order to remove the particles, a force greater than the van der Waals has to be exerted on the substrate. Scrubbing the surface or etching both particle and substrate are two of the solutions to overcome the electrostatic and van der Waals forces. Scrubbing techniques such as brushes are used in contact with the surface to mechanically remove the particles. The optimization of the process is performed by tweaking the rotational speed of the wafer, the DI flow and the height of the brush, this is, how much of the brush is in contact or compressed against the wafer. In the case of the etching process, the thickness of the substrate to be underetch must be considered as it is necessary to increase the distance \((x)\) between particle and substrate in order to decrease the van der Waals interactions. For silicon, it is recommended to remove 2 \(nm\) [49], for oxide removal, a 4 to 5 \(nm\) underetch is necessary [51].

Particle removal is followed by preventing its readhesion into the substrate by canceling the electrostatic forces between the particles and the substrate. The charge, located at the particle terminals or at the surface of the substrate, can be manipulated by modifying the pH of the solution. When the surface of the substrate is dipped into a solution, automatically, the particle is surrounded by its counter charge provided by the solution creating two layers (or areas): i) a high concentrated layer of counter ions close to the particle surface known as Stern layer and then ii) a larger neighboring layer. Within the neighboring layer there is a boundary inside which the ions are bounded to the particle. When the particle moves due to gravity, or by applying an electrical field, those ions beyond the boundary will stay disperse in the solution. The net charge or potential at the boundary is known as Zeta potential [52].

The ionic strength of the solution is defined by the size of the aforementioned double layer: the lower the ionic strength, the thicker the double layer. Similarly, the ionic strength can also modify the Zeta potential. If the ionic strength increases, the Zeta potential decreases and vice versa. The Zeta potential is pH-dependent [53] which means that having solutions with a pH below 1.8 or above 9, the substrate and the particles present the same charge.

Other way of modifying the charges of the particle and the substrate surface is by adding into the solution surfactants that will stick into the particle and substrate. The ionic strength of the solution is also important [49].

1.6.2. Metallic Removal

Metallic contamination can arise from two different sources: i) through the CMP equipment where x-ray fluorescence measurements have shown between \(10^{11}\) to \(10^{12} \text{ atoms/cm}^2\) [51] or ii) during the cleaning step of Inter Metal Dielectric (IMD)
processes in which the scrubber brushes metals away from one location at the surface of the wafer and redeposit them at an adjacent zone.

In order to remove the metallic contamination, the idea is to take advantage of the solubility of the ions or oxides and dissolve them in acids such as HF mixtures.

1.6.3. Damaged Layer Removal

The material planarized and CMP equipment conditions will define the thickness of the damaged layer hence, the importance of measuring and determining the exact thickness for each of the CMP processes. There are different techniques to measure the thickness such as x-ray specular reflectivity or ellipsometry.

Another common approach is to measure the chemical resistance of the damaged layer by bathing the wafer in either 0.1% HF or in hot ammonia [49] where differences in the etch rate define the damaged layer and bulk area. The etch rate, higher at the damaged layer than at the bulk, decreases towards the bulk area until it reaches a constant rate. In order to remove the damaged layer, either scrubbing the wafer and adding a wet chemical etch or by avoiding scrubbers and removing it during the underetch removal process.

1.7. CMP Process Challenges

1.7.1. Within-Wafer Nonuniformity (WIWNU)

There are several factors that have an impact in the final thickness distribution across a single wafer. Among them and before starting the process, human and machine mistakes can affect the WIWNU however, these mistakes can be prevented saving time and costs.

Recipe parameters

The MRR in the CMP process tends to be simplified in the Preston equation (Equation 1.3),

\[ MRR = k_p P_o V_r \]  (1.3)

where MRR is the material removal rate (depth/time), \( P_o \) is the down force or pressure (psi) towards the pad, \( V_r \) (rpm) is the relative velocity of the wafer vs the pad and \( k_p \) is the Preston constant [54]. However, the process itself is more complex than how it is expressed in Equation 1.3. The CMP process has over twenty input variables, mainly slurry (chemistry) related. Therefore, in addition of the relative speed and the down force, the remaining chemical related variables have to be fitted in \( k_p \). Equation 1.3 does not succeed while trying to represent the interaction process between the wafer, the slurry and the pad (i.e. particle size, concentration, pad properties). However, the Preston equation defines simple mechanical polishing between two bodies. Another way of understanding the process variables is by understanding the micro- and nanoscale parameters. For example, if
the particle size is decreased, the amount of particles covering the surface of the pad will increase (microscale), the material removal rate per particle will decrease due to the lower stress (nanoscale). Moreover, the scratching per particle will decrease due to reduced indentation (nanoscale) [55].

Adjusting values such as the down pressure, the head carrier and the platens speed can reduce or increase the NU and increase or decrease the MRR. For instance, Table 1.1 shows that by increasing the down force, both the NU and MRR are improved. Nonetheless, setting the down force to high leads to scratches on the surface. Decreasing both platen and carrier speeds will optimize the NU however, the MRR will decrease. An increase in the down force at a constant platen speed will reduce the NU. Table 1.1 summarizes all the interactions between the down force and the NU and MRR outcome.

Aside from the aforementioned parameters, there are other factors that may reduce the NU such as the RR pressure or the back membrane pressure. The latter can be increased when the wafer etches faster in the edges than in the center.

**Pad conditioner effect**

The continuous supply of slurry into the pad is distributed homogeneously by the rotational movement of the platen and the grooves of the pad. Pads are typically 20-30 inches in diameter however, the wafer size varies from 4 to 12 inches leaving an empty space in the pad while a single wafer is being polished. The slurry deposited on an empty area can become glazed, the pad contraction is lost and then the polishing rate decreased and hydroplaning can occur, which means no more contact between the pad and the wafer surface [57].

A pad conditioner (end effector) is of around 4 inches in diameter and made of diamond grit or silicon carbide and is commonly used to scrape off the topmost layer of the pad giving back its contraction property and at the same time, flattening the pad to improve the polish uniformity [58].

Due to the effect of the relative velocity between the pad and the carrier, the amount of material removed at the edge of the wafer tend to be more than at its center. This behavior leads to a pattern in the polishing pad where the areas that have been in contact to the center of the wafer are less polished than the areas of the pad that have been in contact at the edge. This can be corrected by conditioning with the end effector at those specific areas of the pad to try to compensate for the extra amount removed at the edges. The end effector can be programmed with both the amount of time and location at the polishing pad. The only drawback of the end effector is that if the down force is too high, it can deteriorate the polishing pad and shorten its life.

**1.7.2. Wafer to Wafer Nonuniformity (WTWNU)**

Besides controlling the thickness distribution for WIWNU, the thickness variation from wafer to wafer (WTWNU) also has to be targeted within a specific scope.
1.7. CMP PROCESS CHALLENGES

Table 1.1: CMP process trends. Interactions between down force, head carrier speed and platen speed. (⇔ = constant; ↑ = increases; ↓ = decreases). (Adapted from [56].)

<table>
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<td>↓</td>
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<td>↑</td>
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<tr>
<td>↓</td>
<td>⇔</td>
<td>⇔</td>
<td>⇔</td>
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</tr>
</tbody>
</table>

Prior processing a PMD or ILD step on a whole batch of wafers, the planarization time has to be estimated for a pilot wafer. The incoming wafers may already vary in their thickness distribution therefore adding the human factor into the process will have the outcome of underplanarized wafers that need to be replanarized or overplanarized wafers that need to be redeposited slowing a high throughput rate.

There are two reasons behind the thickness variation from wafer to wafer; i) deviations in the CMP planarization rate or ii) deviations in the thickness distribution.
CHAPTER 1. INTRODUCTION

Deviations in the planarization rate can occur in different ways: either the rate increases or decreases gradually, or it behaves unpredictably. The erratic behavior is commonly due to the bad quality of a pad. However, if the pad quality is good, it will planarize from wafer to wafer consistently until its lifetime ceases. From that point on and until the pad is replaced with a new one, the planarization rate will decrease and the WTWNU will increase. Alternatively, if the polishing pad is not broken-in prior planarizing a batch, the rate will gradually increase. In order to avoid this phenomena, the break-in is used to condition the pad to ensure a consistent planarization between wafers [59]. The second important step is to estimate the time necessary to break-in the pad to achieve a steady state pad that sets up the constant MRR from wafer to wafer [60].

**Endpoint systems**

To prevent reworking wafers, the endpoint system subtracts the human factor by automatically detecting changes of the materials being removed and stopping the process hence increasing the yield and throughput. There are several endpoint systems based on different techniques such as monitoring the motor current, optical light and pad temperature.

The motor current detection occurs when the planarization of a material is close to its end and the pad starts contacting the underneath layer. This leads to a change in the friction force so the current of the head carrier has to change to keep the speed of the rotation pad constant. By controlling the change of the motor current an endpoint can be found.

The optical light endpoint has two approaches, one for dielectrics and the other one for metals. For dielectrics, the endpoint system is based on changes in the film thickness due to interferences between the reflected lights. Changes in thickness lead to a change of interference state. For metals, the high reflectivity of their surface is exploited. Once the metal is planarized, the reflectivity decays and the endpoint triggered [61].

The pad temperature endpoint system is based on the consumed kinematic energy between wafer and pad. Here, it is taken into account that the coefficient of friction between pad and the dielectric film is lower than between the metal and the pad giving rise to the temperature of the pad while planarizing metals [62].

However, even though these endpoint systems succeed at planarizing blank wafers, they still present problems while planarizing wafers with high density pattern due to the complexity of the signals.

1.7.3. Defects

ICs manufacturing of sub-22-nm complementary metal-oxide semiconductor (CMOS) requires a clean environment to produce wafers with less than 5 pcs/cm² [63]. During the planarization, the abrasive particles are pressed against the dielectric film to
1.7. CMP PROCESS CHALLENGES

remove materials but an issue with the equipment or during the post-CMP step, the process can produce defects. Scratches can come from three different sources: lack of a tight distribution of particle size in the slurry, material from the wafer-slurry-pad interaction accumulated in the end effector, and the drop out of the diamond grit from the pad conditioner.

Poor temperature control of the slurry can lead to particle agglomeration increasing its size. Once these particles are delivered to the polishing pad, deep scratches can be produced. Filters in the slurry line can be used to prevent chunks of particles from ending up in the polishing pad. However, the filter system has a couple of drawbacks: the slurry flow rate decreases if the filter clogs and the CMP planarizing rate decreases when the filter reaches its end of life.

The material collected by the end effector from the wafer-pad interaction produces severe scratches. To avoid this, the end effector is thoroughly cleaned with high-pressure water or with a rotating brush. If the slurry is corrosive, the diamond grid bonded with nickel on the end effector will drop out and scratch entirely the wafer. To prevent this from happening, a thin diamond film is epitaxially grown to bond the diamond grit and reduce the risk for the diamond materials to fall off [64].

Other defects such as dielectric cracks can occur if the film is tensile. If so, the down force of the CMP will exert a shear stress that will break the film, specially in areas where there is a step height above a metal line.

1.7.4. Dishing and Erosion

While polishing metals, the NU planarization of the topography leads to defects known as dishing and erosion. These two defects are mainly caused while planarizing two alternate materials. If the metal filling the oxide cavity is removed faster than the surrounding oxide, the defect is known as dishing (see Figure 1.15a). On the other hand, if an excessive wear is caused during the planarization step by removing the dielectric material where the patterned metal fillings are placed then the defect is known as erosion (see Figure 1.15b). Both defects can occur simultaneously.

![Figure 1.15: Dishing and erosion caused during metal planarization.](image)

In the case of copper dishing, the NU increases resulting in complications for the subsequent layer. These two defects have a negative impact in the electrical circuit affecting the capacitance, resistance and inductance parasitics [65], [66]. In order
to minimize the dishing and erosion of the materials, the point of focus is placed in the selectivity of the slurry. Acidic slurries containing inhibitors such as citric acid [67], potassium sorbate [68] or benzotriazole (BTA) between others, create a passivation layer that regulates the chemical rate while maintaining a constant planarization rate. However, using acidic slurries with inhibitors have a couple of drawbacks, they may cause corrosion on the CMP equipment and some of the inhibitors are insoluble sticking into the surface as contaminants. Alkaline slurries made of abrasive particles, surfactants, oxidizers and used without inhibitors have demonstrated that besides reducing the surface roughness, the erosion is decreases while increasing the copper line width [69].

Figure 1.16: Residues under and over planarizing [70].

Etching faster at the edge of the wafer rather that at the center leads to over polishing at the edge thus erosion is originated (see Figure 1.16b). Alternatively, the center of the wafer is under polished (see Figure 1.16a).
Chapter 2

Experimental Work

The experimental work consists of two parts: i) the process fabrication of a set of blank and patterned wafers and its characterization; and ii) the characterization of the external CMP process, provided by Axus Technology, to analyze the planarization efficiency and the polishing capability (surface roughness) of the wafer carrier.

2.1. Process flow: Patterned Wafer

In order to observe different aspects of the CMP process such as the influence of the pattern density or the structure dimension, the process flow is designed to have two different masks. Moreover, another set of blank wafers with Plasma Enhanced Chemical Vapour Deposition (PECVD) oxide are fabricated to analyze and compare the full potential of the Titan™ wafer carrier against a 3rd generation carrier (standard carrier).

2.1.1. Thermal Oxidation

Dry oxidation was performed on 100 mm, p-type blank wafers at 1200°C for 42 minutes in an horizontal Thermco furnace to grow a high temperature oxide layer. In the thermal oxidation process, silicon interacts with oxygen as in Equation 2.1 to grow a silicon dioxide layer.

\[ \text{Si}(s) + \text{O}_2(g) \rightarrow \text{SiO}_2(s) \] (2.1)

2.1.2. Low Pressure Chemical Vapour Deposition (LPCVD)

Before the Low Pressure Chemical Vapour Deposition (LPCVD) process, the lot is soaked in a mixture of sulfuric acid (\(\text{H}_2\text{SO}_4\)) and hydrogen peroxide (\(\text{H}_2\text{O}_2\)), known as 7-up, at a volume ratio of 3:1 respectively, for 15 minutes at 120°C to remove impurities, metals and particles from the surface. After that, the lot is rinsed in \(\text{H}_2\text{O}\) under bubbles for 10 minutes and then rinse and dried.
Polysilicon is deposited by LPCVD technique in a Expertech compact thermal reactor for 193 minutes. The deposition of poly-Si is described in Equation 2.2

\[ \text{SiH}_4(g) \Rightarrow \text{Si}(s) + 2\text{H}_2(g) \] (2.2)

In this process, silane (\(\text{SiH}_4\)), which is in the gas form, is introduced into the furnace and it reacts at the surface of the wafer. The silicon atoms are adsorbed at the surface of the wafer and the byproducts (\(\text{H}_2\)) of the reaction are desorbed and purged from the system.

2.1.3. Lithography

Two steps are required to transfer a specific pattern into a wafer. The first step is the lithography in which a photoresist is spun on the surface of the wafer and patterned by exposing light on specific areas of a photoresist. The second step is the etching of the underlying material.

The lot of wafers is spin coated with 1 \(\mu m\) photoresist. In order to observe the impact of the open area (see Table 2.1), pattern density and distribution, two different masks are transferred to the wafers. Open area is a term used to quantify the area of the resist that is exposed to UV light and later on developed. The open area per die can be determined by calculating the ratio between the area of the structures and the total area of a single die which in this case is \(\approx 53.3 \text{ mm}^2\).

<table>
<thead>
<tr>
<th>Mask ID</th>
<th># Objects</th>
<th>Max size ((\text{mm}^2))</th>
<th>Min size ((\text{mm}^2))</th>
<th>Open area (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>G-mask</td>
<td>48126</td>
<td>0.044</td>
<td>8(\times)10(^{-6})</td>
<td>98.98</td>
</tr>
<tr>
<td>AF-mask</td>
<td>6083</td>
<td>2.9</td>
<td>6(\times)10(^{-6})</td>
<td>14.19</td>
</tr>
</tbody>
</table>

The first lot is exposed in a XLS stepper system where half of the lot is patterned with the \(G\) mask (see Figure 2.1a) and the other half with the \(AF\) mask (see Figure 2.1b). The second lot is exposed with a DSW stepper. Notice that for Figure 2.1a, the recessed area is the one surrounding the structures and for Figure 2.1b, the structures are being recessed.

After exposure and letting the resist to rest for 15 minutes, the whole lot is developed to remove the exposed (unwanted) resist and hardbaked in an oven for 30 minutes.
2.1. PROCESS FLOW: PATTERNED WAFER

2.1.4. Reactive Ion Etching (RIE)

The underlying material (polysilicon) is removed in a Reactive Ion Etching (RIE) tool (P5000) with help of an endpoint system using a chlorine (Cl\(_2\)) gas. Cl\(_2\) generates reactive species that will react with the surface not covered by the photoresist. The chemical reaction occurs as Equation 2.3 describes,

\[
4\text{Cl} \cdot (g) + \text{Si}(s) \Rightarrow \text{SiCl}_4(g)
\]  

(2.3)

In order to obtain a straight profile (anisotropic etch), hydrogen bromide (HBr) is used as passivation layer to protect the walls to avoid undesired underetching.

After etching, the lot is inspected for polysilicon residues and stripped on a Tepla system for 1h under 1000 W and 300 sccm oxygen plasma to remove the remaining resist. To make sure that there are neither polymers (photoresist or HBr) nor residues left in the structures, the lot is soaked in 7-up for 15 minutes and dried.

2.1.5. Plasma Enhanced Chemical Vapour Deposition (PECVD)

PECVD silicon oxide is deposited (see Equation 2.4) on a P5000 tool at a deposition rate of 706 nm/min to grow a 1000 nm SiO\(_2\) layer.

\[
\text{SiH}_4 + 2\text{O}_2 \rightarrow \text{SiO}_2 + 2\text{H}_2\text{O}
\]  

(2.4)
2.2. Blanket Wafer

A set of blanket wafers were processed on a P5000 tool to deposit 1000 nm PECVD silicon oxide on a silicon substrate.

2.3. CMP Characterization Techniques

2.3.1. Atomic Force Microscopy (AFM) & Ellipsometry

Prior to the external CMP process, Atomic Force Microscopy (AFM) is used to measure the step height caused by the conformal coverage of the PECVD process. At the same time, the roughness of the outermost layer is scanned by AFM to observe the impact caused by the underlying layers and structures.

In order to provide a thorough assessment of the CMP process, the analysis is focused on the pattern density defined by the lithography mask. Different locations within the mask can provide different ranges of densities and therefore quantify the step height reduction ratio (SHRR). Measuring the step height before and after the CMP process, at the exact same location, is used to define how well a step height is planarized.

![Figure 2.2: Determining pattern density location at a specific mask.](image)

The AFM analysis is performed by locating a spot within a die in which a pattern has a fixed geometric dimension. Figure 2.2a shows a location marked under a blue square within the G-mask. An amplification of the blue square is seen in Figure 2.2b showing a fixed geometric pattern. Furthermore, in Figure 2.2c the pattern density is measured by calculating the ratio between the chrome area to the total chosen area. Locations with pattern densities of 14, 36, 50, 75 and 84% are measured as shown in Figure 2.3.

AFM analysis is performed by scanning a 10 µm² area with a mechanical probe. The scan is suited to cover an area where there is both an underlying poly-Si structure and a non-patterned (or recessed) area. For roughness analysis, a scan is
2.3. CMP CHARACTERIZATION TECHNIQUES

Figure 2.3: Pattern density locations measured using AFM

performed either over an area where there is a poly-Si structure or over a recessed area. Former processes such as the RIE to pattern the poly-Si layer or the LPCVD of the poly-Si layer can have an effect on the roughness of the resulting layer.

Besides the Step Height (SH) analysis, the thickness distribution across a wafer diameter and polar map are measured using a Horiba ellipsometer tool.
Chapter 3

Results and Discussion

3.1. Patterned Wafer

3.1.1. Thermal Oxidation Process

Prior high temperature processes, it is suggested to perform a clean step to remove impurities such as metals, sodium ions and particles from the surface of the wafer to avoid their diffusion into the interior of the semiconductor or to cause a lattice mismatch. However, before the thermal oxidation step, no clean process was performed as the wafers were introduced into the furnace directly from their container without any former handling. Clean processes are very helpful to reduce impurities after several steps but considering that the number of particles in new wafers are zero, performing a cleaning step will introduce particles, due to the cleaning tool and the wafer handling, rather than reduce them.

In order to observe the influence that the gas flow and temperature distribution has in the oxide thickness growth due to the position of the wafer inside the furnace, three wafers were placed at three different locations within the same boat filler. Table 3.1 shows the thickness measurements for $SiO_2$ performed on a Horiba Uvisel ellipsometer.

The uniformity of the wafer located at the opp-door position, this is defined as the wafer located deep inside the furnace, is as low as $±0.03\%$. Meanwhile at the door position, this is the opposite of the opp-door position, the uniformity within the wafer is as high as $±0.39\%$. For low quantity of wafers, results show that it is favorable to place them deep into the oven to obtain a better within wafer uniformity. Equation 3.1 is used to calculate the uniformity within a wafer with 5-point measurements. The uniformity between wafers is $±2.12\%$ for the first batch and $±1.38\%$ for the second.

\[
Uniformity = \frac{\text{max thickness} - \text{min thickness}}{2 \cdot \text{average thickness}}
\]  

(3.1)

During the experiment, for the first lot, the capacity of the furnace was at its full with 50 wafers (dummies plus processed) however, for the second lot, the full capac-
Table 3.1: SiO$_2$ thickness parameters. The wafer located close to the gas flow pump was defined as 'oven', the one at the center of boat as 'middle' and the closest to the furnace exit as 'door'.

<table>
<thead>
<tr>
<th>Lot</th>
<th>Location</th>
<th>Thickness (nm)</th>
<th>Uniformity [±%]</th>
<th>σ (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>First</td>
<td>opp-door</td>
<td>167</td>
<td>0.03</td>
<td>0.04</td>
</tr>
<tr>
<td></td>
<td>middle</td>
<td>167</td>
<td>0.07</td>
<td>0.08</td>
</tr>
<tr>
<td></td>
<td>door</td>
<td>160</td>
<td>0.34</td>
<td>0.4</td>
</tr>
<tr>
<td>Second</td>
<td>opp-door</td>
<td>168</td>
<td>0.12</td>
<td>0.2</td>
</tr>
<tr>
<td></td>
<td>door</td>
<td>164</td>
<td>0.39</td>
<td>0.5</td>
</tr>
</tbody>
</table>

The uniformity of the oven was 25 wafers. This impedes to understand the growth distribution inside the furnace thus, compare data between locations. Table 3.1 shows that the uniformity within a wafer is lower when the first lot is processed however, the wafer to wafer uniformity is lower for the second batch though in theory, a furnace filled with dummies will improve the overall uniformity. Figure 3.1 shows a schematic of the cross-sectional view of the growth oxide layer.

3.1.2. LPCVD Process

The polysilicon layer is measured with an ellipsometer and a spectrophotometer. Table 3.2 shows the data for the polysilicon and the underlying material, SiO$_2$. The first lot was measured with an ellipsometer (Horiba) and the second lot with a spectrophotometer (Leitz).

The deposition rate for a linear process such as LPCVD can be calculated as in Equation 3.2. The deposition rate for the first and second batch is 0.44 nm/min respective 0.48 nm/min. Notice that the data comes from different tools so it is expected to have variations in the results.

\[
\text{Deposition rate} = \frac{\text{thickness (nm)}}{\text{time (minute)}} \tag{3.2}
\]
3.1. PATTERNED WAFER

Table 3.2: Thickness for Poly-Si and SiO$_2$. The first batch was measured on an ellipsometer meanwhile the second batch was performed on a spectrophotometer.

<table>
<thead>
<tr>
<th>Lot</th>
<th>Layer</th>
<th>Thickness (nm)</th>
<th>Uniformity [±%]</th>
<th>σ (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>First</td>
<td>Poly-Si</td>
<td>85</td>
<td>4.40</td>
<td>2.53</td>
</tr>
<tr>
<td></td>
<td>SiO$_2$</td>
<td>186</td>
<td>3.31</td>
<td>4.11</td>
</tr>
<tr>
<td>Second</td>
<td>Poly-Si</td>
<td>93</td>
<td>0.59</td>
<td>0.44</td>
</tr>
<tr>
<td></td>
<td>SiO$_2$</td>
<td>170</td>
<td>0.12</td>
<td>1.51</td>
</tr>
</tbody>
</table>

Figure 3.2 shows the schematic composition of the wafer after deposition of polysilicon.

![Schematic composition of the wafer after deposition of polysilicon](image.png)

Figure 3.2: Cross-section view of the deposited polysilicon layer on SiO$_2$.

3.1.3. RIE Process

The purpose of the RIE process is to remove the patterned polysilicon layer without disturbing the oxide layer. However, sometimes the depth etched is deeper than the amount deposited causing an overetch of the underlying SiO$_2$ layer. Comparing the data from Table 3.3 and Table 3.2 where the amount deposited is less than the amount removed shows that all wafers are overetch. Having said that, the endpoint system failed after having processed two wafers and the etch time had to be controlled manually, therefore the erratic behavior of the etch depth. However, to avoid having polysilicon residues on the cavities, it is preferable to overetch.

In order to quantify the depth of the cavities or recessed areas, both lots are measured on a profilometer (Dektak) (see Table 3.3). The whole first lot with both masks, G-1 and AF-1, are measured but for the second lot, this is G-2 and AF-2, to avoid unnecessary handling, just the first and last wafer are measured to observe if there is any variation in the etched depth. While etching a large number of wafers, any drifting in the process is a sign of the lack of reproducibility thus, uniformity values from wafer to wafer are useful indicators to assess a process viability.
CHAPTER 3. RESULTS AND DISCUSSION

Table 3.3: Etched (depth) measurements.

<table>
<thead>
<tr>
<th>Mask</th>
<th>#</th>
<th>Center [nm]</th>
<th>Edge [nm]</th>
<th>Average [nm]</th>
<th>Uniformity [±%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>G-1</td>
<td>016</td>
<td>93</td>
<td>94</td>
<td>93</td>
<td>0.27</td>
</tr>
<tr>
<td></td>
<td>155</td>
<td>96</td>
<td>92</td>
<td>94</td>
<td>1.92</td>
</tr>
<tr>
<td></td>
<td>392</td>
<td>95</td>
<td>96</td>
<td>95</td>
<td>0.47</td>
</tr>
<tr>
<td></td>
<td>135</td>
<td>97</td>
<td>96</td>
<td>96</td>
<td>0.41</td>
</tr>
<tr>
<td>AF-1</td>
<td>273</td>
<td>101</td>
<td>97</td>
<td>99</td>
<td>1.87</td>
</tr>
<tr>
<td></td>
<td>132</td>
<td>98</td>
<td>96</td>
<td>97</td>
<td>0.87</td>
</tr>
<tr>
<td></td>
<td>134</td>
<td>95</td>
<td>99</td>
<td>97</td>
<td>1.70</td>
</tr>
<tr>
<td></td>
<td>393</td>
<td>96</td>
<td>97</td>
<td>97</td>
<td>0.47</td>
</tr>
<tr>
<td>G-2</td>
<td>034</td>
<td>96</td>
<td>99</td>
<td>97</td>
<td>1.64</td>
</tr>
<tr>
<td></td>
<td>006</td>
<td>98</td>
<td>98</td>
<td>98</td>
<td>0.20</td>
</tr>
<tr>
<td>AF-2</td>
<td>287</td>
<td>102</td>
<td>101</td>
<td>102</td>
<td>0.69</td>
</tr>
<tr>
<td></td>
<td>401</td>
<td>101</td>
<td>101</td>
<td>101</td>
<td>0.25</td>
</tr>
</tbody>
</table>

The depth of the cavity is quantified by performing a sweep with a silicon stylus from the topmost layer to the bottom of the cavity. Table 3.3 shows the measurements performed for each wafer. To observe the uniformity within wafer, two point, center and edge, are measured. Figure 3.3 shows the cross-section of the patterned wafer.

![Cross-section of the etched polysilicon layer.](image)

3.1.4. PECVD Process

In order to evaluate the PECVD rate for $SiO_2$ handled in a P5000 tool, a blank silicon wafer is processed for 83s (see Table 3.4). Afterwards, five points in the wafer
3.1. PATTERNED WAFER

(top, center, flat, right and left) are measured in a spectrophotometer to control the oxide thickness distribution in the wafer. The average value is used to calculate the new deposition rate for the specific recipe in order to target the right time to deposit 1000 nm SiO$_2$.

Table 3.4: PECVD oxide deposition values.

<table>
<thead>
<tr>
<th>Mask</th>
<th>Wafer order</th>
<th>Average [nm]</th>
<th>Uniformity [±%]</th>
<th>Time [s]</th>
<th>Dep. rate [nm/min]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Blank wafer</td>
<td>-</td>
<td>974</td>
<td>1.10</td>
<td>83</td>
<td>704</td>
</tr>
<tr>
<td>Blank wafer</td>
<td>First</td>
<td>1007</td>
<td>0.95</td>
<td>86</td>
<td>702</td>
</tr>
<tr>
<td>G-1 &amp; AF-1</td>
<td>8 wafers</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Blank wafer</td>
<td>Last</td>
<td>1007</td>
<td>1.01</td>
<td>86</td>
<td>702</td>
</tr>
<tr>
<td>Blank wafer</td>
<td>First</td>
<td>1012</td>
<td>0.86</td>
<td>86</td>
<td>706</td>
</tr>
<tr>
<td>G-2</td>
<td>10 wafers</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Blank wafer</td>
<td>Last</td>
<td>1014</td>
<td>0.75</td>
<td>86</td>
<td>707</td>
</tr>
<tr>
<td>Blank wafer</td>
<td>First</td>
<td>1017</td>
<td>0.76</td>
<td>86</td>
<td>710</td>
</tr>
<tr>
<td>AF-2</td>
<td>10 wafers</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Blank wafer</td>
<td>Last</td>
<td>1017</td>
<td>1.06</td>
<td>86</td>
<td>710</td>
</tr>
</tbody>
</table>

The wafer loading limitation of the P5000 entails the partition of the second lot made of 20 wafers into two groups. Table 3.4 shows the data for three series in the P5000. Each of the series has been processed one right after the other without any delay time. For the first series, the first lot made of 8 wafers with both G-1 and AF-1 masks is processed between 2 blankets. The same procedure is followed for the other two series with the second batch, 10 wafers with the G-2 mask and another 10 with the AF-2 mask are processed between 2 blankets each. The blankets are processed first and last to monitor the SiO$_2$ distribution. Afterwards, the blankets are measured and plotted in Figure 3.4 to observe any drifts or variations in the oxide distribution within a wafer and from wafer to wafer.

Table 3.4 shows a consistency in the process for the first series as the averages for the First and Last blanket wafer from the first lot are 1007 nm each. However, the second and third series with masks G-2 and AF-2 increases progressively. Figure 3.4 plots each of the blankets following the order in which they are processed and shows how the oxide thickness for each location increases progressively from 1007 nm to 1017 nm, this is a 1% increment over 35 wafers. There are some exceptions but it is due to the manual measurements without the use of a template to measure at the exact same location for each of the wafers still, the increment trend can be seen.
CHAPTER 3. RESULTS AND DISCUSSION

Figure 3.4: Wafer to wafer uniformity for a 1000 nm SiO$_2$ PECVD step.

There is a reason behind this trend; every time oxide is deposited on the surface of a wafer inside a chamber, meanwhile the wafer is transferred back to the loading box and before the next wafer is transferred into the chamber, a clean step is performed to remove reactants that still present in the chamber. If the time employed for the cleaning step is not long enough to remove the totality of the reactants left inside the chamber, the next wafer will be exposed to a higher amount of reactants increasing the deposition rate and drifting the oxide thickness from wafer to wafer.

Figure 3.5: Within wafer uniformity. Spectrophotometry (left) and ellipsometry (right) measurements of a 1000 nm PECVD SiO$_2$ layer.

While analyzing the uniformity within a single wafer, the oxide distribution
3.2. CMP CHARACTERIZATION

varies between locations. Figure 3.5 shows a 5-point measurement with the averages for each location of the six blank wafers (see Figure 3.5a) and a 49 point polar map converted into a surface map of a single wafer processed afterwards to be used as a blanket for the CMP process at Axus Technology (see Figure 3.5b). The two graphs in Figure 3.5 show that the oxide deposition is thicker at the right and towards the bottom (flat) side. There are two motivations behind this tendency: i) recipe parameters (i.e pressure) have to be tweaked to enhance the overall uniformity or ii) the direction in which the gas is purged out of the chamber is towards the southeast of the wafer increasing the deposition rate at that location (see Figure 3.5a). Figure 3.6 shows the final PECVD oxide layer on both patterned and blank wafers.

![Figure 3.6: Schematic of the patterned and blanket cross-section after the PECVD step.](image)

3.2. CMP Characterization

The characterization of the post-CMP process is done on a set of non-patterned wafers planarized with a third generation head carrier, and another set of blankets using the state of the art Titan™ wafer carrier. The whole lot of patterned wafers is planarized using the Titan™ carrier.

3.2.1. Influence of the Measurement Pattern in the CMP Characterization

CMP processes are mainly studied by measuring NU values of the top layer’s thickness distribution across a single wafer, and from wafer to wafer. Confusions may arise as CMP has three types of thicknesses to be evaluated: the initial thickness or pre-CMP thickness \( T_i \), the final thickness \( T_f \), known as post-CMP thickness and the amount of thickness that is removed or planarized, known as the delta thickness \( \Delta T \). The tool capability is defined by \( NU_{\Delta T} \). However, for quality control of integrated circuits, the \( NU_{T_f} \) is used.
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Interpretation of the experimental data and how it will influence the NU results requires an understanding of the strong edge effect of the CMP process. Figure 3.7 shows two different measurement patterns: i) a 49 points diameter scan across the wafer (Figure 3.7a) and ii) a 49 point polar map (Figure 3.7c). Figure 3.7b and Figure 3.7d are real representations of a wafer measured after a CMP process on an ellipsometer showing $\Delta T$ for each of the measurement patterns. The polar map in Figure 3.7d is converted into a colorful surface map for clearer readability.

![Diameter Scan 49p](image)

(a) 49 points diameter scan.

![Amount Removed (nm)](image)

(b) Scan diameter displaying 4% of the points at the edge.

![Polar map 49p](image)

(c) 49 points polar map.

![Amount Removed (nm)](image)

(d) Polar map converted into a surface map displaying 49% of the points at the edge.

Figure 3.7: Two different measurement patterns and impact in NU values

Besides the higher relative speeds at the edge, the wafer curvature and the axial stress, the pad rebound effect is one of the main responsible for increasing the NU values. Therefore how the measured points are distributed across the wafer will define the NU and the result will differ from one pattern to another. For instance, in Figure 3.7b, 2 points out of the 49 are located at the extremes of the wafer. These 2 points deviating from the remaining have 49 have a 4% impact in the NU. However, looking at Figure 3.7d, 24 points out of 49 are distributed across the edge of the
3.2. CMP CHARACTERIZATION

wafer thus, 49% of the points have a larger impact in the NU. Even though that the NU differ between patterns, both results are valid and they can be useful for specific analysis. A quick overlook of the head carrier behavior, the back membrane pressure or the wafer stress can be seen with a diameter scan. Alternatively, the final thickness distribution across the wafer is rather seen with a polar map pattern.

3.2.2. Blanket Wafers Planarized with a Third Generation Wafer Carrier

Five blanket wafers were processed on an IPEC 472 automated CMP tool with a third generation head carrier (see Table 3.5) at an average removal rate of $261 \text{nm/min}$. Figure 3.8 plots a 49 point scan diameter across a $100 \text{mm}$ wafer for each of the planarized wafers. The average NU for the set of blankets polished on a third generation carrier with a $3 \text{mm}$ edge of exclusion is $\pm 6.96\%$. The soft pad used for a buffing step achieves a final average roughness ($R_a$) for the blankets of $0.34 \text{nm}$.

Table 3.5: Blanket wafers polished with a third generation carrier and with a 3mm edge of exclusion.

<table>
<thead>
<tr>
<th>Wafer #</th>
<th>$\Delta T$ (nm)</th>
<th>$NU_{\Delta T}$ (diameter) (±%)</th>
<th>$T_f$ (nm)</th>
<th>$NU_{T_f}$ (polar) (±%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>605</td>
<td>7.93</td>
<td>331</td>
<td>7.13</td>
</tr>
<tr>
<td>2</td>
<td>648</td>
<td>6.9</td>
<td>329</td>
<td>11.53</td>
</tr>
<tr>
<td>3</td>
<td>636</td>
<td>7.11</td>
<td>307</td>
<td>10.63</td>
</tr>
<tr>
<td>4</td>
<td>603</td>
<td>6.61</td>
<td>350</td>
<td>15.41</td>
</tr>
<tr>
<td>5</td>
<td>589</td>
<td>6.24</td>
<td>337</td>
<td>8.81</td>
</tr>
<tr>
<td>Averages</td>
<td>617</td>
<td>6.96</td>
<td>331</td>
<td>10.82</td>
</tr>
</tbody>
</table>

The pad rebound effect can be noticed at $\pm 40 \text{mm}$ and towards the edge. This is something expected from the design of the third generation carrier, however, there is room for improvement. Looking at values in between $\pm 25 \text{mm}$ in Figure 3.9a, the process could have been improved in several ways hence, reducing the NU. The multizone back membrane has the possibility to apply pressure at specific radial locations. In this case, the center of the wafer shows a lower planarized profile than the edge giving room for applying higher pressures at the center of the back membrane. If the back membrane effect is not enough, values shown in Figure 3.9a from $\pm 25 \text{mm}$ and towards the each suggest the use of the pad conditioner (or end effector) to reduce the NU values by conditioning for longer time specific places of the polishing pad hence, retrieving higher removal rates than in the adjacent
locations or by wearing out the polishing pad at the location which is in contact to the edge of the wafer. Placing the carrier at the conditioned location would balance the removal rates between the center and edge of the wafer. However, if none of this methods can reduce the NU value, it is always possible to go one step back in the wafer fabrication process and induce a high center bow so the edges are planarized at a slower rate than at the center.

![Diagram](image)

Figure 3.8: Blanket wafers planarized with a 3rd generation head carrier. 49 point diameter scan for a 100 mm wafer.

The WTWNU is ± 3.99%. Aside from wafer # 2 and # 3 shown in Figure 3.11a and Figure 3.12a the process behavior from wafer to wafer appears to be erratic. The reproducibility of the process could be a matter of several factors such as the characteristics of the polishing pad, the slurry flow rate, heat dissipation or pad quality failure. Pad characteristics such as compressibility or hardness have an impact in the NU. Harder pads tend to deform less hence improving the planarization step, however, changes in compression or hardness due to pad wear will affect the WTWNU. The slurry flow rate also has to be kept constant during the whole lot as changes due to clogging of larger abrasive particles will slow the mechanical part of the process. Heat dissipation is also crucial for achieving low WTWNU as it is important to avoid changes in the chemical reaction rate at the pad-wafer interface. The head carrier should rotate along the polishing pad to dissipate the heat.

Figures 3.10 - 3.13, show each of the blankets from Table 3.5 plotted with a 49 point diameter scan of $\Delta T$ and a 49 point surface map with $T_f$ with a 3 mm edge of exclusion. The surface map comes from the conversion of a 49 point polar map. In order to convert the polar map into a surface map, the Cartesian coordinates $(x, y)$ from each point are used to create a two-dimensional grid by using MatLab’s function `meshgrid`. Afterwards, the thickness values $(z)$ are linearly interpolated by using MatLab’s function `griddata`.
3.2. CMP CHARACTERIZATION

Figure 3.9: $\Delta T$ with a 3 mm edge of exclusion is shown in a 49 point scan diameter (left) and $T_f$ with a 10 mm edge of exclusion is shown in a 49 point surface mapping (right) for wafer # 4.

In order to evaluate the post-CMP surface where the importance relies in the $T_f$ for upcoming processes (or layers), the $NU_{T_f}$ for a 49 point polar map in Equation 3.3 and with a 49 point diameter scan in Equation 3.4 is calculated for wafer # 4.

$$NU_{T_f} = \frac{STD(T_f)}{mean(T_f)} \cdot 100\% = \frac{54.0\ nm}{350.5\ nm} \cdot 100 = \pm 15.45\% \quad (3.3)$$

$$NU_{T_f} = \frac{STD(T_f)}{mean(T_f)} \cdot 100\% = \frac{42.5\ nm}{372.5\ nm} \cdot 100 = \pm 11.42\% \quad (3.4)$$

In order to determine the tool planarizing capability for a determined set of parameters and tool equipment (i.e. same polishing pad, head carrier, etc.), the $NU_{\Delta T}$ for a 49 point diameter scan is calculated for wafer # 4 in Equation 3.5. The resulting value can be improved by changing the pad, process parameters, etc.

$$NU_{\Delta T} = \frac{STD(T_f)}{mean(\Delta T)} \cdot 100\% = \frac{42.5\ nm}{603.4\ nm} \cdot 100 = \pm 7.04\% \quad (3.5)$$

For a fixed tool and recipe, Equation 3.5 gives a $NU_{\Delta T} \approx 7\%$ for a diameter scan with 3 mm edge of exclusion with a $\Delta T = 603\ nm$ for wafer # 4. However, if the initial thickness is 975 nm and the intended final thickness is 100 nm instead of the 372 nm shown in Equation 3.4, while using the same recipe, the new $STD(T_f)$ will be $7\% \cdot 875\ nm \approx 61\ nm$ rather than 42.5 nm. The increase of the standard deviation (STD) will lead to a new $NU_{T_f} = \pm 61\%$. This suggest that for step optimization and in order to enhance the $NU_{T_f}$, the sacrificial layer deposited on the wafer should be minimized as much as possible. The less amount planarized ($\Delta T$), the lower $NU_{T_f}$.
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Figure 3.10: Scan diameter and surface mapping for wafer #1.

Figure 3.11: Scan diameter and surface mapping for wafer #2.

Figure 3.12: Scan diameter and surface mapping for wafer #3.
Nevertheless, in order to evaluate the head carrier tool or its capability completely independent of $T_i$ and $T_f$, this is, neglecting the incoming thickness distribution, then only the amount removed ($\Delta T$) is analyzed. The $NU_{\Delta T}$ is now calculated using the STD for $\Delta T$. For instance, wafer #4 is calculated in Equation 3.6.

$$NU_{\Delta T} = \frac{STD (\Delta T)}{mean (\Delta T)} \cdot 100 \% = \frac{39.9 \text{ nm}}{603.4 \text{ nm}} \cdot 100 = 6.61 \%$$

(3.6)

### 3.2.3. Blanket Wafers Planarized with a Titan™ Wafer Carrier

Table 3.6: Blanket wafers planarized with a Titan™ head carrier and with a 3mm edge of exclusion.

<table>
<thead>
<tr>
<th>Wafer #</th>
<th>$\Delta T$ (nm)</th>
<th>$NU_{\Delta T}$ (diameter) (±%)</th>
<th>$T_f$ (nm)</th>
<th>$NU_{T_f}$ (polar) (±%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Titan 10</td>
<td>602</td>
<td>2.54</td>
<td>377</td>
<td>10.54</td>
</tr>
<tr>
<td>Titan 11</td>
<td>599</td>
<td>2.46</td>
<td>377</td>
<td>9.49</td>
</tr>
<tr>
<td>Titan 12</td>
<td>605</td>
<td>2.00</td>
<td>367</td>
<td>8.32</td>
</tr>
<tr>
<td>Titan 13</td>
<td>600</td>
<td>1.98</td>
<td>375</td>
<td>7.60</td>
</tr>
<tr>
<td>Titan 14</td>
<td>602</td>
<td>2.13</td>
<td>368</td>
<td>8.97</td>
</tr>
<tr>
<td>Titan 15</td>
<td>600</td>
<td>1.90</td>
<td>370</td>
<td>6.43</td>
</tr>
</tbody>
</table>

| Averages | 601 | 2.17 | 372  | 8.56 |

Figure 3.13: Scan diameter and surface mapping for wafer # 5.
CHAPTER 3. RESULTS AND DISCUSSION

Table 3.6 shows six blanket wafers processed on an IPEC 472 automated CMP tool with the state of the art Titan™ carrier at an average removal rate of 405 nm/min. Figure 3.14 plots a 49 points diameter scan across a 100 mm wafer for each of the planarized wafers. The average NUΔT for the set of blankets planarized on a Titan™ carrier with a 3 mm edge of exclusion is ±2.17 % and a final average roughness (Ra) of 0.22 nm.

![Figure 3.14: Blanket wafers planarized with a titan head wafer.](image)

The pad rebound effect can also be seen at around ±38 mm and towards the edge for the Titan™ carrier in Figure 3.14. However, the difference between the maximum and minimum value for the wafer with the lowest NUΔT, in this case Titan #15 shown in Figure 3.15a, is ≈ 32 nm.

![Figure 3.15: Scan diameter and surface mapping for Titan 15.](image)
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The $STD (\Delta T)$ from wafer to wafer is $2.0 \text{ nm}$ leading to a WTWNU of $\pm 0.33\%$. Factors such as the Titan™ carrier, the polishing pad behavior and the slurry flow delivered on the surface of the pad are kept constant during the planarization of wafers #10 to #15. However, looking from Figure 3.15b to Figure 3.20b (notice that Figure 3.15b is the last wafer processed with the Titan™ carrier) the thickness ($T_f$) located from the origin (wafer radius (0,0)mm) of the wafer all over to the extent of a radius of 30 mm increases progressively from wafer to wafer with a total $T_f$ increase of $\approx 5\%$. This behavior is due to the incoming thickness variation from the PECVD process shown in Figure 3.4. If instead of 15 wafers a whole batch of 25 wafers are processed on the PECVD tool, the variation in the thickness distribution from wafer to wafer would have increase linearly approximately $13\%$. Having said that, the WTWNU can be reduced by increasing the cleaning time step between wafers during the PECVD process to get rid of the remaining reactants in the chamber.
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Figure 3.18: Scan diameter and surface mapping for Titan 12.

Figure 3.19: Scan diameter and surface mapping for Titan 13.

Figure 3.20: Scan diameter and surface mapping for Titan 14.
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3.2.4. Titan™ Wafer Carrier vs. Third Generation Carrier

Figure 3.21 plots a 49 points diameter scan of a wafer planarized with a 3rd generation carrier and a wafer planarized with a Titan™ carrier. The wafer-edge NU resulting from the pad rebound effect is minimized with the Titan™ carrier but still, the higher relative velocities at the edge of the wafer are planarizing faster the edge than the center.

Figure 3.21: Titan™ vs. 3rd generation wafer carrier.

The 3rd generation carrier has a RR that applies a controlled and independent pressure from the one that the wafer applies against the pad, reducing the edge of exclusion area by distributing the load concentration located at the edge of the wafer and directed towards the center. However, the gap between the RR and the wafer which is in the range of 0.5 to 1 mm causes the pad to rebound. The 3rd generation carrier plot in Figure 3.21 shows a difference between the maximum and minimum ΔT of approximately 196 nm due to the pad rebound. However, the ΔT difference for Titan™ carrier is approximately 32 nm.

(a) Schematic of a 3rd generation carrier
(b) Schematic of Titan™ carrier

Figure 3.22: Pad rebound effect on a Titan™ carrier.
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The distinction between the Titan™ and the 3rd generation carrier comes from the inclusion of the pneumatic IT between the wafer and the RR (see Figure 3.22). The independent and controlled pressure exerted by the pneumatic or bladder against the polishing pad reduces the load concentration at the edge of the wafer by distributing it across the RR, and the polishing pad hence, improving the NU. The addition of the IT decreases the pad rebound effect by almost 84%.

The new design of the Titan™ carrier, this is, the IT and the previously engineered RR, together with the flexible back membrane which provides a wafer-pad control in which the pressure parameter can be adjusted to each area or zones independently.

![Figure 3.23: Radial distribution of the 49 points measured in a polar map.](image)

In order to analyze the pressure exerted from the back membrane into the wafer, and the impact it may have in the pressure and RR profile, average values of $\Delta T$ pertaining to specific radial locations are plotted in Figure 3.23. The polar map is distributed with 1 point at the origin, 8 points at a radius of 13 mm, 16 and 24 points at 27 and 40 mm respectively. Later, the mean of $\Delta T$ for each radial location is plotted in Figure 3.24a and the STD of $\Delta T$ in Figure 3.24b.

The reduced pad rebound effect shown in Figure 3.21 for the Titan™ carrier now shown in Figure 3.24a is not noticeable because the measurements are performed with a 10 mm edge of exclusion area however, it is of interest to note how the MRR increases towards the edge due to the higher relative velocities further from the origin of the wafer planarizing 4% more at the edge than at the center. On the other hand, the beginning of the rabbit-ear-shape caused by the pad rebound effect on the wafer planarized with the 3rd generation carrier, appears already at 25 mm from the origin. However, the pressure exerted by the pneumatic IT and the
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Figure 3.24: Radial comparison between 3\textsuperscript{rd} generation and Titan\textsuperscript{TM}.

RR of the Titan\textsuperscript{TM} carrier helps to control and distribute the load along the wafer displacing the reduced rebound farther to the edge. Simultaneously, the radial plot helps to identify whether the back membrane pressure applied during the process was enough to cancel the higher relative velocities at the edge. In this respect, Figure 3.24a shows with the increasing line for the Titan\textsuperscript{TM} carrier that the process has room for improvement by inducing higher pressure at the back membrane.

Table 3.7: Data comparing the head performance between the 3\textsuperscript{rd} generation and the Titan\textsuperscript{TM} carrier while polishing the same amount of SiO\textsubscript{2}.

<table>
<thead>
<tr>
<th>$\Delta T$ (nm)</th>
<th>MRR (nm/min)</th>
<th>$NU_{\Delta T}$ 3mm (±%)</th>
<th>Defect density</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>3\textsuperscript{rd} Gen</td>
<td>Titan\textsuperscript{TM}</td>
<td>3\textsuperscript{rd} Gen</td>
</tr>
<tr>
<td>605</td>
<td>247</td>
<td>408</td>
<td>7.93</td>
</tr>
<tr>
<td>594</td>
<td>262</td>
<td>404</td>
<td>6.24</td>
</tr>
</tbody>
</table>

Table 3.7 compares the two carriers while planarizing a wafer 594 nm and 605 nm of silicon dioxide. The Titan\textsuperscript{TM} carrier achieves 64\% higher MRR than the 3\textsuperscript{rd} generation carrier. At the same time, Titan\textsuperscript{TM} carrier decreases the edge of exclusion area up to 3mm with a 34\% lower NU.

3.2.5. Patterned Wafers: Within Die Non-Uniformity & SHRR

Six wafers, three patterned with the G-mask and three with the AF-mask were processed on an IPEC 472 automated CMP tool with the state of the art Titan\textsuperscript{TM} carrier (see Table 3.8).
### Table 3.8: Patterned wafers polished with the Titan™ carrier.

<table>
<thead>
<tr>
<th>#</th>
<th>Oxide above Poly (ΔT) (nm)</th>
<th>NU (±%)</th>
<th>Pre-CMP SH (nm)</th>
<th>Post-CMP SH (nm)</th>
<th>SHRR (%)</th>
<th>Post-CMP Ra (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>G 20</td>
<td>666</td>
<td>4.04</td>
<td>120</td>
<td>3.2</td>
<td>97.32</td>
<td>0.13</td>
</tr>
<tr>
<td>G 21</td>
<td>623</td>
<td>3.17</td>
<td>144</td>
<td>4.5</td>
<td>96.88</td>
<td>0.11</td>
</tr>
<tr>
<td>G 22</td>
<td>613</td>
<td>4.35</td>
<td>121</td>
<td>5.8</td>
<td>95.21</td>
<td>0.18</td>
</tr>
<tr>
<td>Averages</td>
<td><strong>634</strong></td>
<td><strong>3.85</strong></td>
<td><strong>128</strong></td>
<td><strong>4.5</strong></td>
<td><strong>96.47</strong></td>
<td><strong>0.14</strong></td>
</tr>
<tr>
<td>AF 23</td>
<td>580</td>
<td>2.50</td>
<td>111</td>
<td>2.4</td>
<td>97.83</td>
<td>0.12</td>
</tr>
<tr>
<td>AF 24</td>
<td>721</td>
<td>3.23</td>
<td>113</td>
<td>1.2</td>
<td>98.93</td>
<td>0.11</td>
</tr>
<tr>
<td>AF 25</td>
<td>594</td>
<td>2.09</td>
<td>105</td>
<td>1.8</td>
<td>98.28</td>
<td>0.14</td>
</tr>
<tr>
<td>Averages</td>
<td><strong>632</strong></td>
<td><strong>2.61</strong></td>
<td><strong>109</strong></td>
<td><strong>1.8</strong></td>
<td><strong>98.35</strong></td>
<td><strong>0.12</strong></td>
</tr>
</tbody>
</table>

The average Step Height Reduction Ratio (SHRR), calculated using Equation 3.7, is 96.47% for the *G-mask* and 98.35% for the *AF-mask*. The average NU for the *AF-mask* is ± 2.61% and for the *G-mask* is ± 3.85%. However, the values of the SHRR are based on a single measurement of the pre- and post-CMP and they are subjected to the pattern density and structure dimensions. Besides, SHRR and NU are parameters completely independent of each other and in order to improved both outputs, different pads (i.e. hard pad for planarization (SH) and soft pad for buffing (NU)) are used hence, there is no correlation between the outputs.

\[
SHRR = 1 - \frac{SH_{\text{final}}}{SH_{\text{initial}}}
\]  

(3.7)

Regarding the SHRR values, wafers with the *G-mask* had resist residues during the process fabrication increasing the pre-SH by 22% when compared to the *AF-mask*. However, the nominal pressure applied during the process is constant but the pressure exerted from structure to structure varies due to their different dimensions. The *G-mask* contains more than 45,000 structures and with different sizes making the surface more prone to variations within the final thickness distribution than the *AF-mask* with over 6,000 structures. Having said that, the lower NU of the *AF-mask* could also be attributed to the lesser amount of structures with bigger and homogeneous in their dimensions reducing the area of planarization across a single die.

The planarization step takes place gradually from local to global areas due to different arrays of structures. The local planarization takes place first in a low pattern density area since the pressure or the down force exerted by the carrier
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is higher there. However, the mechanical force in the high pattern density area is lower and therefore takes more time to complete the planarization. Nonetheless, regardless the time employed for planarization, some pattern densities are hard to eliminate.

![AFM scan image](image1)

(a) Cad of the area measured on AFM

(b) AFM scan image of the area measured

Figure 3.25: AFM analysis of the pre-CMP SH (G-mask).

The difficulty of removing completely the pattern density can be clarified by comparing the measurements between the pre- and post- SH seen in Table 3.8 and Table 3.9 where the pattern density is completely removed if after the planarization step the SH is zero. However, none of the SH at different pattern densities were completely removed.

<table>
<thead>
<tr>
<th>Width (µm)</th>
<th>Linespace (µm)</th>
<th>Pitch (µm)</th>
<th>Pattern density (%)</th>
<th>Pre-CMP SH (nm)</th>
<th>Post-CMP SH (nm)</th>
<th>SHRR (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>9</td>
<td>12</td>
<td>21</td>
<td>84</td>
<td>104.23</td>
<td>0.22</td>
<td>99.80</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>4</td>
<td>75</td>
<td>38.72</td>
<td>0.55</td>
<td>98.59</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>4</td>
<td>50</td>
<td>146.57</td>
<td>2.78</td>
<td>98.10</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>4</td>
<td>36</td>
<td>140.46</td>
<td>2.69</td>
<td>98.09</td>
</tr>
<tr>
<td>1</td>
<td>7</td>
<td>8</td>
<td>13.5</td>
<td>115.34</td>
<td>4.29</td>
<td>96.28</td>
</tr>
</tbody>
</table>

Table 3.9: Planarization efficiency of the patterned wafers.

Figure 3.25 shows a 10µm² scan perform on an AFM over a pattern density of 36 %. The PECVD oxide deposited on the top of the polysilicon structures is ≈ 1012 nm however, the pre-SH shown in Table 3.9 indicates that the SH is 1405 nm.
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and for other cases, the SH is up to 1466 nm. Though the wafers were stripped on a TePla system and afterwards bathed in 7-up, it is most probably that the residues come from non-stripped resist.

![Planarization Efficiency graph](image)

Figure 3.26: Planarization Efficiency

Table 3.9 and Figure 3.26 shows how by increasing the pattern density, the SHRR also increases. This can be attributed to easier accessibility of the pad asperity into the down area for low pattern density locations. The time required to planarized high pattern density locations can lead to a over planarizing due to the higher exposure of the low pattern density areas.
Chapter 4

Conclusions

This thesis has shown the current endeavor of presenting the CMP technique from the tool progression through different generations, wafer carrier advances and challenges faced over the last two decades, slurry and pad functionalities, to the importance of the cleaning step and issues of the process itself. Furthermore, the Titan™ wafer carrier has been compared with a third generation carrier while planarizing oxide blanket wafers and also evaluated while planarizing patterned oxide wafers.

The results have shown that the Titan™ carrier achieved 64% higher removal rates than the third generation carrier while decreasing the edge of exclusion region up to 3 mm with a 34% lower NU and a final $R_a$ of 0.22 nm. Third generation carrier blankets showed slow edge performance at 3 mm with a NU of 7%. The inner tube bladder presented in the Titan™ wafer carrier reduced the pad rebound effect by applying an independent pressure into the polishing pad.

However, in order to get the maximum performance out of the Titan™ wafer carrier and diminish the NU further while expanding the edge of exclusion region up to 3 mm, other processes such as PECVD, LPCVD or thermal oxidation have to improved the thickness distribution or NU values have to be reduced at the edge of the wafer. The same applies to the WTWNU, in order to improve it, the cleaning time for each recipe has be adjust to achieve constant deposition rates.

The Titan™ wafer carrier, while planarizing pattern wafers, showed excellent planarization performance with a 98% SHRR, an average NU of ± 2.61% and $R_a$ of 0.12 nm.

The pattern density analysis shown an increase in the SHRR with an increase of density. Nonetheless, the lack of in-situ instruments made the characterization task slow and tedious. The low roughness values after planarization impedes the use of mechanical profilometers. Also AFM required time and accessibility to find specific locations. While lacking in-situ resources, tools as Scanning Electron Microscope (SEM) can give a clear image of the up and down areas to analyze the step planarization.
Chapter 5

Future work

In order to compensate for the lack of instruments that facilitate the measurements on removal thickness in patterned wafers with small structure dimension, a specific mask as the one shown in Figure 5.1 can be designed to facilitate SEM measurements. The mask comprises a variation in pattern densities and structure width from left to right and top to bottom.

Figure 5.1: Top and cross section view of a density mask (Adapted from [71])

Bigger structures helps to crack the wafer across different pattern densities in a single sample for SEM characterization. At the same time, wider structures (or wider than the incident beam) gives the possibility to measure the oxide thickness
in a ellipsometer or spectrophotometer. Values such as the Total Thickness Variation (TTV) or analyzing the global planarization would become rather accessible. Besides facilitating thickness measurements, the mask can be used for CMP training and it gives the possibility of running processes with different parameters and see how they may impact in the overall process (WIWNU). Another possibility for measurement control is to include dummy measurement boxes into the die layout matching the pattern density within the small feature size area.
Bibliography


[61] H. Xiao, “Chapter 12 chemical mechanical polishing.”


