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An Adaptive FET Sizing Technique for High Efficiency Thermoelectric Harvesters

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Abstract—A theoretical analysis of losses in low power thermo-electric harvester interfaces is used to find expressions for properly sizing the power transistors according to the input voltage level. These expressions are used to propose an adaptive FET sizing technique that tracks the input voltage level and automatically reconfigures the converter in order to improve its conversion efficiency. The performance of a low-power thermoelectric energy harvesting interface with and without the proposed technique is evaluated by circuit simulations under different input voltage/power conditions. The simulation results show that the proposed technique improves the conversion efficiency of the energy harvesting interface up to 12% at the lowest input voltage/power levels.

I. INTRODUCTION

Thermoelectric generators (TEGs) have been proven as a valid energy harvesting solution for powering various size-constrained wireless sensor systems. In recent years, these devices have been increasingly considered even in challenging applications such as wearable/implantable biomedical systems [1], [2]. Compared to other biocompatible harvesting sources, TEGs offer high reliability and superior power density at miniature scales [3], both of which are crucial features for biomedical systems. Nevertheless, temperature gradients across a TEG in a biosystem are very low [4]. In implantable applications temperature gradients between 0.5 K and 2 K can be expected [5]. As a result, the TEG provides extremely low voltage and power levels to a matched load (15 mV–60 mV and 1 μW–17 μW, respectively [3]), which imposes many challenges to the design of an efficient energy harvesting interface for implants.

In order to complement the prior work [6]–[8], recent thermoelectric energy harvesting interfaces have demonstrated operation at extremely low input voltages [9], enhanced the efficiency [10], improved the start-up [11] and minimized the total footprint [4]. However, in all these solutions, the conversion efficiency starts to roll-off as the input power approaches very low levels. Consequently, the efficiency drops to insufficient values above or in the input power range of implantable applications. For instance, in [9], the peak conversion efficiency of 83% drops to only 21% when the input power is around 50 μW. This paper proposes an adaptive FET sizing technique to mitigate the efficiency roll-off and maintain the high efficiency of the energy harvesting interface as input power levels approach μW range. This will allow extending the effective temperature range of the interface.

In order to validate its efficiency, the proposed technique is employed in a complete energy harvesting system.

This paper is organized as follows. Section II introduces the proposed technique and the boost converter architecture used for its validation. Section III presents the losses analysis at very low input voltage/power levels. Section IV focuses on circuit implementations of the adaptive FET sizing technique and driver circuitry. Section V highlights the simulation results. Finally, concluding remarks are given in Section VI.

II. SYSTEM ARCHITECTURE WITH ADAPTIVE FET SIZES

Fig. 1 shows the boost converter architecture that employs the proposed adaptive FET sizing technique. It consists of an adaptive DC-DC core circuit and a control block. The system is based on the single-inductor dual-output (SIDO) boost converter presented in [12], but the DC-DC core circuit and the switch drivers are modified in order to utilize the proposed technique. The power transistors (switches) of the adaptive DC-DC core circuit are divided into multiple smaller sub-switches (four in this particular case, $M_{N\langle 3:0\rangle}$ and $M_{P\langle 3:0\rangle}$). The secondary pMOS switch, M_{PC}, is kept fixed for the sake of simplicity since the main switch is operating most of the time. Every individual sub-switch is carefully sized and driven independently so that the total width of switches can be adjusted as needed. The idea is to change the switch size according to the input voltage/power level in order to achieve the optimal power transistors' widths at any time. The switch drivers consist of logic gates, level shifters and multi-stage tapered buffers. The rest of the control block is kept unchanged so that the system with and without the adaptive FET sizing technique can be compared fairly.

III. LOSSES ANALYSIS AT LOW VOLTAGE/POWER LEVELS

The efficiency of the boost converter depends on the total losses within the converter, P_{loss}, and the power consumption of the control block, P_{ctrl}. The efficiency roll-off occurs when the sum of P_{loss} and P_{ctrl} becomes comparable to the input power. Unlike the conduction losses, the switching losses do not scale down with the input power (voltage) [12]. As a result, at very low power levels, P_{loss} is usually dominated by the switching losses. The proposed technique aims to mitigate the influence of the switching losses and maintain a high efficiency of the converter at low power levels.
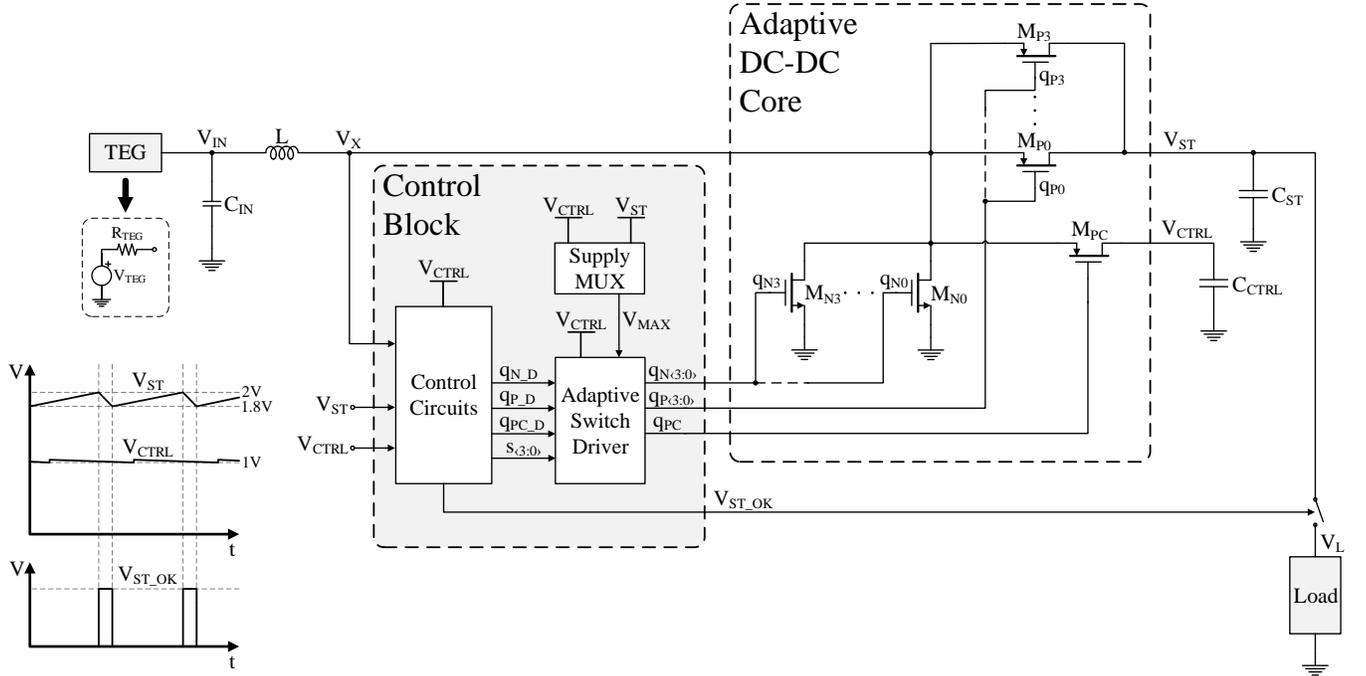
Fig. 1. System architecture of the boost converter with adaptive power FET sizes.

To achieve high efficiency, the optimal values of the power transistors' widths (W_N and W_P), switching frequency (f_s) and inductor (L) can be determined [12], [13]. For these values, the sum of P_{loss} and P_{ctrl} is minimized. The optimal values are obtained for a given input voltage (V_{IN}), which is usually set to a most probable or a typical value. However, in practice, V_{IN} varies (in this particular case between 15 mV and 60 mV). So, to achieve high conversion efficiency for any input voltage, the optimal values have to be adjusted accordingly. Changing the switching frequency and/or inductor value would disrupt the input matching condition (given by $R_{IN} \approx 2L/(\tau_N^2 f_s) = R_{TEG}$ [7]). In addition, altering the value of an external inductor is highly impractical from the implementation and integration points of view. For these reasons, f_s and L are fixed. On the other hand, changing the power transistors' widths according to the input voltage does not affect the input matching and can be fully implemented on-chip.

Assuming that the synchronization losses are suppressed (the control signals are properly timed) and that $V_{ST} \gg V_{IN}$, the sum of P_{loss} and P_{ctrl} can be expressed as [12]:

$$
\begin{aligned}
P_{loss} + P_{ctrl} = {} & \frac{2\sqrt{2}V_{IN}^2}{3\sqrt{R_{IN}^3}\sqrt{f_s}}\left(\frac{R_N'}{W_N\sqrt{L}} + \frac{R_P'V_{IN}}{W_P V_{ST}\sqrt{L}}\right. \\
& \left. + p_1\sqrt{L} + \frac{R_{par}}{\sqrt{L}}\right) + f_s(kC_N'W_N V_{ST}^2 \\
& + kC_P'W_P V_{ST}^2 + \frac{1}{2}C_X V_{ST}^2 \\
& + C_{c,eff}V_{CTRL}^2) + V_{IN}I_{leak,N}W_N
\end{aligned}
$$

$$
+ V_{ST}I_{leak,P}W_P, \tag{1}
$$

where p_1 is the inductor family dependent constant coefficient, R_{par} is the total parasitic series resistance, k is the power consumption factor of a driver circuit, R_N' and R_P' are the resistances per unit width, C_N' and C_P' are the gate capacitances per unit width, $I_{leak,N}$ and $I_{leak,P}$ are the leakage currents per unit width, W_N and W_P are the transistors' widths, C_X is the parasitic capacitance at node X and $C_{c,eff}$ is the total effective capacitance of the control block.

The optimal size of the nMOS switch (for which the sum of P_{loss} and P_{ctrl} is minimized) is obtained when:

$$
\frac{\partial(P_{loss} + P_{ctrl})}{\partial W_N} = 0, \tag{2}
$$

from which $W_{N,opt}$ can be derived as:

$$
W_{N,opt} = \sqrt{\frac{2\sqrt{2}V_{IN}^2 R_N'}{3\sqrt{R_{IN}^3}f_s L(f_s kC_N'V_{ST}^2 + V_{IN}I_{leak,N})}}. \tag{3}
$$

Similarly, the optimal size of the pMOS switch, $W_{P,opt}$, can be obtained:

$$
W_{P,opt} = \sqrt{\frac{2\sqrt{2}V_{IN}^3 R_P'}{3V_{ST}^2\sqrt{R_{IN}^3 f_s L}(f_s kC_P'V_{ST} + I_{leak,P})}}. \tag{4}
$$

The expressions (3) and (4) clearly show how the optimal transistors' widths depend on the input voltage. It is interesting to notice that if the leakage losses are neglected, the optimal size of the nMOS switch is changing linearly with the input
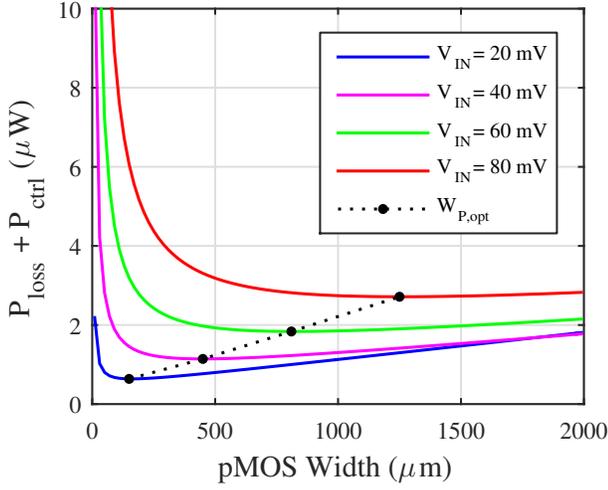
Fig. 2. Sum of P_{loss} and P_{ctrl} versus pMOS sizes at different input voltages.
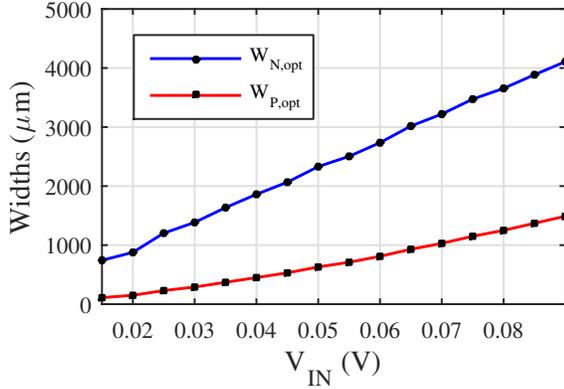

Fig. 3. Optimal transistors' widths versus input voltage.

voltage, and the relation between $W_{N,opt}$ and $W_{P,opt}$ can be derived:

$$\frac{W_{N,opt}}{W_{P,opt}} \approx \sqrt{\frac{\mu_P V_{ST}}{\mu_N V_{IN}}}, \qquad (5)$$

where μ_N and μ_P are the charge-carrier mobilities of nMOS and pMOS transistors, respectively.

Fig. 2 shows how the sum of P_{loss} and P_{ctrl} depends on the size of the pMOS switch for different input voltages. It also illustrates how the optimal size of the pMOS switch is varying when the input voltage is changed. Fig. 3 shows the relation between the optimal sizes of switches and the value of the input signal. Therefore, by accurately adjusting the transistors' sizes, the efficiency of the converter can be maximized for all values of the input voltage. For these plots, the resistance R_{IN} is assumed to be equal to 210 Ω [3], $f_s = 15$ kHz, $L = 33$ μH, $k = 2$ and V_{ST} is set to 1.9 V.

IV. IMPLEMENTATION OF THE ADAPTIVE SIZES

The implementation of the adaptive DC-DC core circuit is shown in Fig. 1. The total width of switches has to be adjusted according to (3) and (4) (as it is shown in Fig. 3) for different

values of the input voltage. The information about the input voltage level can be obtained directly from the control block without any additional circuitry, as in most of the low power energy harvesting systems [6]–[8], [12], [13]. This is because the duration of the pMOS switch ON time, τ_P, generated by the control block, is directly proportional to the input voltage. This relation is defined by the inductor's volt-second balance (assuming that $V_{ST} \gg V_{IN}$) as:

$$\tau_P \approx \tau_N \frac{V_{IN}}{V_{ST}}, \qquad (6)$$

where τ_N is the nMOS switch ON time. The pMOS switch ON time is defined by the counter value (signal $s_{\langle 3:0 \rangle}$ in Fig. 1). Therefore, the counter stores the information about the input voltage level and can be also used to define the width of the switches. The sub-switches are carefully sized so that the total switch sizes follow the values in Fig. 3. However, above the input voltage of 60 mV (the input power of ~17 μW), the switch sizes are not further increased. This is because from this point onward, at a particular power level, the conversion efficiency is improved only marginally, while the introduced parasitic capacitance at node X reduces the efficiency at all other power levels.

The proposed implementation of the driver circuit is shown in Fig. 4. The counter value is combined with the original driving signals, q_{N_D} and q_{P_D}, to generate the driving signals for most of the individual sub-switches, $q_{N\langle 3:1 \rangle}$ and $q_{P\langle 3:1 \rangle}$. The sub-switches M_{N0} and M_{P0} are operating at the lowest input power levels, so their driving signals, q_{N0} and q_{P0}, as well as the driving signal of the secondary pMOS switch, q_{PC}, are generated directly from the original signals. The level shifters modify the high level of signals from V_{CTRL} (power supply of the control block) to the greater of V_{CTRL} and V_{ST}, as required for a proper operation of switches. The tapered buffers drive the gates of the switches. The number of stages and sizes of tapered buffers are customized according to the size of every individual sub-switch.

V. SIMULATION RESULTS

The simulated conversion efficiencies for fixed switch sizes are compared with adaptive switch sizes, as it is shown in Fig. 5. At input voltages above 40 mV a small efficiency improvement can be observed. However, as the input voltage (power) decreases the efficiency improvement becomes more prominent, reaching 12% at the lowest levels (15 mV). This was expected because the proposed technique aims to mitigate the switching losses which start to dominate at very low input voltage/power levels. A 12% efficiency improvement at such extremely low input power levels may be misinterpreted as a modest improvement. In fact, at the lowest input power levels, the boost converter with the adaptive FET sizing technique delivers significantly more power to a load. For instance, at the input voltage of 15 mV (input power ~1 μW), the boost converter without the adaptive FET sizing technique delivers only 190 nW to a load. The same boost converter with the proposed technique delivers 310 nW, which is an improvement of delivered power of around 60%.
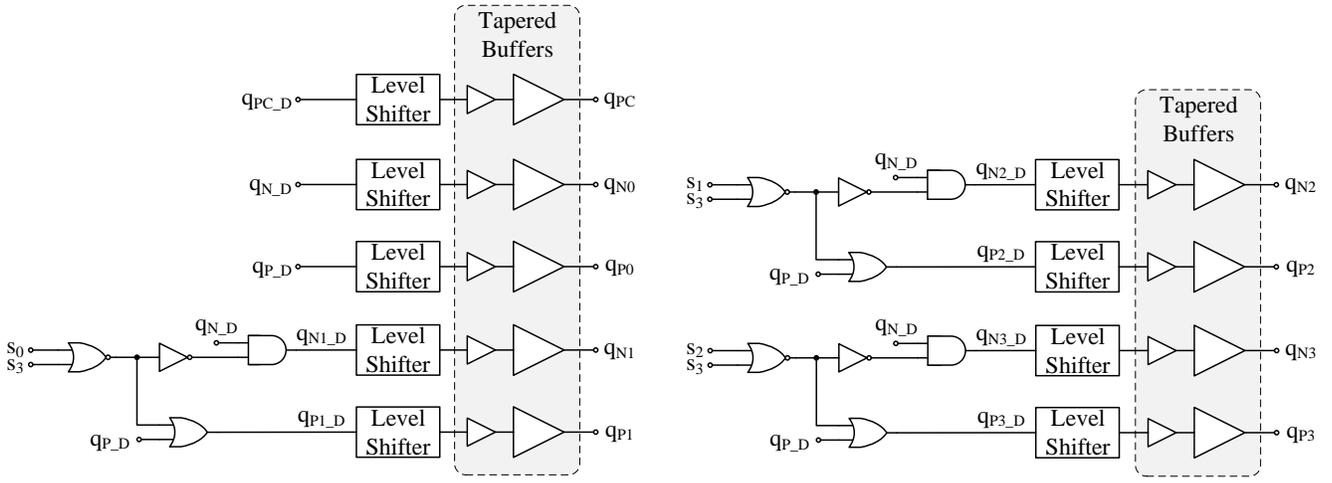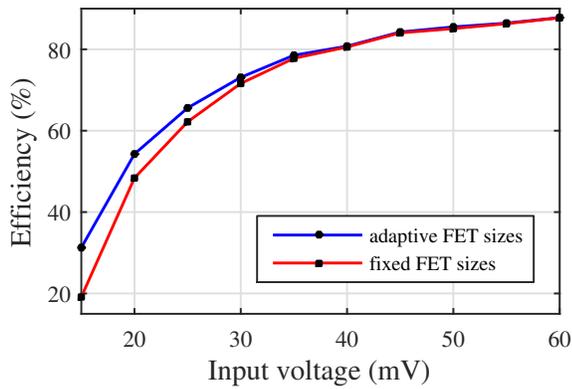
Fig. 4. Driver Circuit.

Fig. 5. Simulated efficiency improvement (maximum is 12% at 15 mV).

VI. CONCLUSION

This paper has presented an adaptive FET sizing strategy for thermoelectric energy harvesting interfaces used in low power applications such as biomedical systems. A brief theoretical analysis of losses at very low voltage/power levels has showed a clear relationship between the input voltage and the FET sizes. This finding has been used to propose a design technique suitable for harvesters that are processing very low voltage/power levels. When the proposed technique is utilized, the conversion efficiency of the boost converter is enhanced by 12% at the lowest input voltage/power levels. This means that the adaptive FET sizing technique increases by up to 60% the power delivered to a load and can potentially extend the operating temperature range of a low power energy harvesting system.

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