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Epitaxial Growth of Ge Strain Relaxed Buffer on Si with Low Threading Dislocation Density

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Epitaxial Ge with low dislocation density is grown on a low temperature grown Ge seed layer on Si substrate by reduced pressure chemical vapor deposition. The surface topography measured by AFM shows that the strain relaxation occurred through pit formation which resulted in freezing the defects at Ge/Si interface. Moreover a lower threading dislocation density compared to conventional strain relaxed Ge buffers on Si was observed. We show that by growing the first layer at temperatures below 300 °C a surface roughness below 1 nm can be achieved together with carrier mobility enhancement. The different defects densities revealed from SECCO and Iodine etching shows that the defects types have been changed and SECCO is not always trustable.

Introduction

Germanium, with its superior electron and hole mobility compared to Si, is considered as a channel material in future CMOS technology [1]. The bandgap of Ge (0.67 eV) also makes it attractive in optoelectronic device applications working in the wavelength range of 1.3-1.5 µm. However, integration of crystalline Ge on Si wafers is challenging due to the high lattice mismatch (4.2%), which may cause two issues: misfit and threading dislocations in Ge strain relaxed buffers (SRBs) and high surface roughness as a result of Stransky-Krostanov growth [2]. Threading dislocations reaching the device layer can degrade the carrier mobility and increase the junction leakage current of MOSFETs and photodetectors. Several groups have reported that threading dislocation density (TDD) can be reduced by different methods such as using compositionally graded SiGe buffer layer [3], surfactant-mediated epitaxy [4], implementing a two-step growth and post growth thermal anneal and/or cyclic thermal annealing [5]. The lowest TDDs of 10^6 cm^{-2} has been achieved by selective epitaxy and using compositionally graded buffer [1]. However, selective epitaxy is a complex technique and compositionally graded buffers need to be around 10 µm thick to achieve such low TDD.

In the two-step growth method, a thin strain relaxed Ge seed layer is grown on Si substrate at a low temperature to suppress three dimensional islands growth. The growth continues at high temperature with high quality Ge layer grown on the Ge template layer [6]. The surface of the Ge layers grown with this method is smooth with surface roughness around 2 nm. However, the TDDs of as grown layers are found to be tremendously high, close to 10^9 cm^{-2} and thermal annealing is required to lower the defect density. Reports show that the TDD of 1 µm Ge layer with ten times cyclic thermal annealing at 780 °C /900 °C can be reduced to $2 \cdot 10^7$ cm^{-2} [1] and increasing the thickness of the layer to more than 2µm can even reduce the TDD to $6 \cdot 10^6$ cm^{-2} [7].

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However, the thermal annealing is not always applicable since it causes dopants out diffusion and also Si and Ge atoms intermixing at their interface.
However, a thin Ge film with smooth surface and low TDD is still not achieved. In this work, we show further reduction of the Ge growth temperature (and optimization of its profile) during the initial step to less than 300 °C together with using Ge_2H_6 as precursor enables a 0.5 µm thin Ge SRB with surface roughness below 1 nm, TDDs as low as $5 \cdot 10^8$ cm^{-2} and room temperature carrier mobility of 950 $cm^2.V^{-1}.s^{-1}$ directly on silicon.

Experiments

The Ge SRB was grown on (100) oriented 100 mm Si wafers by reduced pressure (20 torr) chemical vapor deposition (RPCVD, ASM Epsilon 2000). Digermane (10% Ge_2H_6 in hydrogen) was used as Ge precursor and constant 20 standard liters per minute purified H_2 as the carrier gas. Phosphine (PH_3 5% in hydrogen) and diborane (B_2H_6 10% in hydrogen) were used as phosphorous and boron sources for n- and p-type Ge SRB growth, respectively. The substrates were subjected to a RCA (H_2SO_4(96%):H_2O_2(30%) 3:1) cleaning and dipped in HF (5% in DI water) before loading into the RPCVD reactor. In-situ hydrogen bake was performed at T=1050 °C for 2 min to remove any residual native oxide from the surface. The temperature was ramped down to 280 °C before the Ge_2H_6 was introduced in the chamber followed by a temperature ramp up to 300 °C for 20 min growing a 40 nm strained relaxed Ge layer. The temperature was ramped up to 680 °C in H_2 and a 460 nm thick Ge layer was grown at this temperature. For comparison, a 3 µm thick Ge SRB was deposited with the conventional two step method; i.e. first layer grown at T=400 °C followed by the second layer at T=680 °C and post growth annealing at T=900 °C.

The topography and surface roughness of the grown layers were measured by AFM in tapping mode. The crystal quality of the epitaxial layers was investigated with high resolution X-Ray diffraction (HRXRD) rocking curve and high resolution reciprocal lattice mapping (HRRLM) pattern. A Philips X'pert PANalytical diffractometer tool was used for XRD measurements equipped with a copper anticathode and a four bounce symmetric Ge monochromator. High resolution cross sectional transmission electron microscopy (XTEM) measurement was performed to image the defects at the interface of Ge and Si. The grown Ge SRB was subjected to wet chemical etching using SECCO ($K_2Cr_2O_7$:H_2O:HF) and Iodine (HF:HNO_3:CH_3COOH:I) solutions in order to delineate the threading dislocations. TDD was determined by counting delineated defects on images obtained from both dark field optical microscope, AFM and SEM. Ge layers were in situ doped with boron and phosphorous with dopant concentrations of $10^{17}cm^{-3}$. Wafers were diced to square pieces and four contacts were formed on each corner through metallization and rapid thermal annealing at 300 °C for 90 sec. The carrier mobility was extracted using four probe hall measurements. Both SIMS and four probe sheet resistivity measurements were implemented to calculate the active dopant concentrations.

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Results and discussions

Fig. 1 shows AFM images of the surface morphology for temperature ramped (T=280-300 °C) Ge SRB (left image) and conventional (T=400 °C) Ge SRB (right image). The images indicate that the strain relaxation occurred through pit formation in the temperature ramped Ge SRB while in the conventional Ge SRB, the strain relaxed through island and valley formation. Similar relaxation through pit formation has been reported in Ge grown on Si at T=290 °C using ultra high vacuum CVD and pure germane as germanium source [8]. The pits are generated through stacking faults formations in (111) planes and their dimensions depend on the thickness of the top layer. They are formed in the first low temperature grown Ge layer below the brittle-ductile transition temperature which allows Ge growth in 2D mode instead of 3D. The brittle-ductile transition temperature depends on the experimental conditions and a sharp transition can occur within a few degrees. it has been shown in [9] that the growth mode at temperatures below the brittle-ductile transition results in strain relaxation through 90° Lomer (edge) and screw dislocations formation instead of 60° dislocations . This type of dislocations are sessile and cannot glide and thread into the next layer enabling low TDD in the top Ge film grown at T=680 °C. The root mean squared (RMS) surface roughness of the layers measured from tapping mode AFM images shows that the low temperature growth has improved the surface quality of the grown layers from RMS ~ 2 nm to <1 nm when temperature is decreased from 400 °C to lower than 300 °C which is in a good agreement with the trend reported in [8].

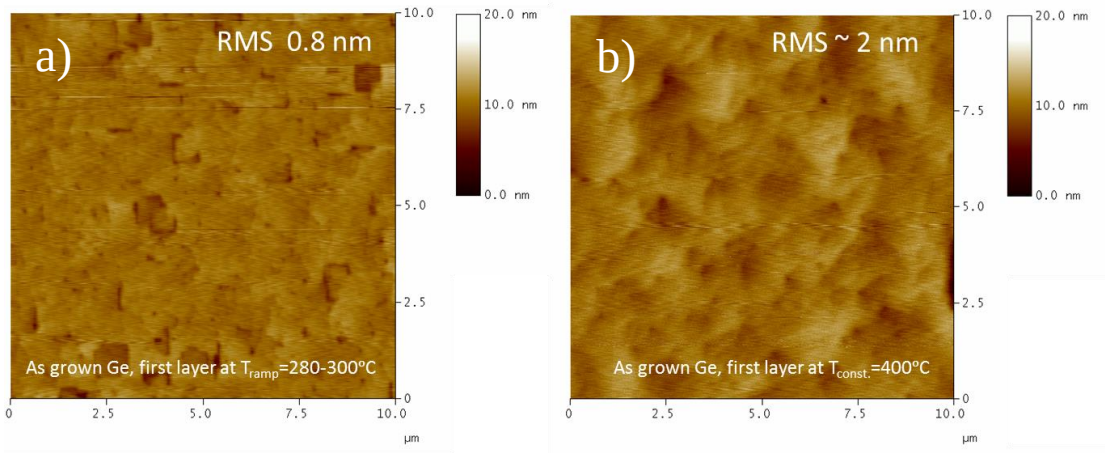

Figure 1. AFM surface morphology of Ge SRB showing a) pit formation during strain relaxation with the first layer grown at 280-300 °C and b) island and valley formation when the first layer is grown at 400 °C.

HRXRD rocking curve of three different layers are shown in figure 2-a. The results show when the layers have the same thickness, the layer grown at temperatures below 300 °C has smaller full width half maximum (FWHM) and higher peak intensity which indicates its higher crystal quality. When the thickness is increased to 3 µm and the layer is annealed, the Ge peak intensity has increased and the peak is broadened toward Si peak which is due to Si and Ge atoms inter-diffusion at the interface. The HRRLM pattern around [224] direction of the layers with the same thickness is shown in figure 2-b. The results show less peak broadening for Ge SRB with the first layer grown at temperatures

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below 300 °C compare to the Ge SRB with the first layer grown at 400 °C. The peak broadening indicates higher amount of imperfections.

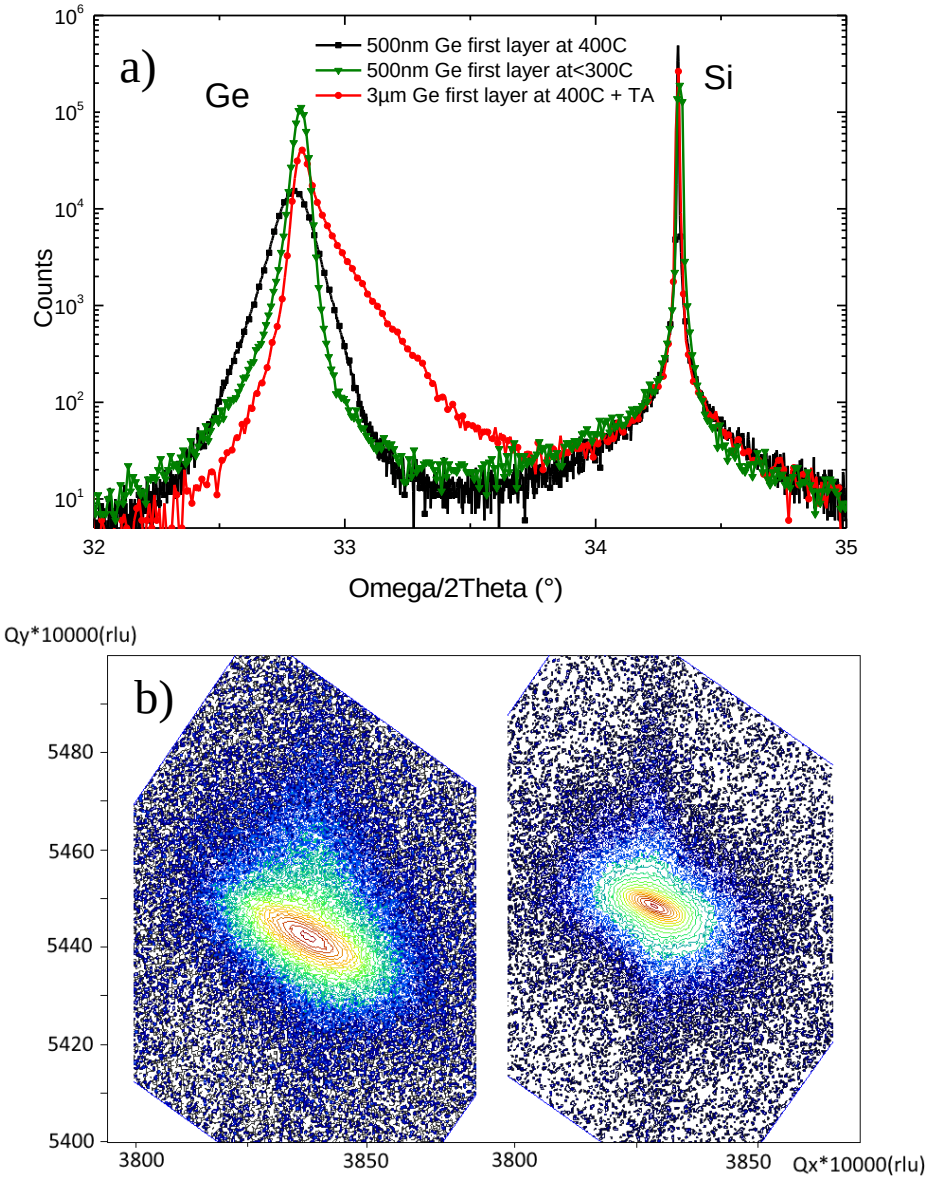

Figure 2. a) XRD rocking curve of 500 nm Ge SRB with the first layer grown at 280-300 °C, 500 nm Ge SRB with the first layer grown at 400 °C and 3 µm Ge SRB with the first layer grown at 400 °C and thermally annealed at 820 °C for 20 min, b) HRRLM pattern around the [224] direction of 500 nm Ge SRB with the first layer grown at 400 °C (left image) and 500 nm Ge SRB with the first layer grown at 280-300 °C (right image).

SIMS results show that the layers have 10^{17} cm^{-3} atomic boron concentration. Four-probe Hall measurement results show when the first layer is grown at temperatures below 300 °C the hole Hall mobility at room temperature and 77 K are 950 and 1450 $cm^2.V^{-1}.s^{-1}$, respectively which are very close to values of 1200 and 2000 $cm^2.V^{-1}.s^{-1}$ for bulk p-type Ge. In case of conventional SRB layer, the Hall mobility values were 450 and 780 $cm^2.V^{-1}.s^{-1}$ at room temperature and 77 K, respectively. The reason for such significant carrier mobility reduction is the type and electrical activity of the dislocations and the defects. The 60° dislocations which are the main defects of conventional Ge

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buffers have a raw of broken dangling bonds in their core along their axis which is believed to be the primary reason for electrical activity of dislocations. But the screw dislocations have no broken dangling bonds, thereby, they are less electrically active and do not increase the carrier scatterings [10].

Figure 3 shows a cross-section transmission electron microscopy (XTEM) of a 500 nm thick Ge SRB with the first layer grown at 280-300 °C. The left image shows that only a small portion of the defects penetrated through the top layer and reached the top surface, while most of the defects remained sessile at the interface of Si and Ge. Strain fields are visible in the vicinity of the Si/Ge interface which are caused by localized misfit dislocation network. Atomic resolution image of the Ge-Si interface (right image) shows that the edge dislocations spacing is approximately 10 nm which is in a good agreement with 9.6 nm spacing needed to completely compensate 4.2% lattice mismatch between Si and Ge crystals.

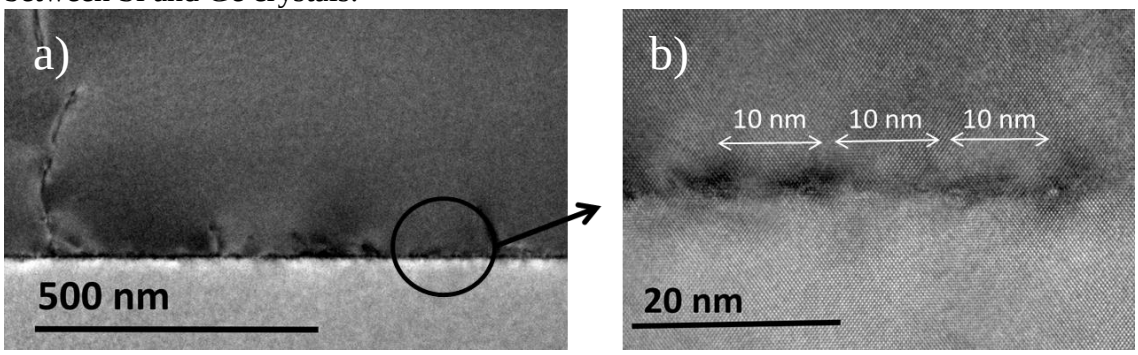

Figure 3. Cross-sectional transmission electron microscopy (XTEM) of a 500 nm thick Ge SRB with the first layer grown at 280-300 °C a) defects are formed at the interface of Si/Ge and only a small portion reached the surface, b) edge dislocations with 10 nm periodicity at the interface of Si/Ge.

Fig. 4 shows dark field optical microscope images of the Ge SRB after delineation of the threading dislocations by SECCO etching for 5 min. SECCO selective defect etching is one of the most used techniques for revealing defects in group IV semiconductors. For the conventional 3 µm thick Ge SRB (left image) a TDD ~ 10^7 cm^{-2} was measured. The Ge SRB with the temperature ramped (T=280-300 °C) exhibits a comparably low TDD ~ $4 \cdot 10^4$ cm^{-2} even after several hours of etching (right image). AFM image of the layer after 40 min etching in SECCO solution is shown in figure 5. The section of the sample shows that Ge has been etched for tens of nanometers in the defects areas while the other areas are intact.

The TDDs decorated by iodine solution treatment technique were not consistent with SECCO results. The SEM images of the layers after etching with iodine solution are shown in figure 6. In case of conventional Ge SRB, the same TDD value of 10^7 cm^{-2} was extracted, but the Ge SRB grown at ramped temperature showed defect density of $5 \cdot 10^8$ cm^{-2}. This inconsistency shows that the defects types are changed when the first layer is grown at temperatures below the brittle-ductile transition and the SECCO etch cannot delineate all types of defects in Ge. One of the reasons for such a behavior is that the SECCO solution does not etch the defects which are not electrically active or do not have broken dangling bonds.

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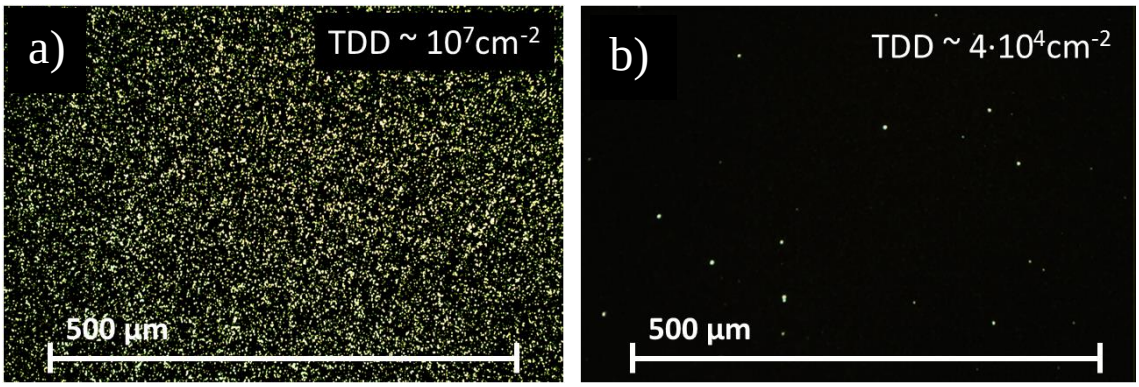

Figure 4. Dark field optical microscope images of the Ge SRB after delineation of the threading dislocations by SECCO etching of a) Conventional Ge buffer and b) Ge SRB with the first layer grown at temperatures below 300 °C.

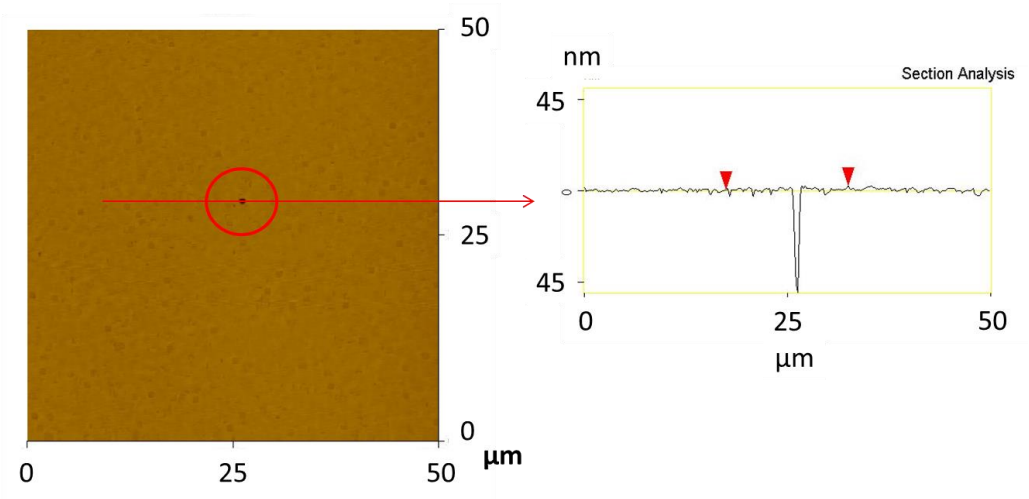

Figure 5. AFM surface topography of the Ge SRB after delineation of the threading dislocations by SECCO etching for 40 min.

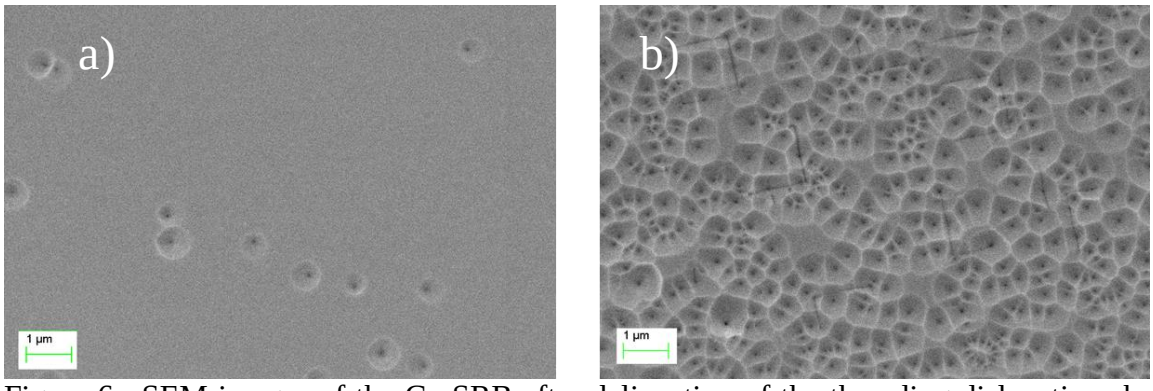

Figure 6. SEM images of the Ge SRB after delineation of the threading dislocations by Iodine etching of a) Conventional Ge buffer and b) Ge SRB with the first layer grown at temperatures below 300 °C.

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Conclusions

We have shown that by using Ge_2H_6 and optimizing a low temperature (280-300 °C) profile of the initial Ge growth it is possible to grow a 0.5 µm thin Ge SRB on Si with surface roughness below 1 nm, threading dislocation density of about $5 \cdot 10^8$ cm^{-2} with high carrier mobility without any post growth annealing. When the first layer is grown at temperatures below 300 °C, the strain relaxation happens through pit formation with edge and screw dislocations instead of 60° dislocations. These defects have less dangling bonds and consequently, they are less electrically active compared to 60° dislocations. Our experimental results show that the SECCO etch is not always a reliable method for etching Ge defects and there are some types of defects which would not be delineated by the SECCO treatment. It is recommended to use multiple defect selective etching to reveal all types of defects in hetroepitaxial grown Ge layers.

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