

# Waveform Relaxation for the Parallel Solution of Large PEEC Model Problems

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**Abstract**—The solution of large 3D electromagnetic models is important for the modeling of a multitude of EMC, PI and SI problems. In this paper, we explore new algorithms for the parallel solution of large time domain 3D electromagnetic problems. Our approach is to use a volume Partial Element Equivalent Circuit (PEEC) electromagnetic formulation in combination with a Waveform Relaxation (WR) algorithm. In WR, we split the system into smaller subsystems and we break weak couplings so that the problem can be solved iteratively. WR has been used to solve a multitude of different problems. It is especially suited for parallel processing due to its favorable compute time to communication ratio. We consider a specific example for the application of WR to PEEC models.

## I. INTRODUCTION

Today, the solution of large 3D electromagnetic problems is key for solving large EMC, PI and SI problems. Ultimately, parallel processing is necessary for the solution of very large problems. For more than 20 years, the performance of high-end computers has been enhanced in speed by using multiple processors. Today – not surprisingly – one of the major trends in the design of the next generation microprocessors is to use multiple cores or processors even for low end systems. On the other hand, supercomputers are available today which have thousands of processors. Hence, it is desirable to have algorithms which work well for many different parallel architectures. In order to utilize efficiently the different machines for electromagnetic solvers, new algorithms need to be devised. In this paper, we explore parallel algorithms for using the volume Partial Element Equivalent Circuit (PEEC) approach [1], together with Waveform Relaxation

(WR). WR techniques have been utilized for a multitude of circuit and other applications, *e.g.*, [2], [3], [4].

Parallel algorithms can be classified by several fundamental properties. A key property we are seeking is a large parallel efficiency even for a large number of processors. For example, the conventional Gauss type matrix solver algorithms are more limited in the number of processors which can be used. This is in contrast to explicit algorithms such as the FDTD/FE methods which can be extended to very large structures and can be subdivided into separate problems. Recently, it was also shown that QR based algorithms can lead to efficient parallel EM solvers for the frequency domain [5]. In this paper, we explore parallel algorithms using PEEC and WR techniques. The only previous work we are aware of in this area is [6]. One of the advantages of this approach is that additional circuits can directly be incorporated into the solution methodology. In the last 25 years, much work has been conducted on WR for Spice type circuits by many researchers, *e.g.*, [7], [8].

The strategy of the WR approach pursued here – in contrast to other more conventional iterative techniques – is to pre-split or partition the system only at weakly coupled connections such that convergence can be accomplished in a few interactions only. Importantly, this guarantees convergence for all problems at hand. Partitioning has to be done as a pre-processing step. Hence, the interactive strategy is fixed beforehand while the number of WR iterations is determined by a convergence test which compares the maximum difference between two consecutive

iterations. Today, the much higher frequencies in VLSI circuits and packaging lead to problems with a much larger number of mutual coupling elements. A very good example of this is the WR work on multiple transmission line coupling [4]. It was shown in this paper how the multiple inductive and capacitive couplings between the transmission lines are solved with the TR-WR algorithm used. For PEEC, similarly, we can identify all coupled partial inductances, capacitances and potential coefficients to find the ones which yield a small enough coupling coefficient for decoupling. Then, only the large couplings needs to be evaluated non-iteratively while all other couplings can be handled with WR. Another source of potential partitioning in the full wave (Lp,R,P, $\tau$ )PEEC models can be the due to the retardation or delay, since all the delayed values required in the solution can be derived from the known past values in time. Parallel processing has been used for speeding up the computation of the delayed past value computations for a time domain integral equation approach in [9]. For the (WR)PEEC approach presented in this paper, we subdivide the system into smaller subsystems so that tasks can be assigned to the processors in such a way that we can keep them simultaneously busy. This can be accomplished in similar ways to some of the strategies used for conventional circuit WR.

## II. WAVEFORM RELAXATION ASPECTS

In Section I, we mentioned that both parallel algorithms and computers have special characteristics which should be matched for best performance. Fortunately, the WR type algorithms are quite flexible and they have the capabilities to work on a large parallel processors provided that the problem at hand is large. The following observation is true in general for WR algorithms.

*Observation 1:* (Parallel efficiency)

The advantage in parallel efficiency for (WR)PEEC, is due to the large subsystem compute time in comparison to the short time spent to exchange waveforms between the circuit solutions. Mainly, the subsystem transient analysis requires considerable compute time for the waveforms. This is in contrast to the fast waveform exchange which updates the waveforms between the subsystems which

is much shorter even for machines with relatively poor latency.

Each WR algorithm consists of several key steps, the *partitioning* into subsystems, *ordering* to determine the order of the dispatched subsystems and the *scheduling* of the transient analysis on the different processors [8]. Here, we concentrate on the fundamental partitioning since the other two steps are predominantly efficiency improvement issues. We suggest the use of weak couplings as the first step for the partitioning of PEEC circuits into different parts along interfaces of weak coupling.

*Remark 1:* (Weakly Coupled Subsystems WCS) A weakly coupled subsystem is connected to any other system or subsystem only through weakly coupled circuit elements. A weakly coupled subsystem can be identified by checking all connections so that the capacitive and inductive couplings are small enough.

As an example, application of the WCS concept in [4] was successfully employed for the WR solution of problems with multiple transmission lines. In this example, we know in advance that the transverse coupling between the lines is weak and that we can consider each line as a WCS. To determine the coupling for general systems, usually heuristic techniques are used coupled with graph algorithms [7], [8]. Coupling factors can be defined, for example, as the conventional inductive coupling factor

$$K_L = \frac{Lp_{12}}{\sqrt{Lp_{11}Lp_{22}}} \quad (1)$$

and for a capacitive voltage divider as

$$K_C = \frac{C_{12}}{(C_{12} + C_{11})} \quad (2)$$

where  $C_{12}$  is the coupling capacitance and  $C_{11}$  is the capacitance to ground. For fast convergence, we require that  $K_L, K_c < 0.7$ . For this paper, we are using as an example a problem where we have a multitude of WCS partitions.

We also want to consider another partitioning issue which is important for the formation of subsystems dependent on the coupling factors. The observation shows that we also need to take other factors into account into the formation of the subsystems.

*Observation 2:* (Sub-circuit size)

A key question which impacts the algorithm is the number of subsystems  $N_c$  in comparison to the number of available processors  $N_p$ . It is always desirable to have  $N_c \gg N_p$ . However, we can trade off the convergence rate with the size of the subsystems to adjust the ratio of  $N_c/N_p$ , especially for highly coupled systems or circuits.

In the transient analysis step at least one subsystem of the form given below in (14) is solved on each processor of the machine. All the coupled voltages and current waveforms which couple to other subsystems on the same or other processors are fixed until the analysis is complete. According to the ordering, we schedule the analysis of each new subsystem. Importantly, the overall solve time is reduced by, at the beginning of each transient analysis, utilizing the latest coupling waveforms. We are using the WCS subsystem approach for partitioning in the example given below. Also, it is easy to adjusting the coupling factors to find the best value for a particular machine.

### III. BASIC VOLUME PEEC MODEL

For the purpose of this work, it is sufficient to consider a simple volume (Lp,R,P, $\tau$ )PEEC model which is based on a mixed potential integral equation (MPIE) of the form

$$\mathbf{E}^i = \frac{\mathbf{J}(\mathbf{r}, t)}{\sigma} + \frac{\partial \mathbf{A}(\mathbf{r}, t)}{\partial t} + \nabla \phi(\mathbf{r}, t) \quad (3)$$

where  $\mathbf{E}^i$  is an incident electric field,  $\mathbf{J}$  is a current density,  $\mathbf{A}$  is the vector magnetic potential, and  $\phi$  is the scalar electric potential at observation point  $\mathbf{r}$ . By using the definitions of the scalar and vector potentials, the current- and charge- densities are discretized by defining pulse basis functions for the conductors and dielectric materials. Pulse functions are also used for the weighting functions resulting in a Galerkin type solution. By defining a specific inner product, as weighted volume integral over a discretization cells, (3) can be interpreted as Kirchhoff's Voltage Law (KVL). This essentially convert the integral over the electric field terms into voltages. Further, using the usual form of circuit elements we can interpret the terms as circuit elements where:

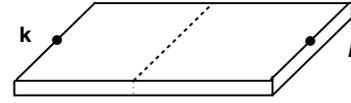


Fig. 1. Flat Conductor with One Inductive Cell

- partial self inductances between the nodes and partial mutual inductances represent the magnetic field coupling in the equivalent circuit. The partial inductance is defined as

$$Lp_{mn} = \frac{\mu}{4\pi} \frac{1}{a_m a_n} \int_{v_m} \int_{v_n} \frac{1}{|\mathbf{r}_m - \mathbf{r}_n|} dv_m dv_n \quad (4)$$

- coefficients of potential to each node and mutual coefficients of potentials between the nodes representing the electric field coupling. A single cell of an inductive cell and capacitative surfaces is shown in Fig. 1. The coefficients of potentials are defined as

$$p_{k\ell} = \frac{1}{S_k S_\ell} \frac{1}{4\pi\epsilon_0} \int_{S_k} \int_{S_\ell} \frac{1}{|\mathbf{r}_k - \mathbf{r}_\ell|} dS_k dS_\ell \quad (5)$$

- the resistive term in series to the partial inductance, is defined as

$$R_m = \frac{l_m}{a_m \sigma_m} \quad (6)$$

In (4) and (6)  $a$  represents the cross section of the rectangular volume cell normal to the current direction where  $v$  represents the current volume and  $S$  are charge surface areas. This approach converts (3) into Kirchoff's voltage law of the form

$$v_m(t) = Ri_{Lm}(t) + \sum_n Lp_{mn} i_{Ln}(t - \tau_{nm}) - \phi_{m1} + \phi_{m2} \quad (7)$$

where the loop  $m$  extends to infinity over the capacitive potentials  $\phi_k, \phi_\ell$  and where  $k$  and  $\ell$  are the nodes as shown. Note that the voltages and potentials are measured to the node at infinity which is the ground node. For a nonorthogonal formulation for the volume PEEC model, see [1].

#### A. Model for Capacitive Currents

In the last section, we considered the inductive path of the PEEC equivalent circuit model in Fig. 2. The capacitive path consists of the capacitive model to infinity at each node where infinity is the ground

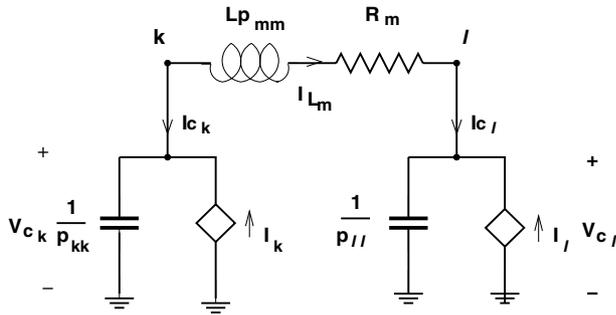


Fig. 2. One cell PEEC model for single KVL loop

node of the circuit. We start from the usual relationship  $\Phi = PQ$  where  $P$  is the coefficient of potential matrix. In the simplest case where all retardation times are very small, we can simply use  $C_S = P^{-1}$  where  $C_S$  is the conventional short circuit capacitance matrix. However, we must recognize that the cost of this is a single inversion  $O(K^3)$  where  $K$  is the number of capacitive cells. This expensive matrix inversion can be applied only for quasi-static PEEC models. Hence, the inversion of the  $P$  matrix is not an option for full-wave WR PEEC models used here. The controlled current sources in the capacitance part in Fig. 2 are derived from the above coefficient of potential equation with the relationship between current and charge  $i = \frac{dQ}{dt}$  where the capacitive surface is a half-cell as is shown in Fig. 1. The capacitive current is then given by

$$i_{c_k}(t) = \frac{1}{p_{kk}} \frac{\partial \phi_k}{\partial t} - \sum_{n \neq k} \frac{p_{kn}}{p_{kk}} i_{c_n}(t'_{kn}) \quad (8)$$

where  $i_{c_k}$  is the total capacitive current for cell  $k$  and the retardation time is

$$t'_k = t - \frac{R_{kn}}{c} = t - \tau \quad (9)$$

where  $R_{kn}$  is the distance between conductor cells  $k$  and  $n$  and  $c$  is the speed of light. We usually measure the distance between some points on the cells. The capacitances, which are due to the self capacitances in (8), lead to a strong diagonal term in the modified nodal (MNA) circuit matrix. Importantly, in (8), we see that the weighting factor of two capacitive couplings is related to  $p_{kn}/p_{kk}$ . Even small problems lead to thousands of capacitive couplings between two subsystems.

#### IV. TIME DOMAIN PEEC CIRCUIT EQUATIONS

One of the aspects which makes WR very attractive for parallel computing is the independent subsystems which are created by the partitioning step. Each of the subsystems is represented by MNA circuit equations in the usual form

$$\mathcal{C}\dot{x} + \mathcal{G}x = \mathcal{B}u \quad (10)$$

where  $\mathcal{C}$  includes the time dependent elements,  $\mathcal{G}$  the resistive elements and  $\mathcal{B}$  is the input connection matrix. We use the conventional MNA PEEC implementation used in [10] to illustrate the formulation for the general case. In this case, the vector of unknowns  $x$  for the most simple PEEC circuit in Fig. 2 is

$$[\Phi_k, V_{c_k}, \Phi_l, V_{c_l}, i_{c_k}, i_{c_l}, i_{L_m}] \quad (11)$$

where we use a zero voltage voltage source stamp for the capacitive controlled currents  $i_{c_k}$  and  $i_{c_l}$ .

Then, the circuit matrix in the operator form  $\mathcal{C} \frac{d}{dt} + \mathcal{G}$  for the circuit in Fig. 2 is

$$\begin{bmatrix} -1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{p_{11}} \frac{\partial}{\partial t} & 0 & 0 & -1 & \frac{-p_{12}}{p_{11}}(t') & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{p_{22}} \frac{\partial}{\partial t} & \frac{-p_{12}}{p_{22}}(t') & -1 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & +1 & -1 \\ -1 & 0 & 1 & 0 & 0 & 0 & R_m + Lp_{11} \frac{\partial}{\partial t} \end{bmatrix} \quad (12)$$

where  $t'$  is again a short notation for the variables which are delayed by  $t - \tau$  in (9). Since some of the variables are delayed, we can subdivide the unknown variables and the circuit matrices into instant and delayed parts. This results in the actual delay MNA equations in the form

$$\mathcal{C}_0 \dot{x} + \mathcal{G}_0 x = \sum_i \mathcal{G}_i x(t - \tau_i) + \sum_i \mathcal{C}_i \dot{x}(t - \tau_i) + \sum_i \mathcal{B}_i u_i(t - \tau_i) \quad (13)$$

where  $\mathcal{C}_0$  and  $\mathcal{G}_0$  are the non-delayed parts of the delay differential equation DDE-MNA equations of a subsystem. Larger PEEC models, which include more than one partial inductance, do also include capacitive inductive derivative terms with or without delay. This term is absent from the single inductance model in (12). Delay differential equations which include delayed derivatives are called Neutral DDEs or NDDEs. This is the general case for the transient analysis of the subsystems to be solved.

## V. SUBSYSTEM EQUATIONS

We use an example problem which is very suitable for the simple algorithms given here to explain the application of the WR. Our example problems can consist of a large number of contacts shown in Fig. 3 where most of the contacts are not connected to any other object while one of the contacts is excited by a voltage source in series with 50 Ohms. All the coupling factors for the system are computed. However, the coupled quantities from each system to other subsystems are replaced by waveform sources. Hence, each subsystem which corresponds to a single contact is analyzed separately. After each subsystem analysis, the waveforms are updated such that the new waveforms are available to the other subsystems depending on the ordering and scheduling. Each transient analysis consists of the solution of a system of the form of (14) where we subdivide the variables according to the ones in the self-system and the ones which couple to other systems in the form

$$\begin{aligned} \mathbf{C}^*_0 \dot{\mathbf{x}} + \mathbf{G}^*_0 \mathbf{x} = & \sum_i \mathbf{G}^*_i \mathbf{x}(t - \tau_i) + \\ & \sum_i \mathbf{C}^*_i \dot{\mathbf{x}}(t - \tau_i) + \sum_i \mathbf{B}^*_i \mathbf{u}_i(t - \tau_i) + \\ & \sum_i \mathbf{C}^+_i \dot{\mathbf{x}}(t - \tau_i) + \sum_i \mathbf{B}^+_i \mathbf{u}_i(t - \tau_i) \end{aligned} \quad (14)$$

where the elements with an \* pertain to the self-subsystem and + represents the elements which couple to the other subsystems. All these variables are equipped with voltage waveforms which are updated each time a subsystem is scheduled and solved on one of the processors. It is clear that the proper updating of the waveforms and the scheduling of the subsystems is much more challenging for PEEC circuits rather than conventional circuits without the couplings to all other subsystems.

## VI. RESULTS

The problem which we solve for our example problem consist of six square contacts with dimensions of  $400 \mu m \times 400 \mu m \times 13 \mu m$  over a ground plane, as shown in Fig. 3. The center to center spacing is 1 mm for all contacts. The overall structure consists of six subsystems with 12 inductive volume cells and 24 capacitive cells. In this simplified example we want to study the difference between open contacts and contacts which are grounded with a  $50 \Omega$  resistor. The first contact is driven by a pulse voltage source with rise time

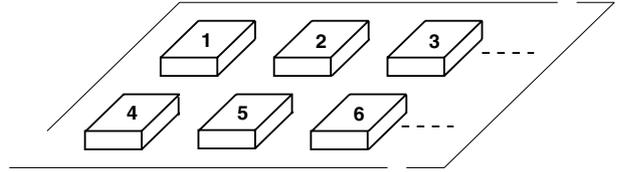


Fig. 3. Set of PBC contacts

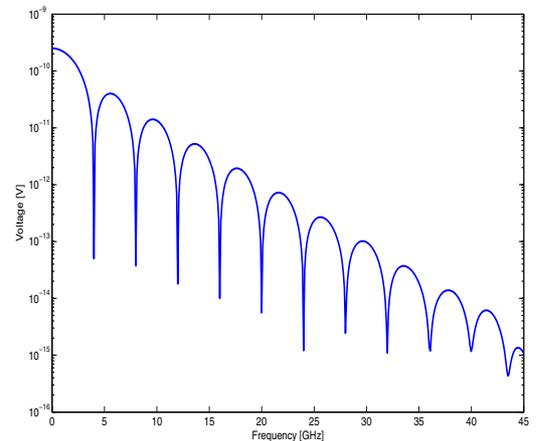
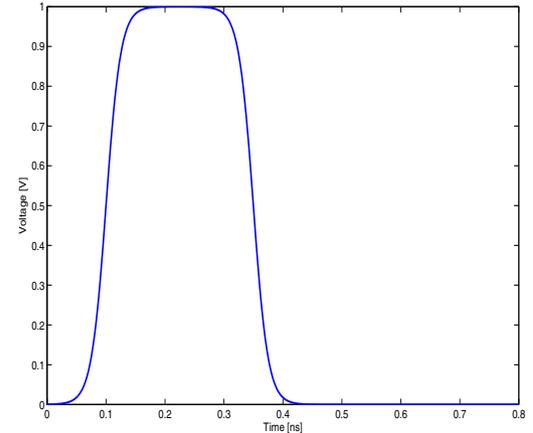


Fig. 4. Voltage source. Top panel: transient voltage; bottom panel: magnitude spectrum.

$\tau_r = 50$  ps. Figure 4 shows the source voltage along with the magnitude of the spectrum.

In the first test, the first contact is terminated with a  $50 \Omega$  resistance while all the other contacts are floating. Figure 5 shows the potential of contacts two ( $C_2$ ) and six ( $C_6$ ) evaluated by the standard PEEC method as well as the (WR)PEEC solver. No significant difference in the waveforms is observed for the two solution approaches. For the second example, contacts  $C_2, \dots, C_6$  are grounded with 50

## VII. CONCLUSIONS

The paper is a first study of using a waveform relaxation based volume PEEC circuit approach for the solution of large systems for parallel processing. So far, the size of the circuit analyzed is relatively modest. However, this work represents a feasibility study for the approach for parallel processing. Aspects which are not included in this work are stability, causality and passivity issues. However, we want to observe that the circuit oriented PEEC approach used in this paper is very suitable for the expansion of the model to include some of these issues.

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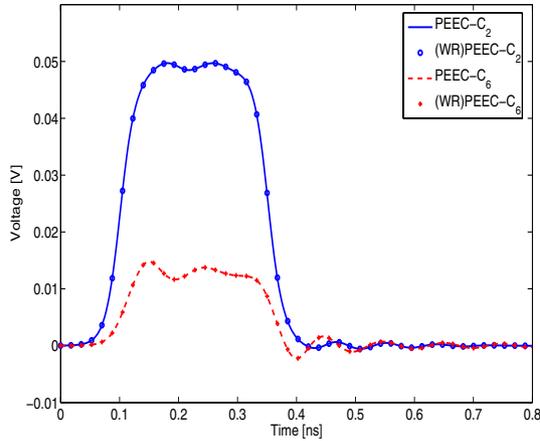


Fig. 5. Potential of floating contacts 2 and 6.

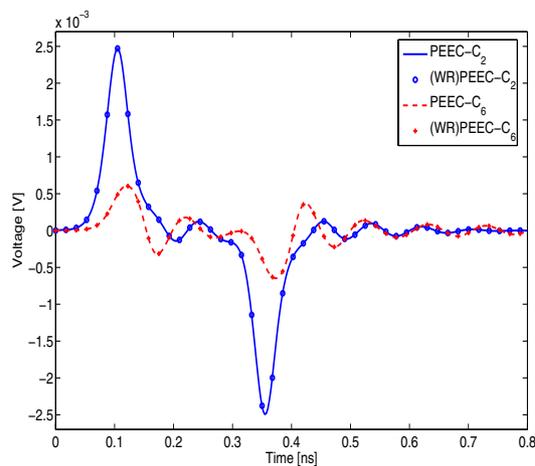


Fig. 6. Potential of grounded contacts 2 and 6.

$\Omega$  resistors. The potential induced on contacts two and six are plotted in Fig. 6. Again, the agreement between the results obtained by using the standard PEEC and the (WR)PEEC solvers is good. All these results are produced with a sequential analysis on a single processor. The basic order [8] we are using to schedule the subsystem transient analysis is 1, 2,  $\dots$ , 6. Convergence is achieved in five iteration. For such a small example with six subsystems we could only apply a limited number of processors, like six. A larger number of processors implies that many of them would not be busy resulting in a reduced efficiency. However, it is evident that a large number of processors can be employed for problems with hundreds of contacts.